A Line-Frequency Commutated HV VSC Embedded Modular Multilevel Converter With DC Fault Blocking Capability

Jian Liu, *Student Member, IEEE*, and Dong Dong, *Senior Member, IEEE*

***Abstract*—Modular multilevel converter (MMC) has become one of the most favored topologies in medium-voltage and high-voltage (HV) applications. However, it still suffers from some drawbacks, including a lot of sizeable capacitors, high conduction losses, and no dc-fault ride-through capability. To circumvent these issues, this article presents a modified MMC, namely hybrid-leg MMC (HL-MMC). HL-MMC integrates a pair of three-phase line-frequency commutated HV voltage source converters (VSC) to replace up to 40% MMC submodules (SMs), leading to lower cost and conduction losses. Due to the ripple energy cancellation in the three-phase HV VSCs, the total energy storage requirement in HL-MMC could be also reduced, leading to up to 30% energy storage capacitance reduction compared with MMC. In addition, by combing the dc hybrid circuit breaker, the HV VSCs in the proposed HL-MMC also help provides the dc fault blocking capability, enabling a dc-fault tolerant HL-MMC without using the full-bridge (FB) MMC SMs. Therefore, a significant device and loss saving can be attained compared with the traditional MMC with FB SMs. The detailed converter operational analysis, control method, high-voltage direct current simulation model, and scale-down prototype are provided to validate the effectiveness of proposed topology.**

***Index Terms*—Capacitor voltage ripple, dc-fault tolerant capability, line frequency, modular multilevel converter (MMC), self-balancing, voltage source converter (VSC).**

I. Introduction

NOWADAYS, the modular multilevel converter (MMC) has become one of the most promising topologies for medium-voltage (MV) and high-voltage direct current (HVdc) applications [1]–[3]. It possesses the merits of high modularity, enhanced reliability, reduced electromagnetic interference noise, and excellent voltage quality. However, MMC-based HVdc systems still face some challenges. First, the number of devices is doubled with the half-bridge (HB) submodule (SM) and quadrupled with full-bridge (FB) SM compared with the classic two-level voltage source converter (VSC). The use of low-voltage IGBTs in SM results in higher conduction losses. Second, the SM capacitors occupy more than 50% of the weight and size of MMC [4], hence resulting in bulky converters and higher construction cost. Third, MMC with only HB SM does not have the dc-fault tolerant capability [5], and the adoption of FB SM means higher cost and conduction losses.

To address these challenges, some new control methods, revised SM structure, and converter topologies have been proposed [6]–[20]. For example, multiple techniques are proposed to inject appropriate harmonics to the so called "circulating current" to reduce the dc-link capacitor voltage ripple [7], [8], such as the second and fourth harmonic current components. These methods could effectively reduce required capacitance, but the device stress and power losses are increased at the same time [9]. In [10], [11], capacitors of the top and bottom SMs of MMC are paralleled through additional cable, which can eliminate the voltage ripple. However, the other SMs still confront large capacitor voltage ripple, which means the benefit is very limited when there is large number of SMs in MMC used for HVdc applications.

On the other hand, various "hybrid multilevel converters" have evolved recently [12], which are derived with a concept of combining the high-voltage (HV) switches and chain-links (CLs). The HV switches operating in low frequency can generate the basic two- or three-level voltage waveform, while the CLs could shape it into the multilevel sinusoidal waveform. Among the hybrid topologies, the most popular one is the alternate arm converter (AAC) [13], [14], which can be regarded as the integration of MMC and the two-level VSC. It possesses the dc-fault blocking capability and reduces the device number as well as capacitor size compared to the FB-MMC. However, a specific "sweet-spot" operation is required for the voltage balancing, and a big dc-side filter is necessary to remove the dc bus current ripple [15]. An extended-overlap AAC was proposed to overcome these drawbacks at the cost of larger voltage rating of HV switch [16]. In addition to AAC, the hybrid converter with cascaded FB SMs at ac side was proposed to achieve the dc fault tolerance and a smaller size, but increases the semiconductor losses from the two-level structure and more device number in the conduction path [17], [18]. Besides, a family of parallel hybrid converter (PHC) [19], [20] and derived topologies has been proposed with the advantage of PHC and is the lower energy storage requirement. However, the incapability to operate over a wide range of modulation index and the difficult HV transformer design are the major technical challenges. Recently, a family of

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The authors are with the Center for Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA (e-mail: jianl@vt.edu; dongd@vt.edu).

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three-level hybrid MMC (HMMC) [21]–[24] has been proposed under high power factor, this topology can save around 30% devices, 50% total capacitor, and 32% power losses compared to MMC. The power density, efficiency, and construction cost could be improved a lot. But the dc bus commutation capacitor limits the application in the MV range and HMMC cannot ride through the dc fault. In the HVdc applications, the dc-fault blocking capability is quite important and saving the capacitor size can also help to reduce the size as well as the cost. In order to address these two issues, this article tries to combine the conventional two-level VSC and MMC with a similar structure in [10], [11] to obtain a new hybrid-leg MMC (HL-MMC). Instead of using VSC at high switching frequency, the VSC in HL-MMC will follow the line-frequency operation concept in most "hybrid multilevel converters." Therefore, the main contribution of this article is as follows:

1) The proposed HL-MMC combines three-phase HV VSC with CLs. Since the VSC has a common dc-link capacitor for three-phases, the capacitor size could be reduced greatly.
2) The HV VSC operates in line frequency, which eases the challenge of device series connection. In addition, the theoretical value of VSC capacitor voltage rating and the self-balancing strategy are illustrated in detail.
3) The proposed HL-MMC is further revised to utilize the VSC capacitor voltage to oppose the current flow and provide the dc fault blocking capability. Compared to the FB-MMC, this surgeless solution could reduce the required device number and power losses.

The rest of this article is organized as follows. The proposed HL-MMC topology and the basic working principle are illustrated in Section II. The self-balancing scheme and dc-fault ride-through topology are discussed as well. Then, in Section III, HL-MMC is compared with the traditional HB-MMC and FB-MMC to evaluate the performance and benefits. Besides, the simulation results are presented to verify the effectiveness of proposed topology. The experimental results are given in Section IV. Finally, Section V concludes this article.

II. System Overview and Operation Principle

A. Proposed Topology

Fig. 1 depicts the topology of a three-phase HL-MMC with embedded HV VSC. Each phase consists of one upper and lower arm, which is composed of an HV HB branch, a CL based on N series HB SMs, and one arm inductor L_s. The top three-phase HB VSC shares a common dc-link capacitor $C_{\rm vsc}$ of voltage $V_{\rm pvsc}$ via two extra cables. As for the lower arm, a symmetrical configuration is applied, and the bottom VSC dc-link capacitance is also $C_{\rm vsc}$ with rated voltage $V_{\rm nvsc}$. It should be emphasized that the dc-link voltage $V_{\rm p(n)vsc}$ is much higher than the voltage $V_{\rm sm}$ of each SM. Therefore, the HV switch in the VSC needs the series-connected devices.

A simplified average model of the single-phase HL-MMC is presented in Fig. 2(a), where the CLs are replaced with the controlled voltage sources, whereas the VSCs still use the switching models due to the line-frequency operation. Same as

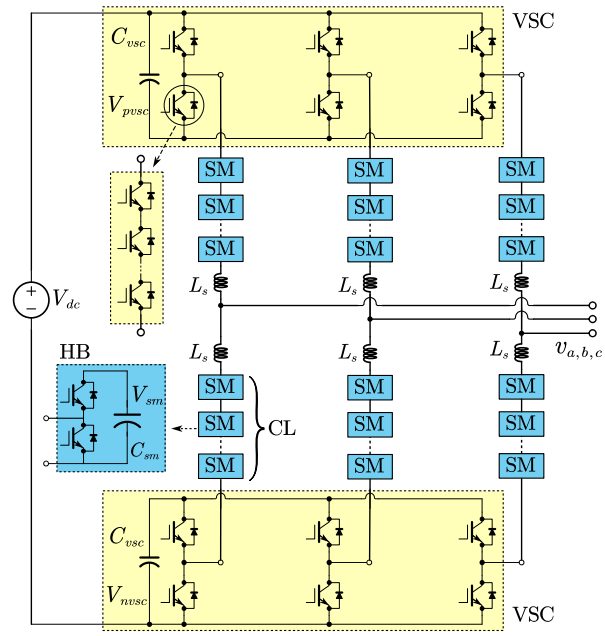

Fig. 1. Structure of three-phase HL-MMC with HV VSCs.

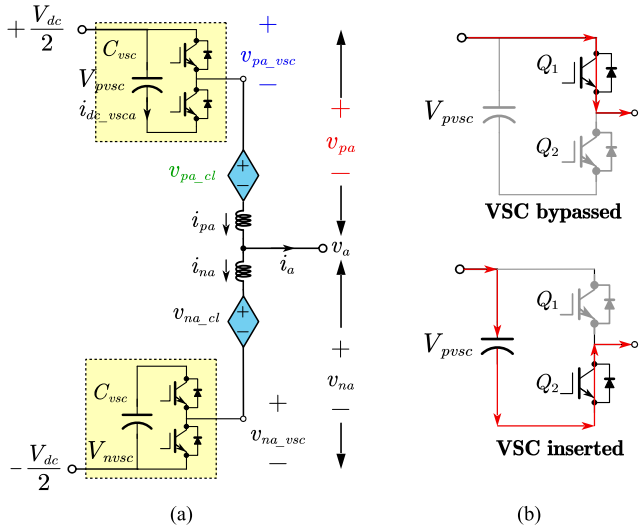

Fig. 2. (a) Simplified model of single-phase HL-MMC. (b) Two working states of top VSC.

the HB SM, there are two working states for HV VSC as shown in Fig. 2(b). When Q_1 is turned ON, the top VSC is bypassed, and when Q_2 is turned ON, it is inserted to the arm.

The arm voltage variables are first defined for classification. v_{pj} and v_{nj} represent the total upper and lower arm voltages of phase j ($j = a, b, c$), respectively. $v_{pj\_\rm vsc}$ and $v_{nj\_\rm vsc}$ denote the VSC output voltages, while $v_{pj\_\rm cl}$ and $v_{nj\_\rm cl}$ are the CL output voltages. As for the current, i_{pj} and i_{nj} refer to the currents of upper and lower arms, respectively. $i_{\rm dc\_vsc}j$ represents to the dc-link capacitor current of top VSC in phase j, which equals to the corresponding arm current when VSC is inserted. Then, the ac side components of phase a are defined as

$$v_a = \frac{M \cdot V_{\rm dc}}{2} \sin(\omega t), \; i_a = I_{\rm ac} \sin(\omega t + \varphi) \tag{1}$$

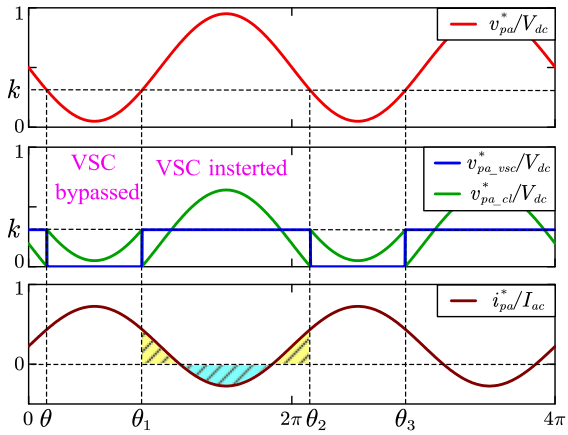

Fig. 3. Waveforms of arm *pa* of HL-MMC with HV VSC.

where M is the modulation index and $I_{\rm ac}$ is the amplitude of ac current. The angular frequency is denoted as ω and the phase angle difference between current and voltage is given by φ.

B. Operation of HV VSC

The operation principle is to keep same arm voltage and current as the traditional MMC [1]–[3] as follows:

$$\begin{cases} v^*_{pa} = \frac{V_{\rm dc}}{2} - v^*_a \\ v^*_{na} = \frac{V_{\rm dc}}{2} + v^*_a \end{cases}, \begin{cases} i^*_{pa} = i_{{\rm cir}a} + \frac{i^*_a}{2} \\ i^*_{na} = i_{{\rm cir}a} - \frac{i^*_a}{2} \end{cases} \tag{2}$$

where i_{cira} is the circulating current flowing in phase a, and should be one-third of the dc-side current with the high-order harmonics suppressed.

Since the arm voltage is the sum of VSC and CL in (3), the key design consideration is the allocation of the voltage between VSC and CL

$$\begin{aligned} v^*_{pa} &= v^*_{pa\_{\rm vsc}} + v^*_{pa\_{\rm cl}} \\ v^*_{na} &= v^*_{na\_{\rm vsc}} + v^*_{na\_{\rm cl}} \end{aligned} \tag{3}$$

Considering the symmetrical structure of the six arms in HL-MMC, the upper arm of phase a is taken as an example for illustration. As shown in (4), the ratio between the VSC dc-link voltage $V_{\rm pvsc}$ and the total dc bus voltage $V_{\rm dc}$ is defined as k

$$k = V_{\rm pvsc}/V_{\rm dc}. \tag{4}$$

In order to reduce the switching frequency of the HV switch in VSC, a simple line-frequency operation scheme is adopted as follows:

$$\begin{aligned} &If\ v^*_{pa} < V_{\rm pvsc}, \text{VSC bypassed} \Rightarrow\ v^*_{pa\_{\rm cl}} = v^*_{pa} \\ &If\ v^*_{pa} \geqslant V_{\rm pvsc}, \text{VSC inserted} \Rightarrow\ v^*_{pa\_{\rm cl}} = v^*_{pa} - V_{\rm pvsc}. \end{aligned} \tag{5}$$

When ${v_{\rm pa}}^*$ is larger than $V_{\rm pvsc}$, VSC is bypassed, and the CL voltage equals to ${v_{\rm pa}}^*$. On the contrary, when it is smaller than $V_{\rm pvsc}$, VSC is inserted, and the CL voltage equals to ${v_{\rm pa}}^* - V_{\rm pvsc}$. In this way, the normalized average waveforms could be plotted in Fig. 3. And for simplification, the VSC capacitor voltage ripple is neglected. Using the proposed scheme, the HV switch in VSC operates at the line frequency, which greatly reduces the difficultly of series device connection and switching loss. From this point of view, the HL-MMC could be regarded as the tradeoff between traditional two-level VSC and MMC.

On the other hand, the maximum voltage stress of CL is also smaller than that of MMC. Therefore, the SM number required in CL will be smaller. And another point worth mentioning is that the ac voltage level is the same as that of the traditional MMC with higher number of SMs.

C. VSC Voltage Range and Self-Balancing Scheme

According to the line-frequency operation of VSC, the capacitor insertion time is closely related with the ratio k, which is not fixed and varies under the different conditions. Therefore, the variation range of k should be determined to design the VSC. Only when the charge and discharge of the VSC capacitor voltage is naturally balanced during the insertion time, can this corresponding coefficient k be selected at this condition.

According to Fig. 2, over one line cycle, only the arm current during the insertion period will charge or discharge the VSC capacitor voltage. In order to derive the general equation for k under different conditions, as shown in Fig. 3, the all the phase angles when ${v_{\rm pa}}^* = V_{\rm pvsc} = kV_{\rm dc}$ are calculated and denoted as $\theta, \theta_1, \theta_2$, and θ_3, respectively. They can be expressed as follows:

$$\begin{aligned} \theta &= \text{asin}\left(\frac{1-k}{M}\right),\ \theta_1 = \pi - \theta \\ \theta_2 &= \theta + 2\pi,\ \theta_3 = 4\pi - \theta. \end{aligned} \tag{6}$$

When the top VSC is inserted between θ_1 and θ_2, its capacitor will be charged with a positive arm current $i_{\rm pa}$ or discharged with a negative $i_{\rm pa}$. Therefore, as long as the blue area of $i_{\rm pa}$ in Fig. 3 equals to the sum of yellow area, the VSC capacitor voltage will be balanced naturally. Then, the equivalent condition is that the integral of arm current during the range of $[\theta_1, \theta_2]$ should be zero

$$f(\theta) = \int_{\theta_1}^{\theta_2} i^*_{pa} d(\omega t) = 0, \theta \in \left[0, \frac{\pi}{2}\right]. \tag{7}$$

Assume that the arm current $i_{\rm pa}$ defined in (2) is not affected by the voltage distribution, then (7) could be simplified and expressed as

$$f(\theta) = \cos\varphi \cdot \left[\frac{M}{2}(\pi + 2\theta) - 2\cos(\theta)\right] = 0. \tag{8}$$

Fig. 4 plots $f(\theta)$ with different modulation index and under unity power factor ($\varphi = 0$). It can be concluded that if HL-MMC works as an inverter ($\cos\varphi > 0$), $f(\theta)$ increases monotonically with larger θ. If the root of $f(\theta) = 0$ is defined as θ_0, any θ smaller than θ_0 will lead to the discharge of $V_{\rm pvsc}$ over the whole line cycle, whereas the θ larger than θ_0 will cause the charge of $V_{\rm pvsc}$. This tendency will be opposite if HL-MMC works as a rectifier ($\cos\varphi < 0$).

Therefore, only when VSC is inserted in the range of ($\pi - \theta_0$, $2\pi + \theta_0$), and $V_{\rm pvsc}$ is set as the value of $k_0 V_{\rm dc}$, can it achieve the natural voltage balancing. This coefficient k_0 could be derived

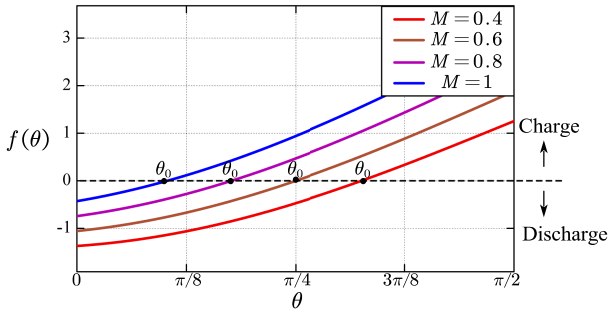

Fig. 4. Plot of $f(\theta)$ with different modulation index M and under unity power factor.

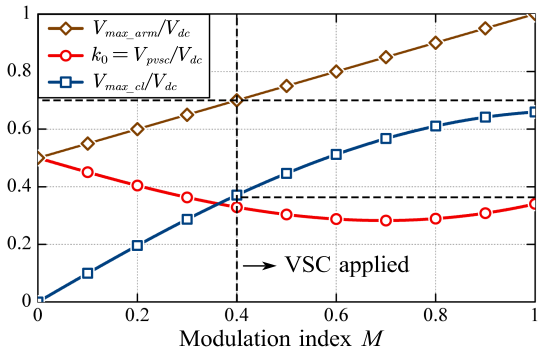

Fig. 5. Relationship between arm voltage stress, ratio k_0, CL voltage stress, and modulation index M.

from

$$k_0 = 1 - M\sin(\theta_0). \tag{9}$$

Then, the normalized maximum CL voltage stress $V_{\max\_cl}$ could be expressed with M and k_0 as

$$\frac{V_{\max\_cl}}{V_{dc}} = \frac{1+M}{2} - k_0. \tag{10}$$

The solution to (7) could be obtained through the numerical calculation. As a result, the tendency of the ratio k_0 and the normalized CL voltage stress with respect to modulation index M are depicted in Fig. 5. It can be observed that $V_{\max\_cl}$ becomes smaller when M is smaller and the largest CL voltage lies on $0.7V_{dc}$ when $M = 1$. Since the VSC works in line frequency, it could be bypassed all the time when M is smaller than 0.4. In this case, only CL is employed to shape the output voltage for good quality. In this way, k_0 could be set as 0.4, and the total arm voltage stress will become $1.1V_{dc}$.

However, the previous analysis is based on the ideal condition, which ignores the arm current harmonics. Actually many nonideal factors, such as the dead-time and control error of the current loop, will distort the arm current. It is impossible to integrate the arm current in real time to determine the accurate insertion time point of VSC. Therefore, a closed-loop feedback control for the VSC capacitor voltage balancing is needed. According to the relationship in Fig. 4, a self-balancing control scheme for the VSC is proposed in this article as shown in Fig. 6. Since the arm energy has been investigated comprehensively in

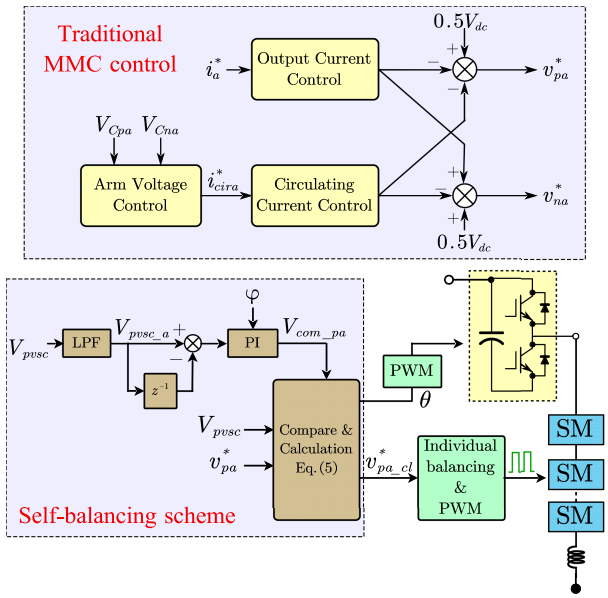

Fig. 6. Proposed self-balancing scheme for upper arm of HL-MMC phase a.

traditional MMC [1]–[4], the arm reference generation $v_{\mathrm{pa}}{}^*$ is not discussed here.

As for the VSC self-balancing part, its voltage is sent to a low-pass filter to obtain the average value $V_{\mathrm{pvsc\_}a}$. And the difference between $V_{\mathrm{pvsc\_}a}$ of the current control cycle and the stored value in the last cycle is sent to a PI controller to get the comparison value $V_{\mathrm{com\_pa}}$. Next, the comparison process and the CL voltage calculation should follow

$$\begin{aligned} If\, v_{pa}^* < V_{\mathrm{com}\_pa} &\Rightarrow v_{pa\_cl}^* = v_{pa}^* \\ If\, v_{pa}^* \geqslant V_{\mathrm{com}\_pa} &\Rightarrow v_{pa\_cl}^* = v_{pa}^* - V_{\mathrm{pvsc}} \end{aligned} \tag{11}$$

The low-level control of CL, such as SM capacitor voltage balancing and multilevel modulation, is same with traditional MMC.

An example in Fig. 7 is taken to illustrate the self-balancing procedure as the inverter. Suppose the initial VSC voltage ratio k_1 is lower than the desired value k_0 and the initial output of PI controller is set as k_1V_{dc}. According to (6), the $\theta_1{}'$ will be larger than the corresponding root θ_0 of $f(\theta) = 0$. As a result, the VSC energy will be charged from E_1 to E_2 after first cycle. Then, the difference value of VSC voltage is accumulated through the PI controller, so that the output comparison value $V_{\mathrm{com\_pa}}$ is increased to k_2V_{dc}, which is still lower than k_0V_{dc}. Therefore, the same charging effect will be applied again. Once the VSC voltage is stabilized after a certain number of cycles, the difference between two cycles becomes zero. It implies that VSC reaches k_0V_{dc} automatically, and θ_0 is obtained by itself as well. Note that the polarity of the PI controller should switch according to the inverter and rectifier mode.

D. Three-Phase HL-MMC and DC-Fault Tolerant HL-MMC 2

In fact, the aforementioned single-phase HL-MMC does not show a big benefit compared to the traditional MMC because

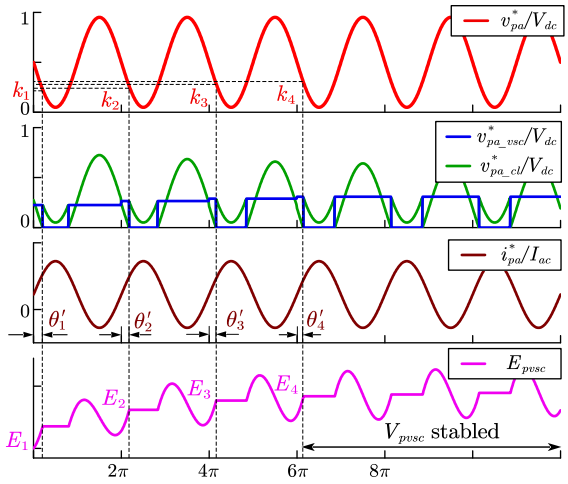

Fig. 7. Illustration of variable changing procedure when self-balancing scheme is applied.

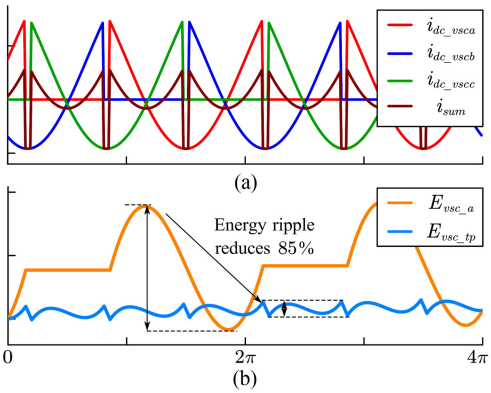

Fig. 8. Waveforms of HV VSC. (a) Three-phase dc-link capacitor currents. (b) Energy ripple of single-phase and three-phase configuration.

the same amplitude of arm energy ripple is distributed between VSC and CL. As a result, the total capacitor energy storage requirement does not change. However, when top three HV HBs are paralleled together to share a common dc-link capacitor, the total dc-link current could be cancelled as shown in Fig. 8. In this figure, $i_{\rm sum}$ is the sum of three-phase dc-link currents when three-phase VSC are connected in parallel. It can be observed that the capacitor energy ripple $E_{\rm vsc\_tp}$ of three-phase configuration is much lower that of single-phase configuration $E_{\rm vsc\_a}$ due to the harmonic cancellation. The detailed energy storage calculation and comparison with traditional MMC will be performed in next section.

In addition to the capacitor reduction, this three-phase VSC structure could be utilized to save device number in the proposed HL-MMC 2 with dc fault blocking capability. As shown in Fig. 9(a), one active switch S_p, free-wheeling diode D_p, and damping resistor R_p are added to the top VSC. A symmetrical circuit is added to the bottom VSC too. In the normal operation, S_p and S_n are turned ON to conduct large dc bus current, so that HL-MMC 2 can operate as described in the aforementioned analysis. When the dc fault happens, S_p and S_n should be turned

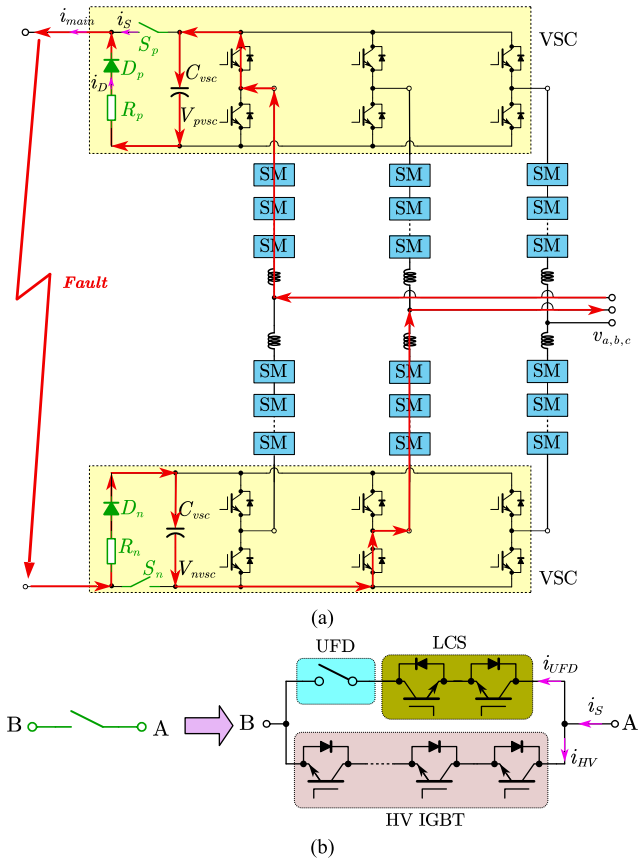

Fig. 9. (a) Topology of three-phase HL-MMC 2 with dc fault tolerant capability. (b) Structure of the active switch S_p and S_n.

OFF to divert the fault current to free-wheeling branch of diode and damping resistor. In this case, they need to withstand the HV VSC voltage at the OFF-state. In this article, one structure similar to the hybrid circuit breaker (HCB) [25], [26] is proposed for S_p and S_n to improve the conduction loss as shown in Fig. 9(b). The ultra-fast disconnector (UFD) and the series-connected load commutation switch (LCS) are responsible for the normal current conduction. The low resistance feature of UFD could save the conduction loss significantly. While the LCS is typically composed of only few series-connected IGBTs because withstanding the entire voltage is unnecessary. The HV branch should interrupt the peak fault current and withstand the peak voltage of $V_{\rm vsc}$.

Fig. 10 depicts the current and voltage waveforms of the HL-MMC 2 during the interruption of the dc fault current. $i_{\rm main}$ is the dc bus current of the MMC, and $i_{\rm S}$ denotes the current of switch S_p, which equals to the sum of UFD branch current $i_{\rm UFD}$ and HV IGBT branch current $i_{\rm HV}$. i_D refers to the current of diode D_p. The detailed dc fault blocking process is explained as follows:

1) t_0–t_1: The dc fault occurs at t_0, then $i_{\rm main}$ increases from $-I_{\rm dc}$ immediately, whose di/dt is limited by the arm inductor. The VSC capacitor is also discharged due to this surge current. After the overcurrent is detected at t_1, all devices of SM and HV VSC are turned OFF, so that the fault current can only flow through the antiparallel diode.

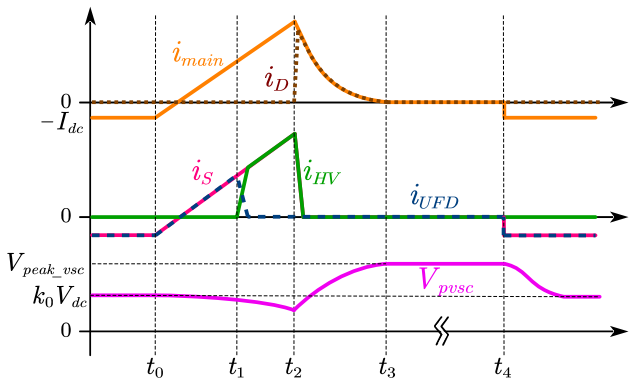

Fig. 10. Waveforms of each branch during interrupting dc fault current.

2) t_1–t_2: The LCS is turned OFF at t_1 to commutate the current of UFD to HV IGBT branch, and UFD can start to open the mechanical contactor without arc. Then, the dielectric strength across the contactor increases gradually, and after it exceeds $V_{\rm pvsc}$, the HV IGBT branch is turned OFF at t_2. It is worth mentioning that IGBT has a high surge current capability, hence the device with smaller current rating could be selected for HV IGBT [27], [28].
3) t_2–t_3: The fault current is transferred to the diode branch and charges the VSC capacitor. The VSC is charged gradually, and the damping resistor can help to absorb the energy from the line and arm inductor. The fault current is also reducing, which follows the KVL equation of (12). A possible current flow path from phase a to phase c is also given in Fig. 9(a)

$$v_{\rm ac} = L_s \frac{di_{\rm main}}{dt} + V_{\rm pvsc} + R_p i_{\rm main}$$
$$V_{\rm pvsc} = k_0\, V_{\rm dc} + \frac{1}{C_{\rm vsc}} \int i_{\rm main} dt \tag{12}$$

where $v_{\rm ac}$ is the output six-pulse voltage of a three-phase rectifier. At t_3, the VSC capacitor is charged to the peak voltage $V_{\rm peak\_vsc}$ as

$$V_{\rm peak\_vsc} = \frac{\sqrt{3}}{4}\,{\rm MV_{dc}} \approx 0.433 V_{\rm dc}. \tag{13}$$

Therefore, the HV VSC could be designed as $0.5V_{\rm dc}$ in HL-MMC 2. Compared to the conventional HCB with metal oxide varistor (MOV), this solution could save the device number of HV IGBT branch. Because the dc voltage of MOV should be higher than $V_{\rm dc}$ to avoid high leakage current and power loss, and the corresponding clamping voltage is usually around $1.8V_{\rm dc}$–$2V_{\rm dc}$.

1) t_4: After the dc fault is cleared at t_4, S_p and S_n are turned ON, and VSC and all SMs recover the normal operation. With the help of self-balancing strategy, $V_{\rm pvsc}$ will reduce gradually to the balancing value $k_0V_{\rm dc}$ again.

TABLE I
ELECTRICAL PARAMETERS OF DESIGNED HVDC CONVERTER

Description	Symbol	Value
Rated power	S (MVA)	200
Ac Line-voltage (RMS)	V_{LL_rms} (kV)	115
Ac frequency	f_{in} (Hz)	60
Dc bus voltage	$V_{\rm dc}$ (kV)	200
Power factor	PF	-π ~ π
SM capacitor voltage	$V_{\rm sm}^*$ (kV)	2.3
Balanced VSC voltage ratio	k_0	0.31
Capacitor voltage ripple ratio	ε	10%
Damping resistor	$R_{\rm p}$, $R_{\rm n}$ (Ω)	10
SM device	FZ825R33HE4D	3.3 kV / 825 A
VSC device	FZ750R65KE3	6.5 kV /750 A

III. PERFORMANCE COMPARISON AND SIMULATION STUDY

As mentioned earlier, the biggest advantage of HL-MMC is the reduced capacitor and power losses with HV VSC. In order to evaluate its performance of under different operating conditions, an HVdc case is designed and the corresponding electrical parameters are listed in Table I. Since the rated modulation index M is 0.94, the ideal balanced VSC voltage ratio k_0 based on (6) and (7) could be calculated as 0.31.

A. Comparison Between HL-MMC and MMC

The CL voltage stress is directly related to the device number used in SM. In this article, the Infineon IGBT module (FZ825R33HE4D) [29] is adopted for the SM power device, and it features a maximum collector–emitter voltage of 3.3 kV and continuous dc collector current of 825 A. The number of SMs in each CL is selected as follows so that the dc-link capacitor voltage $V_{\rm sm}^*$ does not exceed 2.3 kV:

$$N_{\rm sm} = \frac{V_{\rm max\_cl}}{V_{\rm sm}^*} = \frac{V_{\rm max\_cl}}{2.5{\rm kV}}. \tag{14}$$

In traditional HB- and FB-MMC, $V_{\rm max\_cl}$ equals to $V_{\rm dc}$, whereas in HL-MMC, it equals to $0.7V_{\rm dc}$. As for the HV VSC and HV IGBT branch in S_p and S_n, the 6.5 kV commercial devices are selected due to the smaller device number. As explained earlier, the maximum VSC voltage $V_{\rm max\_vsc}$ is designed as $0.4V_{\rm dc}$ in HL-MMC and $0.5V_{\rm dc}$ in HL-MMC 2. Note that the device in LCS is neglected, and a voltage margin of 30% is designed for series device $N_{\rm vsc}$ used in each IGBT stack

$$N_{\rm vsc} = \frac{V_{\rm max\_vsc}}{70\% * 6.5{\rm kV}}. \tag{15}$$

In this way, the total required devices and number of different voltage ratings are summarized in Fig. 11. It can be observed that around 10% device is reduced from HB-MMC to HL-MMC. On the other hand, HL-MMC 2 is able to reduce around 48% total device compared to FB-MMC, which decreases the construction cost significantly.

Capacitors in MMC are also one of the most important factors affecting the power density and cost. The SM dc-link capacitor value in the CL could be expressed as

$$C_{\rm sm} = \frac{\Delta E_{\rm cl}}{2N\varepsilon V_{\rm sm}^{*\,2}} \tag{16}$$

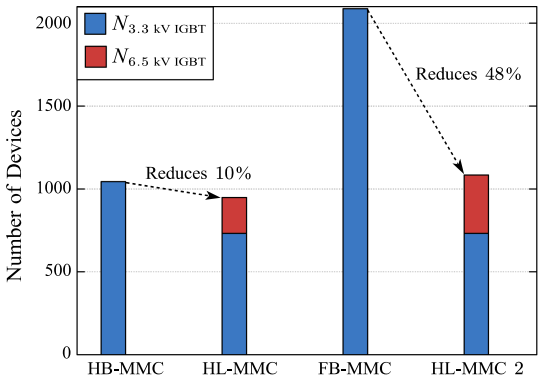

Fig. 11. Comparison of devices number.

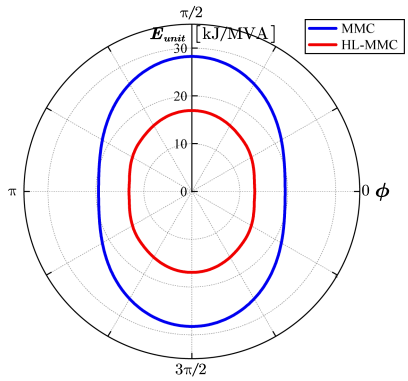

Fig. 12. Numerical analysis of the total energy requirement (in kJ/MVA) in the HL-MMC and MMC, depending on the ac current phase angle.

where $\Delta E_{\rm cl}$ is the maximum energy deviation of CL over one fundamental period, and ε is the maximum voltage ripple ratio in per unit. Similarly, the dc-link capacitor of VSC can be calculated as

$$C_{\rm vsc} = \frac{\Delta E_{\rm vsc}}{2\varepsilon (k_0 V_{\rm dc})^2} \tag{17}$$

where $\Delta E_{\rm vsc}$ is the maximum energy deviation of VSC over one fundamental period. In this way, the total energy storage requirement for per unit apparent power in HL-MMC is derived as

$$E_{\rm unit} = \frac{\left(6N\frac{C_{\rm sm}V_{\rm sm}^{*\,2}}{2} + 2\cdot\frac{C_{\rm vsc}(k_0V_{\rm dc})^2}{2}\right)}{S} = \frac{3\Delta E_{\rm cl} + \Delta E_{\rm vsc}}{2\varepsilon S}. \tag{18}$$

The power factor has an influence of CL current and the total dc-link current of VSC. Assuming $\varepsilon = 10\%$, the relationship between energy storage $E_{\rm unit}$ and phase angle φ is plotted in Fig. 12 . Compared with MMC, 30% capacitor could be saved in HL-MMC at unity power factor and 40% at power factor of 0.

In order to compare these converters about the efficiency, the semiconductor losses are calculated. Since the switching loss is much lower than the conduction loss, it is neglected in this article. Besides, the voltage level of HL-MMC is same with MMC even with fewer SMs, which means the switching frequency of HL-MMC could be selected same with HB-MMC.

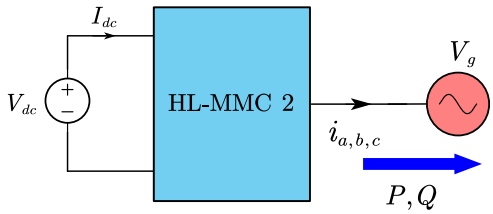

Fig. 13. Simulation model of grid-connected HL-MMC 2.

TABLE II
LOSS COMPARISON

Topology	HB-MMC	HL-MMC	FB-MMC	HL-MMC 2
Losses (MW)	1.14	1.02	2.28	1.21

TABLE III
PERFORMANCE SUMMARY OF FOUR TOPOLOGIES

Topology	HB-MMC	HL-MMC	FB-MMC	HL-MMC 2
Device	1 p.u.	0.9 p.u.	2 p.u.	1.04 p.u.
Capacitor	1 p.u.	0.7 p.u.	1 p.u.	0.7 p.u.
Losses	1 p.u.	0.89 p.u.	2 p.u.	1.06 p.u.

For simplification, the ON-state voltage drop of IGBT and the antiparallel diode are assumed to be same. Therefore, the conduction loss for six CLs in MMC and HL-MMC can be derived as

$$P_{\rm con\_cl} = \frac{6}{2\pi}\int_0^{2\pi} \left(N_{\rm sm}\cdot v_{\rm LV\_IGBT}\cdot |i_{\rm pa}|\right) d(\omega t) \tag{19}$$

where $v_{\rm LV\_IGBT}$ represents the ON-state voltage drop of LV IGBT used in SM. As for the VSC, two IGBT stacks Q_1 and Q_2 of each HB conduct the current $i_{\rm pa}$ alternately. Therefore, their conduction losses can be combined and calculated as

$$P_{\rm con\_vsc} = \frac{6}{2\pi}\int_0^{2\pi} \left(N_{\rm vsc}\cdot v_{\rm HV\_IGBT}\cdot |i_{pa}|\right) d(\omega t) \tag{20}$$

where $v_{\rm HV\_IGBT}$ represents the ON-state voltage drop of HV IGBT used in VSC. On another aspect of HL-MMC 2, the LCS IGBT number is low and the resistance of UFD is very small, so their conduction losses are neglected here. In this way, the losses of various topologies with this calculation method at unity power factor are summarized in Table II. Benefiting from the lower ON-state voltage drop of HV IGBT, the power losses of HL-MMC are relatively smaller. While HL-MMC 2 shows 47% loss reduction due to the smaller number of power devices.

The overall performance of four topologies is summarized in Table III. Compared to HB-MMC, HL-MMC can save 10% devices, 30% capacitor, and 11% losses, whereas HL-MMC 2 can achieve better results compared to FB-MMC.

B. Simulation Verification

In order to validate the functionality of proposed HL-MMC 2, an HV simulation model is built as shown in Fig. 13 with the main circuit parameters listed in Table I. The dc side and ac side are connected to two voltage sources to verify the operation of both inverter and rectifier. The positive power flow is defined from the dc source to ac source.

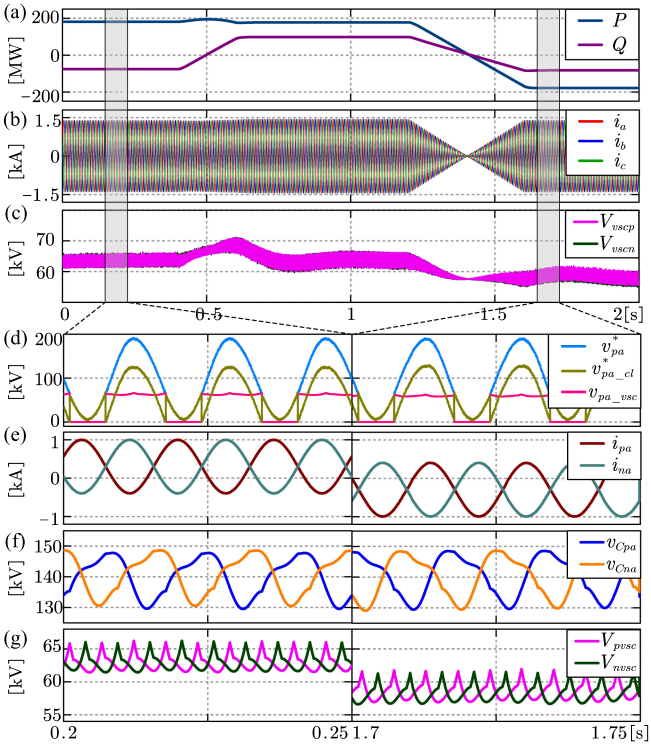

Fig. 14. Dynamic response to the change in active and reactive power commands and zoomed-in waveforms: (a) delivered active and reactive power, (b) ac side currents, (c) VSC capacitor voltage, (d) phase a upper CL, VSC, and total output voltages, (e) phase a upper and lower arm CL currents, (f) phase a upper and lower CL capacitor voltages, and (g) zoomed in VSC capacitor voltage.

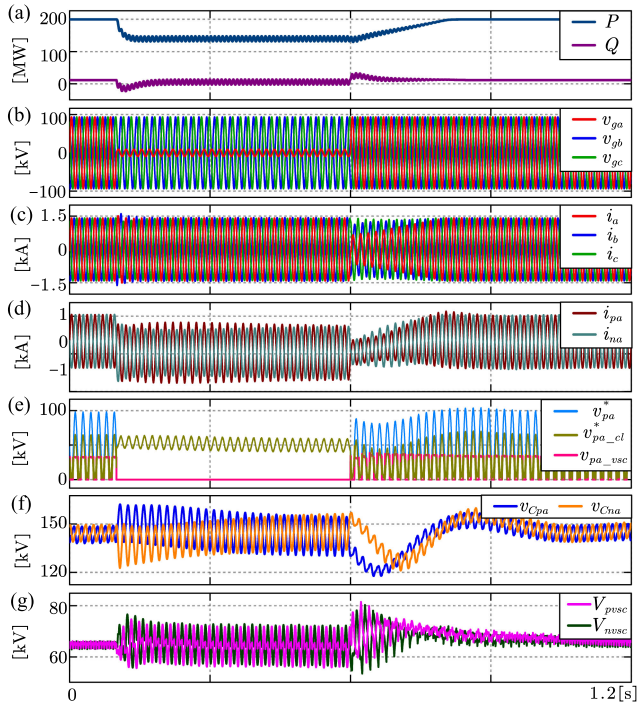

Fig. 15. Dynamic response to the asymmetrical ac fault: (a) delivered active and reactive power, (b) ac side voltages, (c) ac side currents, (d) phase a upper and lower CL currents, (e) phase a upper CL, VSC, and total output voltages, (f) phase a CL capacitor voltages, and (g) VSC capacitor voltages.

In the first case of constant apparent power, the reactive power reference ($Q*$) is ramped up from -76 to 76 MVAr at 0.4 s, and the apparent power is ramped down from 200 to -200 MVA at 1.4 s. Consequently, the dynamic responses of ac currents and VSC capacitor voltages in HL-MMC are obtained and presented in Fig. 14(b). It can be seen that the VSC capacitor voltage is stabled at any condition due to the self-balancing control. To further illustrate the steady-state performance, several zoomed-in waveforms are shown in Fig. 14(d)–(g). The upper arm voltage distribution of phase a is generated according to (5) and is shown in Fig. 14(d). The CL voltages are adjusted to regulate the arm currents in Fig. 14(e). The CL and VSC capacitor voltages in Fig. 14(f) and (g) are stabled at the rated value, which indicates the effectiveness of the voltage balancing scheme.

This hybrid converter topology, which does not have the issue of ac- and dc-sides coupling existed in AAC, can also ride through the severe ac faults. The results of HL-MMC 2 during an asymmetrical ac fault are presented in Fig. 15. A temporary ac fault is emulated by reducing the voltage amplitude of phase a to 10% at 0.1 s and the fault is cleared at 0.6 s as shown in Fig. 15(b). In order to keep the ac side currents in Fig. 15(c) stable, the active power reference of phase a is changed to 0.1 p.u. after the fault occurs. Due to the existence the negative sequence voltage, the second-order ripple occurs in the active and reactive power in Fig. 15(a). Since the modulation index is low for phase a, the VSC is always bypassed for this phase and the arm voltages in Fig. 15(e) are supported only by the CLs. Note that the voltage ripple of CL capacitor in Fig. 15(f) becomes larger when the modulation index reduces. This also happens to the VSC capacitor because the three-phase dc-link currents cannot cancel with each other. Obviously, this simulation validates the capability of HL-MMC 2 to ride through the temporary ac faults.

In addition to the ac fault, another challenge for the traditional MMC is the dc fault, which is also simulated for HL-MMC 2 in Fig. 16. At 0.2 s, a pole-to-pole dc bus short-circuit happens, and the ac grid starts to discharge through the dc side. As a result, the dc bus current is decreasing quickly and triggers the protection threshold at 0.201 s as shown in Fig. 16(b). Then, the active switch S_p and S_n are turned OFF and the fault current is commutated to the VSC capacitor and diode branch in Fig. 16(h). At 0.213 s, the fault current decays to zero, and the VSC capacitor in Fig. 16(i) is charged to the peak voltage. After the fault is cleared at 0.5 s, a soft-start is enabled to make the system resume the normal operation and the VSC capacitor voltages returns to the balanced value again.

IV. Experimental Results and Derived Topologies

A. Experimental Results

The working principle and performance of the proposed HL-MMC is also validated using a laboratory prototype. The circuit parameters are listed in Table IV and the setup is shown in Fig. 17. The whole system is controlled by digital signal processor TMS320F28388, and each CL has three HB SMs.

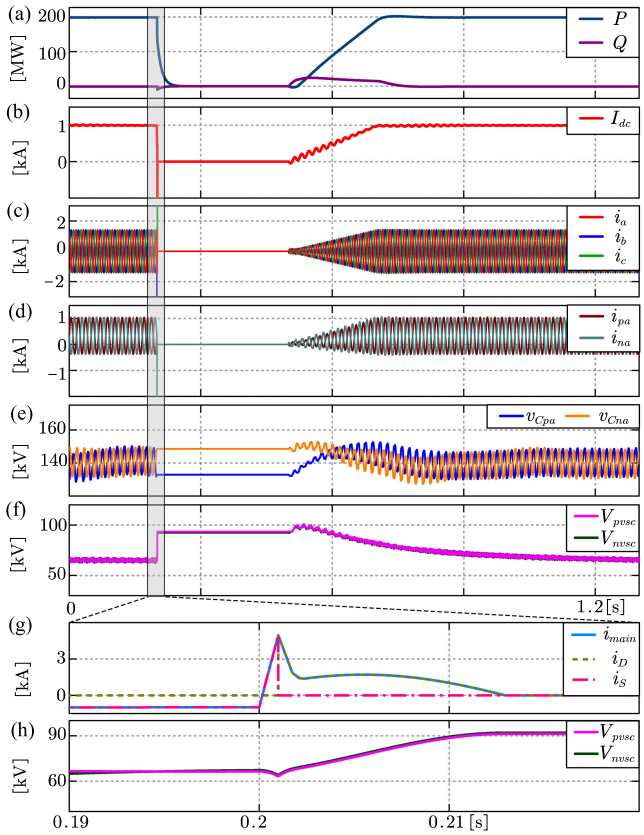

Fig. 16. Dynamic response to dc fault and soft start process: (a) delivered active and reactive power, (b) dc side current, (c) ac side currents, (d) phase *a* upper and lower CL currents, (e) phase *a* CL capacitor voltages, (f) VSC capacitor voltages, (g) zoomed-in circuit breaker currents, and (h) zoomed-in VSC capacitor voltages.

TABLE IV
ELECTRICAL PARAMETERS OF HL-MMC SYSTEM

Parameters	Symbol	Values
Ac voltage amplitude (phase)	V_o	180 V
Rated ac frequency	f_o	60 Hz
Dc bus voltage	V_{dc}	400 V
Arm inductance	L_{arm}	3 mH
SM voltage	V_{CSM}	100 V
SM capacitance	C_{SM}	1.32 mF
Number of HB SM per CL	N_h	3
Carrier frequency	f_c	14.4 kHz
VSC capacitance	C_{vsc}	0.45 mF

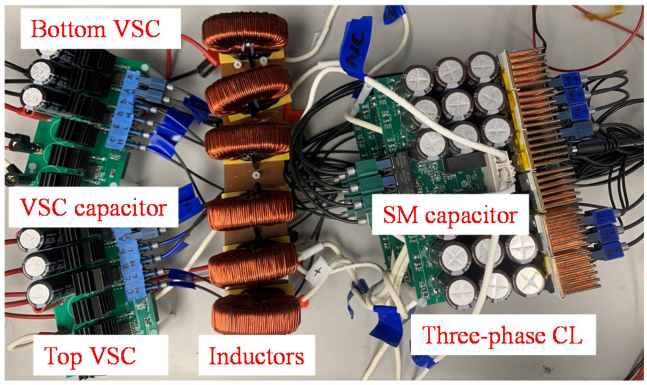

Fig. 17. Picture of laboratory HL-MMC prototype.

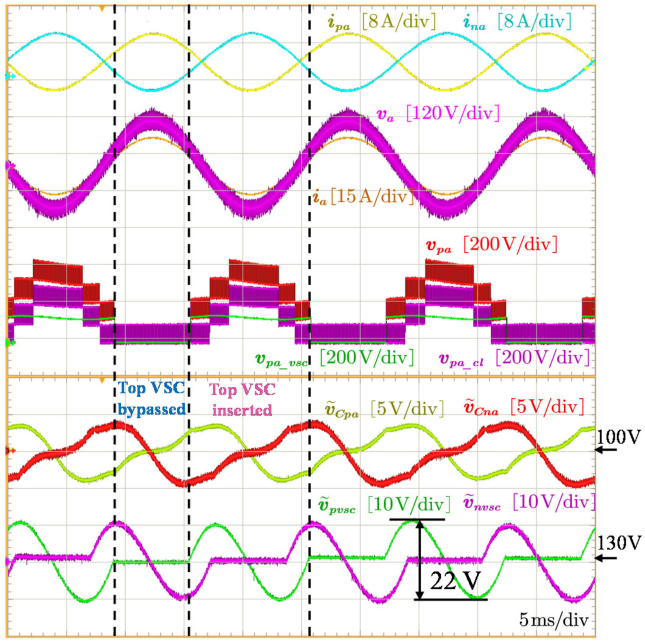

Fig. 18. Waveforms of single-phase HL-MMC with three SMs.

The SM capacitor and arm currents sampling results are sent back to the controller through the serial peripheral interface communication. All the SM PWM commands, VSC firing, and communication signals are transmitted through the fiber. The VSC capacitance is much smaller than that of SM, considering that the three-phase VSCs share a common one. Results and key observations from this prototype of the steady state and transient conditions are provided to confirm the operating and control schemes.

The steady-state waveforms of single-phase HL-MMC are shown in Fig. 18. The ac side current is sinusoidal as desired, which indicates the good design of current loop parameter. It can be seen that the arm voltage level is not reduced with only three HB-SMs. As explained earlier, the VSC is bypassed or inserted alternately. And when it is inserted, the capacitor is charged and discharged according to the arm current polarity, which matches with the capacitor ripple tendency. With the help of self-balancing scheme, the average value of VSC capacitor voltage is balanced pretty well.

In order to show the feasibility of HV-VSC at higher voltage, the phase *b* SMs are connected in series with phase *a* so that the dc voltage is increased to 800 V. It can be seen from Fig. 19 that the similar VSC operation is applied and the multilevel waveforms are obtained. The self-balancing strategy of VSC capacitor is still effective in the case of HV operation.

Once the three-phase VSC are connected in parallel, the corresponding waveforms are given in Fig. 20. The three-phase currents and dc current are controlled pretty well with low harmonic contents. Most importantly, the amplitude of VSC capacitor voltage fluctuation is reduced from 22 to 5 V successfully. It verifies the benefits of the three-phase HL-MMC.

In order to evaluate the dynamic response of this system, the reference of ac voltage is reduced from 180 to 100 V suddenly

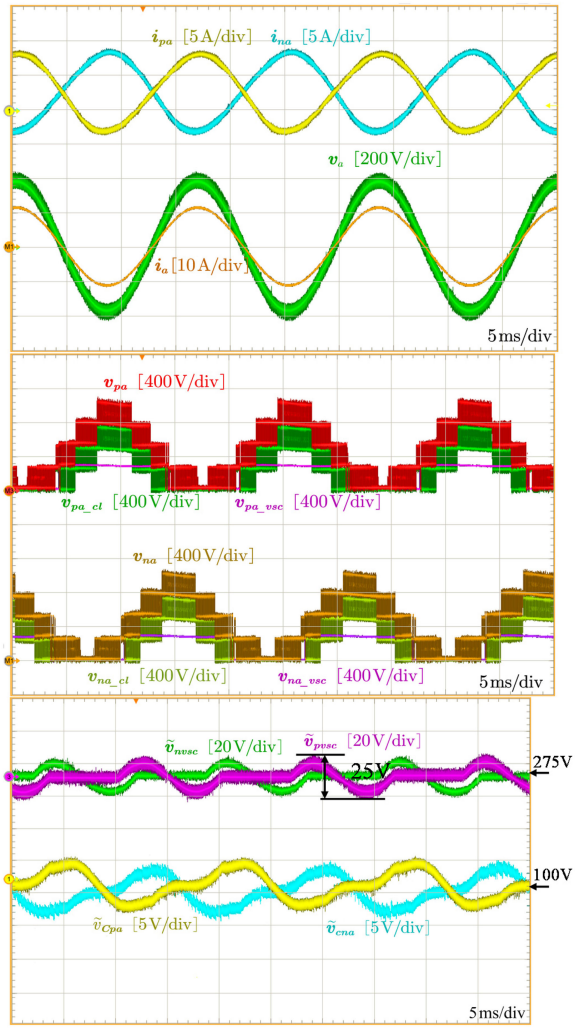

Fig. 19. Waveforms of single-phase HL-MMC with six SMs.

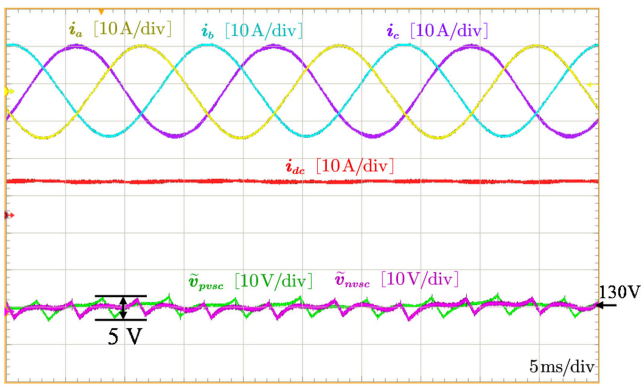

Fig. 20. Waveforms of three-phase HL-MMC.

as shown in Fig. 21. It can be observed that the average values of V_{pvsc} and V_{nvsc} stable at a new balanced value after the step change. The voltage ripple is larger due to the smaller modulation index, which is same with the simulation results in Fig. 15.

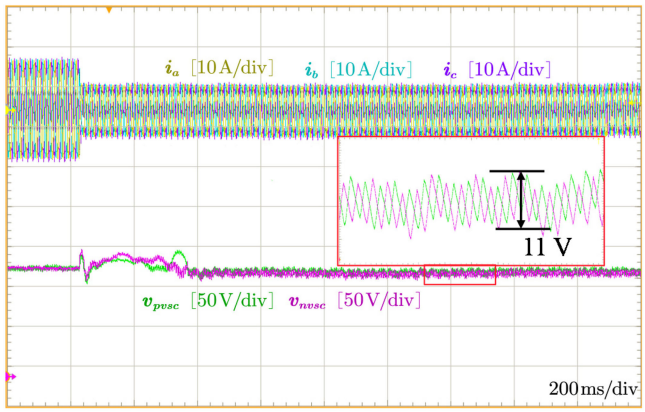

Fig. 21. Dynamic response to step change of ac voltage reference.

V. Conclusion

This article presents a new HL-MMC with reduced capacitor and dc-fault blocking capability. It is derived by integrating the line-frequency commutated HV VSC and high-frequency chopping CLs together. And the parallel connection of three-phase VSC achieves a significant reduction of the capacitance due to the current cancellation. Besides, the proposed self-balancing scheme shows a good performance according to the simulation and experimental results. Furthermore, an HL-MMC with the dc-fault tolerant capability is introduced by utilizing the HV VSC capacitor. Such a surgeless structure can save the required device number greatly compared to the FB-MMC. The performance evaluation demonstrates that this HL-MMC can save around 48% device number, 30% capacitor, and 47% losses compared to the FB-MMC. Above all, the proposed HL-MMC has great potential to replace the traditional MMC in the MV and HV power conversion and transmission applications to realize a higher power density and efficiency.

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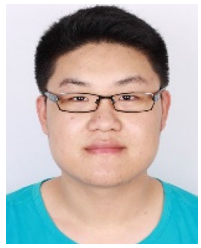

Jian Liu (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering from the Zhejiang University, Hangzhou, China, in 2016 and 2019, respectively. He is currently working toward the Ph.D. degree with the Center for Power Electronics Systems, Virginia Tech, Blacksburg, VA, USA.

His research interests include multilevel converters and Hybrid dc circuit breaker.

Mr. Liu is the recipient of the Best Paper Award of ECCE-Asia 2020 and the Outstanding Presentation Award of APEC 2021.

Dong Dong (Senior Member, IEEE) received the B.S. degree from the Tsinghua University, Beijing, China, in 2007, and the M.S. and Ph.D. degrees in electrical engineering from the Virginia Tech, Blacksburg, VA, USA, in 2009 and 2012, respectively.

From 2012 to 2018, he was with the GE Global Research Center, Niskayuna, NY, USA, as an Electrical Engineer. At GE, he participated in and led multiple technology programs including MV/HVdc power distribution and power delivery, SiC high-frequency high-power conversion systems, solid-state transformers, and energy storage system. Since 2018, he has been with the Bradley Department of Electrical and Computer Engineering, Virginia Tech. He has authored or coauthored more than 30 referred journal publications and more than 80 IEEE conference publications. He currently holds 30 granted U.S. patents. His research interests include wide-band-gap power semiconductor-based high-frequency power conversion, soft-switching and resonant converters, high-frequency transformers, and MV and HV power conversion system for grid, renewable, and transportation applications.

Dr. Dong was the recipient of the GE Gold Medallion Patent Award and GE Technology Transition Awards. He is currently an Associate Editor of IEEE TRANSACTIONS ON POWER ELECTRONICS. He was the recipient of two prize paper awards from the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS, William Portnoy Prize Paper Award from IEEE IAS, and NSF CAREER Award. He has served as the Vice Chair of IEEE Industry Application Society Schenectady Region Chapter in 2017 and General Chair of IEEE International Conference on DC Microgrids in 2021.