A Hybrid Model Predictive Control With Integrated Phase-Disposition and Phase-Shifted PWM for an Inner-Interleaved Hybrid Multilevel Converter

Yufei Li, *Member, IEEE*, Fei Diao, *Student Member, IEEE*, Yue Zhao, *Senior Member, IEEE*, and H. Alan Mantooth, *Fellow, IEEE*

***Abstract*—This article puts forward a hybrid model predictive control (H-MPC) for an inner-interleaved hybrid multilevel converter (IHMC). The sign patterns of the original and shifted reference vectors in the original and virtual space vector diagrams (VSVDs) are used, respectively, to realize the phase-disposition pulsewidth modulation (PWM) and determine the low-frequency switching states. Then, the three adjacent vectors are selected in the second-layer VSVD and the optimal current tracking is safeguarded by the duty cycle optimization of the three adjacent vectors. Finally, through applying the phase-shifted PWM to the two interleaved legs, a constant and doubled equivalent switching frequency can be achieved, which further paves the way for dc-link and floating capacitor voltages balancing and circulating current mitigation with the use of the straightforward duty cycle adjustments. The proposed H-MPC enables the decoupling of the low- and high-frequency stages in the IHMC and also reduces both output current ripples and computational burden while achieving a constant switching frequency simultaneously. Comprehensive simulation and experimental studies on an all silicon carbide prototype verify the effectiveness of the proposed control strategy.**

***Index Terms*—Hybrid multilevel converter (HMC), inner-interleaved, model predictive control (MPC).**

Nomenclature

HMC	Hybrid multilevel converter.
CHB	Cascaded H-bridge.
MMC	Modular multilevel converter.
ANPC	Active-neutral-point-clamped converter.
FPGA	Field programmable gate array.
IHMC	Inner-interleaved hybrid multilevel converter.
PEBB	Power electronic building block.
SVD/VSVD	Space vector and virtual space vector diagram.
MPC	Model predictive control.
C/H-MPC	Conventional/hybrid model predictive control.
LFS/HFS	Low-/high-frequency stage.
PWM	Pulsewidth modulation.
PD-PWM	Phase-disposition pulsewidth modulation.
PS-PWM	Phase-shifted pulsewidth modulation.
SVM	Space vector modulation.
THD	Total harmonic distortion.
j	Three phases, $j \in \{a, b, c\}$.
x	Power switch index, $x \in \{1, 2, \ldots, 10\}$.
m, n	Indices of the VSVDs, $m, n \in \{1, \ldots, 6\}$.
R, L	Load resistance and inductance.
$U_{\rm dc}$	External dc-source voltage.
$u_{\rm dc\_1}$, $u_{\rm dc\_2}$	DC-link capacitor voltages.
$\Delta u_{\rm dc}$	Deviation of dc-link capacitor voltages.
L_0, $L_{\rm eq}$	Interleaved and equivalent inductance.
C, C_1	DC-link and floating capacitance.
$u_{{\rm dc}\_j1}$, i_{fj}	Voltages and currents of floating capacitors.
$i_{\rm dc\_1}$, $i_{\rm dc\_2}$	Currents of the dc-link capacitors.
i_{oj}, i_o	Three-phase and total neutral point currents.
i_j, i_{cj}	Converter phase and circulating currents.
i_{j1}, i_{j2}	Currents of the interleaved legs.
u_{jo1}, u_{jo2}	Voltages of the interleaved legs.
M_{jx}	Power switches in each phase.
S_j, S_{jx}	Switching states of phase j and power switches.
d_{jx}	Duty cycles of the power switches.
T_s	Control or sampling period.
$\boldsymbol{v}$, $\boldsymbol{i}$	Converter voltage and current vectors.
$y(k)$	Variable y at k time instant.
v_j	Equivalent output voltages of the IHMC.
$v_{j79}{}^*$	Reference modulation wave of M_{j7}/M_{j9}.
θ_0	Phase angle of the PD-PWM modulation wave.
v_{ma}, M	Modulation wave/index of the equivalent voltage.
ω, φ	Angular frequency and current initial phase.
$\boldsymbol{v}^*$	Reference vector in the $\alpha\beta$-frame.
$\boldsymbol{v_{\rm I}}^*$, $\boldsymbol{v_{\rm II}}^*$	First- and second-layer virtual reference vector.
$\boldsymbol{V_{\rm I}}$, $\boldsymbol{V_{\rm II}}$	First- and second-layer transfer vectors.
$\boldsymbol{VV_i}$	Chosen adjacent virtual vectors.
t_i, dd_i	Dwell time and duty cycles of the virtual vectors.
S_{jv79}	Virtual switching states of S_{j7}/S_{j9}.
d_{jv79}	Virtual duty cycles of M_{j7}/M_{j9}.

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Yufei Li is with the Department of Electrical and Computer Engineering and Andlinger Center for Energy and the Environment, Princeton University, Princeton, NJ 08544 USA (e-mail: yl5385@princeton.edu).

Fei Diao, Yue Zhao, and H. Alan Mantooth are with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR 72701 USA (e-mail: feidiao@uark.edu; yuezhao@uark.edu; mantooth@uark.edu).

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S_{jv79_i}	The *i*th virtual switching state of S_{j7}/S_{j9}.
$dd_{j5/7/9}$	Transition duty cycles of M_{j5} and M_{j7}/M_{j9}.
k_{np}	Coefficient of dc-link voltages.
$k_{j\mathrm{cir}}$	Coefficient of circulating current.
d_{np}	Duty cycle adjustment for dc-link voltages.
$d_{j\mathrm{cir}}$	Duty cycle adjustment for circulating current.

I. Introduction

THE emerging hybrid multilevel converter (HMCs) [1] find widespread applications in the renewable energy generation systems [2], [3], electric power transmission systems [4], electrified transportation systems [5], etc. Compared with the multilevel converters using one particular PEBB [6], HMCs enjoy the merits of various PEBBs thanks to the arbitrary combination of them [7]. In particular, the inner-interleaved hybrid multilevel converter (IHMCs), with the partially inner-interleaved topology, feature additional benefits such as increased output voltage level, reduced device current stress, modularity [8], etc. Despite indisputable advantages, the integration of various PEBBs complicates the control of HMCs, especially the IHMCs, which therefore, needs in-depth research to enhance the controller in dealing with multiple control objectives, such as capacitor voltages regulation, output current quality improvement, and inner-circulating current suppression.

To date, the control of HMCs predominately uses the PD-pulsewidth modulation (PWM) [9], PS-PWM [10], [11], or SVM [3], [12], which, although simple and mature, suffers from inherent drawbacks. For instance, the zero-sequence injection approach can be used to increase the dc voltage utilization ratio of the PD-PWM or PS-PWM [9], [13]; however, the mathematical complexity experiences an exponentially increasing manner. The SVM, on the other hand, when applied to HMCs, can result in massive calculation burden. In addition, the difficulty of balancing dc capacitor voltages or fulfilling multiple control objectives, complicated controller parameters tuning due to the coexistence of multiple control loops, and the cross-coupling among various control loops may all lead to tremendous computational complexity and poor system performance.

Since its inception [14], the MPC has been applied to nearly all power electronic applications over the past few decades [14]–[17]. Due to its remarkable advantages, such as fast dynamic response, straightforward implementation concept, compatibility with the nonlinear nature of converters, the multitasking capability [16], etc., MPC is suitable to address the challenges to control HMCs. However, there are two major issues associated with the MPC when applied to HMCs:

1) The necessity to evaluate the exponentially increasing switching states of the HMC significantly burdens the processor resources, which can make it impractical to complete the whole algorithm within each control iteration using the state-of-the-art processors [16].
2) Applying only one switching state over each control period results in a relatively low ratio of the switching frequency to the sampling frequency, e.g., usually ranging from 1/4 to 1/5 [18], [19], which severely degenerates the current tracking performance and leads to variable equivalent switching frequency, which further translates into difficulties in filter design [19].

As a result, it is impractical to improve the switching frequency by unlimitedly increasing the sampling rate, so as to improve the current tracking, since the sampling frequency will eventually reach the limitation of the processor, especially when it comes to the emerging wide bandgap (WBG) devices, such as the silicon carbide (SiC) or gallium nitride devices, which need comparatively high switching frequency to fully exploit their low power loss potentials.

In an effort to address these issues, a broad range of research has been conducted. On one hand, a simplified MPC strategy involving the geometric positioning approach can theoretically push up the sampling rate to 60 kHz, such that the high-frequency feature of the WBG power devices can be entirely exploited [19]. To cut down computational burden in MMCs [20] and CHB converters [21], the dc capacitors voltages sorting approach is employed, which can effectively reduce the calculation burden to an acceptable extent. Another path to enhance the operation efficiency is to employ faster control platforms, e.g., FPGA, to implement the MPC, which also significantly reduces the processing time [22]. On the other hand, to advance the steady-state performance, the long-horizon MPC is introduced in [23], which nevertheless encounters exponential increase of calculation burden when the prediction horizon increases. The authors thereby present a modified sphere decoding algorithm to drastically enhance the computational efficiency. However, as it can be observed from the implementation process, the long-horizon MPC still remains a mathematically complicated approach [18]. In [24], the sampling cycle is divided into *N* parts, enabling insertion of *N* voltage vectors within each control period, such that the current tracking can be improved. However, the performance of this method depends largely on the circuit parameters. An improved MPC method that combines the reference trajectory tracking and its derivative trajectory tracking together is presented in [25] to reduce the voltage total harmonic distortion (THD). In addition, the virtual-vectors-based MPC method has also been extensively studied to improve the steady-state performance [7], [26]–[28]. Whereas, there are several shortcomings associated with this approach. First, due to the control cycle subdivision, the pulse pattern may be asymmetric [27], which may lead to unnecessary switching actions and less competitive current quality. Second, the design of the virtual vectors scope seems to vary significantly on a case-by-case basis [28]. Third, synthesis of the virtual vectors results in higher switching frequencies, which leads to further power losses, unless the WBG devices are used [7].

In addition, to achieve a constant equivalent switching frequency, the harmonics of the output current are shaped into concentrated harmonic groups by a notch filter [14], [29] or other period management method [30], [31]. However, these reshaped harmonics are limited to the frequency barrier set by the sampling frequency, i.e., half of the sampling frequency. In other words, the modification of the harmonics can only be conducted within the half sampling frequency range. When it comes to HMCs, the sampling frequency is very hard to be too high to provide enough degree of freedom for regulations

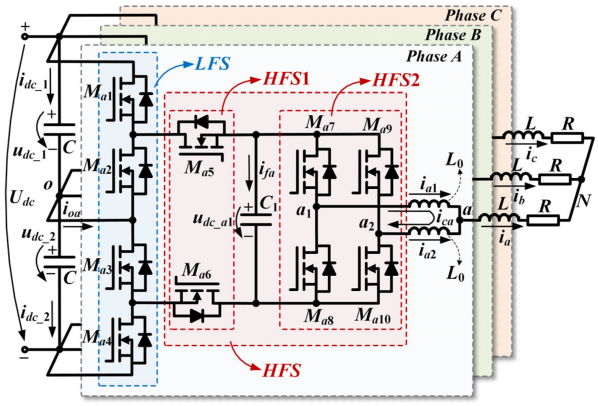

Fig. 1. Nine-level IHMC connected to the *RL*-load.

TABLE I
SWITCHING STATES OF THE IHMC

Switching States S_j	LFS S_{j1} ($\overline{S_{j2}}$)	LFS S_{j3} ($\overline{S_{j4}}$)	HFS S_{j5} ($\overline{S_{j6}}$)	HFS S_{j7} ($\overline{S_{j8}}$)	HFS S_{j9} ($\overline{S_{j10}}$)	u_{jo1}	u_{jo2}	i_{oj}	i_{fj}
8 (U_{dc}/2)	1	1	1	1	1	U_{dc}/2	U_{dc}/2	0	0
7 (3U_{dc}/8)	1	1	1	1	0	U_{dc}/2	U_{dc}/4	0	i_{j2}
	1	1	1	0	1	U_{dc}/4	U_{dc}/2	0	i_{j1}
6 (U_{dc}/4)	1	1	1	0	0	U_{dc}/4	U_{dc}/4	0	i_j
	1	1	0	1	1	U_{dc}/4	U_{dc}/4	i_j	$-i_j$
5 (U_{dc}/8)	1	1	0	1	0	U_{dc}/4	0	i_j	$-i_{j1}$
	1	1	0	0	1	0	U_{dc}/4	i_j	$-i_{j2}$
4 (0)	1	1	0	0	0	0	0	i_j	0
	0	0	1	1	1	0	0	i_j	0
3 ($-U_{dc}$/8)	0	0	1	1	0	0	$-U_{dc}$/4	i_j	i_{j2}
	0	0	1	0	1	$-U_{dc}$/4	0	i_j	i_{j1}
2 ($-U_{dc}$/4)	0	0	1	0	0	$-U_{dc}$/4	$-U_{dc}$/4	i_j	i_j
	0	0	0	1	1	$-U_{dc}$/4	$-U_{dc}$/4	0	$-i_j$
1 ($-3U_{dc}$/8)	0	0	0	1	0	$-U_{dc}$/4	$-U_{dc}$/2	0	$-i_{j1}$
	0	0	0	0	1	$-U_{dc}$/2	$-U_{dc}$/4	0	$-i_{j2}$
0 ($-U_{dc}$/2)	0	0	0	0	0	$-U_{dc}$/2	$-U_{dc}$/2	0	0

of current harmonics. Moreover, the output current can reveal obvious regulated frequency oscillations when applying these methods [29]. Based on the concept of optimal duty cycle control proposed in [32], the three-vector-based MPC [33] or the multivector MPC [34] for motor drives are brought forward recently, which are also capable of achieving both satisfactory steady-state performance and a constant switching frequency. Unfortunately, these abovementioned approaches cannot be directly used in HMCs because of the enormous number of exponentially increasing voltage vectors and the difficulty in shaping symmetric switching patterns.

To this end, this article presents a hybrid model predictive control (H-MPC) for a nine-level IHMC, which integrates the PD-PWM and PS-PWM within itself and overcomes aforementioned inherent obstacles of the C-MPC. Compared with the C-MPC, the proposed method can enable the decoupling of the LFS and HFS in the IHMC and reduce both the output current THD and computational burden while fulfilling constant switching frequencies. The remainder of this article is organized as follows. Section II presents the circuit analysis and modeling of the IHMC. Section III analyzes the integration of the PD-PWM and PS-PWM in terms of floating capacitor balancing. Section IV elaborates the proposed H-MPC strategy on a step-by-step basis. Sections V and VI validate the proposed method through comprehensive simulation and experimental studies on an all-SiC prototype. Finally, Section VII concludes this article.

II. IHMC Circuit Analysis and Modeling

This section analyzes the nine-level IHMC and aims to lay the groundwork for the proposed control strategy elaborated in the following sections.

A. Circuit Analysis

Fig. 1 illustrates the topology of the nine-level IHMC, which outputs nine voltage levels when the dc voltages are $u_{\mathrm{dc\_1}} = u_{\mathrm{dc\_2}} = U_{\mathrm{dc}}/2$ and $u_{\mathrm{dc}\_j1} = U_{\mathrm{dc}}/4$. Table I enumerates all the switching states, which indicates that M_{j1}–M_{j4} can work at fundamental switching frequency to reduce switching losses, the IHMC can thereby be split into an LFS and HFS working at fundamental and high switching frequency, respectively.

It is noteworthy that though the nine-level IHMC topology investigated in this article evolves from the internal parallel converter (IPC) topologies presented in [8], it fundamentally differs from the former ones. First, compared with the half-bridge (HB) IPC (HB-IPC) in [8], the nine-level IHMC in this article has half voltage stresses of the HB-IPC in the HFS. Second, compared with the flying capacitor (FC) IPC (FC-IPC) in [8], the nine-level IHMC in this article has two fewer power devices when outputting a nine-level voltage. Also, voltage stresses across devices of the HFS and the current stresses of M_{j7}–M_{j9} are also reduced; these facts enable the option of using lower cost devices with lower voltage or current ratings.

Further, comparisons between other nine-level multilevel topologies and the nine-level IHMC are also hereby investigated. Fig. 2 illustrates a variety of both classical and emerging multilevel converter topologies, including the CHB and MMC topology [10], the flying capacitor converter [35], the hybrid MMC [4], the nine-level ANPC [36], the five-level ANPC cascaded with H-bridge [2], the T-type converter cascaded with H-bridge [3], the ANPC cascaded with H-bridge [37], the stacked T-type converter [38], the T-type ANPC converter [9], the FC-IPC [8], and the nine-level IHMC in this article. Table II lists comparisons of the above nine-level topologies in terms of LFS, HFS, inductors, and FCs count. As shown, the nine-level IHMC has the lowest device count, even when taking into account the extra interleaved inductors. Table III exhibits the comparison of capacitor energy storage, a common practice for comparisons [9], for these topologies. As it can be seen, although the conventional CHB and MMC have lower capacitor energy storages compared with other topologies, the calculation does not take into account the dc-link capacitors. Except the CHB and MMC topology, the nine-level IHMC has the lowest energy storage among other topologies.

Since the interleaved topology inherently brings about circulating current, leading to additional power loss and exacerbating

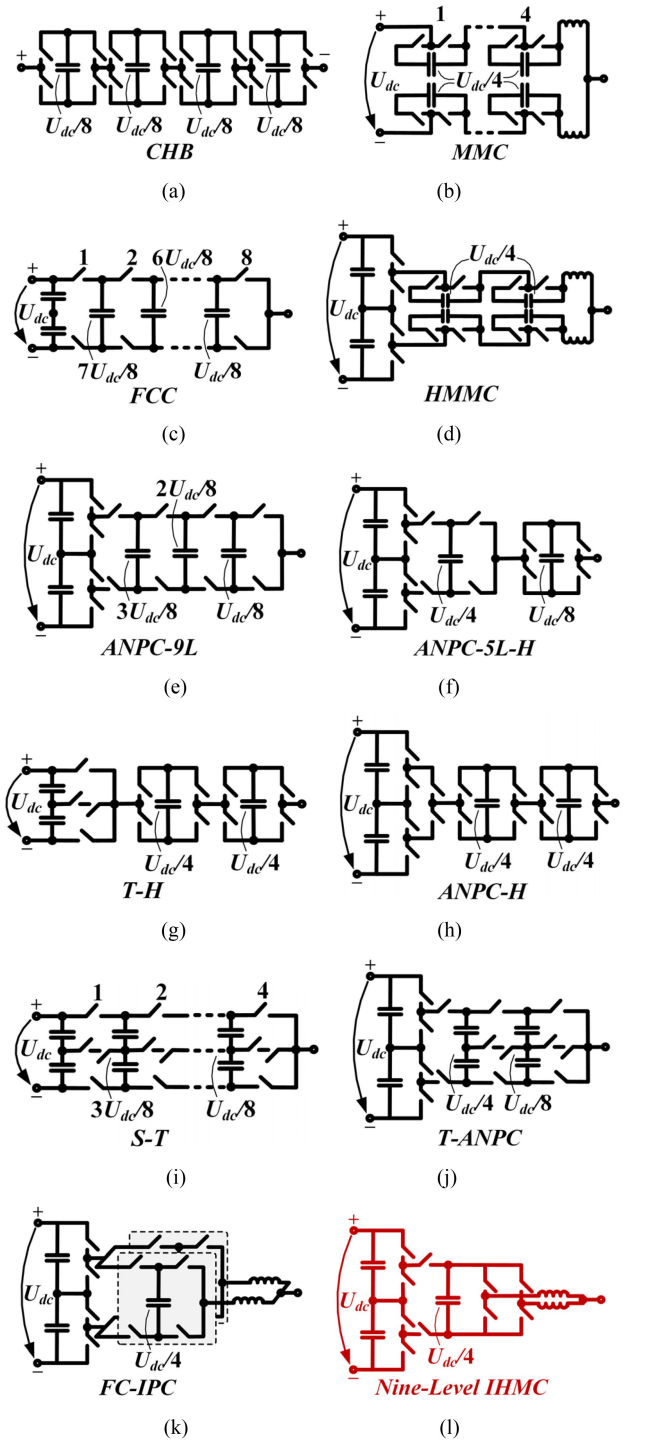

Fig. 2. Various nine-level multilevel topologies: (a) CHB, (b) MMC, (c) FCC, (d) HMMC, (e) ANPC-9L, (f) ANPC-5L-H, (g) T-H, (h) ANPC-H, (i) S-T, (j) T-ANPC, (k) FC-IPC, and (l) nine-level IHMC.

TABLE II
COMPARISON OF VARIOUS NINE-LEVEL MULTILEVEL CONVERTERS

Topology	Device Count			
	LFS Switch	HFS Switch	FC	Inductor
CHB	0	16	4	0
MMC	0	16	8	2
FCC	0	16	7	0
HMMC	4	8	4	2
ANPC-9L	4	8	3	0
ANPC-5L-H	4	8	2	0
T-H	0	12	2	0
ANPC-H	4	10	2	0
S-T	0	16	6	0
T-ANPC	4	10	4	0
FC-IPC	4	8	2	2
Nine-Level IHMC	4	6	1	2

TABLE III
COMPARISON OF CAPACITOR ENERGY STORAGE

Topology	Energy Storage
CHB	$\varepsilon = 4\cdot\frac{C}{2}\left(\frac{U_{dc}}{8}\right)^2 = \frac{1}{32}CU_{dc}^2$
MMC	$\varepsilon = 8\cdot\frac{C}{2}\left(\frac{U_{dc}}{4}\right)^2 = \frac{1}{4}CU_{dc}^2$
FCC	$\varepsilon = \frac{C}{2}\sum_{i=1}^{7}\left(i\frac{U_{dc}}{8}\right)^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{43}{32}CU_{dc}^2$
HMMC	$\varepsilon = 4\cdot\frac{C}{2}\left(\frac{U_{dc}}{4}\right)^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{3}{8}CU_{dc}^2$
ANPC-9L	$\varepsilon = \frac{C}{2}\sum_{i=1}^{3}\left(i\frac{U_{dc}}{8}\right)^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{23}{64}CU_{dc}^2$
ANPC-5L-H	$\varepsilon = \frac{C}{2}\cdot\frac{5}{64}U_{dc}^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{37}{128}CU_{dc}^2$
T-H	$\varepsilon = 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{4}\right)^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{5}{16}CU_{dc}^2$
ANPC-H	$\varepsilon = 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{4}\right)^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{5}{16}CU_{dc}^2$
S-T	$\varepsilon = 2\cdot\frac{C}{2}\sum_{i=1}^{3}\left(i\frac{U_{dc}}{8}\right)^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{15}{32}CU_{dc}^2$
T-ANPC	$\varepsilon = 2\cdot\frac{C}{2}\cdot\frac{5}{64}U_{dc}^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{21}{64}CU_{dc}^2$
FC-IPC	$\varepsilon = 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{4}\right)^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{5}{16}CU_{dc}^2$
Nine-Level IHMC	$\varepsilon = \frac{C}{2}\left(\frac{U_{dc}}{4}\right)^2 + 2\cdot\frac{C}{2}\left(\frac{U_{dc}}{2}\right)^2 = \frac{9}{32}CU_{dc}^2$

the system efficiency, the interleaved inductors are of great significance in reducing the circulating current. Over the past few years, the design of interleaved inductors has been extensively investigated in the interleaved converter family [39]–[44]. In general, the lowest limit of the interleaved inductance is framed by the peak amplitude of the circulating current. As discussed in [39] and [40], the interleaved inductance should be able to suppress the circulating current to an extent that phase leg currents are balanced, such that the converter can function properly [40]. In addition, there are a variety of control methods aiming at mitigating the circulating current, which can potentially lessen the requirement of the interleaved inductance [41]. For instance, the modified discontinuous PWM in [42] and the phase-shifted carrier PWM method proposed in [43], all targeting at reducing the peak amplitude of the circulating current. Further, by using coupled inductors and integrating the magnetic components all together, both total volume of magnetic core and copper usage can be reduced, which can result in significant decrease in both

system weight and volume [39], [41], [44]. Under the proposed H-MPC framework, the H-bridge cell in the HFS2, as depicted in Fig. 1, can be considered as an equivalent HB cell when applying the PS-PWM (as will be detailed in Section IV). Therefore, the design of the floating capacitor in the nine-level IHMC is the same as that in the well-studied five-level ANPC [13], which can be found in the commercially available design report [45].

B. Circuit Modeling

1) System Model: According to the Kirchhoff's voltage law, the system current model can be given by

$$u_{jo} = L\frac{di_j}{dt} + i_j R + u_{No}. \tag{1}$$

The output voltage has the relationship as follows:

$$\begin{cases} u_{jo} = u_{jo1} - L_0\frac{di_{j1}}{dt} \\ u_{jo} = u_{jo2} - L_0\frac{di_{j2}}{dt} \end{cases}. \tag{2}$$

Combining the two equations in (2) yields

$$u_{jo} = \frac{1}{2}\left(u_{jo1} + u_{jo2}\right) - \frac{L_0}{2}\frac{di_{j1}}{dt}. \tag{3}$$

Substituting (3) into (1) yields

$$v_j = L_{\text{eq}}\frac{di_j}{dt} + i_j R + u_{No} \tag{4}$$

where v_j is defined as $v_j = (u_{jo1}+u_{jo2})/2$ [46] and L_{eq} is defined as $L_{\text{eq}} = L_0/2+L$. Applying the Clarke's Transformation [47] leads to the current model in the $\alpha\beta$-frame

$$\boldsymbol{v} = L_{eq}\frac{d\boldsymbol{i}}{dt} + \boldsymbol{i}R \tag{5}$$

where $\boldsymbol{v} = [v_\alpha\ v_\beta]^{\text{T}}$ and $\boldsymbol{i} = [i_\alpha\ i_\beta]^{\text{T}}$.

2) Capacitor Model: The dc capacitors models are given by

$$i_o = C\frac{d\Delta u_{\text{dc}}}{dt} \tag{6}$$

$$i_{fj} = C_1\frac{du_{\text{dc\_}j1}}{dt} \tag{7}$$

where

$$\Delta u_{\text{dc}} = u_{\text{dc\_1}} - u_{\text{dc\_2}} \tag{8}$$

$$i_o = \sum_{j=a,b,c} i_{oj} = \sum_{j=a,b,c}\left(S_{j1} + S_{j5} - 2S_{j1}S_{j5}\right)i_j \tag{9}$$

$$i_{fj} = S_{j5}i_j - S_{j7}i_{j1} - S_{j9}i_{j2} \tag{10}$$

$$i_j = i_{j1} + i_{j2}. \tag{11}$$

3) Inner Circulating Current Model: The inner circulating current model can be given by

$$u_{jo1} - u_{jo2} = 2L_0\frac{di_{cj}}{dt} \tag{12}$$

where

$$\begin{cases} u_{jo1} = \frac{U_{\text{dc}}}{4}\left(2S_{j1} + S_{j5} + S_{j7} - 2\right) \\ u_{jo2} = \frac{U_{\text{dc}}}{4}\left(2S_{j1} + S_{j5} + S_{j9} - 2\right) \end{cases} \tag{13}$$

$$i_{cj} = \frac{1}{2}\left(i_{j1} - i_{j2}\right). \tag{14}$$

Thus, the slope of the inner circulating current can be given by

$$s_{cj} = \frac{1}{2L_0}\left(u_{jo1} - u_{jo2}\right) = \frac{1}{8L_0}\left(S_{j7} - S_{j9}\right). \tag{15}$$

4) Discrete-Time Current Model: This can be derived by applying the Euler Forward Approximation as

$$\boldsymbol{i}\left(k+1\right) = \frac{T_s}{L_{\text{eq}}}\boldsymbol{v}\left(k\right) + \left(1 - \frac{RT_s}{L_{\text{eq}}}\right)\boldsymbol{i}\left(k\right). \tag{16}$$

5) Duty Cycle Model: The duty-cycle-based models of the capacitors currents and inner circulating currents can be performed as [48]

$$i_o = \sum_{j=a,b,c}\left(d_{j1} + d_{j5} - 2d_{j1}d_{j5}\right)i_j \tag{17}$$

$$i_{fj} = d_{j5}i_j - d_{j7}i_{j1} - d_{j9}i_{j2} \tag{18}$$

$$s_{cj} = \frac{1}{8L_0}\left(d_{j7} - d_{j9}\right) \tag{19}$$

$$\begin{cases} u_{jo1} = \frac{U_{\text{dc}}}{4}\left(2d_{j1} + d_{j5} + d_{j7} - 2\right) \\ u_{jo2} = \frac{U_{\text{dc}}}{4}\left(2d_{j1} + d_{j5} + d_{j9} - 2\right) \end{cases} \tag{20}$$

$$v_j = \frac{U_{\text{dc}}}{4}\left[2d_{j1} + d_{j5} + \frac{1}{2}\left(d_{j7} + d_{j9}\right) - 2\right]. \tag{21}$$

III. Analysis of the PD-PWM and PS-PWM

This section analyzes the integration of the PD-PWM and PS-PWM in terms of floating capacitor voltages balancing, which leads to the conclusion that simple integration of the two modulation strategies cannot guarantee a stable floating capacitor voltage, and hence, additional control efforts need to be conducted as appropriate.

A. Integration of the PD-PWM and PS-PWM

As it can be inferred from Table I, S_{j7} and S_{j9} contribute to a $U_{\text{dc}}/8$ voltage step alike, it is therefore a very straightforward idea to apply the PS-PWM to them [48]. Also, since S_{j5} and S_{j1}/S_{j3} lead to $U_{\text{dc}}/4$ and $U_{\text{dc}}/2$ voltage steps, respectively, the PD-PWM can be applied [9], [48], [49]. Fig. 3 shows the integration of the PD- and PS-PWM, which generates a nine-level output voltage and five-level voltages in interleaved legs. As shown, S_{a1}/S_{a3} and S_{a5} operate at fundamental and quasi-fundamental frequencies, respectively [50]. As it can be also seen, the modulation waveform in the range of [1, 2], [−2, −1], and [−1, 0] is equivalently shifted into the range of [0, 1] without changing output waveforms [50]. In addition, the switches in the LFS, i.e., S_{a1}/S_{a3} and S_{a5}, are determined on a sinusoidal-threshold basis, that is, they are turned ON when the original modulation waveform is greater than the threshold value, e.g., 0 for S_{a1}/S_{a3} and ±1 for S_{a5}.

Fig. 4 demonstrates the spectra comparison of the output voltages in the five-level ANPC using the PS-PWM [13] and the equivalent output voltages of the nine-level IHMC using the

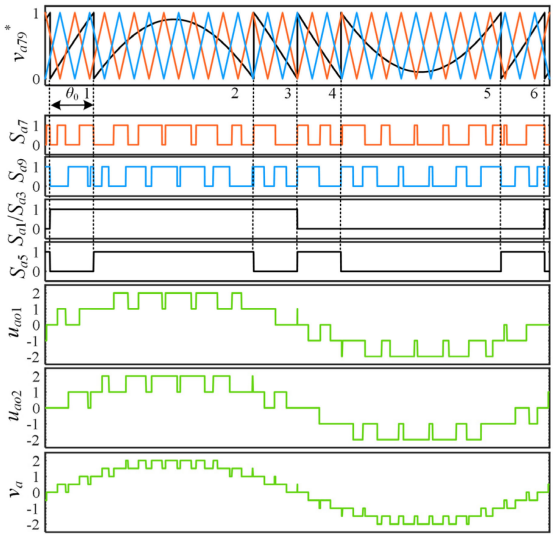

Fig. 3. Integration of the PD-PWM and PS-PWM for the IHMC (Phase A). From top to bottom are reference and carriers of S_{a7}/S_{a9}, pulse trains of S_{a7}, S_{a9}, S_{a1}/S_{a3}, and S_{a5}, output voltages of the interleaved legs, and the equivalent output voltage.

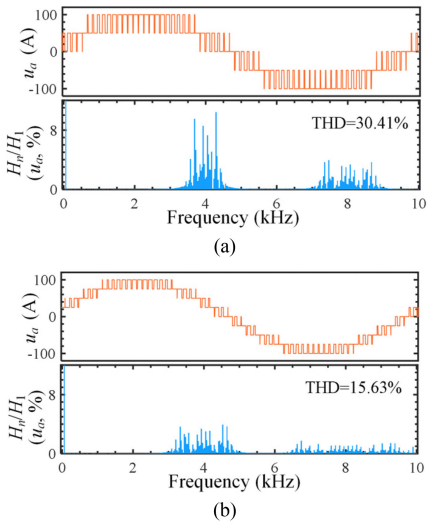

Fig. 4. Equivalent output voltage spectra comparison between the five-level ANPC and the nine-level IHMC (in both cases, the parameters are carrier frequency 2 kHz, modulation index 0.95, fundamental frequency 60 Hz, dc-link voltage 200 V). (a) Five-level ANPC. (b) Nine-level IHMC.

modulation method in Fig. 3. In both simulations, the dc-link voltages are kept constant. As shown, ideally, the nine-level output can approximately enable 49% reduction of voltage THD. In addition, the spectra reveal concentrated harmonic groups at the doubled carrier frequency, i.e., 4 kHz, 8 kHz, etc., due to the use of the PS-PWM.

B. Analysis of the Floating Capacitor Energy

Defining the modulation waveform of the equivalent output voltage and the phase current as

$$\begin{cases} v_{ma} = M\sin(\omega t) \\ i_a = I\sin(\omega t + \varphi). \end{cases} \tag{22}$$

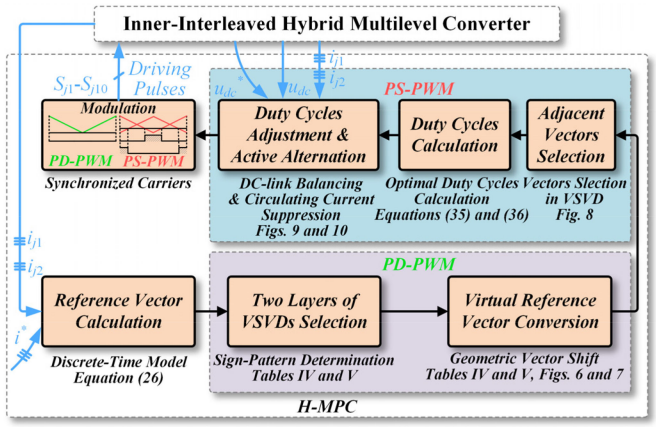

Fig. 5. Control framework of the proposed H-MPC strategy.

One of the corollaries of applying the PS-PWM in S_{a7}/S_{a9} is that $d_{a7} = d_{a9}$. Therefore, the floating capacitor currents are

$$i_{fa} = d_{a5}i_a - d_{a7}i_{a1} - d_{a9}i_{a2} = (d_{a5} - d_{a7})\, i_a. \tag{23}$$

Consequently, the cumulative energies over one fundamental cycle in the floating capacitor, respectively, can be given as per the six sectors in Fig. 3 as

$$\begin{cases} Q_1 = \int_0^{\theta_0} (-2v_{ma})\, I\sin(\omega t + \varphi)\, d(\omega t) \\ Q_2 = \int_{\theta_0}^{\pi-\theta_0} [1 - (2v_{ma} - 1)]\, I\sin(\omega t + \varphi)\, d(\omega t) \\ Q_3 = \int_{\pi-\theta_0}^{\pi} (-2v_{ma})\, I\sin(\omega t + \varphi)\, d(\omega t) \\ Q_4 = \int_{\pi}^{\pi+\theta_0} [1 - (2v_{ma} + 1)]\, I\sin(\omega t + \varphi)\, d(\omega t) \\ Q_5 = \int_{\pi+\theta_0}^{2\pi-\theta_0} (-2v_{ma} - 2)\, I\sin(\omega t + \varphi)\, d(\omega t) \\ Q_6 = \int_{2\pi-\theta_0}^{2\pi} [1 - (2v_{ma} + 1)]\, I\sin(\omega t + \varphi)\, d(\omega t). \end{cases} \tag{24}$$

Substituting (22) into (24) yields the overall energy

$$Q = \sum_{i=1}^{6} Q_i = 8I\cos\varphi\cos\theta_0. \tag{25}$$

When the modulation index M is fixed, θ_0 is also a constant, which represents the intersection of the original sinusoidal-wave and the threshold value. As such, the overall energy Q in the floating capacitor is solely determined by the current phase angle φ or the power factor, which leads to zero energy only when $\varphi = \pi/2$. In other words, the floating capacitor voltages can never be balanced in the vast majority of cases. In addition, when considering the third-harmonic injection, e.g., control in the $\alpha\beta$-frame, the cumulative energy, through similar mathematical derivation, also unfolds an unbalanced fashion [51]. Therefore, it is indispensable to enhance the balancing of floating capacitor voltages when integrating the PD- and PS-PWM, which will be discussed in the following sections.

IV. Proposed Hybrid Model Predictive Control

This section details the implementation process of the proposed H-MPC approach on a step-by-step basis. Fig. 5 illustrates the framework of the proposed control strategy.

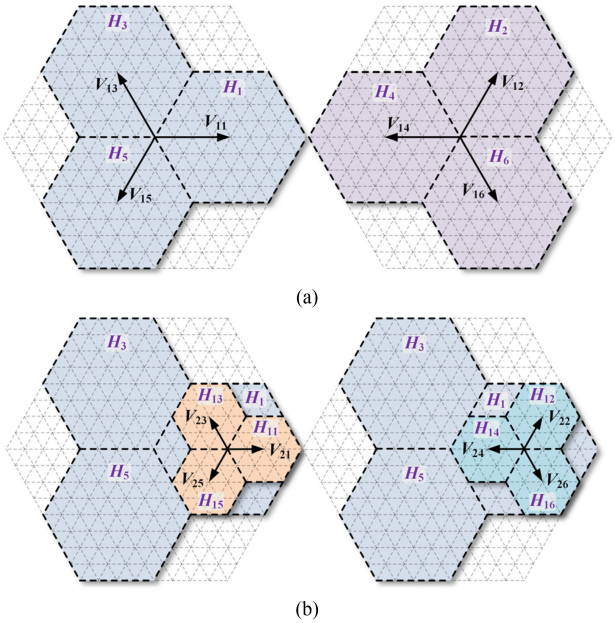

Fig. 6. VSVDs in the original SVD. (a) First-layer VSVDs and their transfer vectors. (b) Second-layer VSVDs and their transfer vectors.

TABLE IV
SIGN PATTERNS AND SWITCHING STATES OF THE FIRST-LAYER VSVD

Sign Pattern v_a^* v_b^* v_c^*	$S_{a1}S_{b1}S_{c1}$ ($S_{a3}S_{b3}S_{c3}$)	VSVD (H_m)	Transfer Vector ($\boldsymbol{V_1}$)
≥ 0 ≤ 0 ≤ 0	100	H_1	$\boldsymbol{V_{11}} = [3\ 0]$
≥ 0 ≥ 0 ≤ 0	110	H_2	$\boldsymbol{V_{12}} = [3/2\ 3\sqrt{3}/2]$
≤ 0 ≥ 0 ≤ 0	010	H_3	$\boldsymbol{V_{13}} = [-3/2\ 3\sqrt{3}/2]$
≤ 0 ≥ 0 ≥ 0	011	H_4	$\boldsymbol{V_{14}} = [-3\ 0]$
≤ 0 ≤ 0 ≥ 0	001	H_5	$\boldsymbol{V_{15}} = [-3/2\ -3\sqrt{3}/2]$
≥ 0 ≤ 0 ≥ 0	101	H_6	$\boldsymbol{V_{16}} = [3/2\ -3\sqrt{3}/2]$

A. VSVD Selection

The reference voltage vector can be given by [7]

$$\boldsymbol{v}^*(k) = \frac{L_{\text{eq}}}{T_s}\left[\boldsymbol{i}^*(k+1) - \boldsymbol{i}(k)\right] + \boldsymbol{i}(k)\,R \tag{26}$$

where $\boldsymbol{i}^*(k+1)$ can be extrapolated from $\boldsymbol{i}^*(k)$ by the fourth-order Lagrange Extrapolation [17]. Thus, the reference vector in the *abc*-frame can be further derived by the inverse Clarke's Transformation as $\boldsymbol{v_{abc}}^* = [v_a{}^*\ v_b{}^*\ v_c{}^*]^{\mathrm{T}}$.

Recapping Table I, it can be concluded that S_{j1}/S_{j3} can be directly determined by the sign of the reference voltage vector $\boldsymbol{v_{abc}}^*$. Further, the original SVD of the IHMC can be split into six first-layer virtual space vector diagram (VSVDs) [44], i.e., the hexagons H_m, which are a quarter of original SVD, as depicted in Fig. 6(a). All vectors in these first-layer VSVDs are subject to six switching states of S_{j1}/S_{j3} described in Table IV, respectively. Subsequently, the reference vector can be transferred to the first-layer VSVDs by the transfer vector $\boldsymbol{V_I}$ as

$$\boldsymbol{v_I}^* = \boldsymbol{v}^* - \boldsymbol{V_I}. \tag{27}$$

Similarly, the virtual reference vector $\boldsymbol{v_I}^*$ can be converted to the *abc*-frame as $\boldsymbol{v_{abc1}}^* = [v_{a1}{}^*\ v_{b1}{}^*\ v_{c1}{}^*]^{\mathrm{T}}$ as well. And S_{j5} can also be confirmed through the sign of $\boldsymbol{v_{abc1}}^*$, by introducing six more second-layer VSVDs, i.e., the hexagons H_{mn}, as illustrated in Fig. 6(b). Table V lists the switching states of the second-layer VSVDs. As shown, the initial point of the transferred virtual reference vectors $\boldsymbol{v_I}^*$ and $\boldsymbol{v_{II}}^*$ are in the center of the two layers of the VSVDs. As illustrated in Fig. 7, the vectors transferring process can be readily conducted, when $m = n$, the first- and second-layer transfer vectors are subject to

$$\boldsymbol{V_{2n}} = \frac{1}{2}\boldsymbol{V_{1m}}. \tag{28}$$

TABLE V
SIGN PATTERNS AND SWITCHING STATES OF THE SECOND-LAYER VSVD

Sign Pattern v_{a1}^* v_{b1}^* v_{c1}^*	$S_{a5}S_{b5}S_{c5}$	VSVD (H_{mn})	Transfer Vector ($\boldsymbol{V_{II}}$)
≥ 0 ≤ 0 ≤ 0	100	H_{m1}	$\boldsymbol{V_{21}} = [3/2\ 0]$
≥ 0 ≥ 0 ≤ 0	110	H_{m2}	$\boldsymbol{V_{22}} = [3/4\ 3\sqrt{3}/4]$
≤ 0 ≥ 0 ≤ 0	010	H_{m3}	$\boldsymbol{V_{23}} = [-3/4\ 3\sqrt{3}/4]$
≤ 0 ≥ 0 ≥ 0	011	H_{m4}	$\boldsymbol{V_{24}} = [-3/2\ 0]$
≤ 0 ≤ 0 ≥ 0	001	H_{m5}	$\boldsymbol{V_{25}} = [-3/4\ -3\sqrt{3}/4]$
≥ 0 ≤ 0 ≥ 0	101	H_{m6}	$\boldsymbol{V_{26}} = [3/4\ -3\sqrt{3}/4]$

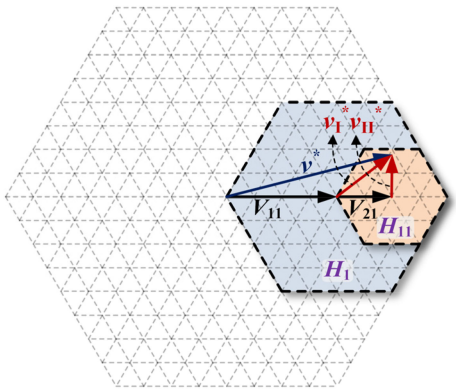

Fig. 7. Vectors transferring process in the first- and second-layer VSVDs.

As such, through the selection of the first- and second-layer VSVDs, the S_{j1}/S_{j3} and S_{j5} can all be secured in a way that is simple, straightforward, and computationally efficient. To further achieve the integration of the PD-PWM and PS-PWM, the adjacent vectors selection and duty cycle calculation for the PS-PWM can be performed in the second-layer VSVDs, which further reduce the computational complexity.

It is noteworthy that when regarding the proposed H-MPC as a whole, it is a framework particularly designed for the nine-level IHMC. However, the selection of the VSVD is a generic approach that enables the separation of LFS and HFS in HMCs that comprises potentially decoupled stages [52]. It is also worth noting that the method in [52] is designed to control the five-level ANPC which has one layer of VSVD and the floating capacitor voltage balancing can be readily achieved by duty cycle adjustments but needless to consider the circulating currents mitigation; hence, it cannot be directly applied to the nine-level IHMC in this article.

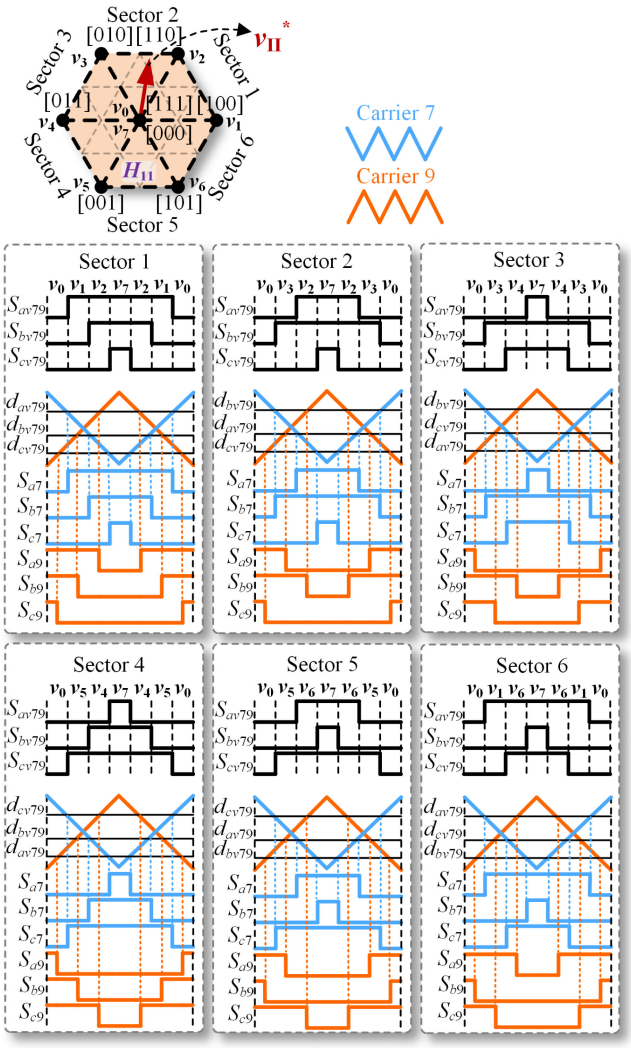

Fig. 8. Switching sequences of M_{j7}/M_{j9} enabled by the PS-PWM.

B. Duty Cycle Calculation

The duty cycle calculation can be conducted in the second-layer VSVD by using the second-layer virtual reference vector, which, as depicted in Fig. 7, can be given by

$$\boldsymbol{v_{II}}^* = \boldsymbol{v_I}^* - \boldsymbol{V_{II}}. \tag{29}$$

At this point, the second-layer VSVD can be regarded as a two-level-converter SVD (Fig. 7), referring to the switching states of S_{j7}/S_{j9}, which is composed of eight virtual vectors, i.e., $\boldsymbol{v_0}$ through $\boldsymbol{v_7}$, among which $\boldsymbol{v_0}$ and $\boldsymbol{v_7}$ are the virtual zero-vectors. The virtual switching states of the eight vectors, i.e., [S_{av79} S_{bv79} S_{cv79}], can also be found in Fig. 8. These vectors are

$$\begin{cases} \boldsymbol{v_0} = \boldsymbol{v_7} = \boldsymbol{V_I} + \boldsymbol{V_{II}} \\ \boldsymbol{v_n} = \boldsymbol{V_I} + \boldsymbol{V_{II}} + \boldsymbol{V_{2n}}. \end{cases} \tag{30}$$

The three adjacent vectors can be simply selected by judging which sector the second-layer reference vector $\boldsymbol{v_{II}}^*$ locates, as illustrated in Fig. 8. The current slopes of the chosen vectors can be given by

$$\boldsymbol{s_i} = \frac{1}{L_{\text{eq}}} (\boldsymbol{VV_i} - \boldsymbol{i}R) \tag{31}$$

where $i \in \{0, 1, 2\}$, $\boldsymbol{s_i} = [s_{\alpha i}\ s_{\beta i}]^{\text{T}}$, $\boldsymbol{VV_0}$ is the chosen zero-vector, while $\boldsymbol{VV_1}$ and $\boldsymbol{VV_2}$ are the selected nonzero-vectors. The predicted currents over each control cycle are

$$\begin{cases} i_\alpha(k+1) = i_\alpha(k) + s_{\alpha1}t_1 + s_{\alpha2}t_2 + s_{\alpha0}t_0 \\ i_\beta(k+1) = i_\beta(k) + s_{\beta1}t_1 + s_{\beta2}t_2 + s_{\beta0}t_0. \end{cases} \tag{32}$$

Then, the current error can be given by

$$\begin{cases} \Delta I_\alpha = I_\alpha - s_{\alpha1}t_1 - s_{\alpha2}t_2 - s_{\alpha0}(T_s - t_1 - t_2) \\ \Delta I_\beta = I_\beta - s_{\beta1}t_1 - s_{\beta2}t_2 - s_{\beta0}(T_s - t_1 - t_2) \end{cases} \tag{33}$$

where $I_\alpha = i_\alpha{}^*(k{+}1){-}i_\alpha(k)$ and $I_\beta = i_\beta{}^*(k{+}1){-}i_\beta(k)$. Subsequently, the cost function of current error is given by

$$J = \Delta I_\alpha{}^2 + \Delta I_\beta{}^2. \tag{34}$$

To solve the quadratic programming problem, the optimal condition can be obtained by using the gradient method [53]

$$\frac{\partial J}{\partial t_1} = 0; \frac{\partial J}{\partial t_2} = 0. \tag{35}$$

Solving (35) yields the optimal duty cycles as

$$\begin{cases} dd_1 = \frac{I_\alpha(s_{\beta0}-s_{\beta2}) + I_\beta(s_{\alpha2}-s_{\alpha0}) + T_s(s_{\alpha0}s_{\beta2} - s_{\alpha2}s_{\beta0})}{T_s s_{\beta1}(s_{\alpha2}-s_{\alpha0}) + T_s s_{\beta2}(s_{\alpha0}-s_{\alpha1}) + T_s s_{\beta0}(s_{\alpha1}-s_{\alpha2})} \\ dd_2 = \frac{I_\alpha(s_{\beta1}-s_{\beta0}) + I_\beta(s_{\alpha0}-s_{\alpha1}) + T_s(s_{\alpha1}s_{\beta0} - s_{\alpha0}s_{\beta1})}{T_s s_{\beta1}(s_{\alpha2}-s_{\alpha0}) + T_s s_{\beta2}(s_{\alpha0}-s_{\alpha1}) + T_s s_{\beta0}(s_{\alpha1}-s_{\alpha2})} \\ dd_0 = 1 - dd_1 - dd_2 \end{cases} \tag{36}$$

where $dd_i = t_i/T_s$. Since the zero-vectors $\boldsymbol{v_0}$ and $\boldsymbol{v_7}$ occupy half of the $\boldsymbol{VV_0}$'s dwell time, therefore, the duty cycles of the four chosen vectors, respectively, can be given by

$$d_1 = \frac{dd_0}{2}; d_2 = dd_1; d_3 = dd_2; d_4 = \frac{dd_0}{2}. \tag{37}$$

To apply the PS-PWM to S_{j7}/S_{j9}, the virtual duty cycles for each phase can be given by

$$d_{jv79} = \sum_{i=1}^{4} d_i S_{jv79\_i} \tag{38}$$

which serve as the reference waves of the two complementary carriers of the PS-PWM [54]. It is worth noting that when the carrier amplitude ranges from 0 to 1, the reference actually equals to the duty cycle of the switching state; therefore, the duty cycle can be considered as the reference wave of the carriers in the PS-PWM in this article. As demonstrated in Fig. 7, by using two complementary carriers for M_{j7}/M_{j9}, the calculated virtual duty cycles, or the references, lead to typical PS-PWM pulse trains. In addition, the virtual switching sequences are the same as those of M_{j7}, which represent the switching sates of the M_{j7}/M_{j9} as a whole.

C. Capacitor Voltage Balancing

As discussed in Section III, the capacitor voltage balancing control in the IHMC is an issue of paramount significance, but

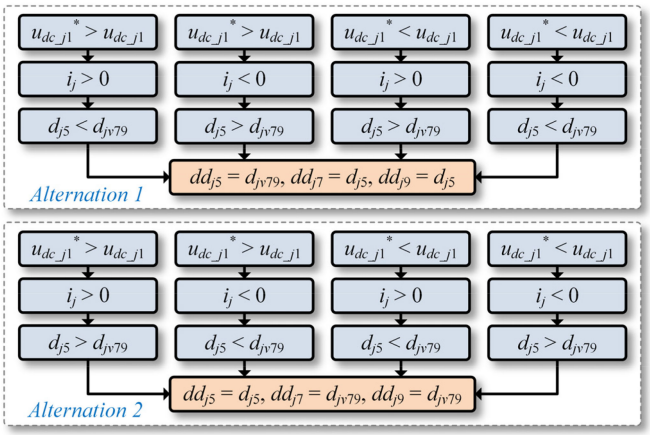

Fig. 9. Redistribution process of the duty cycles.

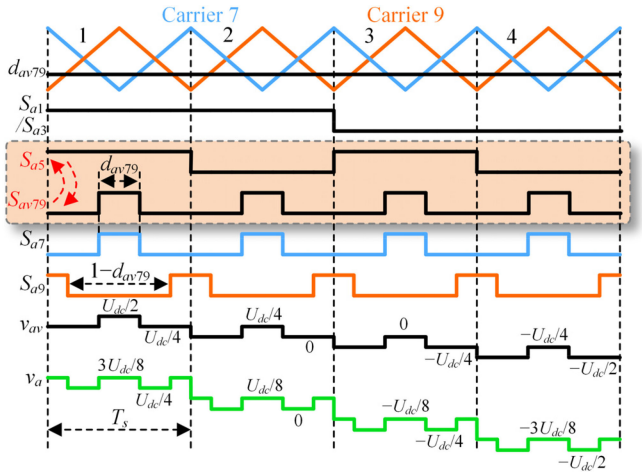

Fig. 10. Equivalence of the output voltages (Phase A).

needs further enhancement when combining the PD- and PS-PWM. The following paragraphs detail the balancing method.

1) Floating Capacitor Voltage Balancing: First of all, the floating capacitor voltage balancing can be achieved through an active duty-cycle-alternation approach. Recapping (18), it can be concluded that when $i_j > 0$, the charging/discharging effect can be interpreted as follows: 1) when $d_{j5} > d_{jv79}$, then $i_{fj} > 0$, the floating capacitor is charged, and 2) when $d_{j5} < d_{jv79}$, then $i_{fj} < 0$, the floating capacitor is discharged, and vice versa when $i_j < 0$. As aforementioned in subsection A, d_{j5} equals to either 0 or 1 when S_{j5} is either 0 or 1 over the entire switching cycle. As depicted in Fig. 1, the HFS can be divided into two equivalent counterparts of each other, i.e., the HFS1 and HFS2; therefore, by alternating the duty cycles of M_{j5} and M_{j7}/M_{j9} between d_{j5} and d_{jv79}, the floating capacitor voltage can be balanced without changing the overall output voltage, which can be further interpreted as unlike the waveforms in Fig. 3, the HFS1 and HFS2 all work at high switching frequency in this regard. Specifically, the redistribution process of the duty cycles is presented in Fig. 9. Exemplifying one redistribution path, when $u_{\mathrm{dc}\cdot a1}{}^{*} > u_{\mathrm{dc}\cdot a1}$, the floating capacitor needs to be charged to approach the reference. When $i_a > 0$ and $d_{a5} < d_{av79}$, which means $d_{a5} = 0$, therefore, to charge the floating capacitor, the duty cycles of M_{a7} and M_{a9} are set to $dd_{a7} = dd_{a9} = 0$, and the duty cycle of M_{a5} is set to $dd_{a5} = d_{av79}$.

In addition, the alternation of the duty cycles between the HFS1 and HFS2 can never influence the current tracking. The equivalence of the alternation is demonstrated in Fig. 10, where v_{av} and v_a are the output voltages of the "Alternation 1" and "Alternation 2" scenarios (Fig. 9). Exemplifying Sector 1 in Fig. 9, the average voltages of v_a and v_{av} over each control period, respectively, can be given by

$$\overline{v_{\mathrm{av}}} = d_{\mathrm{av}79}\frac{1}{2}U_{\mathrm{dc}} + (1 - d_{\mathrm{av}79})\frac{1}{4}U_{\mathrm{dc}} \tag{39}$$

$$\overline{v_a} = 2d_{\mathrm{av}79}\frac{3}{8}U_{\mathrm{dc}} + (1 - 2d_{\mathrm{av}79})\frac{1}{4}U_{\mathrm{dc}} \tag{40}$$

which indicates that $\bar{v_a} = \bar{v_{av}}$. Thus, they have the same impact on current tracking, although having five- and nine-level output voltages, respectively.

2) DC-Link Voltage Balancing: The dc-link voltages can be balanced through adjusting the duty cycles of the two virtual zero-vectors [13], i.e., $\boldsymbol{v_0}$ and $\boldsymbol{v_7}$, respectively, which have no impact on the line-to-line output voltage, but can lead to opposite neutral-point currents [55]. In consequence, the adjusted virtual duty cycles d_{jv79} can be assigned to M_{j5} when conducting duty-cycle-alternation in floating capacitor voltage balancing, such that the dc-link voltages can be balanced.

Specifically, the switching state $[S_{a5}\ S_{b5}\ S_{c5}] = [0\ 0\ 0]$ is defined as N-type mode, which has an outward total neutral point current, leading to the increase of Δu_{dc}; while the switching state $[S_{a5}\ S_{b5}\ S_{c5}] = [1\ 1\ 1]$ is called the P-type mode, which has an inward total neutral point current, leading to the decrease of Δu_{dc} [49]. Therefore, through adjustment of the duty cycles of the two zero-vectors, the dc-link voltages can be readily balanced. The amount of the duty cycle adjustment can be given by

$$d_{np} = k_{np}\left(0 - \Delta u_{\mathrm{dc}}\right) \tag{41}$$

where the tuning of k_{np} is based on a heuristic approach. Thus, the duty cycles of the two zero-vectors can be given by

$$d_1 = \frac{dd_0}{2} + d_{np};\ d_4 = \frac{dd_0}{2} - d_{np}. \tag{42}$$

D. Inner Circulating Current Suppression

In essence, the inner circulating current is caused by the voltage difference between the two interleaved phase legs. Given that the parameter discrepancy and nonideal factors always exist in real-world scenario, the inner circulating current should be suppressed to enhance the system reliability. As shown in (19), the circulating current is determined by the deviation of d_{j7} and d_{j9}, it can therefore be mitigated by adjusting the two duty cycles while keeping the sum of the two being constant simultaneously, such that both the equivalent output voltage remains unchanged too, as shown in (21). The amount of the duty cycle adjustment can be given by

$$d_{j\mathrm{cir}} = k_{\mathrm{cir}}\left[0 - \frac{1}{2}\left(i_{j1} - i_{j2}\right)\right]. \tag{43}$$

TABLE VI
CIRCUIT PARAMETERS

Description	Variable	Simulation	Experiment
Interleaved inductance	L_0	2.5 mH	2.5 mH
Load inductance	L	1.5 mH	1.5 mH
Load resistance	R	10 Ω	10 Ω
DC-link capacitance	C	240 μF	240 μF
Floating capacitance	C_1	200 μF	200 μF
DC-link voltage	U_{dc}	160 V	160 V
Floating capacitor voltage	$u_{dc\ j1}$	40 V	40 V
Dead time	T_d	-	1 μs
Fundamental frequency	f	60 Hz	60 Hz

Then, the duty cycles of M_{j7} and M_{j9} can be given by

$$d_{j7} = dd_{j7} + d_{jcir}; d_{j9} = dd_{j9} - d_{j\text{cir}}. \tag{44}$$

In addition, when there are negative duty cycles or greater-than-one duty cycles, they are forced to be equal to either 0 or 1, respectively.

In addition, as demonstrated in Fig. 8, when d_{j5} is applied to M_{j5}, the circulating current is suppressed by applying the adjusted dd_{j7} and dd_{j9} to M_{j7}/M_{j9}; when d_{j5} is applied to M_{j7}/M_{j9}, the circulating current should be ideally zero, since duty cycles of M_{j7} and M_{j9} are the same, which offers zero voltage deviation between the two interleaved phase legs. Therefore, the floating capacitor voltage balancing and circulating current mitigation can be achieved simultaneously under the proposed H-MPC framework.

E. Delay Compensation

The delay effect caused by digital platform may severely exacerbate control performance of the MPC [16], It is therefore of utmost significance to eradicate the adverse effect of the delay through two-step prediction of not only the current but also the dc voltages [17], which can enable the mitigation of dc capacitor voltage fluctuations. The details of the two-step prediction process can be found in [7], and noteworthily, the predicted inner circulating and capacitor currents at the $k+1$ time instant can be calculated through the duty cycle models (17)–(19).

V. SIMULATION STUDIES

Simulations are conducted in MATLAB/Simulink with system parameters listed in Table VI. Due to the massive calculation burden in the implementation of the C-MPC, a modified C-MPC [19] is used for comparison, which only assesses three vectors that encompass the reference vector; then, among the redundant switching states of the three vectors, the switching state with optimal capacitor voltage balancing and circulating current suppression is selected through the use of the cost function approach.

Fig. 11 exhibits the average switching frequency comparison between the C-MPC and proposed H-MPC, where the average switching frequency is obtained by counting the switching actions of each switch over one fundamental cycle using a moving averaging tool in MATLAB/Simulink. As it can be seen, the average switching frequencies of the proposed H-MPC method and

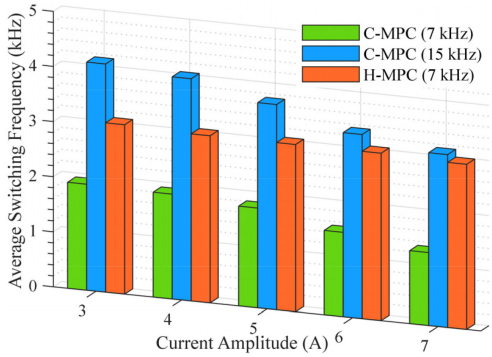

Fig. 11. Comparison of the average switching frequency.

the C-MPC, at 7 and 15 kHz sampling frequency, respectively, can be used as benchmarks for comparison, since the latter one is higher than the former one. And of course, they are all higher than that of the C-MPC at 7 kHz sampling frequency.

Fig. 12 presents the simulation waveforms of the proposed H-MPC and the C-MPC at steady state. Obviously, the C-MPC at 15 kHz sampling frequency has more switching actions over each control cycle than at 7 kHz sampling frequency, which leads to enhanced current THD, more mitigated dc voltages fluctuations, and more attenuated circulating current. Also, the switching states of S_{j1}/S_{j3} unveil a relatively high-frequency fashion, which is the reason for relatively higher average switching frequency compared with the proposed H-MPC. Unlike the C-MPC, the switching states of S_{j1}/S_{j3} in the proposed H-MPC reveal fundamental frequency, while the switching states of S_{j5}, S_{j7}, and S_{j9} are expected to have high-frequency pulse trains according to the discussion in the prior section. It is evident that the current ripples of the proposed H-MPC at 7 kHz sampling frequency are even smaller than those of the C-MPC at both 7 and 15 kHz sampling frequency. The dc voltages are all well balanced to their reference under these control strategies, while the C-MPC at 7 kHz sampling frequency has slightly larger dc voltages ripples due to the lower sampling frequency.

Fig. 13 gives simulation waveforms of the proposed H-MPC and the C-MPC at transient state, where the reference current drops to half and resumes later. It can be seen that the dc capacitor voltages are all well-regulated under both control strategies during the transients, while the responses are relatively fast, which indicates that the proposed H-MPC can retain the fast-dynamic merit of the MPC. It is noteworthy that since the transition time is set to the peak value point on purpose, the voltage spike reaches the maximum extent that it can possibly be. With that being said, the proposed H-MPC reveals comparatively less voltage spikes due to the hybrid frequency operation of the converter. In addition, the C-MPC suffers relatively higher *dv/dt* compared with the proposed H-MPC at both steady and transient state, which shows another superior aspect of the proposed H-MPC. Also, the responding time has direct correlation with the sampling rate, which leads to slower response at 7 kHz for both C-MPC and H-MPC.

Fig. 14 demonstrates the spectra comparisons between the proposed H-MPC and the C-MPC. Obviously, the current THD

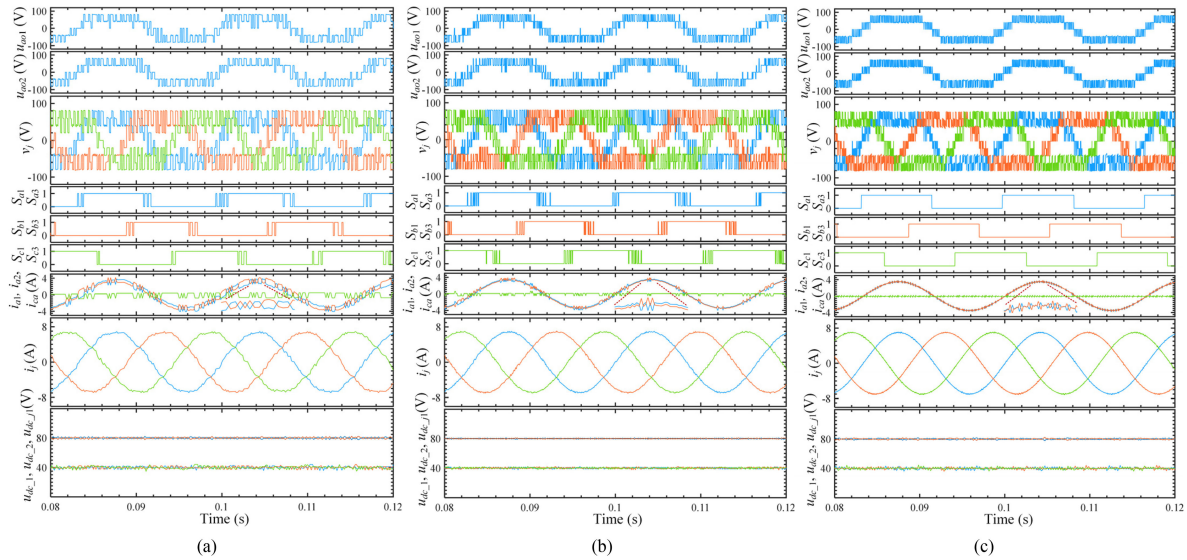

Fig. 12. Simulation waveforms of the steady state. (a) C-MPC at 7 kHz sampling frequency. (b) C-MPC at 15 kHz sampling frequency. (c) H-MPC at 7 kHz sampling frequency. For each figure, from top to bottom are interleaved legs voltages u_{ao1} and u_{ao2}, equivalent output voltages v_j, switching states S_{j1}/S_{j3}, currents of interleaved legs and circulating current i_{a1}, i_{a2}, and i_{ca}, three-phase output currents i_j, and dc capacitor voltages $u_{\mathrm{dc\_1}}$, $u_{\mathrm{dc\_2}}$, and $u_{\mathrm{dc\_}j1}$.

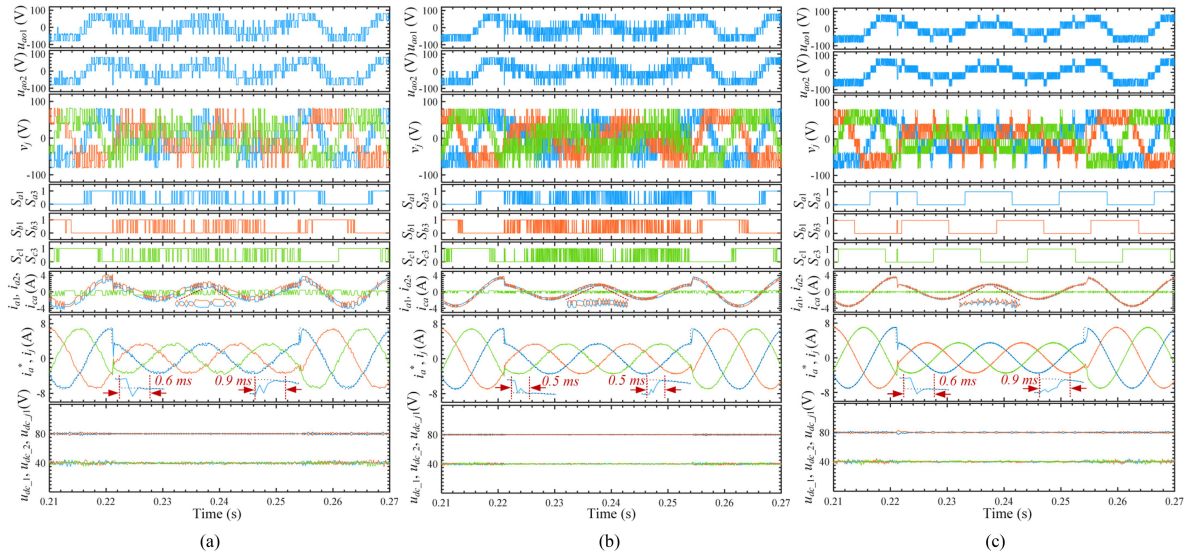

Fig. 13. Simulation waveforms of transient state. (a) C-MPC at 7 kHz sampling frequency. (b) C-MPC at 15 kHz sampling frequency. (c) H-MPC at 7 kHz sampling frequency. For each figure, from top to bottom are interleaved legs voltages u_{ao1} and u_{ao2}, equivalent output voltages v_j, switching states S_{j1}/S_{j3}, currents of interleaved legs and circulating current i_{a1}, i_{a2}, and i_{ca}, three phase output currents i_j and reference $i_a{}^*$, and dc capacitor voltages $u_{\mathrm{dc\_1}}$, $u_{\mathrm{dc\_2}}$, and $u_{\mathrm{dc\_}j1}$.

of proposed H-MPC at 7 kHz sampling rate is much lower than that of the C-MPC at both 7 and 15 kHz sampling rate. Further, the spectra of interleaved legs currents possess concentrated harmonic group around 7 kHz under the proposed H-MPC, while in the output current spectrum, the 7 kHz harmonic group is considerably mitigated while the 14 kHz harmonic group is amplified, which in other words, shows a frequency doubling effect thanks to the use of the PS-PWM. On the contrary, current spectra of C-MPC unfold more widespread fashions. Fig. 15 depicts the comparison of the current THD versus amplitude. As shown, the current THD gradually increases as the current amplitude decreases, and the current THD of the proposed H-MPC at 7 kHz sampling rate is lower than that of the C-MPC at 15 kHz sampling rate and much lower than that of the C-MPC at 7 kHz sampling rate. Fig. 16 demonstrates the comparison of power loss breakdown when sampling rates of both C-MPC and H-MPC are 7 kHz and current amplitude is 7 A. The loss modeling methods for the SiC MOSFET and the converter system can be found in the prior article [55]. As shown, due to the low switching loss characteristic of the SiC device, the switching loss only contributes to a very minor portion. The total power loss, when applying the proposed H-MPC, does not increase significantly even though the average switching frequency is higher than that of the C-MPC (Fig. 11). Also,

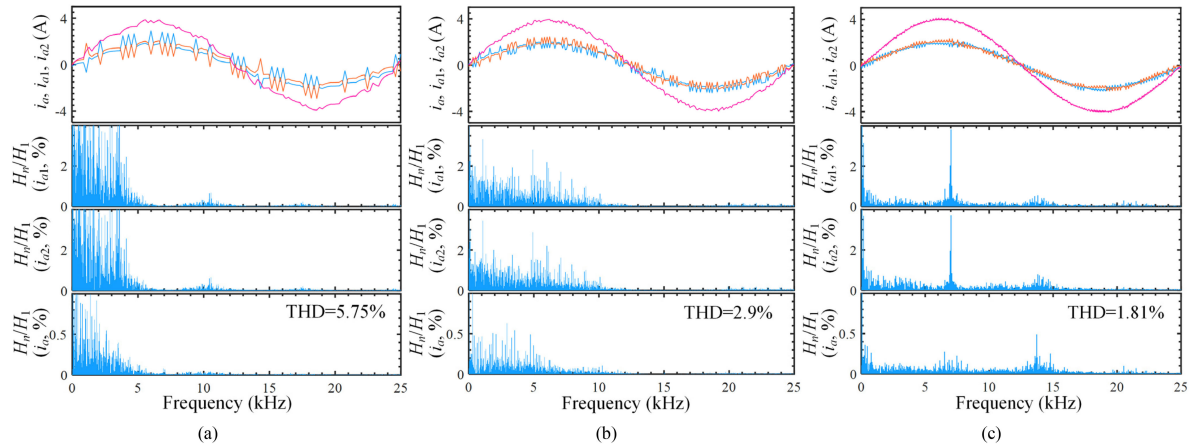

Fig. 14. Simulation results of current spectra comparisons. (a) C-MPC at 7 kHz sampling frequency. (b) C-MPC at 15 kHz sampling frequency. (c) H-MPC at 7 kHz sampling frequency.

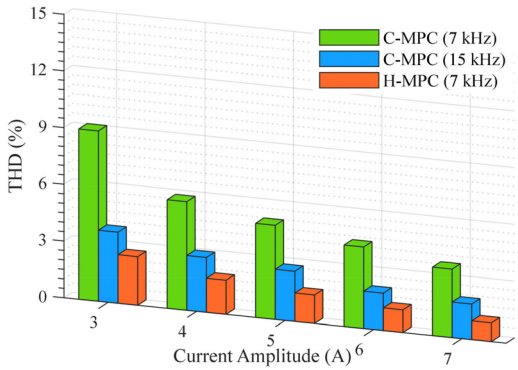

Fig. 15. Comparison of the output current THD (simulation).

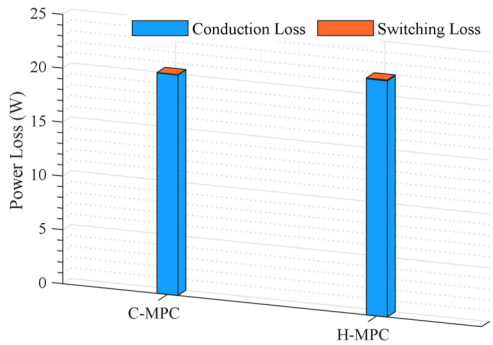

Fig. 16. Comparison of the power loss breakdown (7 kHz sampling rate).

the SiC MOSFETs (CREE/Wolfspeed: C2M0160120D, 1.2 kV, 18 A, 160 mΩ) [56] used in the prototype have comparatively high ON-state resistances (160 mΩ), which is the reason why it reveals relatively high conduction losses.

VI. Experimental Studies

To verify the proposed H-MPC strategy in a real-world platform, an all-SiC IHMC prototype is developed using discrete SiC MOSFETs (CREE/Wolfspeed: C2M0160120D, 1.2 kV, 18 A, 160 mΩ) [56]. The system parameters are also given in Table IV. Fig. 17 shows the experimental rig, where the dSPACE MicroLabBox and Intel Max-10 FPGA are used for control and the optic fibers are used to enhance the noise immunity. The load and dc power source feeding the dc-link are not shown.

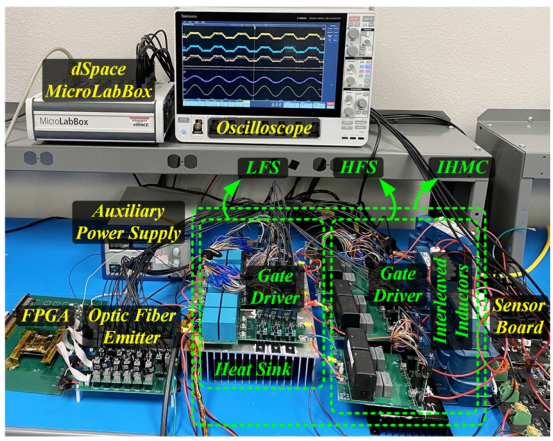

Fig. 17. Experimental rig of the IHMC.

Fig. 18 shows the steady-state waveforms, where the pulse trains of S_{j1} of the proposed H-MPC unveil fundamental- frequency patterns, which aligns with the control objective, while the pulse trains of S_{j5}, S_{j7}, and S_{j9} are expected to reveal high-frequency patterns. In contrast, the C-MPC unfolds high-frequency patterns for pulse trains of S_{j1}. As abovementioned in Section V, the stark contrast of the low-frequency pulse trains with the high-frequency ones enables fewer switching actions and thus lower switching losses. Fig. 19 also demonstrates the steady-state waveforms, where Phase A is exemplified. As shown, the current ripples of the proposed H-MPC at 7 kHz sampling rate are smaller than those of the C-MPC at both 7 and 15 kHz sampling rate, which is in line with the simulation results. The dc voltages can all be well-regulated under both control strategies. Fig. 20 demonstrates the waveforms at transient state. As shown, all the dc voltages are well-balanced to their reference despite some trivial surges, which are brought by the regulation

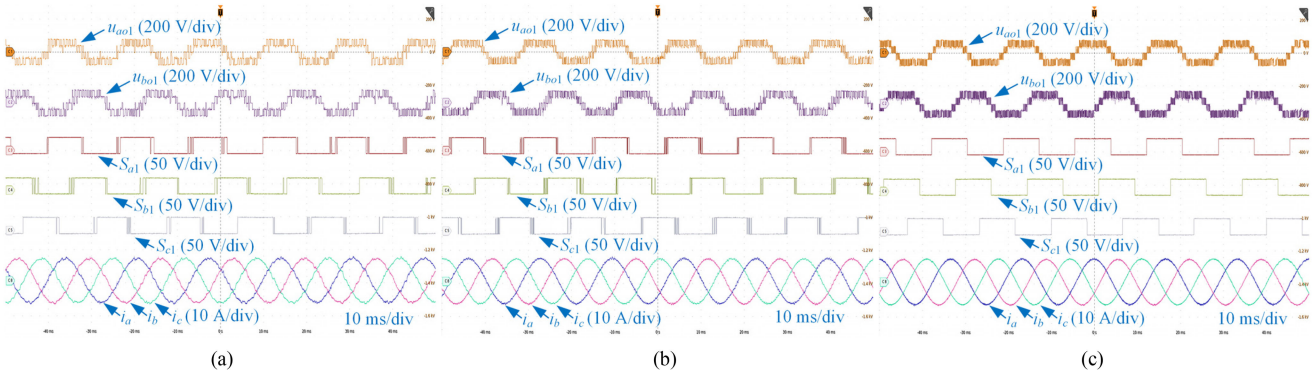

Fig. 18. Experimental results of steady state. (a) C-MPC at 7 kHz sampling frequency. (b) C-MPC at 15 kHz sampling frequency. (c) H-MPC at 7 kHz sampling frequency. For each figure, from top to bottom are interleaved legs voltages u_{ao1} and u_{bo1}, switching states S_{j1}, and three-phase output currents.

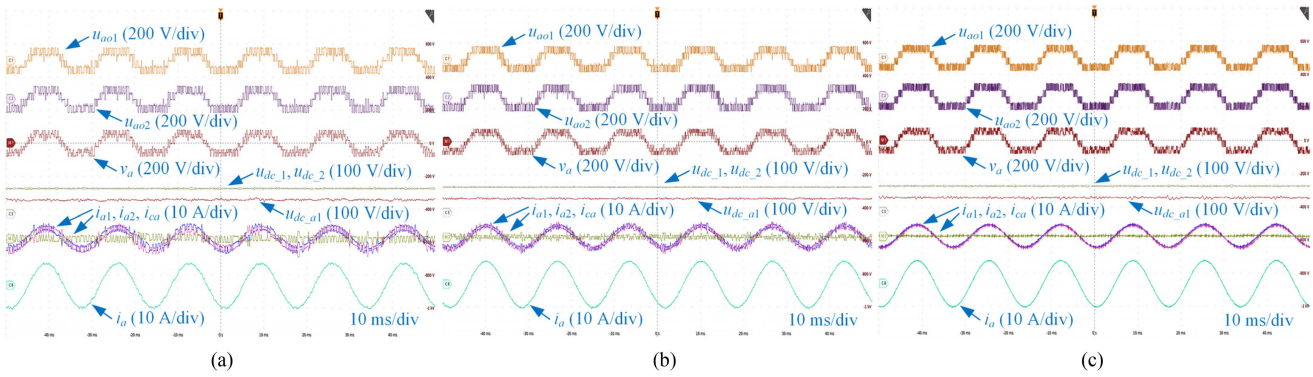

Fig. 19. Experimental results of steady state. (a) C-MPC at 7 kHz sampling frequency. (b) C-MPC at 15 kHz sampling frequency. (c) H-MPC at 7 kHz sampling frequency. For each figure, from top to bottom are interleaved legs voltages u_{ao1} and u_{ao2}, equivalent output voltage v_a, dc-link capacitors voltages u_{dc_1} and u_{dc_2}, floating capacitor voltage u_{dc_a1}, currents of interleaved legs and circulating current i_{a1}, i_{a2}, and i_{ca}, and output current of Phase A i_a.

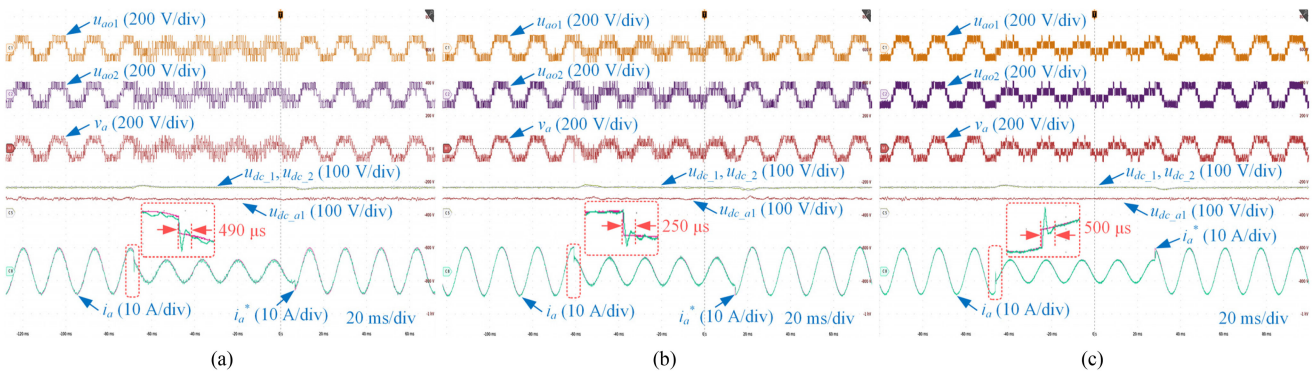

Fig. 20. Experimental results of transient state. (a) C-MPC at 7 kHz sampling frequency. (b) C-MPC at 15 kHz sampling frequency. (c) H-MPC at 7 kHz sampling frequency. For each figure, from top to bottom are interleaved legs voltages u_{ao1} and u_{ao2}, equivalent output voltage v_a, dc-link capacitors voltages $u_{\mathrm{dc\_1}}$ and $u_{\mathrm{dc\_2}}$, floating capacitor voltage $u_{\mathrm{dc\_a1}}$, output current of Phase A i_a and its reference $i_a{}^*$.

of the dc power source. The proposed H-MPC and the C-MPC at 7 kHz sampling rate have approximately the same responding time, while the C-MPC at 15 kHz has shorter responding time due to a higher sampling rate. In a nutshell, the responding time at all scenarios is relatively fast.

To further validate the current THD enhancement brought by the proposed H-MPC, the currents spectra comparisons based on the experimental data are illustrated in Fig. 21. It can be observed that the current THD of the proposed H-MPC at 7 kHz sampling rate is much lower than those of the C-MPC at both 7 and 15 kHz sampling rate. In addition, there are concentrated harmonic groups around 7, 14 kHz, and so on in the spectrum of the output current under the proposed H-MPC, while the current spectra of C-MPC at both 7 and 15 kHz exhibit more widespread fashions. It is worth noting that due to the experimental nonidealities, the 7 kHz harmonic group is not as well-mitigated as in the simulation results (Fig. 14), but the doubled-frequency harmonic group can still be observed around 14 kHz.

Fig. 22 depicts the comparison of the current THD versus amplitude. As shown, the current THD of the proposed H-MPC

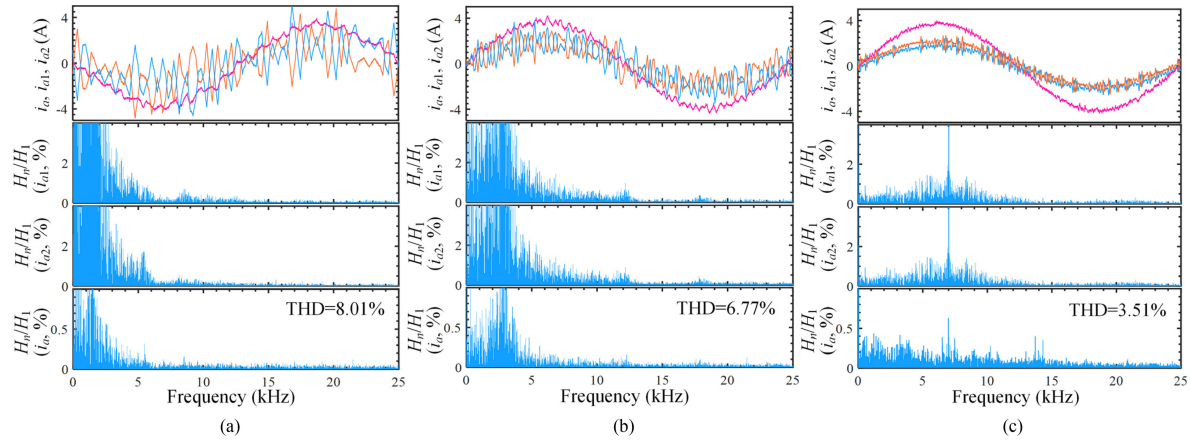

Fig. 21. Experimental results of current spectra comparisons. (a) C-MPC at 7 kHz sampling frequency. (b) C-MPC at 15 kHz sampling frequency. (c) H-MPC at 7 kHz sampling frequency.

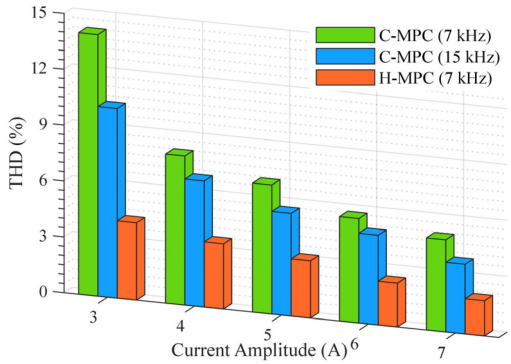

Fig. 22. Comparison of the output current THD (experiment).

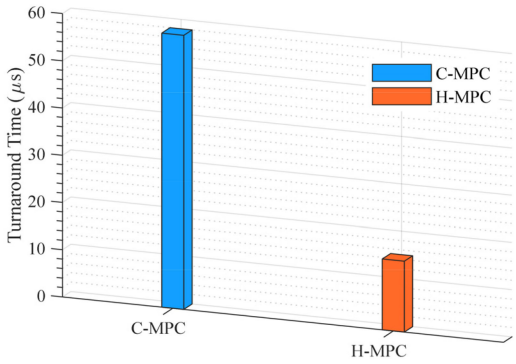

Fig. 23. Turnaround time comparison.

at 7 kHz sampling rate is lower than those of the C-MPC at both 7 and 15 kHz sampling rate. Thus, the proposed H-MPC has better current tacking performance than the C-MPC does with even lower average switching frequency. These experimental results are all in accordance with the simulation results. Further, Fig. 23 illustrates the turnaround time comparison between the two algorithms, where the turnaround time is measured in dSPACE using the real-time mode. Evidently, the proposed H-MPC consumes shorter time than the C-MPC, which enables approximately 74% reduction.

VII. Conclusion

This article presents an H-MPC strategy for an IHMC, which incorporates both the PD-PWM and PS-PWM. Compared with the C-MPC, the proposed method can enable the decoupling of the LFS and HFS in the IHMC and reduce both the output current THD and computational burden while achieving a constant switching frequency. The performances of the proposed H-MPC are comprehensively investigated through both simulation and experimental studies performed on an all-SiC prototype, where the results consolidate the following aspects:

1) The proposed method can enable the decoupling of the LFS and HFS, leading to easier heat dissipation design and lower average switching frequencies.
2) The proposed method can reduce both the calculation burden and output current THD while retaining the fast-dynamic response feature of the C-MPC.
3) The proposed method can achieve a constant switching frequency, and doubled equivalent switching frequency, thanks to the integration of PS-PWM, and thus, brings forward concentrated harmonic groups around the sampling frequency in the output current, which further translates into easier filter design.
4) The dc capacitor voltage balancing and circulating currents mitigation needs no weighting factors and can be achieved without affecting the current tracking; thus, the current tracking performance is relatively superior.
5) The proposed strategy is simple and less time-consuming, and thus, can theoretically push up the sampling rate to above even 50 kHz, which can thereby pave the way for the application of high-frequency WBG power devices.

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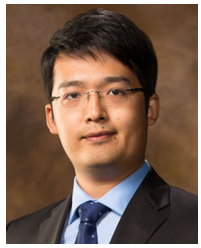
Yufei Li (Member, IEEE) received the B.S. degree in electrical engineering in 2009 from Xi'an Jiaotong University, Xi'an, China, where he was subsequently given the exam-exemption for outstanding undergraduates to pursue the M.S. degree and pivoted to directly pursue the Ph.D. degree in 2011, and received the Ph.D. degree in electrical engineering from Xi'an Jiaotong University in 2016.

From 2016 to 2017, he was an Electrical Engineer with State Grid Corporation of China, Xi'an. From 2017 to 2019, he was an Assistant Professor with the Department of Electrical Engineering, Northwestern Polytechnical University, Xi'an. From 2019 to 2021, he was a Postdoctoral Fellow with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR, USA. Since 2021, he has been with the Department of Electrical and Computer Engineering and Andlinger Center for Energy and the Environment, Princeton University, Princeton, NJ, USA, where he is currently an Associate Research Scholar. His research interests include power converter control, multilevel converters, machine learning methods for power electronics, and wide bandgap power device applications.

Fei Diao (Student Member, IEEE) received the B.E. and M.E. degrees in electrical engineering from the Southwest Jiaotong University, Chengdu, China, in 2015 and 2018, respectively. He is currently working toward the Ph.D. degree in electrical engineering with the Department of Electrical Engineering, University of Arkansas, Fayetteville, AR, USA.

In 2020 and 2021, he was a Summer Intern with the Eaton Corporation, Menomonee Falls, WI, USA. His research interests include modulation and control of multilevel converters and wide bandgap power device applications.



Yue Zhao (Senior Member, IEEE) received the B.S. degree in electrical engineering from the Beijing University of Aeronautics and Astronautics, Beijing, China, in 2010, and the Ph.D. degree in electrical engineering from the University of Nebraska-Lincoln, Lincoln, NE, USA, in 2014.

He was an Assistant Professor with the Department of Electrical and Computer Engineering, Virginia Commonwealth University, Richmond, VA, USA, from 2014 to 2015. Since August 2015, he has been with the University of Arkansas, Fayetteville, AR, USA, where he is currently an Associate Professor with the Department of Electrical Engineering. He has authored/coauthored 4 U.S. patents granted and coauthored more than 100 papers in refereed journals and international conference proceedings. His research interests include electric machines and drives, power electronics, and renewable energy systems.

Dr. Zhao serves as the Site Director for the National Science Foundation Center for GRid-connected Advanced Power Electronic Systems. He is an Associated Editor of the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS and the IEEE OPEN JOURNAL OF POWER ELECTRONICS. He was a recipient of the 2018 U.S. National Science Foundation CAREER Award, the 2020 IEEE Industry Applications Society Andrew W. Smith Outstanding Young Member Achievement Award, and the 2020 UA College of Engineering Dean's Award of Excellence.

H. Alan Mantooth (Fellow, IEEE) received the B.S. and M.S. degrees from the University of Arkansas, Fayetteville, AR, USA, in 1985 and 1986, respectively, and the Ph.D. degree from Georgia Tech, Atlanta, GA, USA, in 1990, all in electrical engineering.

He then joined Analogy, Beaverton, OR, USA, a startup company where his research was focused on semiconductor device modeling and the research and development of modeling tools and techniques. In 1998, he joined the faculty of the Department of Electrical Engineering, University of Arkansas, where he is a Distinguished Professor. His research interests include analog and mixed-signal IC design and CAD, semiconductor device modeling, power electronics, power electronics packaging, and cybersecurity.

Dr. Mantooth helped establish the National Center for Reliable Electric Power Transmission (NCREPT) at the UA in 2005. He is the Executive Director of NCREPT as well as two of its centers of excellence: the NSF Industry/University Cooperative Research Center on GRid-connected Advanced Power Electronic Systems (GRAPES) and Cybersecurity Center on Secure, Evolvable Energy Delivery Systems (SEEDS) funded by the U.S. Department of Energy. In 2015, he also helped to establish the UAs first NSF Engineering Research Center entitled Power Optimization for Electro-Thermal Systems (POETS) that focuses on high power density systems for electrified transportation applications. He cofounded three companies in design automation (Lynguent), IC design (Ozark Integrated Circuits), and cybersecurity (Bastazo) as well as advising a fourth in power electronics packaging (Arkansas Power Electronics International) to maturity and acquisition as a board member. He holds the 21st Century Research Leadership Chair in Engineering. He is a Senior Past-President for the IEEE Power Electronics Society and the Editor-in-Chief of the IEEE OPEN JOURNAL OF POWER ELECTRONICS. He is a Member of Tau Beta Pi, Sigma Xi, and Eta Kappa Nu, and registered professional engineer in Arkansas.