A High-Efficiency and High-Power-Density Interleaved Integrated Buck-Boost-*LLC* Converter and Its Comprehensive Optimal Design Method

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***Abstract*—Integrated buck-boost-*LLC* (IBBL) dc converter is a good solution for high efficiency and high power density applications. However, the bridge leg integration causes asymmetrical zero-voltage-switching process and asymmetrical secondary current. The method of high quality factor or symmetric phase shift modulation proposed in the existing research can improve the asymmetrical current issue under heavy load, but is ineffective for light load conditions. This article proposes a novel Interleaved IBBL converter to improve the asymmetry issue for whole load range. Interleaving makes the secondary current be symmetric naturally. In addition, a comprehensive optimal design method for phase-shift angle and choke inductor is proposed to minimize the total power loss of all primary elements. A 600 W/1 MHz prototype verifies that the proposed IIBBL converter achieves symmetric secondary current in whole load range, and it achieves 95.7% efficiency and 180 W/in^3 under the proposed comprehensive optimal design method.**

***Index Terms*—High efficiency, high power density, integrated converter, interleaving, phase shift.**

I. Introduction

TO ACHIEVE the energy conservation and conform to the development trend of miniaturization and lightweight, efficiency, and power density have always been the core requirements and important indicators of the power electronic converters. The key to achieve high efficiency and high power density is to decrease power loss and increase switching frequency. Soft switching technology is an effective way to decrease the high switching loss under high frequency. *LLC* resonant converter (see Fig. 1) can achieve zero-voltage-switching (ZVS) of primary switches and zero-current-switching of secondary switches in wide voltage range and wide load range, so it is a good candidate for high efficiency and high power density isolated dc–dc applications [1]–[7]. However, voltage regulation limits the efficiency and power density improvement of *LLC*.

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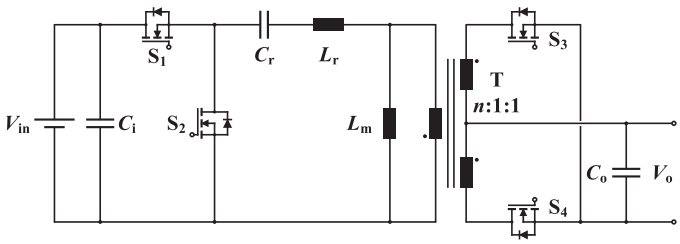

Fig. 1. Topology of the *LLC* resonant converter.

There are two main reasons. First, voltage gain range limits the design of resonant parameters Q and k. This results in very low magnetizing inductance and high current stress for primary switches, which goes against efficiency improvement. Second, regulation requires variable frequency. It makes difficulty in magnetic elements design and synchronous rectification, which goes against frequency and power density improvement [8], [9].

To achieve high efficiency and high power density and solve the difficulty caused by regulation, an *LLC*-based two-stage scheme is proposed and adopted in many research works [10]–[16]. An additional non-isolated PWM regulator with simple structure is used to regulate output so that *LLC* can operate at fixed frequency. Under this circumstance, the voltage gain of *LLC* stage is almost constant, so it is known as *LLC* dc transformer (*LLC* DCX). *LLC* DCX eliminates the above two disadvantages of regulated *LLC*. First, magnetizing inductance can be designed very large so that the current stress of primary switches is decreased. Second, magnetic elements work at fixed frequency, so they are easier to design. Synchronous rectification needs no detection circuit, so that frequency and power density can be raised. *LLC* DCX has achieved extremely high efficiency and high power density in many research works [17]–[21]. Benefited from higher frequency, the power density of *LLC*-based two-stage converter also reaches considerably high level, as 107 W/in^3 in [12] and 195 W/in^3 in [13]. However, the efficiency of two-stage converter is degraded due to more switches and more passive components.

To improve the efficiency of two-stage converter, Sun *et al.* [22] proposed an integrated two-stage scheme. It employs four-switch buck-boost as regulation stage and merges boost bridge leg and *LLC* bridge leg together, then the integrated buck-boost-*LLC* (IBBL) converter is derived, as shown in Fig. 2. S_3 and S_4 form the multiplexed bridge leg. Though the number

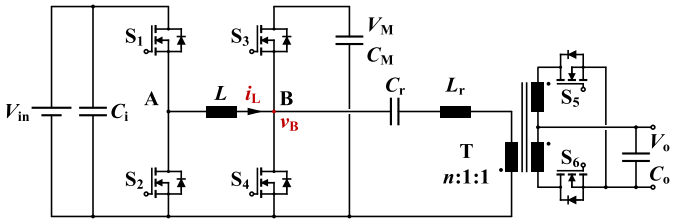

Fig. 2. Topology of the IBBL converter.

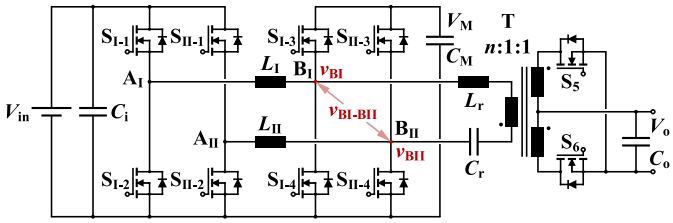

Fig. 3. Topology of the IIBBL converter.

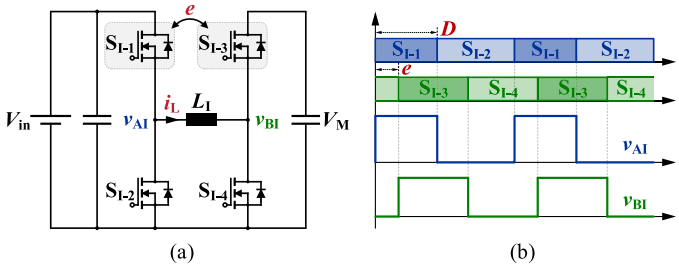

Fig. 4. Definition of phase-shift angle e. (a) circuit and (b) waveforms.

of components of IBBL converter is same as that of conventional buck + *LLC* or boost + *LLC*, the IBBL converter has two obvious advantages according to the analysis in [23]. First, the choke inductor current can reduce the current stress of *LLC* primary switches. Second, the choke inductor current can help achieve ZVS so that magnetizing current is unnecessary. In consequence, the air gap of the transformer is cancelled and eddy current loss is decreased. In summary, bridge leg integration optimizes *LLC* stage and increases the efficiency, and these can't be achieved in the buck + *LLC* or boost + *LLC* converter.

Except for above advantages, bridge leg integration also causes an unexpected issue. The integration makes the choke inductor current i_L change the ZVS process of *LLC* stage and causes difference in the commutation process of upper switch S_3 and lower switch S_4. The voltage of switching node, i.e., the input voltage v_B of resonant tank is asymmetrical. Wang *et al.* [23] indicated that this asymmetrical voltage v_B will distort the resonant current and make the secondary current be asymmetrical. To improve this issue, Wang *et al.* [23] proposed a modulation-based method, which is to eliminate the difference of commutation process by modulating the phase-shift angle between two bridge legs. The specific phase-shift angle varies with the input voltage and the load, and it is unsolvable under light load conditions. Thus, the modulation method can't improve the asymmetry issue under light load. Sun *et al.* [22] and Li and Ruan [24] employed a hardware-based solution, which is to correct the distortion of resonant current by using larger quality factor Q. However, larger Q requires larger resonant inductance, and this will degrade efficiency and power density. Moreover, Q decreases with the decrease of load condition, so that the effect of Q is weak under light load conditions.

To solve the asymmetry issue, this article proposes a topology-based method, which is interleaved IBBL. The proposed topology is shown in Fig. 3.

In the IIBBL converter, the phase angle between two phases buck-boost is 180°. Even if each switching node voltage of *LLC*, i.e., v_{BI} or v_{BII} is asymmetrical, the input voltage of the resonant tank, i.e., $v_{\mathrm{BI\text{-}BII}}$, is naturally symmetric. Therefore, no more large quality factor or symmetric modulation strategy is necessary for balancing the secondary current. Moreover, whether $v_{\mathrm{BI\text{-}BII}}$ is symmetric or not is irrelevant with the load conditions, so that this topology can achieve symmetric secondary current in full load range.

The main design parameters in the IIBBL converter are the choke inductance L and the phase-shift angle e between two bridge legs. e is defined as the lag time between the turn-ON moment of $S_{\mathrm{I\text{-}1}}$ and $S_{\mathrm{I\text{-}3}}$, as shown in Fig. 4. Because there is no coupling between two phases, the design of L and e only need to consider single phase, just like the IBBL converter. The existing research about IBBL also focuses on the design of L and e. In [23], the design of L and e is limited by the symmetric commutation process and is the optimal design for heavy load (light load condition is not analyzed). Sun *et al.* [22] and Li and Ruan [24] aimed at minimizing the ripple of choke inductor current and modulate the current as unipolar. This makes upper switch of buck bridge work at hard switching and is a burden for high frequency. Sun *et al.* [25] aimed at achieving ZVS of all primary switches and modulate the choke inductor current as bipolar. However, there are three drawbacks in the design in [25]. First, the analysis about operation modes is not comprehensive. Though all possible eight modes are listed, only two modes are excluded by evaluating ZVS feasibility. In the remaining six modes, only two modes are discussed. Second, the analysis about power loss related to L and e is not comprehensive. Only the conduction loss of switches is considered while the switching loss is ignored. In terms of loss of the choke inductor, only the current stress is given. The winding resistance and the core loss are not considered. Third, L and e are designed individually. Power loss is a binary function of L and e. The optimal solution cannot be obtained by separate design. Therefore, to make up above design procedure, this article proposes a comprehensive optimal design method of L and e. The advantages are as follows.

1) All possible operation modes are discussed and compared. Two optimal modes are chosen.
2) All power loss related to L and e are analyzed, including conduction loss P_{con} and switching loss P_{sw} of all primary switches, winding loss P_{cu} and core loss P_{fe} of the choke inductor. All loss is based on detailed hardware design.
3) L and e are comprehensively designed. As aforementioned, total loss is a binary function of L and e, i.e., $P_{\mathrm{loss}} = P_{\mathrm{con}} + P_{\mathrm{sw}} + P_{\mathrm{cu}} + P_{\mathrm{fe}} = f(e, L)|_{V_{\mathrm{in}}, P_{\mathrm{o}}}$. The optimal

solution $P_{\text{lossmin}} = f(e_0, L_0)|_{V_{\text{in}},P_{\text{o}}}$ is hard to obtain considering the complex express of P_{loss} and the wide range of input voltage V_{in} and output power P_{o}. To achieve ZVS and minimize power loss, this article finds the relationship between e and L, i.e., $e = g(L)|_{V_{\text{in}},P_{\text{o}}}$. This function decreases the number of designed parameters from two (L and e) to only one (L), which is $P_{\text{loss}} = f(e, L)|_{V_{\text{in}},P_{\text{o}}} = f(g(L), L)|_{V_{\text{in}},P_{\text{o}}} = f(L)|_{V_{\text{in}},P_{\text{o}}}$. According to this unary function, the optimal L_0 is easily obtained: $L_0 = f^{-1}(P_{\text{lossmin}})$. Furthermore, the optimal e_0 is obtained: $e_0 = g(L_0)$. The design procedure is significantly simplified.

A 600 W/1 MHz prototype verifies that the proposed IIBBL converter can achieve symmetric resonant tank voltage in full load range, which is hard to achieve in the IBBL converter. Under the proposed comprehensive optimal design method of L and e, 95.7% full load efficiency and 180 W/in^3 power density are achieved.

The rest of this article is organized as follow. Section II introduces the topology and regulation principle of the proposed IIBBL converter; Section III discusses all possible operation modes and gives the best modes based on efficiency; Section IV gives the comprehensive optimal design method of L and e and designs L in a specific converter; Section V is the experiment to verify above analysis. Finally, Section VI concludes this article.

II. Regulation Method and the Symmetry Principle

The IBBL converter shown in Fig. 2 is obtained by merging the bridge leg of four-switch buck-boost converter and *LLC* converter. Switches S_1–S_4, choke inductor L, input dc-bus capacitor C_i and output dc-bus capacitor C_M make up the front stage four-switch buck–boost converter. Primary switches S_3–S_4, secondary rectifier switches S_5–S_6, resonant elements C_r and L_r, transformer T, input dc bus capacitor C_M and output dc-bus capacitor C_{o} make up the back stage *LLC* converter. The bridge leg S_3–S_4 is the multiplexed bridge. C_i, C_M, and C_{o} are large enough to hold the input voltage V_{in}, the intermediate bus voltage V_M and the output voltage V_{o}. The regulation principle of IBBL is basically same as conventional non-integrated buck-boost + *LLC* DCX two-stage converter. The output is regulated by buck-boost stage. The distinction is that the duty cycle of S_3 and S_4 are limited as 0.5 by *LLC* stage. This makes the average voltage of node B in a switching period is $0.5V_{\text{M}}$. The duty cycle of S_1 is denoted as D. When S_2 is controllable MOSFET, the average voltage of node A in a switching period is DV_{in}. According to the voltage-second balance principle of choke inductor L, we have

$$DV_{\text{in}} = 0.5V_M. \tag{1}$$

LLC stage operates at fixed resonant frequency. The voltage gain is related to the transformer ratio n, the type of inverter and rectifier. When it is half bridge inverter and push-pull rectifier, the gain of *LLC* stage is

$$\frac{V_{\text{o}}}{V_M} = \frac{1}{2n}. \tag{2}$$

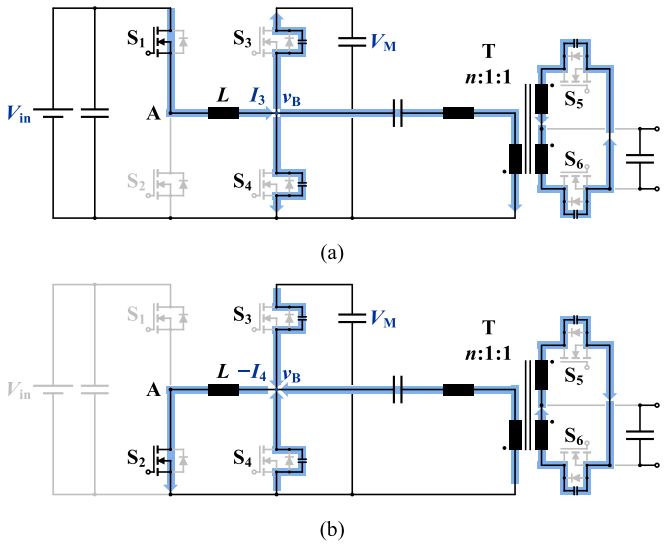

Fig. 5. ZVS process of *LLC* stage. (a) ZVS of S_3. (b) ZVS of S_4.

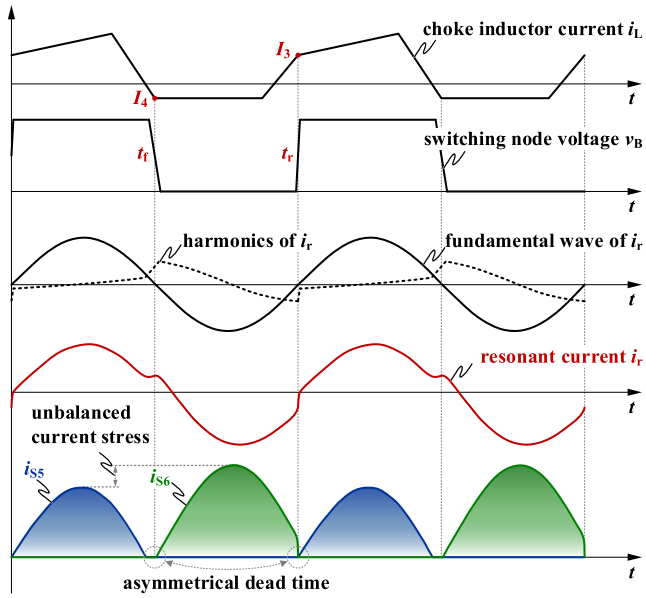

Fig. 6. Main waveforms under the asymmetrical commutation process.

According to (1) and (2), the voltage gain of IBBL is

$$\frac{V_{\text{o}}}{V_{\text{in}}} = \frac{D}{n}. \tag{3}$$

Equation (3) indicated that the IBBL converter can regulate output easily by adjusting duty cycle D of S_1.

As discussed in [23], ZVS of *LLC* in the IBBL converter is achieved by choke inductor current i_L, as shown in Fig. 5. The values of i_L at the turn-ON moment of S_3 and S_4 are denoted as I_3 and I_4, which are the ZVS current for S_3 and S_4. The difference between I_3 and I_4 will cause different rising time t_{r} and falling time t_{f} of v_B (v_B is the voltage of *LLC* switching node), as shown in Fig. 6. By the harmonics analysis of v_B, it is found that the v_B with different t_r and t_f has more even order harmonics than that with same t_r and t_f, as shown in Fig. 7. The even order harmonics in v_B brings harmonics in resonant current i_r, so that i_{r}

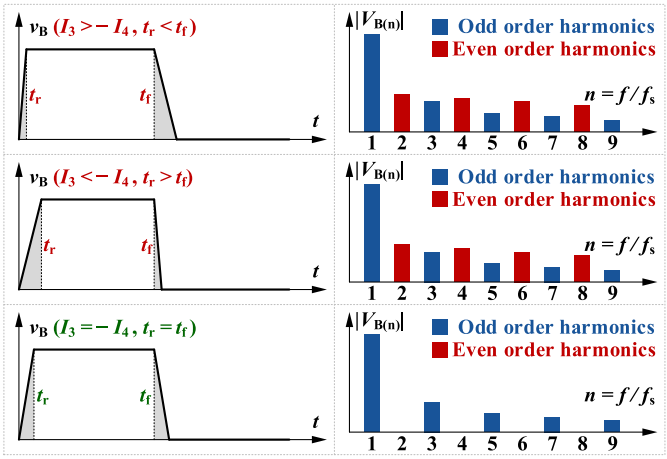

Fig. 7. Frequency characteristic of v_B.

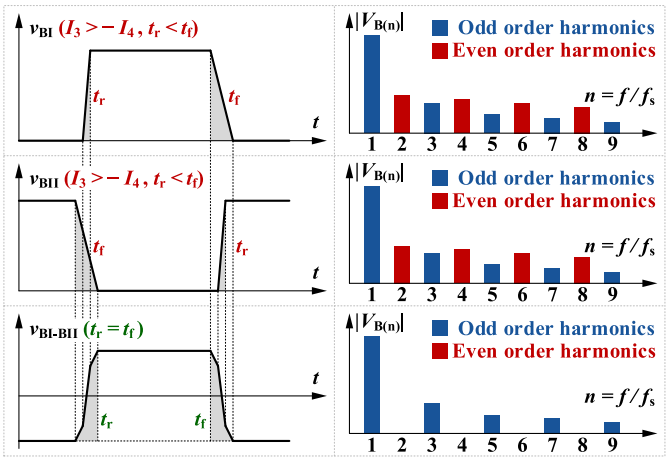

Fig. 8. Frequency characteristic of v_{BI}, v_{BII}, and $v_{BI\text{-}BII}$.

is distorted. Furthermore, it causes asymmetrical secondary current i_{S5} and i_{S6}, as shown in Fig. 6.

To correct the resonant current i_r, Wang *et al.* [23] modulated $I_3 = -I_4$ so that $t_r = t_f$ and the even harmonics in v_B is eliminated; Sun *et al.* [22] and Li and Ruan [24] used large quality factor to eliminate the even harmonics in i_r. However, because $I_3 = -I_4$ is unachievable under light load conditions and quality factor decreases with load, all above methods cannot correct the resonant current under light load condition. Therefore, this article proposes an interleaving method to correct the resonant current in full load range. The interleaved IBBL converter is shown in Fig. 3. The front stage is two-phase interleaved four-switch buck-boost. Because of interleaving, the inverter part of *LLC* is full bridge. In this converter, although the voltage of *LLC* switching node B_I and B_{II} is still asymmetrical, the resonant tank input voltage $v_{BI\text{-}BII}$ obtained by interleaving is symmetrical and contains no even order harmonics, as shown in Fig. 8.

With this symmetric $v_{BI\text{-}BII}$ forcing on resonant tank, the resonant current i_r is naturally sinusoidal, and two branches of secondary current are symmetric. Related waveforms are shown in Fig. 9.

Since there is no coupling between two phases buck-boost, the analysis of voltage gain is same as the IBBL converter.

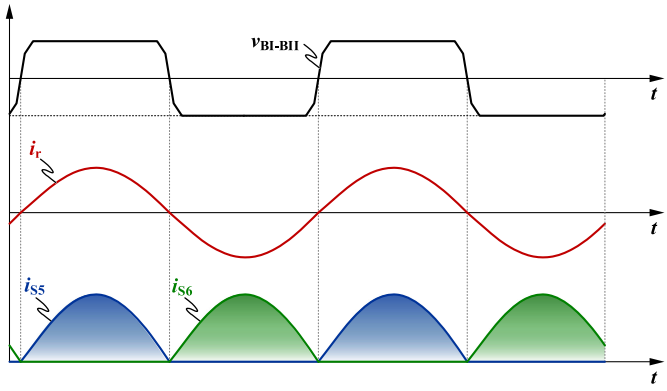

Fig. 9. Main waveforms under the symmetric resonant tank voltage.

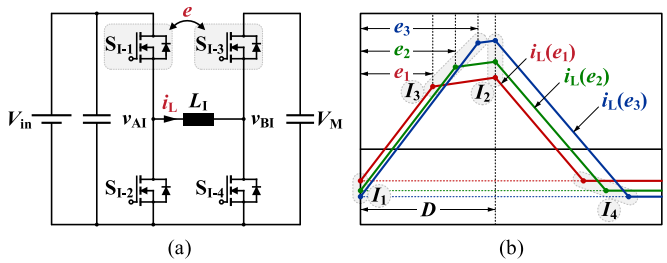

Fig. 10. i_L varies with e. (a) circuit and (b) waveforms.

When duty cycle of $S_{I\text{-}1}$ and $S_{II\text{-}1}$ is D, the voltage gain of front stage is also (1). *LLC* stage also operates at fixed resonant frequency. Here is full bridge inverter and push-pull rectifier, the gain of *LLC* stage is

$$\frac{V_o}{V_M} = \frac{1}{n}. \tag{4}$$

According to (1) and (4), the voltage gain of IIBBL is

$$\frac{V_o}{V_{in}} = \frac{2D}{n}. \tag{5}$$

Equation (5) indicates that the IIBBL converter also regulates output by adjusting duty cycle D.

III. Comparison and Choice of Operation Modes

Since there is no coupling between two phases buck–boost, the optimal design of choke inductor L and phase-shift angle e only need to consider one single phase. In the next analysis, only phase I is discussed. According to (5), angle e will not change the voltage gain. However, e determines the choke inductor current i_L together with input voltage V_{in}, output power P_o and choke inductor L_I. Fig. 10 simply shows how i_L varies with e.

In Fig. 10, the four turning points correspond to the turn-ON moment of the four switches. The value of i_L at the turn-ON moment of $S_{I\text{-}1}$ is denoted as I_1. Similarly, i_L at the turn-ON moment of $S_{I\text{-}2}$, $S_{I\text{-}3}$, and $S_{I\text{-}4}$ are denoted as I_2, I_3, and I_4, respectively. As Fig. 10 indicates, changing e will change i_L, and i_L determines the ZVS operation. Moreover, i_L determines the conduction loss and switching loss of switches, as well as the winding loss and core loss of the choke inductor. Therefore, e deeply influences the performance of primary side and should

TABLE I
POSSIBLE OPERATION MODES

Mode	a: Buck ($0 < D \le 0.5$)	b: Boost ($0.5 < D \le 1$)
1	$0 < e < D$	$0 < e < D - 0.5$
2	$D < e < 0.5$	$D - 0.5 < e < 0.5$
3	$0.5 < e < D + 0.5$	$0.5 < e < D$
4	$D + 0.5 < e < 1$	$D < e < 1$

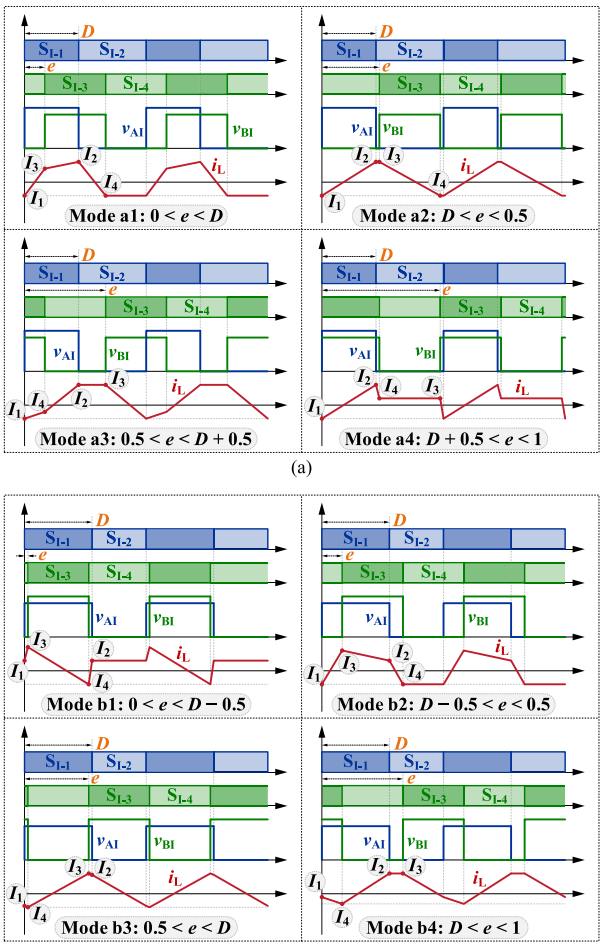

Fig. 11. Main waveforms of primary side. (a) Buck mode. (b) Boost mode.

be carefully designed. According to the relationship between D and 0.5, and the relationship between e and D, the possible operation modes are given in Table I.

The waveforms of switching node voltage v_{AI}, v_{BI} and choke inductor current i_L under each mode are shown in Fig. 11.

In mode a4, there is $I_3 = I_4$, so $S_{I\text{-}3}$ and $S_{I\text{-}4}$ cannot achieve ZVS simultaneously. Similarly, in mode b1, there is $I_1 = I_2$, so $S_{I\text{-}1}$ and $S_{I\text{-}2}$ cannot achieve ZVS simultaneously. These two modes are hard to achieve high frequency, so they are excluded. In the remaining six modes, the ripple ΔI_L (peak to peak) of choke inductor current are given in Table II. Substituting the range of e in Table I into ΔI_L, then the range of ΔI_L can be obtained and is also listed in Table II.

TABLE II
CHOKE INDUCTOR CURRENT RIPPLE AND ITS RANGE

Mode	Current Ripple ΔI_L	Range of ΔI_L
a1	$(e+0.5-D)\cdot V_M T_s / L_I$	$(0.5-D\sim 0.5)\cdot V_M T_s / L_I$
a2	$0.5\cdot V_M T_s / L_I$	$0.5\cdot V_M T_s / L_I$
a3	$(1-e)\cdot V_M T_s / L_I$	$(0.5-D\sim 0.5)\cdot V_M T_s / L_I$
b2	$e\cdot V_{in} T_s / L_I$	$(D-0.5\sim 0.5)\cdot V_{in} T_s / L_I$
b3	$0.5\cdot V_{in} T_s / L_I$	$0.5\cdot V_{in} T_s / L_I$
b4	$(D+0.5-e)\cdot V_{in} T_s / L_I$	$(D-0.5\sim 0.5)\cdot V_{in} T_s / L_I$

As given in Table II, under same choke inductor L_I, the ripple ΔI_L of mode a2 is higher than that of mode a1 and a3. Similarly, the ripple ΔI_L of mode b3 is higher than that of mode b2 and b4. Higher ripple means larger core volume and higher core loss, which goes against the improvement of power density and efficiency. Thus, mode a2 and b3 are excluded.

Mode a1 and b2 share same expression of i_L. Mode a3 and b4 also share same expression of i_L. If take the turn-ON moment of $S_{I\text{-}1}$ as $t = 0$, then i_L under mode a1 and b2 can be expressed in (6), and i_L under mode a3 and b4 is expressed as

$$i_{L\_a1b2}(t) = \begin{cases} I_1 + V_{in}t/L_I, & 0 \le t \le eT_s \\ I_1 + [eV_M T_s + (V_{in} - V_M)t]/L_I, & eT_s < t \le DT_s \\ I_1 + [eV_M T_s + DV_{in}T_s - V_M t]/L_I, & DT_s < t \le (e+0.5)T_s \\ I_1, & (e+0.5)T_s < t \le T_s \end{cases} \tag{6}$$

$$i_{L\_a3b4}(t) = \begin{cases} I_1 + [(V_{in} - V_M)t]/L_I, & 0 \le t \le (e-0.5)T_s \\ I_1 + [(0.5-e)V_M T_s + V_{in}t]/L_I, & (e-0.5)T_s < t \le DT_s \\ I_1 + [(1-e)V_M T_s]/L_I, & DT_s < t \le eT_s \\ I_1 + [V_M T_s - V_M t]/L_I, & eT_s < t \le T_s \end{cases}. \tag{7}$$

If we ignore the power loss of $S_{I\text{-}1}$ and $S_{I\text{-}2}$, then the input power P_{in} is the average of integration of the product of voltage v_{AI} and current i_L in a switching period T_s. For mode a1 and b2, there is

$$\begin{aligned} P_{in\_a1b2} &= 2 \times \frac{1}{T_s} \int_0^{T_s} v_{AI}(t) i_{L\_a1b2}(t) dt \\ &= \frac{2DV_{in}^2}{L_I f_s} \left[-e^2 + 2De - D^2 + \frac{1}{2}D \right] + 2DV_{in}I_1. \end{aligned} \tag{8}$$

f_s is the switching frequency: $f_s = 1/T_s$.

For mode a3 and b4. There is

$$\begin{aligned} P_{in\_a3b4} &= 2 \times \frac{1}{T_s} \int_0^{T_s} v_{AI}(t) i_{L\_a3b4}(t) dt \\ &= \frac{2DV_{in}^2}{L_I f_s} \left[e^2 - (2D+1)e + \frac{3}{2}D + \frac{1}{4} \right] + 2DV_{in}I_1. \end{aligned} \tag{9}$$

The phase-shift angle e can be obtained in (10) and (11) by (8) and (9)

$$e_{a1b2} = D - \sqrt{\frac{D}{2} + \frac{f_s L_\mathrm{I} I_1}{V_\mathrm{in}} - \frac{f_s L_\mathrm{I} P_{\mathrm{in}\_a1b2}}{2DV_\mathrm{in}^2}} \tag{10}$$

$$e_{a3b4} = D + \frac{1}{2} - \sqrt{D^2 - \frac{D}{2} - \frac{f_s L_\mathrm{I} I_1}{V_\mathrm{in}} + \frac{f_s L_\mathrm{I} P_{\mathrm{in}\_a3b4}}{2DV_\mathrm{in}^2}}. \tag{11}$$

Substituting (10) and (11) into Table II, then the ripple ΔI_L under mode a1, a3, b2, and b4 is

$$\Delta I_{\mathrm{L}\_a1} = \left[\frac{1}{2} - \sqrt{\frac{D}{2} + \frac{f_s L_\mathrm{I} I_1}{V_\mathrm{in}} - \frac{f_s L_\mathrm{I} P_\mathrm{in}}{2DV_\mathrm{in}^2}}\right] \cdot \frac{V_M}{L_\mathrm{I} f_s} \tag{12}$$

$$\Delta I_{\mathrm{L}\_a3} = \left[\frac{1}{2} - D + \sqrt{D^2 - \frac{D}{2} - \frac{f_s L_\mathrm{I} I_1}{V_\mathrm{in}} + \frac{f_s L_\mathrm{I} P_\mathrm{in}}{2DV_\mathrm{in}^2}}\right] \cdot \frac{V_M}{L_\mathrm{I} f_s} \tag{13}$$

$$\Delta I_{\mathrm{L}\_b2} = \left[D - \sqrt{\frac{D}{2} + \frac{f_s L_\mathrm{I} I_1}{V_\mathrm{in}} - \frac{f_s L_\mathrm{I} P_\mathrm{in}}{2DV_\mathrm{in}^2}}\right] \cdot \frac{V_\mathrm{in}}{L_\mathrm{I} f_s} \tag{14}$$

$$\Delta I_{L\_b4} = \sqrt{D^2 - \frac{D}{2} - \frac{f_s L_\mathrm{I} I_1}{V_\mathrm{in}} + \frac{f_s L_\mathrm{I} P_\mathrm{in}}{2DV_\mathrm{in}^2}} \cdot \frac{V_\mathrm{in}}{L_\mathrm{I} f_s}. \tag{15}$$

To compare above ΔI_L under same conditions: same V_in (same D), same P_in, same inductor L_I, same f_s and same I_1 (achieving ZVS of $S_{\mathrm{I}\text{-}1}$), we assume that

$$d^2 = \frac{D}{2} + \frac{f_s L_\mathrm{I} I_1}{V_\mathrm{in}} - \frac{f_s L_\mathrm{I} P_\mathrm{in}}{2DV_\mathrm{in}^2} \tag{16}$$

then the above ΔI_L is simplified as

$$\begin{aligned}
\Delta I_{L_a1} &= (0.5 - d) \cdot V_M / L_\mathrm{I} f_s \\
\Delta I_{L_a3} &= (0.5 - D + \sqrt{D^2 - d^2}) \cdot V_M / L_\mathrm{I} f_s \\
\Delta I_{L_b2} &= (D - d) \cdot V_\mathrm{in} / L_\mathrm{I} f_s \\
\Delta I_{L_b4} &= \sqrt{D^2 - d^2} \cdot V_\mathrm{in} / L_\mathrm{I} f_s.
\end{aligned} \tag{17}$$

It is easy to prove that $\Delta I_{L\_a1} < \Delta I_{L\_a3}$ and $\Delta I_{L\_b2} < \Delta I_{L\_b4}$, so mode a1 and mode b2 are the best choice.

In summary, this section analyzes all possible operation modes, and gives two best modes based on the feasibility of ZVS and ripple of choke inductor current.

IV. Optimal Design of the Choke Inductor and the Phase-Shift Angle

In the IIBBL converter, the back stage *LLC* operates at fixed resonant frequency, so its volume and loss of resonant tank, transformer and rectifier are irrelevant with the choke inductor L and phase-shift angle e. However, L and e determine the conduction loss and switching loss of primary switches, as well as the winding loss and core loss of the choke inductor. Therefore, designing L and e properly is the key to optimize efficiency and power density. ZVS is important to the high efficiency under high frequency, so how L and e influence ZVS is first discussed.

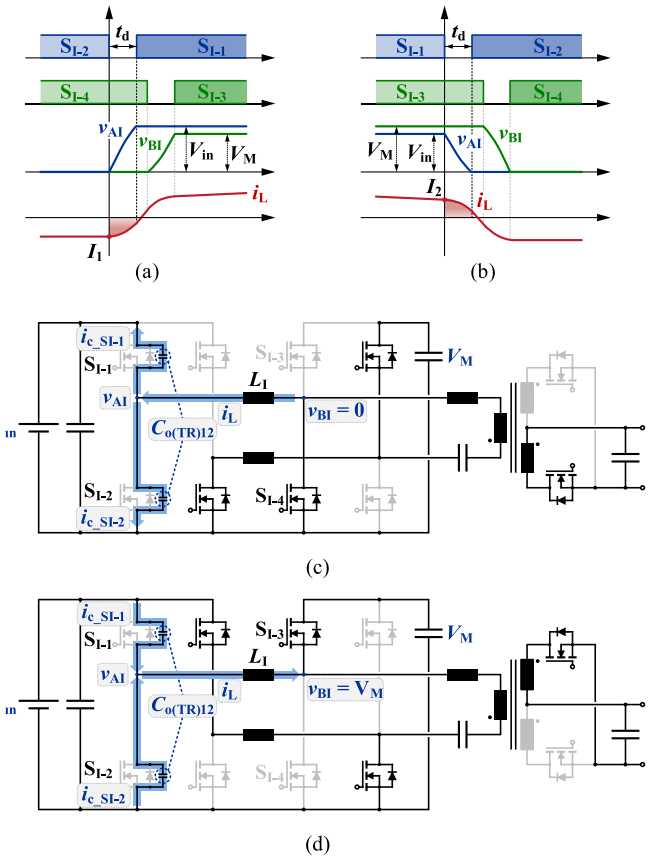

Fig. 12. ZVS process of $S_{\mathrm{I}\text{-}1}$ and $S_{\mathrm{I}\text{-}2}$. (a) Waveforms of ZVS of $S_{\mathrm{I}\text{-}1}$. (b) Waveforms of ZVS of $S_{\mathrm{I}\text{-}2}$. (c) Circuit of ZVS of $S_{\mathrm{I}\text{-}1}$. (d) Circuit of ZVS of $S_{\mathrm{I}\text{-}2}$.

A. ZVS Characteristic

Since the expressions of i_L under modes a1 and b2 are same, the analysis of ZVS does not distinguish two modes. $I_1 \sim I_4$ are the ZVS current for $S_{\mathrm{I}\text{-}1} \sim S_{\mathrm{I}\text{-}4}$. For the ZVS of $S_{\mathrm{I}\text{-}1}$ and $S_{\mathrm{I}\text{-}2}$, I_1 and I_2 are the initial current during deadtime t_d. In whole deadtime, they keep decreasing, as shown in Fig. 12(a) and (b). If i_L cannot entirely discharge C_oss of $S_{\mathrm{I}\text{-}1}$ and $S_{\mathrm{I}\text{-}2}$ before it decreases to zero, then ZVS will fail, no matter how long the deadtime is. Therefore, to achieve ZVS of $S_{\mathrm{I}\text{-}1}$ and $S_{\mathrm{I}\text{-}2}$, I_1 and I_2 should be larger than a certain value, and the minimum value of I_1 and I_2 need to be predicted accurately.

Fig. 12(a) and (c) show the waveform and circuit about ZVS process of $S_{\mathrm{I}\text{-}1}$. For the convenience of analysis, the voltage-related junction capacitor C_oss is replaced by the constant capacitor $C_{o(\mathrm{TR})12}$ provided by the datasheet. According to the *V–I* relationship of $C_{o(\mathrm{TR})12}$ and L_I, a group of differential equation about v_AI and i_L in the deadtime is obtained in (18).

$$\begin{cases}
i_{c_\mathrm{SI}-1} = C_{o(\mathrm{TR})12} \cdot \frac{dv_\mathrm{AI}}{dt} \\
i_{c_\mathrm{SI}-2} = C_{o(\mathrm{TR})12} \cdot \frac{dv_\mathrm{AI}}{dt} \\
i_L = -(i_{c_\mathrm{SI}-1} + i_{c_\mathrm{SI}-2}) \qquad , 0 \le t \le t_d. \\
v_\mathrm{AI} - v_\mathrm{BI} = L_\mathrm{I} \cdot \frac{di_\mathrm{L}}{dt} \\
i_\mathrm{L}(0) = I_1, v_\mathrm{AI}(0) = 0, v_\mathrm{BI} = 0
\end{cases} \tag{18}$$

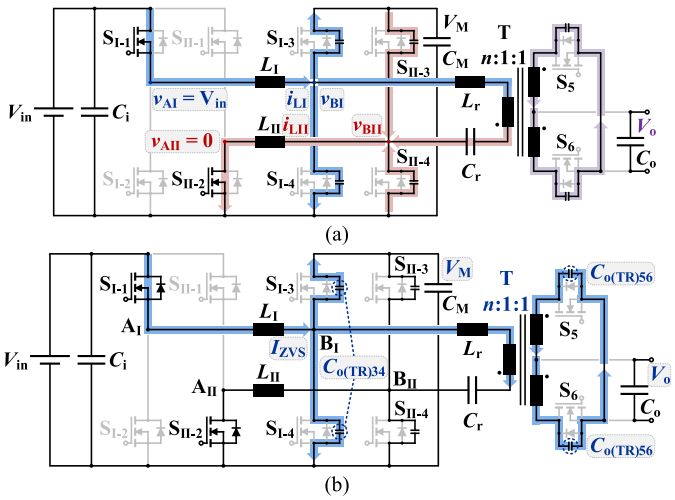

Fig. 13. ZVS process of $S_{\text{I-3}}$. (a) Actual model. (b) Simplified model.

The solution of (18) is (19)

$$v_{\text{AI}}(t) = -I_1\sqrt{\frac{L_{\text{I}}}{2C_{o(\text{TR})12}}}\cdot\sin\frac{t}{\sqrt{2L_{\text{I}}C_{o(\text{TR})12}}}, 0\le t\le t_d. \tag{19}$$

According to $v_{AI}(t_{d1}) = V_{\text{in}}$, t_{d1} is obtained as

$$t_{d1} = \sqrt{2L_{\text{I}}C_{o(\text{TR})12}}\sin^{-1}\left(-\frac{\text{V}_{\text{in}}}{\text{I}_1}\sqrt{\frac{2\text{C}_{\text{o(TR)12}}}{\text{L}_{\text{I}}}}\right). \tag{20}$$

Whether (20) is solvable or not is based on the premise: $0 \le -\frac{V_{\text{in}}}{I_1}\sqrt{\frac{2C_{o(\text{TR})12}}{L_{\text{I}}}} \le 1$. Therefore, the minimum of $|I_1|$ is

$$|I_1|_{\min} = V_{\text{in}}\sqrt{2C_{o(\text{TR})12}/L_{\text{I}}}. \tag{21}$$

Similar, the differential equation about ZVS of $S_{\text{I-2}}$ can be obtained by Fig. 12(b) and (d), and the minimum of $|I_2|$ is

$$|I_2|_{\min} = V_{\text{in}}\sqrt{(8D-2)C_{o(\text{TR})12}/L_{\text{I}}}. \tag{22}$$

As for the ZVS of $S_{\text{I-3}}$ and $S_{\text{I-4}}$, because airgap of the transformer is zero (as discussed in [23]), the magnetizing current is not considered. The ZVS current for $S_{\text{I-3}}$ and $S_{\text{I-4}}$ are I_3 and I_4, respectively. Because they keep increasing during deadtime, ZVS can always be achieved as long as that deadtime is long enough. However, too small $|I_3|$ and $|I_4|$ will cause too long deadtime, which is not desired. Thus, it is necessary to determine the minimum ZVS current under specific deadtime. During the ZVS process of $S_{\text{I-3}}$, $S_{\text{II-4}}$ is also being discharged. The circuit during ZVS process of $S_{\text{I-3}}$ and $S_{\text{II-4}}$ is shown in Fig. 13(a). Because two phases commutate simultaneously, the differential equation about ZVS process involves four variables: v_{BI}; v_{BII}; $i_{LI;}$ and i_{LII}, and the initial value of i_{LI} and i_{LII} is unknown, so the differential equation is hard to solve by manual work. Although simulation or software can give the numerical solution, it is not friendly to the design procedure.

To determine the minimum of I_3 and I_4, constant current I_{ZVS} are used to replace the variable ZVS current i_{LI} and i_{LII}. The simplified model about ZVS process after decoupling two phases is shown in Fig. 13(b). If the junction capacitor of $S_{\text{I-3}}$ and $S_{\text{I-4}}$ is $C_{o(\text{TR})34}$, and the junction capacitor of S_5 and S_6 is $C_{o(\text{TR})56}$, then the relationship between I_{ZVS} and t_d is

$$I_{\text{ZVS}}(t_d) = \left[2C_{o(\text{TR})34} + \frac{4C_{o(\text{TR})56}}{n^2}\right]\cdot\frac{V_M}{t_d}. \tag{23}$$

The minimum of $|I_3|$ and $|I_4|$ are

$$|I_3|_{\min} = |I_4|_{\min} = I_{\text{ZVSmin}} = I_{\text{ZVS}}(t_{d\max}). \tag{24}$$

In summary, the minimum of $|I_1|$–$|I_4|$ are expressed as (21), (22), and (24). On the other hand, according to (6), the expression of $|I_1| \sim |I_4|$ is given in (25)

$$\begin{aligned}
|I_1| &= \frac{V_{\text{in}}}{f_sL_{\text{I}}}\left[-e^2+2De-D^2+\frac{1}{2}D\right]-\frac{P_{\text{in}}}{2DV_{\text{in}}}\\
|I_2| &= \frac{V_{\text{in}}}{f_sL_{\text{I}}}\left[e^2-D^2+\frac{1}{2}D\right]+\frac{P_{\text{in}}}{2DV_{\text{in}}}\\
|I_3| &= \frac{V_{\text{in}}}{f_sL_{\text{I}}}\left[e^2+(1-2D)e+D^2-\frac{1}{2}D\right]+\frac{P_{\text{in}}}{2DV_{\text{in}}}\\
|I_4| &= \frac{V_{\text{in}}}{f_sL_{\text{I}}}\left[-e^2+2De-D^2+\frac{1}{2}D\right]-\frac{P_{\text{in}}}{2DV_{\text{in}}}.
\end{aligned} \tag{25}$$

According to the relationship between e and D, it can be proved that $|I_1|$–$|I_4|$ increases with the increase of e whether mode is a1 or b2. Therefore, to achieve ZVS of $\text{S}_{\text{I-1}}$–$\text{S}_{\text{I-4}}$, the related minimum of e can be obtained according to (21), (22), (24), and (25), as shown

$$\begin{aligned}
e_{1\min} &= D-\sqrt{\frac{D}{2}-\frac{f_sL_{\text{I}}P_{\text{in}}}{2DV_{\text{in}}^2}-\sqrt{2L_{\text{I}}C_{o(\text{TR})12}f_s^2}}\\
e_{2\min} &= \sqrt{D^2-\frac{D}{2}-\frac{f_sL_{\text{I}}P_{\text{in}}}{2DV_{\text{in}}^2}+\sqrt{(8D-2)L_{\text{I}}C_{o(\text{TR})12}f_s^2}}\\
e_{3\min} &= D-\frac{1}{2}+\sqrt{\frac{1}{4}-\frac{D}{2}-\frac{f_sL_{\text{I}}P_{\text{in}}}{2DV_{\text{in}}^2}+\frac{f_sL_{\text{I}}I_{\text{ZVSmin}}}{V_{\text{in}}}}\\
e_{4\min} &= D-\sqrt{\frac{D}{2}-\frac{f_sL_{\text{I}}P_{\text{in}}}{2DV_{\text{in}}^2}-\frac{f_sL_{\text{I}}I_{\text{ZVSmin}}}{V_{\text{in}}}}.
\end{aligned} \tag{26}$$

To achieve ZVS of $S_{\text{I-1}} \sim S_{\text{I-4}}$ simultaneously, e must be the maximum value in (26), i.e.,

$$e_{\min} = \max\{e_{1\min}, e_{2\min}, e_{3\min}, e_{4\min}\}. \tag{27}$$

B. Power Loss Related to Phase-Shift Angle and the Choke Inductor

The choke inductor and the phase-shift angle shape the waveform of i_L. i_L determines the conduction loss and switching loss of primary switches, and determines the winding loss and core loss of the choke inductor. These four types of loss are discussed as follow.

1) Conduction Loss of Primary Switches: The RMS current of the choke inductor L_{I}, resonant inductor L_r and switches $S_{\text{I-1}} \sim S_{\text{I-4}}$ are denoted as I_L, I_R, and $I_{SI\text{-}1} \sim I_{SI\text{-}4}$, respectively.

According to the KCL principle of switching node $A_{\rm I}$, there is

$$I_{\rm SI-1}^2 + I_{\rm SI-2}^2 = I_L^2. \tag{28}$$

According to the KCL principle of switching node $B_{\rm I}$, there is

$$\begin{aligned} I_{\rm SI-3}^2 + I_{\rm SI-4}^2 &= \frac{1}{T_s}\int_0^{T_s} (i_L - i_r)^2 dt \\ &= I_L^2 + I_R^2 - \frac{1}{T_s}\int_0^{T_s} 2 i_L i_r dt. \end{aligned} \tag{29}$$

According to (6) and (8), I_L can be obtained as

$$\begin{aligned} I_L^2 = {} & \left[2D^2 - (4e+1)D + 4e^2\right] \cdot \frac{P_{\rm in}}{4Df_sL_{\rm I}} + \frac{P_{\rm in}^2}{4D^2V_{\rm in}^2} \\ & + \begin{bmatrix} 4D^4 - (12e+4)D^3 + (18e^2+6e+1)D^2 \\ -(16e^3+3e^2)D + 6e^4 \end{bmatrix} \cdot \frac{V_{\rm in}^2}{6f_s^2L_{\rm I}^2}. \end{aligned} \tag{30}$$

The resonant current $i_{\rm r}$ is

$$i_r = \frac{\pi P_{\rm in}}{2V_M}\sin(2\pi f_s t) = \frac{\pi P_{\rm in}}{4DV_{\rm in}}\sin(2\pi f_s t). \tag{31}$$

Thus

$$I_R^2 = \frac{1}{T_s}\int_0^{T_s} i_r^2 dt = \frac{\pi^2 P_{\rm in}^2}{32D^2V_{\rm in}^2} \tag{32}$$

$$\frac{1}{T_s}\int_0^{T_s} 2 i_L i_r dt = \frac{P_{\rm in}}{8\pi D f_s L_{\rm I}}\left[\sin 2\pi(D-e) - \sin 2\pi(1-e)\right]. \tag{33}$$

If the ON-resistance of buck bridge and boost bridge are $R_{\rm ds(on)1}$ and $R_{\rm ds(on)2}$, then the total conduction loss of primary switches is

$$P_{\rm con} = 2\left[(I_{\rm SI-1}^2 + I_{\rm SI-2}^2)R_{\rm ds(on)1} + (I_{\rm SI-3}^2 + I_{\rm SI-4}^2)R_{\rm ds(on)2}\right]. \tag{34}$$

Equations (28)–(34) indicate that $P_{\rm con}$ is a binary function of $L_{\rm I}$ and e under specific $V_{\rm in}$ and $P_{\rm in}$.

2) Switching Loss of Switches: The turn-ON loss is eliminated by ZVS, so only turn-OFF loss is discussed. The turn-OFF loss relates to the driver circuit, the switching device, the turn-OFF voltage and the turn-OFF current. It can be calculated by the model proposed in [26], but the process is complicated. For the convenience of analysis, the turn-OFF loss under several voltage and current is calculated by that model, and then the turn-OFF loss under any voltage or any current is obtained by curve fitting. The turn-OFF voltage of buck bridge is $V_{\rm in}$, which is variable. Thus, the turn-OFF loss of buck bridge is fitted as a binary function about $V_{\rm in}$ and $I_{\rm off}$

$$\begin{aligned} P_{\rm sw-buck} = {} & k_1(V_{\rm in}I_{\rm off})^2 + k_2V_{\rm in}^2 + k_3I_{\rm off}^2 + k_4V_{\rm in} \\ & + k_5I_{\rm off} + k_6. \end{aligned} \tag{35}$$

The turn-OFF voltage of boost bridge is V_M, which is constant. Thus, the turn-OFF loss of boost bridge is fitted as a unary function about $I_{\rm off}$

$$P_{\rm sw-boost} = l_1I_{\rm off}^2 + l_2I_{\rm off} + l_3. \tag{36}$$

The total turn-OFF loss of primary side switches is

$$P_{\rm sw} = 2\begin{bmatrix} P_{\rm sw-buck}(V_{\rm in}, |I_1|) + P_{\rm sw-buck}(V_{\rm in}, |I_2|) \\ +P_{\rm sw-boost}(|I_3|) + P_{\rm sw-boost}(|I_4|) \end{bmatrix}. \tag{37}$$

Equations (25) and (35)–(37) indicate that $P_{\rm sw}$ is a binary function of $L_{\rm I}$ and e under specific $V_{\rm in}$ and $P_{\rm in}$.

3) Winding Loss of the Choke Inductor: Toroidal core is used in the inductor, so the winding loss can be estimated by the dc resistance of coils. The current stress of the choke inductor is given in (30). If the dc resistance of coils is R_L, then the winding loss is

$$P_{\rm cu} = 2I_L^2R_L. \tag{38}$$

Equations (30) and (38) indicate that $P_{\rm cu}$ is a binary function of $L_{\rm I}$ and e under specific $V_{\rm in}$ and $P_{\rm in}$.

4) Core Loss of the Choke Inductor: The waveform of i_L is not sinusoidal, so the method in [27] is employed to calculate core loss. The calculation formula is

$$P_v = \frac{1}{T_s}\int_0^{T_s} k_i\left|\frac{dB}{dt}\right|^{\alpha}(\Delta B)^{\beta-\alpha}dt \tag{39}$$

$$k_i = \frac{k}{(2\pi)^{\alpha-1}\int_0^{2\pi}|\cos\theta|^{\alpha}2^{\beta-\alpha}d\theta}. \tag{40}$$

where k, α, and β are from datasheet of core. dB/dt and ΔB are related to $I_1 \sim I_4$ expressed in (25). The core loss of the choke inductor is

$$P_{\rm fe} = 2P_vV_e. \tag{41}$$

Equations (25) and (39)–(41) indicate that $P_{\rm fe}$ is a binary function of $L_{\rm I}$ and e under specific $V_{\rm in}$ and $P_{\rm in}$.

The above four types of loss are all related to the components, input voltage $V_{\rm in}$, input power $P_{\rm in}$, choke inductor $L_{\rm I}$ and phase-shift angle e. Under specific $V_{\rm in}$, $P_{\rm in}$ and components, the total loss $P_{\rm loss}$ is a binary function of $L_{\rm I}$ and e, as shown as

$$P_{\rm loss} = P_{\rm con} + P_{\rm sw} + P_{\rm cu} + P_{\rm fe} = f(e, L_{\rm I})|_{V_{\rm in},P_{\rm in}} \tag{42}$$

where $L_{\rm I}$ and e are independent of each other, so it is hard to solve the minimum of $P_{\rm loss}$. However, it is found that if e is larger than the $e_{\rm min}$ expressed in (27), then $P_{\rm con}$, $P_{\rm sw}$, $P_{\rm cu}$, and $P_{\rm fe}$ will increase with the increase of e. It means that $P_{\rm loss}$ is a monotonic function of e, no matter what $V_{\rm in}$, $P_{\rm in,}$ and $L_{\rm I}$ are. Therefore, the relative minimum $P_{\rm lossmin\text{-}r}$ under specific $L_{\rm I}$ must be obtained at $e = e_{\rm min}$

$$P_{\rm lossmin-r} = f(e_{\rm min}, L_{\rm I})|_{V_{\rm in},P_{\rm in}}. \tag{43}$$

Equation (26) and (27) indicate that $e_{\rm min}$ is the function of $L_{\rm I}$

$$e_{\rm min} = g(L_{\rm I})|_{V_{\rm in},P_{\rm in}}. \tag{44}$$

By substituting (44) into (43), $P_{\rm lossmin\text{-}r}$ is simplified as a unary function

$$\begin{aligned} P_{\rm lossmin-r} &= f(e_{\rm min}, L_{\rm I})|_{V_{\rm in},P_{\rm in}} = f(g(L_{\rm I}), L_{\rm I})|_{V_{\rm in},P_{\rm in}} \\ &= f(L_{\rm I})|_{V_{\rm in},P_{\rm in}}. \end{aligned} \tag{45}$$

According to (45), the curve describing $L_{\rm I}$ and $P_{\rm lossmin\text{-}r}$ can be obtained, then the absolute minimum $P_{\rm lossmin}$ and related optimal $L_{\rm I}$ can be determined.

TABLE III
PARAMETERS OF THE CONVERTER

Input voltage V_{in}	350 V ~ 430 V
Intermediate bus voltage V_M	384 V
Output voltage V_o	24 V
Output power P_o	600 W
Switching frequency f_s	1 MHz

TABLE IV
OPTIONAL COMBINATIONS OF PRIMARY SWITCHES

Optional Combinations		S_{I-3} and S_{I-4}		
		GS66504B	GS66506T	GS66508T
S_{I-1} and S_{I-2}	GS66504B	04B/04B	04B/06T	04B/08T
	GS66506T	06T/04B	06T/06T	06T/08T
	GS66508T	08T/04B	08T/06T	08T/08T

C. Design Example

A specific converter is employed in this section to explain the proposed design procedure more clearly. The detailed parameters are given in Table III.

As indicated in (23)–(27), the parameter $C_{o(\mathrm{TR})12}$, $C_{o(\mathrm{TR})34}$, and $C_{o(\mathrm{TR})56}$ are required to obtain $e_{\min} = g(L_{\mathrm{I}})|_{V_{\mathrm{in}},P_{\mathrm{in}}}$. Therefore, first step is selecting switching devices. The voltage stress and current stress of device S_5 and S_6 are irrelevant with L_{I} and e, so they are selected according to the $R_{\mathrm{ds(on)}}$ and thermal resistance. GaN device EPC2065 is chosen. Four switches are connected in parallel to avoid overheating. Its $C_{o(\mathrm{TR})}$ and $R_{ds(on)@70\,^{\circ}\mathrm{C}}$ are 842 pF and 3.7 mΩ. As for $S_{\mathrm{I}\text{-}1} \sim S_{\mathrm{I}\text{-}4}$, the optional devices under rated input voltage and full load are GS66504B, GS66506T and GS66508T. Their $C_{\mathrm{o(TR)}}$ are 71, 106 and 142 pF, and their $R_{ds(on)@70\,^{\circ}\mathrm{C}}$ are 150, 100, and 75 mΩ, respectively. Since the current stress of $S_{\mathrm{I}\text{-}1}$ and $S_{\mathrm{I}\text{-}2}$ are close, they are chosen as same type, so are $S_{\mathrm{I}\text{-}3}$ and $S_{\mathrm{I}\text{-}4}$. There are nine choices of switch combinations, as given in Table IV ("04B/06T" means that $S_{\mathrm{I}\text{-}1} \sim S_{\mathrm{I}\text{-}2}$ are GS66504B, and $S_{\mathrm{I}\text{-}3} \sim S_{\mathrm{I}\text{-}4}$ are GS66506T). Under rated input voltage (384 V), different load, different L_{I} and related $e_{\min}$ expressed in (27), the conduction loss is figured out according to (23)–(34) and drawn in Fig. 14 (t_{dmax} in (24) is taken as 30 ns).

Under rated input voltage and full load, the ZVS of $S_{\mathrm{I}\text{-}3}$ and $S_{\mathrm{I}\text{-}4}$ dominates $e_{\min}$. In other words, e takes $e_{\min 3}$ or $e_{\min 4}$ in (27). $S_{\mathrm{I}\text{-}1}$ and $S_{\mathrm{I}\text{-}2}$ could achieve ZVS if $S_{\mathrm{I}\text{-}3}$ and $S_{\mathrm{I}\text{-}4}$ can achieve ZVS. Thus, P_{con} is lower as long as the $R_{\mathrm{ds(on)}}$ of $S_{\mathrm{I}\text{-}1}$ and $S_{\mathrm{I}\text{-}2}$ is smaller (for same shape point, blue line is below green line, and green line is below red line, as shown in Fig. 14(a)). However, if the $R_{\mathrm{ds(on)}}$ of $S_{\mathrm{I}\text{-}3}$ and $S_{\mathrm{I}\text{-}4}$ is smaller, their $C_{o(\mathrm{TR})}$ is larger, and higher ZVS current is required. This increases the conduction loss P_{con} instead [for same color line, round points are above square points, and square points are above triangle points, as shown in Fig. 14(a)]. Therefore, smaller $R_{\mathrm{ds(on)}}$ of $S_{\mathrm{I}\text{-}1}$ and $S_{\mathrm{I}\text{-}2}$ and larger $R_{\mathrm{ds(on)}}$ of $S_{\mathrm{I}\text{-}3}$ and $S_{\mathrm{I}\text{-}4}$ are better for decreasing the conduction loss. It means that the combination "08T/04B" induces minimum P_{con}, as shown in Fig. 14(a). The situation of

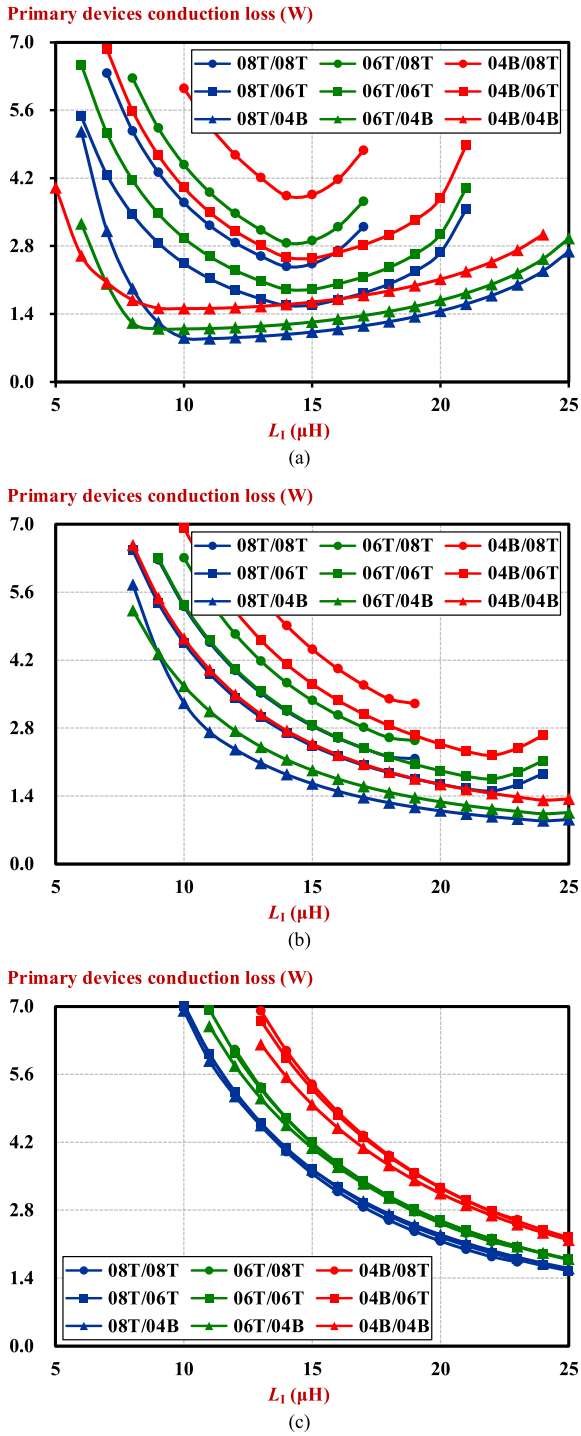

Fig. 14. Conduction loss of primary switches under rated voltage, different load and different choke inductance. (a) Full load condition. (b) 60% load condition. (c) 20% load condition.

60% load is similar to that of full load, as shown in Fig. 14(b). In very light load condition (20% load), the $R_{\mathrm{ds(on)}}$ of $S_{\mathrm{I}\text{-}1}$ and $S_{\mathrm{I}\text{-}2}$ domains the conduction loss while the $R_{\mathrm{ds(on)}}$ of $S_{\mathrm{I}\text{-}3}$ and $S_{\mathrm{I}\text{-}4}$ is not very important, as shown in Fig. 14(c). In summary, the combination "08T/04B" is the best choice in whole load range. However, from Fig. 14, it is also noticed that the P_{con} in combination "06T/04B" is only slightly higher than "08T/04B",

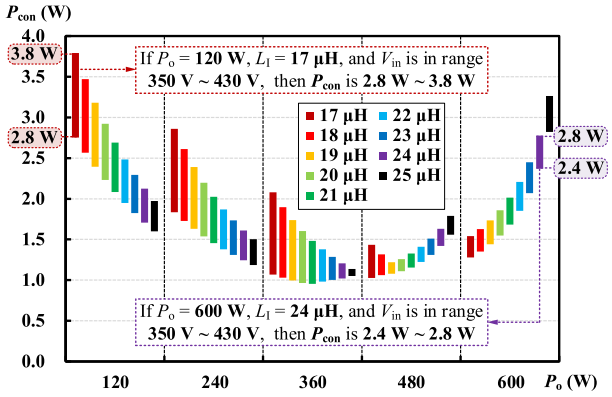

Fig. 15. Conduction loss varies with voltage, load, and inductance.

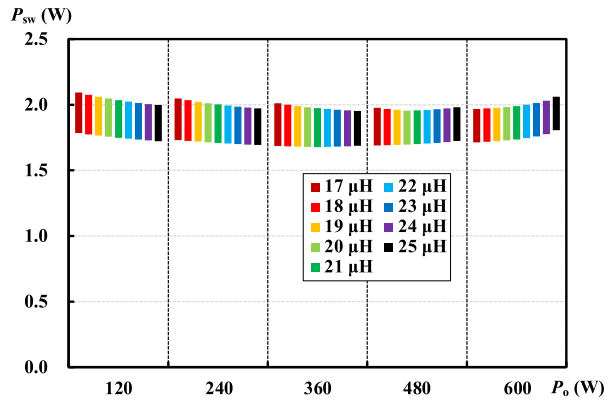

Fig. 16. Switching loss varies with voltage, load, and inductance.

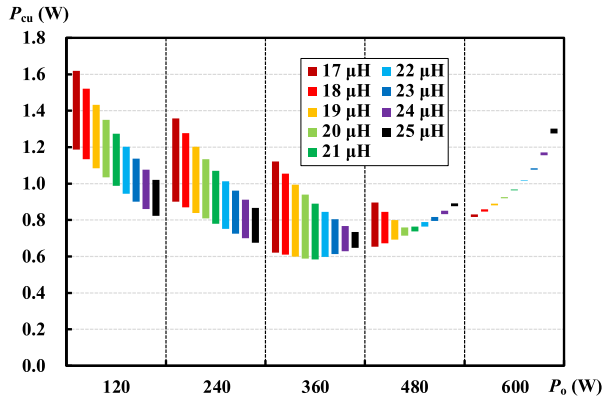

Fig. 17. Winding loss varies with voltage, load, and inductance.

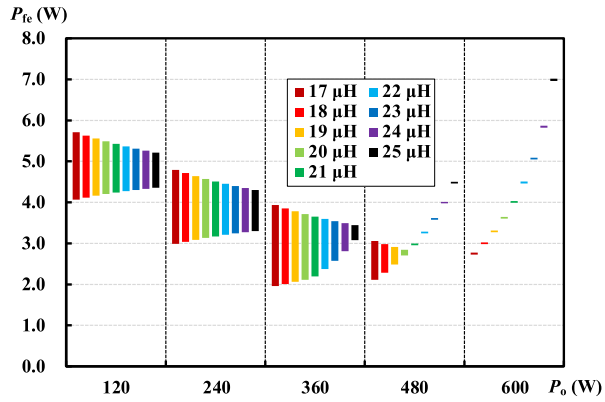

Fig. 18. Core loss varies with voltage, load, and inductance.

but the price of GS66506T is lower than that of GS66508T. Thus, the final design result for $S_{I\text{-}1}$–$S_{I\text{-}4}$ is "06T/04B", i.e., $S_{I\text{-}1}$–$S_{I\text{-}2}$ are GS66506T, and $S_{I\text{-}3}$–$S_{I\text{-}4}$ are GS66504B.

Once the switches are chosen, the function $e_{\min} = g(L_I)|_{V_{in},P_{in}}$ is obtained. Furthermore, the conduction loss P_{con} and the switching loss P_{sw} can be obtained under specific V_{in}, P_{in} and L_I. P_{con} and P_{sw} under different input voltage, load ($P_{in} = P_o/\eta$, η is estimated as 95%) and choke inductance are given in Figs. 15 and 16. Fig. 15 is divided into five columns horizontally, and every column represents a load condition. Nine colored lines in every column represent loss range under different inductance. For example, the first deep red line in first column means that when P_o is 120 W, L_I is 17 μH, and V_o is in range 350–430 V, the related conduction loss P_{con} is in range 2.8–3.8 W. The eighth purple line in fifth column means that when P_o is 600 W, L_I is 24 μH, and V_{in} is in range 350–430 V, the related conduction loss P_{con} is in range 2.4–2.8 W. Fig. 15 indicates that the conduction loss P_{con} decreases with the increase of L_I in light load condition (less than 240 W), and it increases with the increase of L_I in heavy load condition (higher than 480 W). In other words, if L_I is small (like 17 μH, deep red line), P_{con} roughly decreases with the increase of load; if L_I is large (like 25 μH, black line), P_{con} roughly increases with the increase of load; a medium L_I (like 23 μH, blue line) leads to the P_{con} curve formed like high at both ends and low in the middle. The trend of the switching loss P_{sw} shown in Fig. 16 is same as the trend of P_{con}, but it is less obvious.

To obtain the winding loss P_{cu} and the core loss P_{fe} of the choke inductor, the parameters of coils and core are necessary. Therefore, the hardware of inductor needs to be preset. According to the rms value and ripple of inductor current, the powder core T68-2-D manufactured by Micrometals is used. Corresponding to the inductance range 17–25 μH, the number of turns of winding is from 39 to 47. With these parameters of coils and cores, the winding loss P_{cu} and core loss P_{fe} can be obtained. The curves of them are given in Figs. 17 and 18.

The trend of P_{cu} and P_{fe} are similar to that of P_{con}. The total loss P_{loss} curve is given in Fig. 19.

As shown in Fig. 19, the trend of total loss P_{loss} is also similar to that of P_{con}. If desire the converter to have high efficiency at heavy load and full load, and the devices will not be damaged due to overheating in light load condition (the light load operation time is short or thermal condition is enough), then the choke inductor can be designed smaller (17 μH, deep red line). If desire the converter to stably operate in whole load range, then the designed choke inductance should ensure approximately same loss in two ends of load condition. A medium inductance (23 μH, blue line) satisfies this requirement. In this article, 23 μH is chosen.

In summary, this section discusses the ZVS condition of all primary switches and four types of loss related to L_I and e.

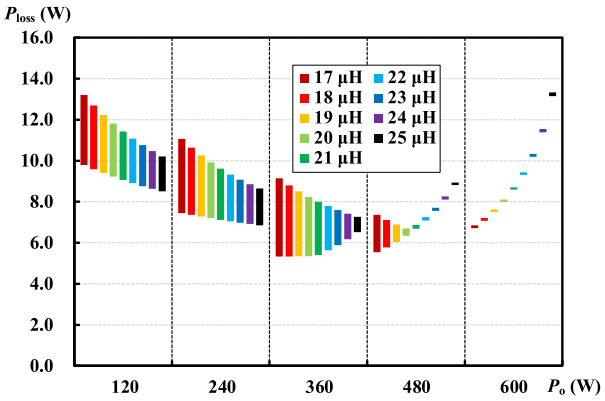

Fig. 19. Total primary loss varies with voltage, load, and inductance.

TABLE V
PARAMETERS OF MAIN COMPONENTS

Choke inductance $L_{\rm I}$ and $L_{\rm II}$	23 μH, T68-2D, 47 turns
Resonant inductance $L_{\rm r}$	3.8 μH
Resonant capacitance $C_{\rm r}$	6.6 nF
Magnetizing inductance $L_{\rm m}$	450 μH
Transformer T	16:1:1, EQ25, PC200
Quality factor under full load	0.12
Input capacitance $C_{\rm i}$	4.4 μF
Intermediate capacitance $C_{\rm M}$	4.4 μF
Output capacitance $C_{\rm i}$	200 μF
Switches $S_{\rm I\text{-}1}$, $S_{\rm I\text{-}2}$, $S_{\rm II\text{-}1}$ and $S_{\rm II\text{-}2}$	GS66506T
Switches $S_{\rm I\text{-}3}$, $S_{\rm I\text{-}4}$, $S_{\rm II\text{-}3}$ and $S_{\rm II\text{-}4}$	GS66504B
Switches S_5, S_6	EPC2065
Primary Drivers	Si8271
Secondary Drivers	FAN3122
MCU	STM32F334

The relationship between loss and e is used to simplify the design procedure: the total loss becomes a unary function of $L_{\rm I}$. Thus, the optimal $L_{\rm I}$ is easy to be determined.

V. EXPERIMENTAL VERIFICATION

In this section, a prototype is built to verify the high efficiency and high power density characteristic of both the proposed converter and the proposed comprehensive optimal design method. The parameters of the prototype are given in Table III. The parameters of main components are given in Table V.

The size of prototype is given in Fig. 20. The volume is 70 × 65 × 12 mm^3, and its power density under full load 600 W is 180 W/in^3.

Fig. 21 gives the voltage and current of two choke inductors under rated input voltage (384 V) and full load (600 W): i_{LI}; $v_{\rm AI\text{-}BI}$; $i_{\rm LII;}$ and $v_{\rm AII\text{-}BII}$. It is noticed that the difference between i_{LI} and i_{LII} is ignorable. It means that the consistency between two phases is acceptable, so it is not necessary to consider current

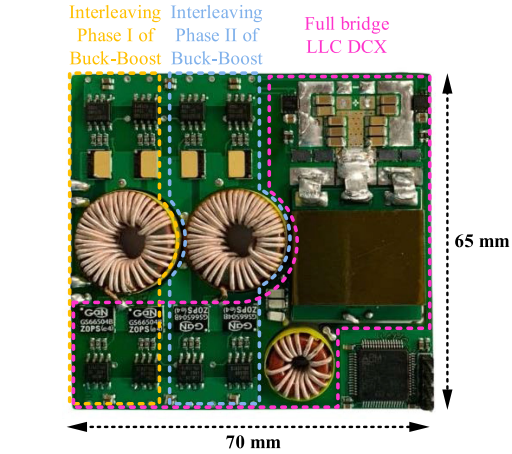

Fig. 20. Prototype of the IIBBL converter.

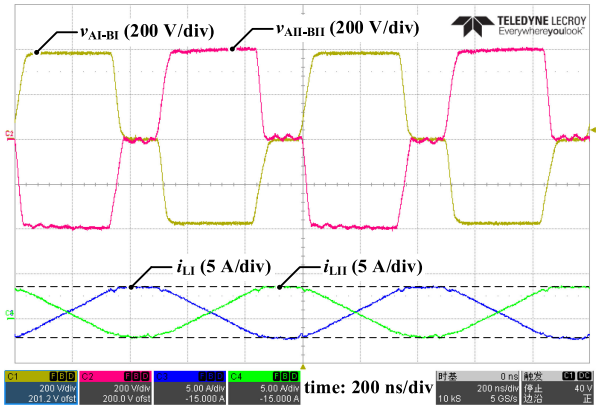

Fig. 21. Voltage and current of two phase choke inductors.

sharing issues. The difference between $v_{\rm AI\text{-}BI}$ and $v_{\rm AII\text{-}BII}$ is caused by the two different probes.

The main waveforms under different input voltage (350, 384, and 430 V) and different load condition (25%, 62.5%, and100%) are given in Fig. 22. $i_{\rm L}$ is the current through choke inductor $L_{\rm I}$, and $v_{\rm AI\text{-}BI}$ is the voltage across $L_{\rm I}$. Each turning point of $i_{\rm L}$ and $v_{\rm AI\text{-}BI}$ represents a switching moment of primary switches. Phase-shift angle e is labelled in the figure. $v_{\rm BI\text{-}BII}$ is the input voltage of the resonant tank. The rising time and falling time of $v_{\rm BI\text{-}BII}$ are almost same so that the resonant current i_r is purely sinusoidal, no matter how load condition is. It ensures symmetric secondary current. This result can not be achieved in [22] and [23] which use large resonant inductor or symmetric modulation.

Fig. 23 gives the $v_{\rm DS}$ and $v_{\rm GS}$ of primary switches under rated input voltage and full load. It can be seen that ZVS of all switches are achieved. This proves the analysis in Section IV isxbrk proper.

The solid line in Fig. 24 gives the measured efficiency of proposed design. The topology in [22], [23], and [25] is single phase integrated buck-boost-*LLC*, but their voltage level are close to this article, and the main design considerations are also choke inductor and phase-shift angle, so their efficiencies

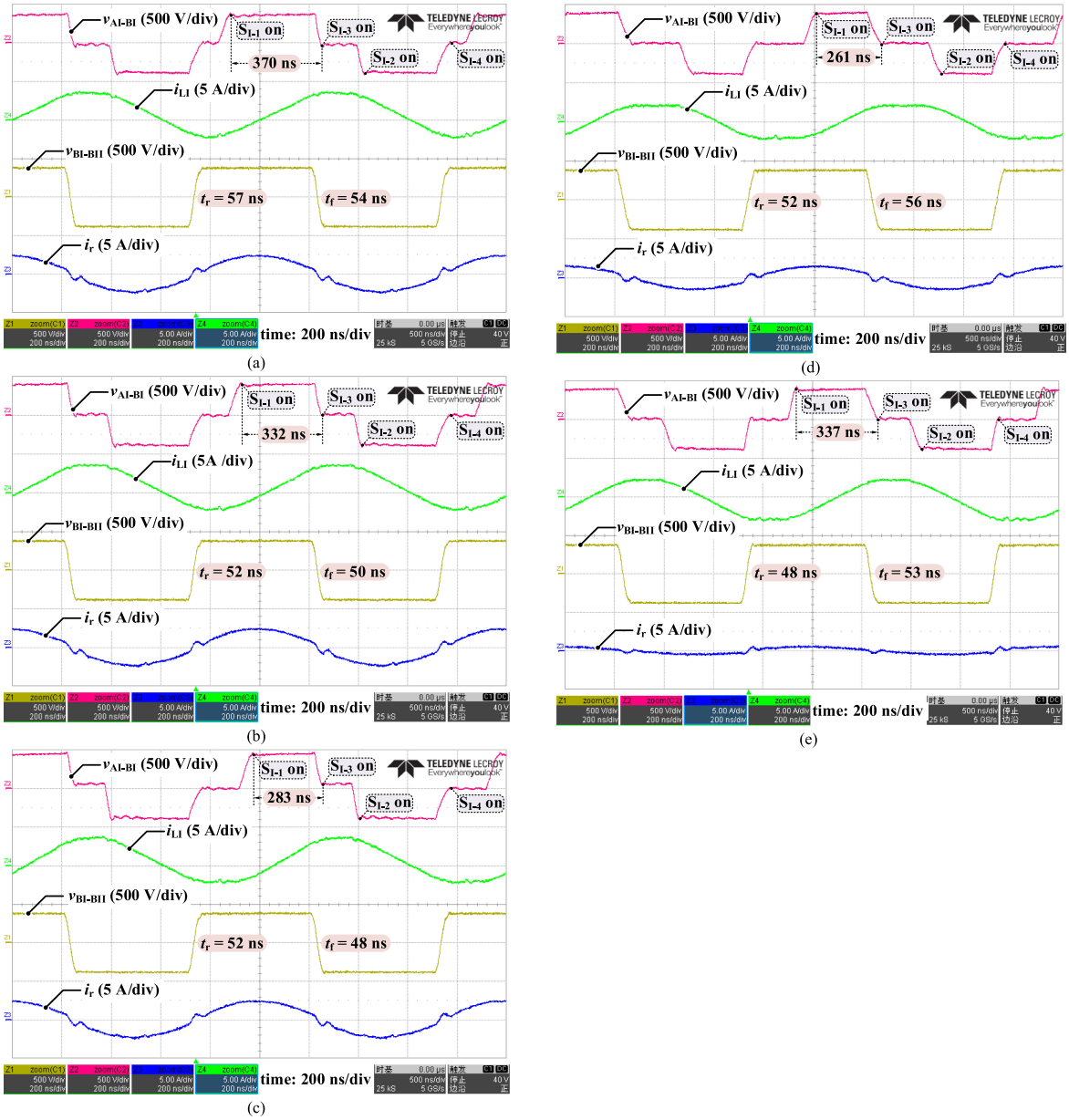

Fig. 22. Main waveforms under different voltage and load. (a) $V_{\text{in}} = 350$ V and $P_o = 600$ W (100% load). (b) $V_{\text{in}} = 384$ V and $P_o = 600$ W (100% load). (c) $V_{\text{in}} = 430$ V and $P_o = 600$ W (100% load). (d) $V_{\text{in}} = 384$ V and $P_o = 375$ W (62.5% load). (e) $V_{\text{in}} = 384$ V and $P_o = 150$ W (25% load).

are also drawn for comparison (see dushed line). Clearly, the design proposed in this article achieves higher efficiency than [22] and [25] in whole load range. The full load efficiency of the proposed design is 95.7%. Under rated voltage, the light load efficiency in this article is higher than that in [23], because the modulation method in [23] cannot improve the asymmetry issues under light load. In heavy load condition, Wang *et al.* [23] achieves higher efficiency because it can also achieve symmetric secondary current and its frequency is only half of this article.

Fig. 25 gives the detailed loss distribution under rated input voltage and full load condition. Other loss includes the loss of capacitors, resonant inductor, copper of PCB and so on.

With the results in Fig. 25, the reason why heavy load efficiency decreases compared with [23] can be explained in more detail. The loss comparison between the proposed design and [23] under rated voltage and power is given in Fig. 26.

The loss is divided into four types: switches, inductor(s), transformer and others. The loss ratio is obtained by dividing the loss by the input power. 100% minus the sum of the loss ratio is the converter efficiency. As indicated by Fig. 26, the loss ratio of switches in proposed design is less than that in [23] despite more switches. The obvious parts of increased loss are the inductor(s) and the transformer. The core loss of powder core inductor and the winding loss of PCB planar transformer will significantly increase with frequency.

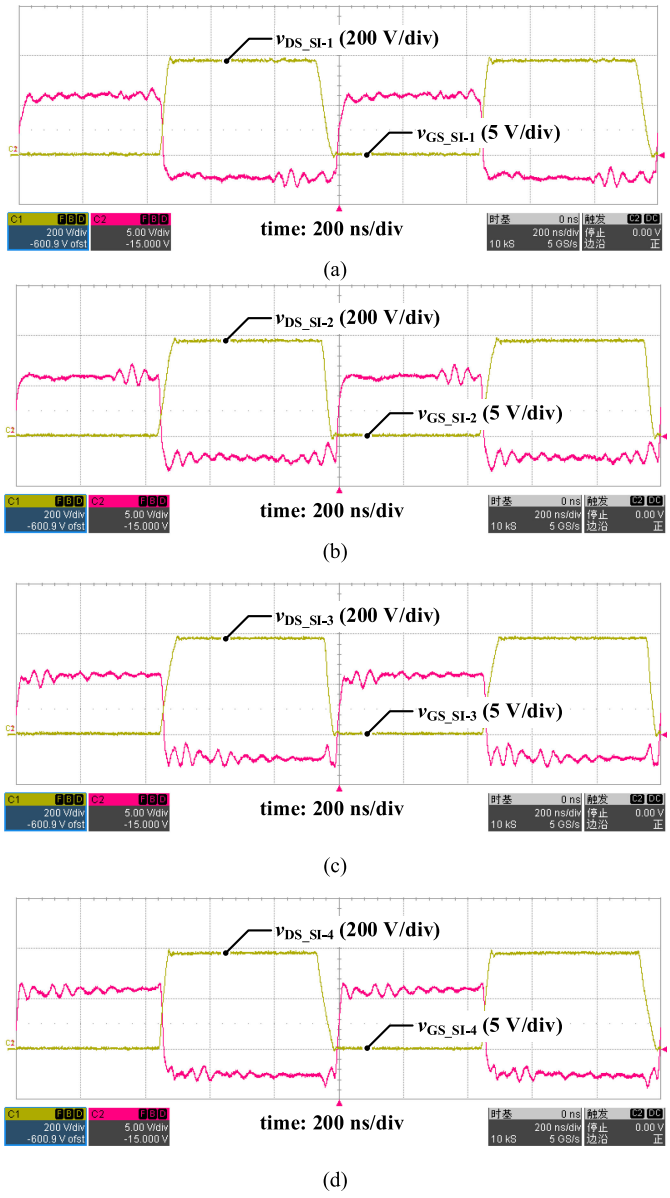

Fig. 23. ZVS of primary switches under rated input voltage (384 V) and full load (600 W) condition. (a) ZVS of S_{I-1}. (b) ZVS of S_{I-2}. (c) ZVS of S_{I-3}. (d) ZVS of S_{I-4}.

Driving loss and PCB copper loss also increases with frequency. Therefore, the reason for lower heavy load efficiency is the raised switching frequency but not the increased number of switches. Besides, the proposed IIBBL converter achieves higher light load efficiency despite higher frequency. Predictably, the enhancement of light load efficiency will be more distinct under same frequency. The increased frequency degrades efficiency but improves power density. The power density of [23] is 142 W/in^3 (not contains controller), while the power density of proposed design is 180 W/in^3 (contains controller). Exactly because of severe asymmetry issue under light load, 1 MHz is not achieved in [23]. One benefit of the proposed IIBBL converter is the possibility of higher frequency and higher power density.

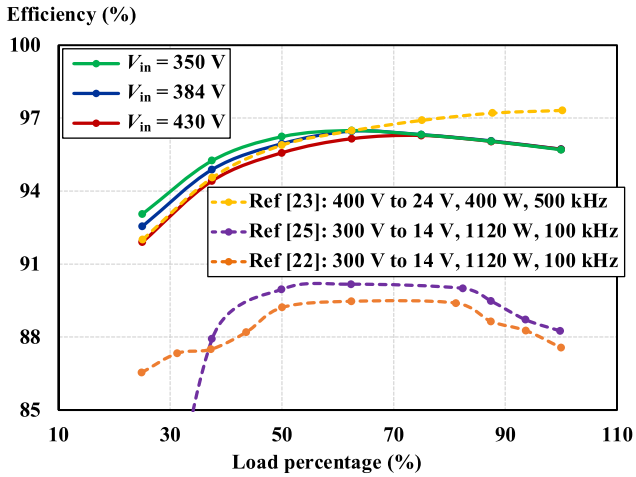

Fig. 24. Measured efficiency.

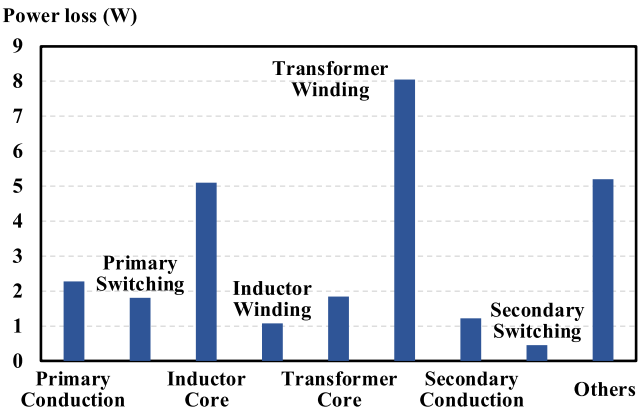

Fig. 25. Loss breakdown under rated voltage and full load.

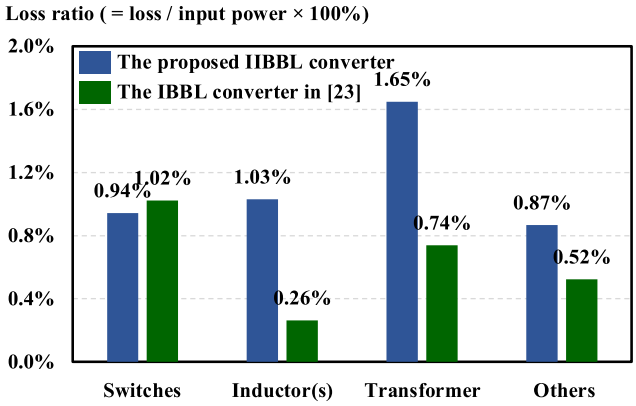

Fig. 26. Loss breakdown and loss ratio under rated voltage and power.

Fig. 27 gives the full-load thermal result of the prototype. The ambient temperature is 25°C and the fan speed is 2850 r/min. Because of high temperature of secondary windings and tiny size of the rectifier switches, the most heated devices are the rectifier switches. The high loss of powder core is also observed. The temperature of all primary switches is much lower, which means this prototype can afford heavier load if the thermal design of secondary devices is better.

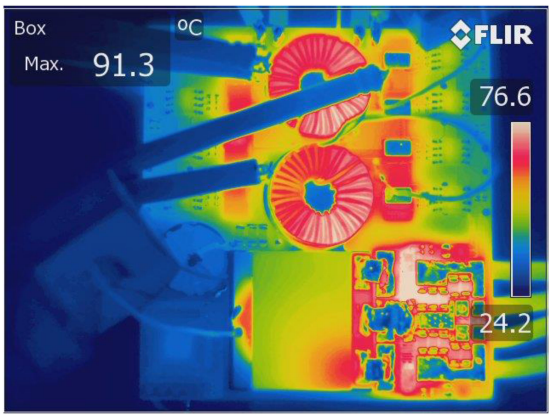

Fig. 27. Thermal test under rated input voltage and full load condition.

VI. Conclusion

This article proposes a two-phase interleaved integrated buck-boost-*LLC* converter with which it is easy to achieve high efficiency and high power density. Besides, a comprehensive optimal design method for this converter is given. The proposed topology can solve the distorted resonant current and asymmetrical secondary current issue which occurs in single phase converter. Therefore, the design limitation of the choke inductor, the phase-shift angle and the resonant parameters is dismissed. In other words, the design freedom of the converter is improved. The proposed method for designing the choke inductor and the phase-shift angle can achieve ZVS of all switches and minimize the power loss of primary side components, so the efficiency is improved. Frequency is raised to 1 MHz because ZVS is achieved in whole voltage range and load range, so that high power density is also achieved. The experiment results verify that the proposed converter achieves sinusoidal resonant current in whole load range, and 95.7% full load efficiency and 180 W/in^3 power density are achieved under the proposed optimal design method.

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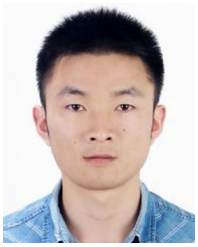

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