Letters

Transformerless Series-Connected Current Source Converter

Ling Xing, Qiang Wei, *Senior Member, IEEE*, and Yunwei Li, *Fellow, IEEE*

***Abstract*—Series-connected current source converters (SC-CSCs) are a good candidate for high-power, medium-/high-voltage applications. However, existing SC-CSCs require the use of bulky and costly transformer. In this article, a transformerless SC-CSC is proposed. The operation principle of the proposed SC-CSC is presented, and the modulation is developed. A case study is conducted to verify the performance of the converter.**

***Index Terms*—Series-connected current source converters (SC-CSCs).**

I. Introduction

CURRENT source converters (CSCs) with inherent reliable short-circuit protection and without *dv*/*dt* issue are preferable converters for high-power applications [1]–[3]. Existing CSCs can be classified into conventional CSC [4]–[7], multilevel CSC [8]–[11], parallel-connected CSC [12]–[14], and series-connected CSC (SC-CSC) [15]–[20]. Both conventional CSC and multilevel CSC can be used in both low-/medium-voltage, low-/high-power applications, while the parallel-connected and SC-CSCs are proposed for higher power applications. The SC-CSC is a good candidate for medium-/high-voltage, high-power applications.

Existing SC-CSCs require the use of transformers either at the input [15] or at the output [16]–[20]. Fig. 1 shows an example of the SC-CSC with transformers at the output. The transformers play two roles: One is to provide independent current path for each CSC module to enable series connections of CSCs, and the other is to boost voltage to reduce power loss. However, such transformers are bulky and costly. To address this issue, a transformerless SC-CSC is proposed. It does not need transformers and has inherent current/voltage balancing.

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Ling Xing and Yunwei Li are with the Electrical and Computer Engineering Department, University of Alberta, Edmonton, AB T6G 2R3, Canada (e-mail: lxing1@ualberta.ca; yunwei.li@ualberta.ca).

Qiang Wei is with the Electrical Engineering Department, Lakehead University, Thunder Bay, ON P7B 5E1, Canada (e-mail: qwei@lakeheadu.ca).

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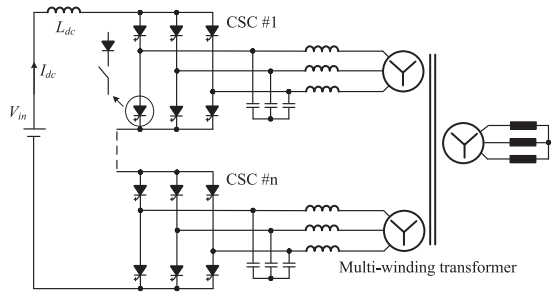

Fig. 1. Example of existing series-connected CSCs.

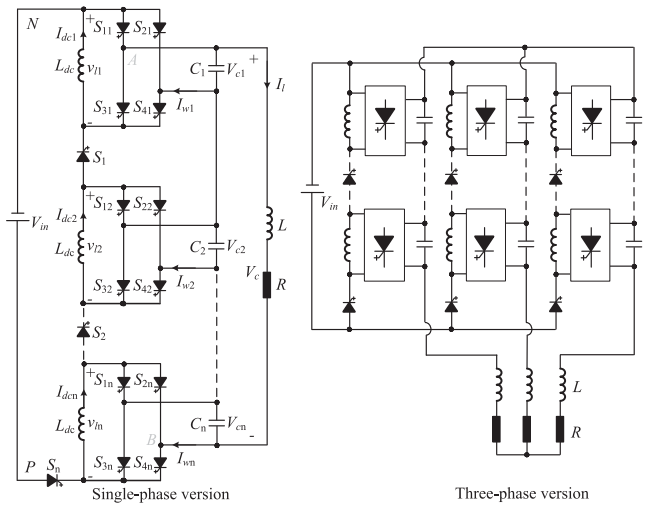

Fig. 2. Proposed transformerless SC-CSC.

II. Transformerless Series-Connected CSC

A. Operation Principle

Fig. 2 shows the proposed transformerless SC-CSC consisting of n identical modules connected in series at both input and output. Each module consists of an H-bridge CSI and an extra switch $S_{\rm n}$ ($n = 1, 2, \ldots$). In the following, a two-module converter is taken as an example to illustrate the operation principle of the converter. The three-phase version of the proposed converter is not discussed here.

Mode 1: As shown in Fig. 3, CSCs are OFF and switches S_1 and $S_{\rm n}$ are ON, and the dc inductors $L_{\rm dc}$ are charging. Inherent dc current balancing ($I_{\rm dc1} = I_{\rm dc}n$) is ensured.

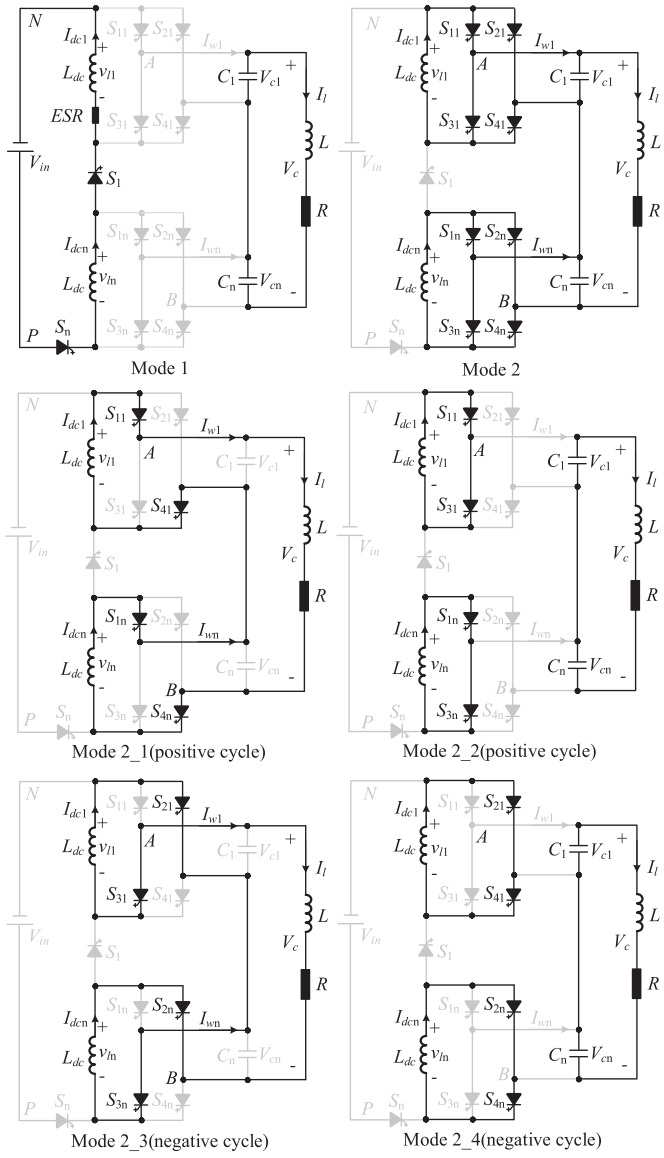

Fig. 3. Operation principle of the proposed SC-CSC.

Mode 2: Switches S_1 and S_n are OFF to provide independent current sources (I_{dc1}, I_{dcn}) for each H-bridge CSC. As a result, the output capacitors are connected in series to build high voltages without the transformer used in existing SC-CSCs. Mode 2 can be further divided into four modes as shown in Fig. 3 in which all H-bridge CSIs are controlled in a synchronous manner. In this mode, $I_{dc1} = I_{dcn}$ is ensured; balanced capacitor currents are achieved according to kirchhoffs circuit law (KCL); and inherent voltage balancing ($V_{c1} = V_{cn}$) is achieved.

Assuming a grid-connected operation, the common mode model is shown in Fig. 4 where the filter inductor is divided into two parts to limit the common mode current. C_{st} is the stray capacitance, and Z is the equivalent impedance of the common mode circuit. The proposed converter has a total of five operating modes as shown in Fig. 3. The common mode voltage and current under each mode are listed in Table I. Note that under Mode 1, the common mode voltage is not defined by the switching

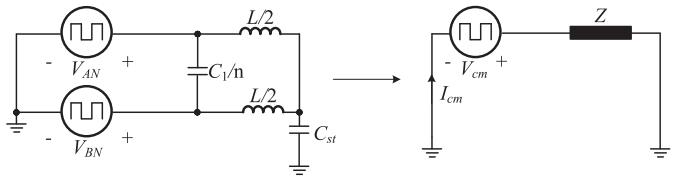

Fig. 4. Common mode model for the proposed converter: single-phase version.

TABLE I
COMMON MODE VOLTAGE AND CURRENT

Modes	V_{AN}	V_{BN}	$V_{cm} = (V_{AN} + V_{BN})/2$	I_{cm}
Mode 1	Floating	Floating	Floating	Floating
Mode 2_1	0	$-V_c$	$-V_c/2$	$-V_c/2Z$
Mode 2_2	0	$-V_c$	$-V_c/2$	$-V_c/2Z$
Mode 2_3	V_c/n	$-V_c/n$	0	0
Mode 2_4	V_c/n	$-V_c/n$	0	0

and its magnitude depends on the parasitic parameters, switches junction capacitances, etc.

The passive components of each module are designed the same as the conventional CSC. The dc inductor is designed based on the voltage-second principle. For example, the required dc inductor for a given current ripple can be obtained based on Mode 1 in which the inductor is charging and Mode 2_1 in which the inductor is discharging. The *LC* filter design depends on harmonics requirements. For example, under a switching frequency of around several hundred Hertz, the filter inductor is sizing around 0.1 p.u. and the filter capacitor around 0.5 p.u. [1]. Note that coupled inductors are a well-proven technology for reducing the inductors and can be used here. As the number of modules increases, the manufacturing of such coupled inductors may be a challenge.

B. Modulation Scheme

The switching pattern design for the proposed SC-CSC should satisfy the following two conditions simultaneously.

1) Sinusoidal Output Current i_{wn}: The conventional sinusodial pulse width modulation (SPWM) is applied to each CSC module in which S_{1n} ($n = 1, 2, \ldots$) and S_{2n} are operating with a fundamental frequency, while S_{3n} and S_{4n} are switching with the modulating frequency. For example, in the positive half cycle shown in Fig. 5, switches S_{1n} are ON and S_{2n} are OFF. The dwell time of S_{4n}, that is, T_1, is obtained by comparing the modulating wave (T_1) and the carrier wave. T_0 is divided into T_{01} for S_n and T_{02} for S_{3n}

$$\begin{aligned} T_1 &= m_a \sin(\omega t) T_s \\ T_s &= T_0 + T_1 = T_{01} + T_{02} + T_1. \end{aligned} \tag{1}$$

2) Voltage-Second Principle of Inductors L_{dc}: On this basis, the duty cycle T_{01} for switches S_n is obtained

$$\begin{cases} v_{\text{ln\_charging}} = -\frac{V_{in}}{n} + V_s + V_{ESR} \\ v_{\text{ln\_discharging}} = v_{cn} + 2V_s + V_{ESR} \\ v_{\text{ln\_discharging}} T_1 + v_{\text{ln\_charging}} T_{01} = 0 \\ v_{cn} = \frac{\sqrt{2} V_c}{n} |\sin(\omega t - \theta)| \end{cases} \rightarrow T_{01} = -\frac{v_{\text{ln\_discharging}} T_1}{v_{\text{ln\_charging}}} \tag{2}$$

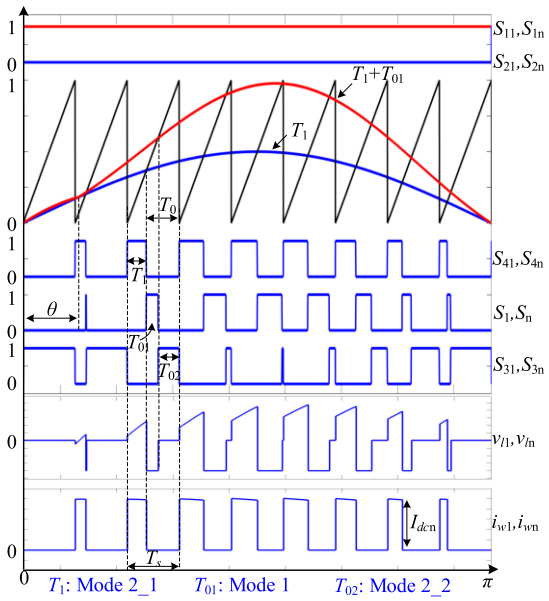

Fig. 5. Proposed modulation-positive half cycle of i_{wn}.

where $v_{\text{ln\_charging}}$ and $v_{\text{l\_discharging}}$ are inductor voltages under charging and discharging, respectively, V_s is the voltage drop on each switch, V_{ESR} is the voltage drop on the inductor equivalent series resistor (ESR), ω is the angular speed, m_a is the modulation index, V_c is output voltage, and θ is the phase displacement between v_{cn} and i_{wn} and is obtained based on the *LRC* circuit

$$\theta = \arctan\left(\frac{\omega RC_n/n}{1-\omega^2 LC_n/n}\right) - \arctan\left(\frac{\omega L}{R}\right). \quad (3)$$

The dwell time T_{02} is then obtained based on (1) and (2). And meeting the above two conditions simultaneously as well as ensuring a linear modulation generates the following:

$$T_1 + T_{01} \le T_s \quad (4)$$

from which the operation range of modulation index m_a for a given system can be defined. Note that overmodulation is not discussed in this work. The gain of the converter is obtained based on (1) and (2)

$$\frac{v_{\text{ln\_discharging}}}{-v_{\text{ln\_charging}}} = \frac{k(T_s - T_1)}{T_1}$$
$$\rightarrow \frac{\sqrt{2}V_c + 2nV_s + nV_{\text{ESR}}}{V_{\text{in}} - nV_s - nV_{\text{ESR}}} = \frac{k(1 - m_a \sin(\frac{\pi}{2}+\theta))}{m_a \sin(\frac{\pi}{2}+\theta)} \quad (5)$$

where k is defined as $k = T_{01}/T_0$ at the time instant of $\omega t = \pi/2 + \theta$ and ranges from 0 to 1.

For a lossless converter in which V_s and V_{ESR} are 0, the gain shown in (5) becomes

$$\frac{V_c}{V_{\text{in}}} = \frac{k(1 - m_a \sin(\frac{\pi}{2}+\theta))}{\sqrt{2} m_a \sin(\frac{\pi}{2}+\theta)}. \quad (6)$$

As shown in (6), for a given m_a, the minimum and maximum gains occur at $k = 0$ and $k = 1$, respectively. Then, on the basis of $k = 1$, m_a is ranging from 0 to 1; the range of m_a for a given gain and the range of gain for a given m_a are defined by the constraint shown in (4). For example, theoretically, the maximum gain is infinity at $m_a = 0$ and the minimum gain is zero. The proposed converter is essentially a buck−boost feature. The modulation m_a is obtained based on (6)

$$m_a = \frac{k}{\sin(\frac{\pi}{2}+\theta)\left(k + \frac{\sqrt{2}V_c}{V_{in}}\right)}. \quad (7)$$

TABLE II
COMPARISON BETWEEN DIFFERENT CONVERTERS

Items	VSCs with similar structures [1]		Existing SC-CSCs [15-20]	Proposed SC-CSC
	CHB	MMC		
Transformer	Yes	No	Yes	No
Short protection	No	No	Yes	Yes
Dv/dt performance	Good	Good	Superior	Superior
Unbalance issue	No	Yes	No	No
Inherent balance	Yes	No	Yes	Yes
Dynamic performance	High	High	Low	Low
Levels	>3	>3	3	3
Dc inductor count	0	0	n	n
Dc capacitor count	n	n	0	0
Output/input	Buck	Buck	Boost	Buck-boost

TABLE III
EXPERIMENT PARAMETERS

V_{in}	120 V	m_a	0.5	L_{dc}	20 mH
V_c	70 V	k	0.95	C_{n}	200 μF
I_{dc}	14 A	f_{sw} ($S_{1\text{n}}$, $S_{2\text{n}}$)	50 Hz	L	5 mH
I_l	5 A	f_{sw} ($S_{3\text{n}}$, $S_{4\text{n}}$, S_{n})	900 Hz	R	10 Ω
ESR	0.6 Ω	V_s	1 V	n	2

C. Comparison With Existing Similar Converters

As shown in Table II, compared with existing SC-CSCs, the proposed one does not need the bulky and costly transformer, is a buck−boost inverter, and has inherent current and voltage balancing. In addition, all the advantages of existing SC-CSCs, such as inherent short-circuit protection, no *dv/dt* issue, and modular structure, are inherited. The comparison between the proposed SC-CSC and its voltage source converter (VSC) counterparts, such as the CHB and MMC inverters, is the same as that between conventional CSCs and VSCs. For example, CSCs have low dynamic performance but feature inherent reliable short circuit protection and have no *dv/dt* issue with only three current levels at the output. The CHB and MMC inverters achieve a low *dv/dt* by generating more levels at the output through employing more modules. Note that the transformerless PV inverters are different from the proposed one in terms of favorable applications, power/voltage ratings, configurations, etc. For example, the dc-link voltage of the PV inverters is up to 1500 V, while the proposed one is with medium-/high-voltage levels.

D. Experimental Verification

A lab-scaled case study is conducted, and the used parameters are listed in Table III. Fig. 6 shows the gating signals over one fundamental cycle, and Figs. 7 and 8 show the experimental waveforms under steady and dynamic states, respectively. As shown in Fig. 6, the switches S_{1n} and S_{2n} are switching with a fundamental frequency, while switches S_{3n} and S_{4n} and S_{n} are switching alternatively with the modulating frequency as analyzed earlier. As shown in Fig. 7, when the inverter is operating

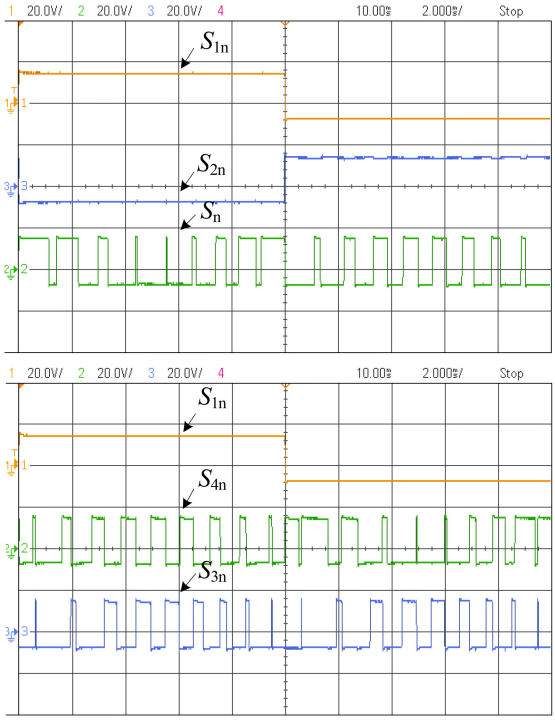

Fig. 6. Gating signals over a fundamental cycle.

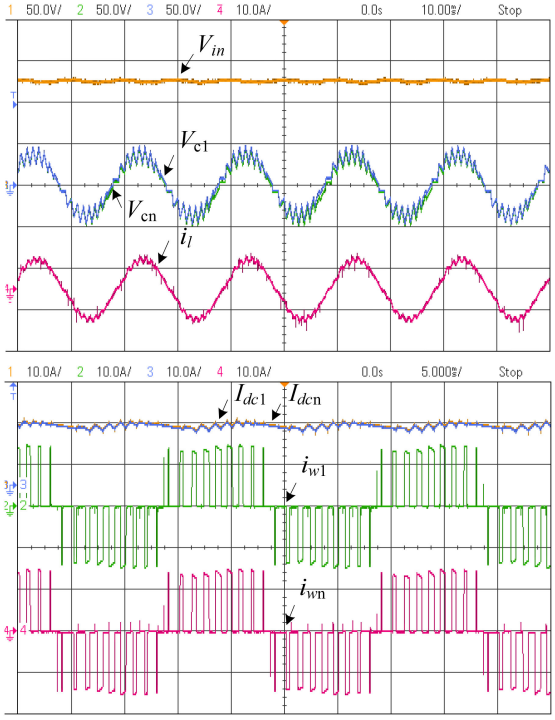

Fig. 7. Experimental waveforms under steady state.

under steady state ($V_{\rm in}$ = 120 V), the inductor currents $I_{\rm dc1}$ and $I_{{\rm dc}n}$ are balanced at around 14 A, and the output capacitor voltages V_{c1} and V_{cn} are also balanced at about 35 V. i_{w1} and i_{wn} are the output pulsewidth modulation currents of the two modules of the proposed SC-CSC, and i_l is the load current.

Fig. 8 shows the dynamic performance of the proposed inverter. As shown in Fig. 8, when the input voltage is increased

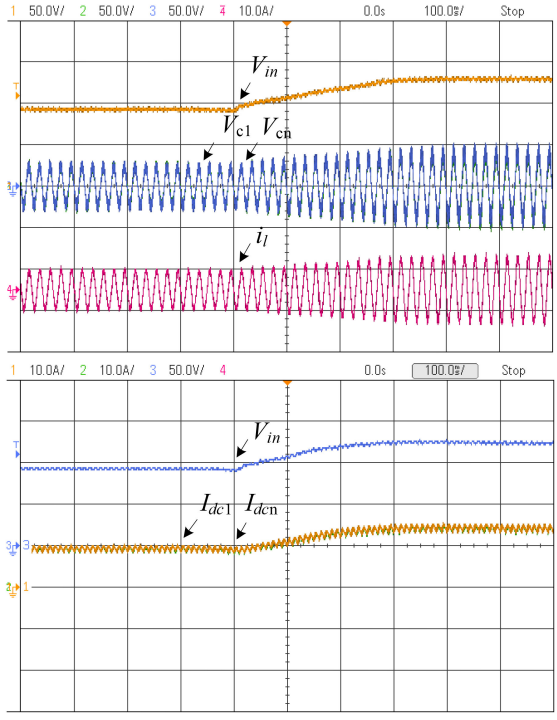

Fig. 8. Experimental waveforms under dynamic state.

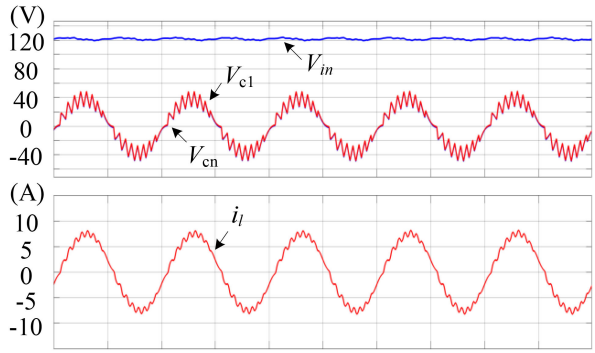

Fig. 9. Simulated results with experiment parameters.

from 90 to 120 V, the output capacitor voltages increase from 18 to 35 V, and the input dc inductor currents increase from 10 to 14 A. Both inductor currents and capacitor voltages are well balanced in the process. To sum up, the proposed inverter has inherent current and voltage balancing. Also, as shown in Fig. 7, the experimental gain considering voltage drops on the inductor ESR and switches is $V_c/V_{\rm in}$ = 0.59 which well agrees with the derivation as shown in (5). To further verify the derivation, simulation with same experimental parameters is conducted and shown in Fig. 9. As shown in Fig. 9, the simulated waveforms with experimental parameters are well matching the experimental waveforms shown in Fig. 7. This well proves the accuracy of the derivation. Experimental parameters are listed in Table III.

III. Conclusion

A transformerless SC-CSC is proposed, and a modulation scheme is developed. Compared with existing SC-CSCs, the

proposed one does not require the bulky and costly transformers, features inherent current and voltage balancing, and has a buck−boost input/output characteristic. Lab-scaled experiments have been conducted and the results verified the performance of the proposed converter as well as the proposed modulation.

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