Optimal Tracking and Resonance Damping Design of Cascaded Modular Model Predictive Control for a Common-Mode Stabilized Grid-Tied LCL Inverter

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***Abstract*—A cascaded modular model predictive control (MMPC) method is designed for a modified nonisolated LCL grid-connected inverters to provide resonance damping, improved dynamic performance, and leakage current attenuation capabilities. The continuous control set model predictive control strategy is applied for the proposed method. The active damping function of the inner loop MMPC is analyzed in detail to illustrate the mechanism of improving the system dynamic performance. The cascaded MMPC method is compared with the conventional proportional-integral (PI) control methods with/without a notch filter to show the merits in resonance damping and dynamic response. The optimal control parameters design procedure is elucidated with the tuning mechanism of the MMPC weighing factor and PI gain. With the proposed optimal MMPC design method, the dynamic performance of rising time and overshoot are improved compared to the conventional PI control methods with/without the notch filter. The simulation and experimental results verified the proposed control design method.**

***Index Terms*—Active damping, dynamic performance, LCL filter, modular model predictive control (MMPC), nonisolated grid-connected inverter, zero-sequence voltage control.**

I. Introduction

MODEL predictive control (MPC) is an advanced control technique that is gaining more attention with the increasing demand of better system dynamic performance in power electronics. Different from the conventional proportional-integral (PI) control, the MPC has a better transient performance in the aspects of rising-time, steady-state error, overshoot, and disturbance rejection. Especially in high-order-filtered power converter system, such as LCL-filtered converter, there exists an intrinsic resonance frequency that can cause oscillation or instability issues with a conventional PI controller [1]. The resonance cannot be naturally attenuated by PI control.

Passive/active damping resistors can be added in the physical/control loops to compensate for the resonance [2]. However, on one hand, a passive resistor in the main physical loop will introduce extra power losses [3]. On the other hand, the active damping method requires extra voltage/current sensors that brings more system cost [4], [5]. Besides the hardware solutions of passive/active damping methods with extra physical resistors/sensors, another option to attenuate the resonance is the notch filter from the software perspective [6]. The notch filter can be added at the resonant frequency of the LCL filter to compensate for the resonant spikes. However, the inserted notch filter will also reduce the control bandwidth and slow down the reference tracking. The notch filter is a desired solution to reduce the high-frequency electromagnetic interference noise [7]. But at the same time, the system dynamic performance might be deteriorated.

MPC is capable of increasing the control bandwidth to achieve a high reference tracking speed [8], [9]. Based on this characteristic of MPC, the resonant frequency of an LCL-filtered converter can be shifted to a higher range by down sizing the filter values and increasing the switching frequency [10], [11]. With the advantageous dynamic performance of MPC, the volume and weight of the LCL filter can be reduced. Thus, the system cost will be saved. Another intrinsic function of MPC is active damping for the LCL resonance, which has not been studied in detail [12]. The MPC can be functioned as an active damping control block that compensates the system resonance especially in a cascaded PI+MPC control architecture. Thus, the stability of the system can be improved which makes it possible to enlarge the proportional gain and increase the control bandwidth without exciting oscillation [13].

This article designs a cascaded modular model predictive control (MMPC) architecture for a modified nonisolated LCL-filtered grid-connected inverter. The proposed method is configured as continuous control set model predictive control (CCS-MPC) for the implementation. The designed MMPC includes an upper level grid-side inductor current PI control and lower level per phase switch-side inductor, output capacitor (LC) filter MPC. The inner loop MPC can be functioned as an active damping term to attenuate the resonance and improve the system stability. Thus, the control bandwidth can be increased by enlarging the outer loop gain without exciting oscillations. Also, since only the switch-side LC parameters are leveraged for the MPC state-space model and the grid-side inductor current is controlled by the PI, the uncertainty of grid-side inductance will not influence the control performance. This article is organized as follows. First, the modified nonisolated LCL-filtered inverter

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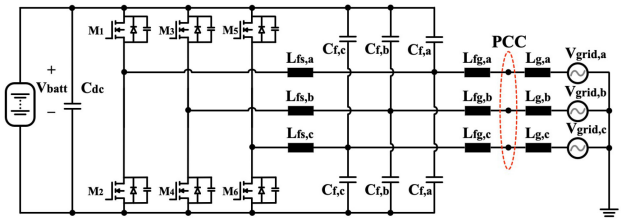


Fig. 1. Nonisolated LCL inverter with a low leakage current.

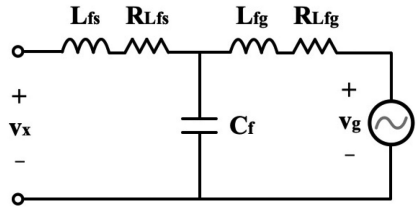


Fig. 2. Equivalent LCL circuit with consideration of the ESR.

is introduced with the system modeling in abc and $dq0$ reference frames. The modified topology is capable of bypassing the leakage current from flowing into the grid. Second, three control structures are designed for the modified nonisolated converter with zero-sequence stabilization capabilities to attenuate the leakage current that include PI control, PI control+notch filter, and PI control cascaded with MMPC. Third, three control architectures are compared and analyzed with transfer functions to study the resonance rejection capabilities. The cascaded MMPC method attenuates most of the resonance and achieves the highest control bandwidth with the help of intrinsic active damping capability. An optimal control design method is developed for the cascaded MMPC to achieve a better dynamic performance. Finally, the active damping analysis and proposed control design method are validated experimentally.

II. LCL System Modeling

The LCL system modeling is based on a modified nonisolated three-phase dc/ac converter, which has been shown in Fig. 1. Several methods have been proposed to improve the common-mode performance of the traditional dc/ac converters. Hintz *et al.* [14] connected the grid neutral to the three-phase output capacitors common point for the compensation of unbalanced three-phase power system. Ayano *et al.* [15] inserted a grounding capacitor between the three-phase output capacitors common point and the ground to create a zero-sequence bypassing path to reduce the leakage current. Chee *et al.* [16] introduced a fourth leg to be connected between the common point of three-phase output capacitors and dc bus neutral to attenuate the common-mode voltage. Guo *et al.* [17] directly connected the fourth leg to the three-phase output capacitors common point with an extra LC circuit to stabilize the common-mode voltage. Most of the them cost extra switches to attenuate the common-mode voltage. Different from the traditional two-level three-phase dc/ac converter, the common point of three-phase capacitors is connected to the dc bus positive/negative terminals to create a bypassing path for zero-sequence capacitor voltage and zero-sequence switch-side inductor current control. By leveraging the topological modification and zero-sequence control methods, the common-mode voltage can be stabilized to reduce the leakage current. From the perspective of system dynamic performance, the state-space equations and transfer functions of the LCL plant model are derived for optimal design.

A. DC/AC LCL Plant Modeling

For a precise modeling of the LCL-filtered converter system, the equivalent series resistors (ESR) of the switch-side and grid-side inductors are both taken into considerations [18], [19]. For per phase switch-side inductor current, i_{Lfs}, capacitor voltage, v_{Cf}, grid-side inductor current, i_{Lfg}, grid voltage, v_g, and phase leg output voltage, v_x, the equivalent LCL circuit with ESR has been shown in Fig. 2. The corresponding state-space equations can be expressed as

$$L_{fs}\frac{di_{Lfs}}{dt} = -v_{Cf} - R_{Lfs}i_{Lfs} + v_x \tag{1a}$$

$$C_f\frac{dv_{Cf}}{dt} = i_{Lfs} - i_{Lfg} \tag{1b}$$

$$L_{fg}\frac{di_{Lfg}}{dt} = v_{Cf} - R_{Lfg}i_{Lfg} - v_g \tag{1c}$$

where L_{fs}, C_f and L_{fg} are the switch-side inductor, output capacitor, and grid-side inductor, respectively. R_{Lfs} and R_{Lfg} are the ESR of the switch-side inductor and grid-side inductor, respectively.

To further derive the standardized format for transfer function, the state-space equations can be expressed as matrix format [20]

$$\frac{d\boldsymbol{X}}{dt} = \mathbf{A}\boldsymbol{X} + \mathbf{B_c}v_x + \mathbf{B_g}v_g \tag{2a}$$

$$i_{Lfs} = \mathbf{C_c}\boldsymbol{X} \tag{2b}$$

$$i_{Lfg} = \mathbf{C_g}\boldsymbol{X} \tag{2c}$$

where X is the state variable matrix and can be illustrated as

$$\boldsymbol{X} = \begin{bmatrix} i_{Lfs} \\ v_{Cf} \\ i_{Lfg} \end{bmatrix}. \tag{3}$$

$\mathbf{A}$, $\mathbf{B_c}$, $\mathbf{B_g}$, $\mathbf{C_c}$, and $\mathbf{C_g}$ are the system matrices and can be expressed as

$$\mathbf{A} = \begin{bmatrix} \frac{-R_{Lfs}}{L_{fs}} & \frac{-1}{L_{fs}} & 0 \\ \frac{1}{C_f} & 1 & \frac{-1}{C_f} \\ 0 & \frac{1}{L_{fg}} & \frac{-R_{Lfg}}{L_{fg}} \end{bmatrix} \tag{4a}$$

$$\mathbf{B_c} = \begin{bmatrix} \frac{1}{Lfs} \\ 0 \\ 0 \end{bmatrix}, \quad \mathbf{B_g} = \begin{bmatrix} 0 \\ 0 \\ \frac{-1}{Lfs} \end{bmatrix} \tag{4b}$$

$$\mathbf{C_c} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}, \quad \mathbf{C_g} = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}. \tag{4c}$$

Based on the state-space matrix equations, the transfer functions can be derived accordingly to illustrate the LCL plant model. Specifically, the transfer function from phase leg output voltage, v_x, to switch-side inductor current, i_{Lfs}, can be

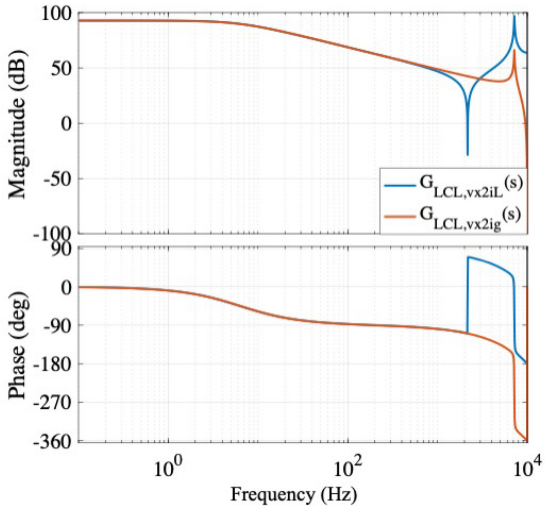


Fig. 3. LCL plant model transfer function bode plots with consideration of the ESR.

expressed as

$$G_{LCL,vx2iL}(s) = \frac{i_{Lfs}(s)}{v_x(s)} = \mathbf{C_c}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B_c} \tag{5}$$

where $\mathbf{I}$ is the 3×3 identity matrix. The transfer function from phase leg output voltage, v_x, to grid-side inductor current, i_{Lfg}, can be expressed as

$$G_{LCL,vx2ig}(s) = \frac{i_{Lfg}(s)}{v_x(s)} = \mathbf{C_g}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{B_c}. \tag{6}$$

For the illustration of the resonance issue in the LCL filter system to control the grid current and consider the ESR, (6) can be expanded as

$$G_{LCL,vx2iLfg}(s) = \frac{i_{Lfg}(s)}{v_x(s)} = \frac{V_{dc}}{(sL_{fs} + R_{Lfs})(sL_{fg} + R_{Lfg})sC_f + (L_{fs} + L_{fg})s + (R_{Lfs} + R_{Lfg})}. \tag{7}$$

In the plant model transfer function, the quadratic term coefficient of the denominator is multiplied by the ESR of switch- and grid-side inductors, R_{Lfs} and R_{Lfg}. These two ESR values are ranged at a level of milliohms, which are not enough to damp the resonance because of a too small portion of the quadratic term coefficient [21]. The bode plots of (5) and (6) have been shown in Fig. 3. In the resonant frequency of

$$\omega_{\text{res}} = \sqrt{\frac{L_{fs} + L_{fg}}{L_{fs}L_{fg}C_f}} \tag{8}$$

there exists a convex magnitude spike that could cause system stability issue.

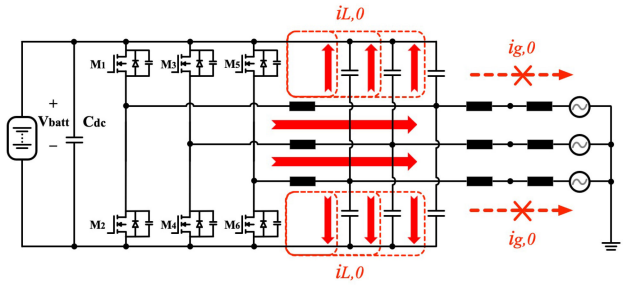


Fig. 4. Leakage current bypassing paths with the modified nonisolated topology.

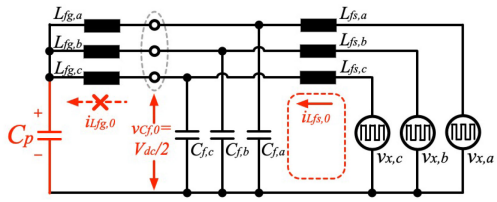


Fig. 5. Equivalent common-mode circuit of the modified nonisolated topology.

B. Zero-Sequence Modeling

In a traditional transformerless three-phase grid-connected inverter, a leakage current path could be excited by the high-frequency fluctuation of the common-mode voltage [22], [23]. In a $dq0$ reference frame system, the common-mode voltage is represented as the zero-sequence component. Thus, a high-frequency oscillation of the zero-sequence voltage can cause a high leakage current in the parasitic paths [24]. The value of leakage current, i_{lkg}, is mainly determined by the parasitic capacitance, C_{para}, and the change rate of the zero-sequence voltage, $v_{Cf,0}$, [5]

$$i_{\text{lkg}} = C_{\text{para}}\frac{dv_{Cf,0}}{dt} \tag{9}$$

where $v_{Cf,0}$ is the mean value of three-phase output capacitor voltages, $v_{Cf,a}, v_{Cf,b}$, and $v_{Cf,c}$. In a conventional LCL-filtered grid-tied inverter, the zero-sequence voltage always fluctuates in high frequency

$$v_{Cf,0} = \frac{v_{Cf,a} + v_{Cf,b} + v_{Cf,c}}{3}. \tag{10}$$

However, with the modified nonisolated converter topology in Fig. 1, the zero-sequence voltage can be stabilized as half of the dc bus voltage, $V_{\text{dc}}/2$. And the connections of three-phase output capacitors common points to the positive/negative dc bus terminals enables the grid-side leakage current to be bypassed and attenuated as is shown in Fig. 4. With the improved topology, the zero-sequence current only flows through the switch-side inductors and output capacitors instead of further injecting into the grid. The corresponding equivalent common-mode circuit of the modified non-isolated topology has been shown in Fig. 5. Leveraging the zero-sequence voltage/current control methods, the leakage current can be limited within the standard requirements of less than 30 mA in an electric vehicle system by the IEC 62955:2018 and IET Wiring Regulation 18th Edition (BS 7671:2018) Section 722.531.2.101 [25].

III. Control Structures Analysis

The control strategies of the modified LCL-filtered inverter are analyzed in this section. Different from the conventional control methods of grid-connected inverters [26], the zero-sequence components of output capacitor voltage and switch-side inductor current are stabilized with specific controllers. To analyze the dynamic performances and resonance behaviors of different control strategies in the LCL filter system, four control structures are studied including PI control, PI control with notch filter, cascaded PI, and cascaded MMPC methods.

A. PI Control

The PI method of the control diagram is shown in Fig. 6(a). The grid current is transformed from abc to $dq0$ reference frame based on Park and Clarke transformations. Then, the d, q, and 0 sequences of the grid current are controlled by PI in the dc frame for a better dynamic tracking performance. d, q, and 0 are corresponding to active power, reactive power, and common-mode components, respectively. The output of the grid current controller will be transformed from $dq0$ back to the abc reference frame for duty cycle of pulsewidth modulation (PWM). With the zero-sequence controller to minimize the zero-sequence grid current with a tracking reference of 0 A, the common-mode leakage current on the grid side can be attenuated to a low level.

The transfer functions of $dq0$ grid current controllers can be expressed as

$$G_{iLfgd,\mathrm{PI}}(s) = K_{p,iLfgd} + \frac{K_{i,iLfgd}}{s} \tag{11a}$$

$$G_{iLfgq,\mathrm{PI}}(s) = K_{p,iLfgq} + \frac{K_{i,iLfgq}}{s} \tag{11b}$$

$$G_{iLfg0,\mathrm{PI}}(s) = K_{p,iLfg0} + \frac{K_{i,iLfg0}}{s}. \tag{11c}$$

With the PI control strategy, the resonance of the LCL filter in Fig. 3 still exists at the resonant frequency point.

B. PI Control With the Notch Filter

To attenuate the resonance of the LCL system, a notch filter can be added after the output of grid current controllers as is shown in Fig. 6(b). The principle of the notch filter is to flatten the spike within a certain range centered at the resonant frequency point. The notch filter can be designed in continuous time as

$$G_{\mathrm{Notch}}(s) = \frac{s^2 + \omega_{\mathrm{res}}^2}{s^2 + \frac{\omega_{\mathrm{res}}}{Q}s + \omega_{\mathrm{res}}^2} \tag{12}$$

and implemented in discrete time as difference equations. The variable Q represents the quality factor and is configured to adjust the frequency range of the notch filter.

With the help of the notch filter, the resonance of the peak spike from the LCL system can be attenuated. However, on one hand, another concave spike may be excited because of the notch filter. On the other hand, the added notch filter reduces the control bandwidth and slows down the dynamic performance.

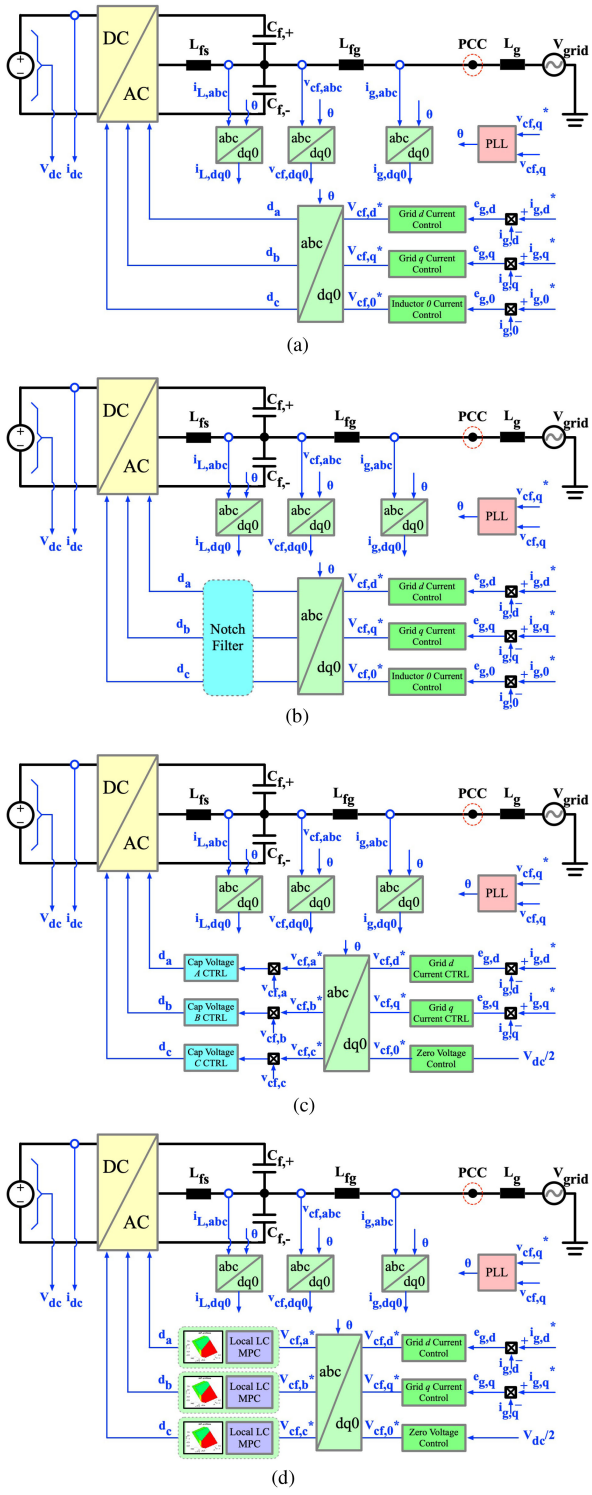


Fig. 6. Control diagrams of the (a) PI, (b) notch-filtered PI, (c) cascaded PI, and (d) active-damping MPC for the transformerless LCL inverter.

C. Cascaded PI Control

To make a comprehensive comparison of resonance damping and dynamic performance before introducing the proposed cascaded MMPC method, the cascaded PI control is analyzed as is shown in Fig. 6(c). The cascaded PI control diagram for the LCL-filtered inverter includes the outer loop of grid-side

inductor current control and inner loop capacitor voltage control. The references for the inner loop capacitor voltage control are derived from the output of the outer loop grid-side inductor current control.

The transfer functions of the capacitor voltage controller can be expressed as

$$G_{vCf,\mathrm{PI}}(s) = K_{p,vCf} + \frac{K_{i,vCf}}{s}. \tag{13}$$

The output of the capacitor voltage controller will be transformed to the duty cycle for PWM.

D. Cascaded MMPC

To increase the control speed and solve the concave spike of the PI+notch filter method and attenuate the resonance spike issue of the PI control method, a cascaded MMPC method is developed in this section. The control diagram of the cascaded MMPC is shown in Fig. 6(d). It includes the following two cascaded control layers: the outer loop of grid-side inductor current PI control in the $dq0$ reference frame; and the inner loop of per phase switch-side LC filter inductor current/capacitor voltage MPC in the abc reference frame and zero-sequence output capacitor voltage MPC. The reasons for implementing the grid-side inductor current PI control in $dq0$ and per phase switch-side LC current/voltage MPC in abc reference frames, respectively, can be concluded in the following two aspects: the MPC has better tracking performance and transient behavior on time-varying ac reference signals than PI; and the outer loop grid-side d and q current are corresponding to the active and reactive power, respectively. Thus, instead of configuring ac references for the grid-side abc phase current, dq grid current references can be directly linked to the active/reactive power control when grid services are required.

1) Outer Loop Grid Current PI Control: For the outer loop control, the grid-side inductor current is first transformed from abc to dq reference frame with Clarke and Park transformations. Then, two PI controllers are configured to regulate the dq sequence of grid currents, $i_{Lfg,d}$ and $i_{Lfg,q}$, respectively. The d and q components of grid current references, $i^*_{Lfg,d}$ and $i^*_{Lfg,d}$, represent the active and reactive power, respectively. Then, the outputs of the grid current controller are configured as the references for dq sequence output capacitor voltages, $v^*_{Cf,d}$ and $v^*_{Cf,q}$, which will be transformed to the abc reference frame and configured as the references of inner loop per phase LC capacitor voltage MPC.

2) Zero-Sequence Capacitor Voltage MPC: For the stabilization of the common-mode voltage to bypass the grid-side leakage current, the zero-sequence component of output capacitor voltages is independently controlled through MPC as half of the dc bus voltage. Thus, half of the dc bus voltage measurement, V_{dc}, is configured as the reference of per phase zero sequence voltage MPC. With the zero-sequence voltage MPC, the grid-side leakage current can be attenuated to be lower than the standard requirement.

3) Inner Loop Per Phase LC MPC: An explicit MPC method is designed for the switch-side capacitor voltage and inductor current control. As is shown in Fig. 6(d) of the control diagram, the three-phase capacitor voltages are controlled in the abc frame to follow the references from the cascaded grid current controller's outputs. The switch-side inductor currents are also regulated with the MPC by adjusting the weighing factor between $i_{Lfs,abc}$ and $u_{Cf,abc}$. The benefits to configure the MPC per phase in the abc frame can be concluded as follows:

1) the state-space matrix of the *LC* per phase is simpler than the dq system to implement the offline piecewise affine optimization code in a less costly DSP controller;
2) the time-varying angular speed term, ω, can be omitted in the explicit MPC state-space matrix for the offline optimization calculation;
3) per phase MPC for *LC* is more flexible for a modular design perspective to extend the paralleled phase number and other topologies, e.g., dc/dc, single-phase dc/ac converters.

For the MPC implementation, in every control period, the MPC controller receives the measured switch-side inductor current, $i_{Lfs,abc}$, output capacitor voltage, $v_{Cf,abc}$, grid-side inductor current, $i_{Lfg,abc}$, from analog-to-digital converter (ADC), and output capacitor voltage references, $v^*_{Cf,abc}$, from the outer loop grid-side inductor current PI controller. An offline generated piecewise affine search tree is applied to derive the optimal duty cycle for the explicit MPC. The state equations of the switch-side *LC* filter can be expressed as

$$i_{Lfs}(k+1) = i_{Lfs}(k) - \frac{T_s}{L_{fs}} v_{Cf}(k) + \frac{V_{\mathrm{dc}} T_s}{L_{fs}} d(k) \tag{14a}$$

$$v_{Cf}(k+1) = \frac{T_s}{C_f} i_{Lfs}(k) + v_{Cf}(k) - \frac{T_s}{C_f} i_{Lfg}(k). \tag{14b}$$

For the flexibility of implementing the explicit MPC and the convenience of experimentally adjusting the dc bus voltage during test, the last term of (14), $V_{\mathrm{dc}}d(k)$, can be replaced by the phase leg output voltage, $v_x(k)$. The state-space model can be expressed in a standard matrix format of

$$X_{k+1} = AX_k + Bu_k + Ee_k \tag{15}$$

where the variables and matrices represent

$$A = \begin{bmatrix} 1 - \frac{R_{Lfs}}{L_{fs}} & -\frac{T_s}{L_{fs}} \\ \frac{T_s}{C_f} & 1 \end{bmatrix}, B = \begin{bmatrix} \frac{T_s}{L_{fs}} \\ 0 \end{bmatrix}, E = \begin{bmatrix} 0 \\ -\frac{T_s}{C_f} \end{bmatrix} \tag{16a}$$

$$X_k = \begin{bmatrix} i_{Lfs}(k) \\ v_{Cf}(k) \end{bmatrix}, u_k = \begin{bmatrix} V_{\mathrm{dc}} d(k) \end{bmatrix}, e_k = \begin{bmatrix} i_{Lfg}(k) \end{bmatrix}. \tag{16b}$$

In the MPC formulation, the inductor current/capacitor voltage references can be defined as $\bar{X}$ and the tracking errors between the measurement and the references are expressed as $\tilde{X}$, which are composed of

$$\bar{X}_k = \begin{bmatrix} i_{Lfs,\mathrm{ref}}(k) \\ v_{Cf,\mathrm{ref}}(k) \end{bmatrix}, \tilde{X}_k = \begin{bmatrix} i_{Lfs,\mathrm{ref}}(k) - i_{Lfs}(k) \\ v_{Cf,\mathrm{ref}}(k) - v_{Cf}(k) \end{bmatrix}. \tag{17}$$

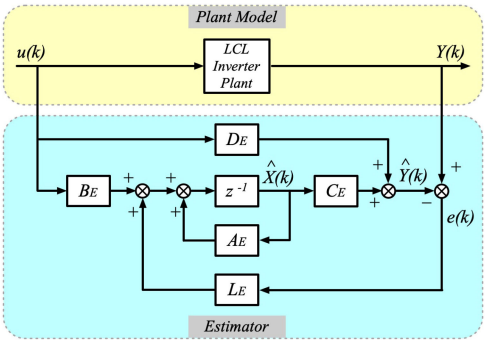


Fig. 7. Diagram of the state estimator.

Thus, the cost function includes two terms

$$\min \sum_{k=0}^{N_c} \tilde{X}_k^T Q \tilde{X}_k + \sum_{k=0}^{N_p-1} \triangle u_k^T R \triangle u_k. \tag{18}$$

For the penalties of the cost function, Q and R represent the weighing factor matrices that are implemented on the state values and input values, respectively.

The constraints of the MPC controller can be expressed as

$$\tilde{X}_{k+1} = A\tilde{X}_k + Bu_k + Ee_k \in \mathcal{X} \tag{19}$$

$$\triangle u_k = u_k - u_{k-1} \in \mathcal{U} \tag{20}$$

$$\begin{bmatrix} -I_{Lfs,\max} \\ 0 \end{bmatrix} \leq X_k \leq \begin{bmatrix} I_{Lfs,\max} \\ V_{\text{dc}} \end{bmatrix} \tag{21}$$

$$\begin{bmatrix} 0 \end{bmatrix} \leq u_k \leq \begin{bmatrix} V_{\text{dc}} \end{bmatrix} \tag{22}$$

$$\begin{bmatrix} -I_{Lfg,\max} \end{bmatrix} \leq e_k \leq \begin{bmatrix} I_{Lfg,\max} \end{bmatrix}. \tag{23}$$

For the implementation of the MPC algorithm in every control period [27], the cost function in (18) will be solved to predict the future steps of optimal input variable, u_k. And the first step of the input value will be implemented as the MPC output for the PWM modulation. Different from the PI control process, the MPC algorithm derives the optimal duty cycle by processing the state variable, X_k, and tracking error, $\tilde{X}_k$, in a linear way with specific coefficients. Since no integration procedure is needed in MPC, the dynamic performance of MPC is better than PI with less overshoot and higher tracking speed. Also, the inner loop MPC has higher control bandwidth, which can be functioned as an active damping term to solve the LCL resonance. Due to the active damping and high bandwidth of the inner loop MPC, the outer loop PI gains can be largely increased to speed up the dynamic reference tracking performance without causing extra resonance issue.

For the cascaded model predictive control of the LCL filter system, a state estimator is designed in Fig. 7 to reduce the sensor count. One of the three variables, i_{Lfs}, v_{Cf}, i_{Lfg}, can be estimated by the other two. The merits of the estimator include the antinoise capability for better control performance and the reduction of sensor cost.

Specifically, the Luenberger observer is designed to estimate the switch-side inductor current, $\hat{i}_{Lfs}$, capacitor voltage, $\hat{v}_{Cf}$, and grid-side inductor current, $\hat{i}_{Lfg}$, with the samplings of capacitor voltage, v_{Cf}, and grid-side inductor current, i_{Lfg}. The state-space equations for the discrete-time state estimator can be expressed in a standard matrix format of

$$\hat{X}_{k+1} = A_E \hat{X}_k + B_E u_k + L_E(Y_k - \hat{Y}_k) \tag{24a}$$

$$\hat{Y}_{k+1} = C_E \hat{X}_k + D_E u_k \tag{24b}$$

where the variables and matrices for the Luenberger observer represent

$$A_E = \begin{bmatrix} 0 & -\frac{1}{L_{fs}} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} \\ 0 & 0 & 0 \end{bmatrix}, B_E = \begin{bmatrix} \frac{1}{L_{fs}} \\ 0 \\ 0 \end{bmatrix} \tag{25a}$$

$$C_E = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}, D_E = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{25b}$$

$$\hat{X}_k = \begin{bmatrix} \hat{i}_{Lfs}(k) \\ \hat{v}_{Cf}(k) \\ \hat{i}_{Lfg}(k) \end{bmatrix}, \hat{Y}_k = \begin{bmatrix} \hat{v}_{Cf}(k) \\ \hat{i}_{Lfg}(k) \end{bmatrix}. \tag{25c}$$

L_E is a 3×2 observer gain matrix that can be tuned to achieve minimal estimation errors. The diagram of the state estimator is shown in Fig. 7. The state observer minimizes the estimation error, $e(k)$, with a dynamic equation of

$$e_{k+1} = (A_E - L_E C_E) e_k. \tag{26}$$

The estimation gain can be derived by

$$L_E^T = RM^{-1} \tag{27}$$

where R is composed of tuning factors and M is determined by solving the Sylvester equation

$$A_E^T M - M\Lambda = C_E^T R \tag{28}$$

in which Λ is a matrix with the desired eigenvalues.

IV. Optimal Control Design for Resonance Damping and Dynamic Performance

The optimal control design for resonance damping and dynamic performance of the LCL-filtered grid-connected inverter is analyzed in this section. Four control strategies in Fig. 6 are compared with transfer functions, bode plots, step responses, and root locus to illustrate the active damping and dynamic performance improvement capabilities of the cascaded MMPC method [28].

A. Control Plant Model Analysis

The LCL filter and the integrated control plant models are derived in Fig. 8 and Fig. 9, respectively. The former stages are the four types of control blocks with the input variable of grid-side inductor current and output variable of duty cycle. The latter stage is the LCL filter plant model that has been derived in Fig. 8. Thus, the complete transfer functions can be expressed based on different control strategies.

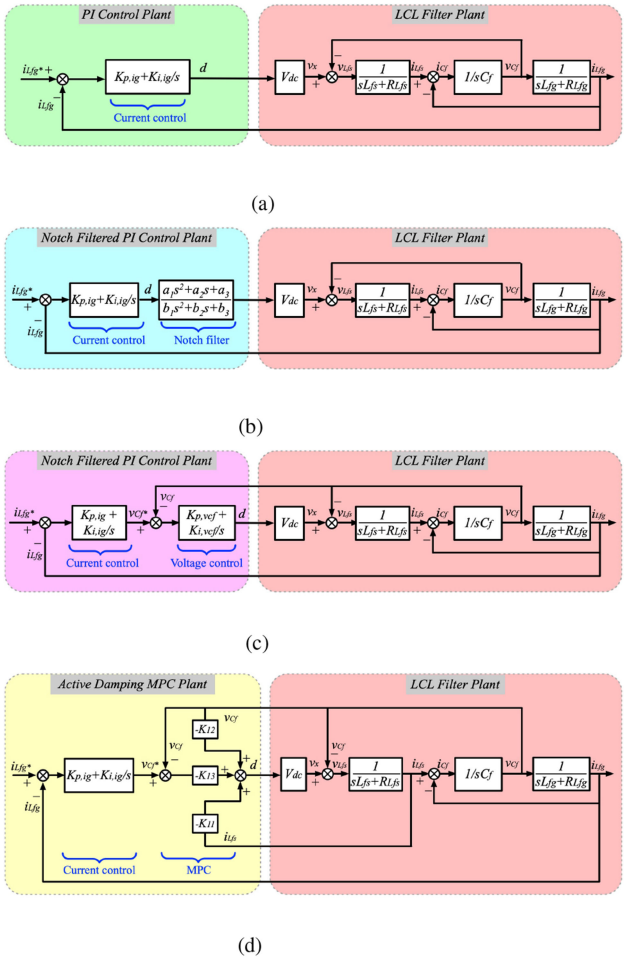


Fig. 8. Plant models of the (a) PI, (b) notch-filtered PI, (c) cascaded PI, and (d) active-damping MPC for the transformerless LCL inverter.

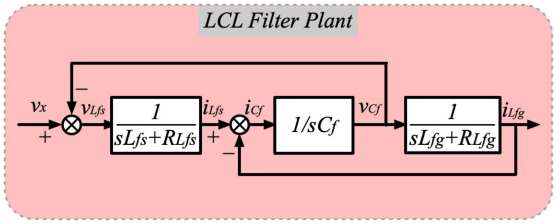


Fig. 9. LCL plant model with consideration of the ESR.

1) PI Control Transfer Function: For the first control strategy of the PI method in Fig. 6(a), the corresponding system plant model has been shown in Fig. 8(a). Based on the derivations in (7) and (11), the transfer function from tracking error, $i_{Lfg,\text{err}}$, to the measurement, i_{Lfg}, of grid-side inductor current can be expressed as

$$G_{iLfg\text{err}2iLfg,\text{PI}}(s) = G_{iLfg,\text{PI}}(s) \cdot G_{LCL,vx2iLfg}(s). \quad (29)$$

2) Notch-Filtered PI Control Transfer Function: For the second control strategy of adding a notch filter after the PI controller to attenuate the resonance spike in Fig. 6(b), the corresponding system plant model has been shown in Fig. 8(b). Based on the derivation of notch filter design in (12), the transfer function from tracking error, $i_{Lfg,\text{err}}$, to the measurement, i_{Lfg}, of the grid-side inductor current can be expressed as

$$G_{iLfg\text{err}2iLfg,\text{NotchPI}}(s) = G_{iLfg,\text{PI}}(s) \cdot G_{\text{Notch}}(s) \cdot G_{LCL,vx2iLfg}(s). \quad (30)$$

3) Cascaded PI Control Transfer Function: For the third control strategy of the cascaded PI controller in Fig. 6(c), the corresponding system plant model has been shown in Fig. 8(c). Based on the derivations in (7) and (13), the transfer function from the tracking error of the output capacitor voltage, $v_{Cf,\text{err}}$, to the measurement of the grid-side inductor current, i_{Lfg}, can be derived as

$$G_{vCf\text{err}2iLfg,\text{CascadedPI}}(s) = G_{vCf,\text{PI}}(s) \cdot G_{LCL,vx2iLfg}(s). \quad (31)$$

Then, the transfer function from the reference of output capacitor voltage, $v_{Cf,\text{ref}}$, to the measurement of the grid-side inductor current, i_{Lfg}, can be expressed as

$$G_{vCf\text{ref}2iLfg,\text{CascadedPI}}(s) = \frac{G_{vCf\text{err}2iLfg,\text{CascadedPI}}(s)}{1 + G_{vCf\text{err}2iLfg,\text{CascadedPI}}(s)}. \quad (32)$$

Furthermore, adding the outer loop grid-side inductor current PI control, the transfer function from the tracking error, $i_{Lfg,\text{err}}$, to the measurement, i_{Lfg}, of the grid-side inductor current can be expressed as

$$G_{iLfg\text{err}2iLfg,\text{CascadedPI}}(s) = G_{vCf\text{ref}2iLfg,\text{CascadedPI}}(s) \cdot G_{vCf\text{ref}2iLfg,\text{CascadedPI}}(s). \quad (33)$$

Then, the transfer function from the reference, $i_{Lfg,\text{ref}}$, to the measurement, i_{Lfg}, of the grid-side inductor current can be derived as

$$G_{iLfg\text{ref}2iLfg,\text{CascadedPI}}(s) = \frac{G_{iLfg\text{err}2iLfg,\text{CascadedPI}}(s)}{1 + G_{iLfg\text{err}2iLfg,\text{CascadedPI}}(s)}. \quad (34)$$

And, based on (34) and the LCL plant model in Fig. 9, the transfer function from the reference of the switch-side inductor current, $i_{Lfg,\text{ref}}$, to the measurement of the output capacitor voltage, v_{Cf}, can be derived as

$$G_{iLfg\text{ref}2vCf,\text{CascadedPI}}(s) = G_{iLfg\text{ref}2iLfg,\text{CascadedPI}}(s) \cdot (sL_{fg} + R_{Lfg}). \quad (35)$$

4) Cascaded MMPC Transfer Function: For the fourth control strategy of cascaded MMPC in Fig. 6(d), the corresponding system plant model has been shown in Fig. 8(d). The inner loop per phase switch-side LC MMPC is cascaded with the outer loop of grid-side inductor current control. A linear-quadratic regulator (LQR) can be applied to derive the transfer function for the MPC algorithm part in the control plant model of Fig. 8(d) to solve the cost function of (18).

A typical LQR control diagram integrated with a dynamic system is shown in Fig. 10, where x, y, u, and r represent the

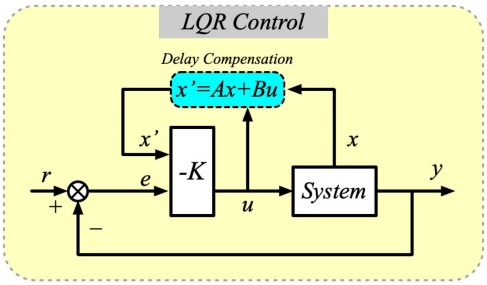


Fig. 10. Typical LQR control diagram with delay compensation.

state variable, $[i_{Lfs}; v_{Cf}]$, output variable, i_{Lfs}, input variable of duty cycle, d, and tracking reference, $i_{Lfs,\text{ref}}$, respectively. The middle block of Fig. 10 is the core algorithm of MPC to calculate the optimal duty cycle, which is a linear coefficient matrix, -**K**. And the MPC equation to calculate the optimal duty cycle based on the tracking error and state variable can be expressed as

$$d = -\mathbf{K}\begin{bmatrix} i_{Lfs} \\ v_{Cf} \\ v_{Cf,\text{err}} \end{bmatrix} = -[K_{11}, K_{12}, K_{13}]\begin{bmatrix} i_{Lfs} \\ v_{Cf} \\ v_{Cf,\text{err}} \end{bmatrix} \tag{36}$$

where $v_{Cf,\text{err}}$ is the tracking error of the MPC calculated as $v_{Cf,\text{ref}} - v_{Cf}$.

Thus, the inner loop of MPC can be expressed in the transfer function as Fig. 8(d). The transfer function from tracking error, $v_{Cf,\text{err}}$, to the measurement, v_{Cf}, of output capacitor voltage can be expressed as

$$\begin{aligned} &G_{vCf\text{err}2vCf,\text{MPC}}(s) \\ &= \frac{-K_{13}G_{LCL,vx2ig}(s)(sL_{fg}+R_{Lfg})(sL_{fs}+R_{Lfs})/V_{\text{dc}}}{\begin{array}{c}\{(sL_{fs}+R_{Lfs})+K_{11}[V_{\text{dc}}-G_{LCL,vx2ig}(s) \\ \times(sL_{fg}+R_{Lfg})]/V_{\text{dc}}+K_{12}G_{LCL,vx2ig}(s) \\ \times(sL_{fs}+R_{Lfs})(sL_{fg}+R_{Lfg})/V_{\text{dc}} \\ -K_{13}G_{LCL,vx2ig}(s)(sL_{fs}+R_{Lfs}) \\ \times(sL_{fg}+R_{Lfg})/V_{\text{dc}}\}\end{array}}. \end{aligned} \tag{37}$$

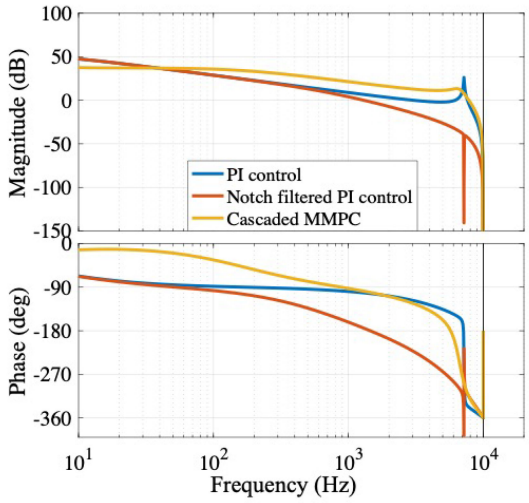
Furthermore, the transfer function from the reference, $v_{Cf,\text{ref}}$, to the measurement, v_{Cf}, of output capacitor voltage can be expressed as

$$\begin{aligned} &G_{vCf\text{ref}2vCf,\text{MPC}}(s) \\ &= G_{vCf\text{err}2vCf,\text{MPC}}(s)/[1+G_{vCf\text{err}2vCf,\text{MPC}}(s)]. \end{aligned} \tag{38}$$

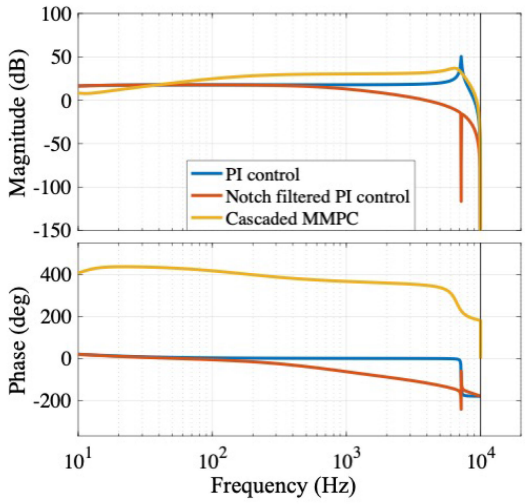
Based on (38) and the LCL plant model in Fig. 9, the transfer function from the reference of output capacitor voltage, $v_{Cf,\text{ref}}$, to the measurement of grid-side inductor current, i_{Lfg}, can be derived as

$$\begin{aligned} &G_{vCf\text{ref}2iLfg,\text{MPC}}(s) \\ &= G_{vCf\text{ref}2vCf,\text{MPC}}(s)/(sL_{fg}+R_{Lfg}). \end{aligned} \tag{39}$$

Then, taking the outer loop grid-side inductor current PI control into consideration, the cascaded MMPC transfer function from tracking error, $i_{Lfg,\text{err}}$, to the measurement, i_{Lfg}, of grid-side inductor current can be expressed as



(a)



(b)

Fig. 11. Comparison of bode plots for three control strategies (a) from $i_{Lfg,\text{err}}$ to i_{Lfg} and (b) from $i_{Lfg,\text{err}}$ to v_{Cf}.

$$\begin{aligned} &G_{iLfg\text{err}2iLfg,\text{MPC}}(s) \\ &= G_{vCf\text{ref}2iLfg,\text{MPC}}(s)\cdot G_{iLfg,\text{PI}}(s). \end{aligned} \tag{40}$$

The cascaded MMPC transfer function from tracking error of the grid-side inductor, $i_{Lfg,\text{err}}$, to the measurement of the output capacitor voltage, v_{Cf}, can be expressed as

$$\begin{aligned} &G_{iLfg\text{err}2vCf,\text{MPC}}(s) \\ &= G_{vCf\text{ref}2vCf,\text{MPC}}(s)\cdot G_{iLfg,\text{PI}}(s). \end{aligned} \tag{41}$$

B. Mechanism of Inner Loop MMPC for Active Damping

The resonance behavior and dynamic performance of the four control strategies for LCL-filtered grid-connected inverter are analyzed based on the derived transfer functions. Figs. 11(a), 12(a) and 11(b), 12(b) show the bode plots comparison of transfer functions from the tracking error to the measurement of grid-side inductor current and from the tracking error of grid-side

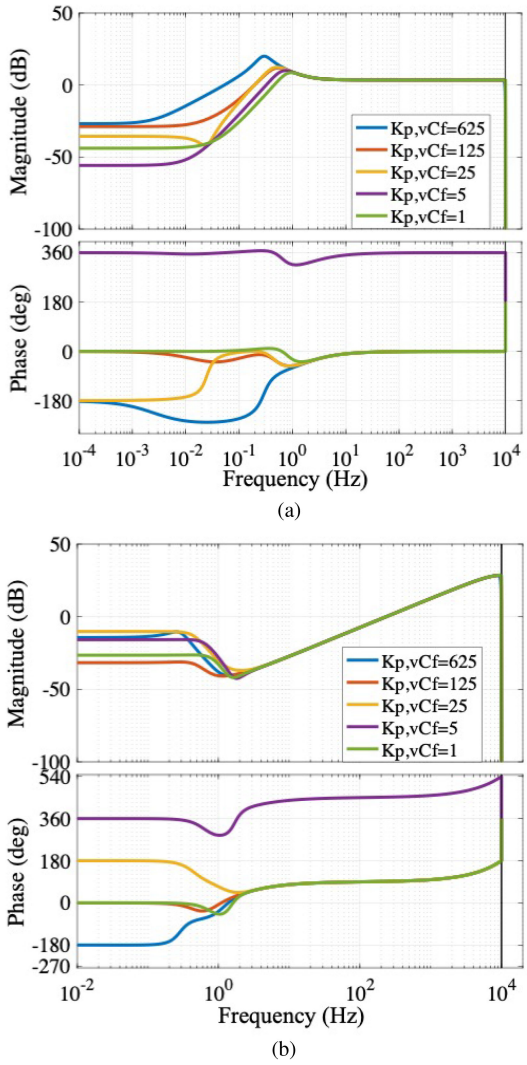


Fig. 12. Bode plots for cascaded PI control from (a) $i_{Lfg,\text{err}}$ to i_{Lfg} and (b) $i_{Lfg,\text{err}}$ to v_{Cf} with the inner loop $K_{p,vCf}$ gain swept from 1 to 625.

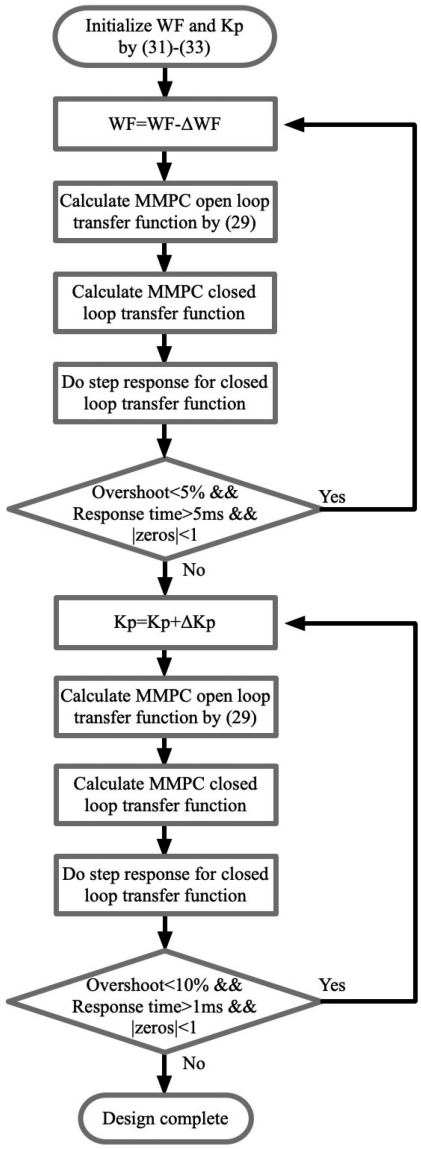


Fig. 13. Cascaded MMPC parameter design flow chart.

inductor current to the measurement of output capacitor voltage, respectively. The magnitude plots manifest that the PI control in Fig. 8(a) has a convex spike at the resonant frequency point. The notch-filtered PI control in Fig. 8(b) has a concave spike at the resonant frequency point. The cascaded PI control in Fig. 8(c) has a narrow bandwidth at high frequency range. The cascaded MMPC in Fig. 8(d) attenuates the spike at the resonant frequency point and the control bandwidth is wider than the conventional PI, notch-filtered PI, and cascaded PI methods.

Thus, the inner loop MPC of the cascaded MMPC is functioned as an active damping term to mitigate the resonance in the LCL system. This active damping term contributes to the improvement of stability and control bandwidth. Furthermore, the fast response and active damping characteristics of the inner loop MPC permits a wider control bandwidth for the outer loop PI control. Instead of concerning about the instability of resonance in the PI control method of Fig. 8(a), the gains of the outer loop grid-side inductor PI controller can be largely increased to improve the dynamic performance. So, by carefully designing the outer loop PI control gain, K_p, and the inner loop MPC weighing factor of the cascaded MMPC, $WF = Q/R$, the LCL system dynamic performance can be further improved.

C. Cascaded Control Design for Dynamic Performance

The control design of the proposed cascaded MMPC is analyzed in this section. Two key parameters of outer loop PI control gain, K_p, and the inner loop MPC weighing factor, WF, need to be designed. The bode plots of open loop transfer functions, closed loop step responses, and zero-pole maps are evaluated for the design procedure.

The optimal cascaded control design flowchart is shown in Fig. 13, which includes inner loop MPC weighing factor, WF, design and outer loop grid-side inductor current PI gain, K_p, design. Since the inner loop MPC can attenuate the resonance spike by functioning as an active damping term, the outer loop

PI gain is permitted with a larger tuning range without losing stability. The control parameter design starts from the inner loop.

First, the design parameters should be initialized based on the bandwidths of inner and outer loop controllers. Typically, the PI control bandwidth, $\mathrm{BW_{PI}}$, is configured to be 5–10 times slower than the inner loop MPC bandwidth, $\mathrm{BW_{MPC}}$ [29]

$$5\mathrm{BW_{PI}} \leq \mathrm{BW_{MPC}} \leq 10\mathrm{BW_{PI}}. \tag{42}$$

And the PI control cutoff frequency, ω_c, should be set below 30% of the LCL resonant frequency, ω_{res}

$$\omega_c \leq 30\%\omega_{\mathrm{res}}. \tag{43}$$

The initial values for the optimal PI gains design flow chart can follow the following equations [12]:

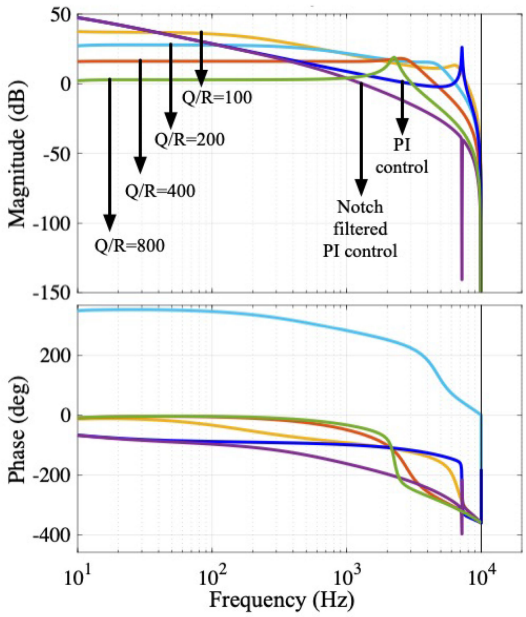
$$K_{p,iLfg} = \frac{(L_{fs} + L_{fg})f_{\mathrm{sw}}}{3} \tag{44a}$$

$$\tau_{i,iLfg} = \frac{L_{fs} + L_{fg}}{R_{fs} + R_{fg}} \tag{44b}$$

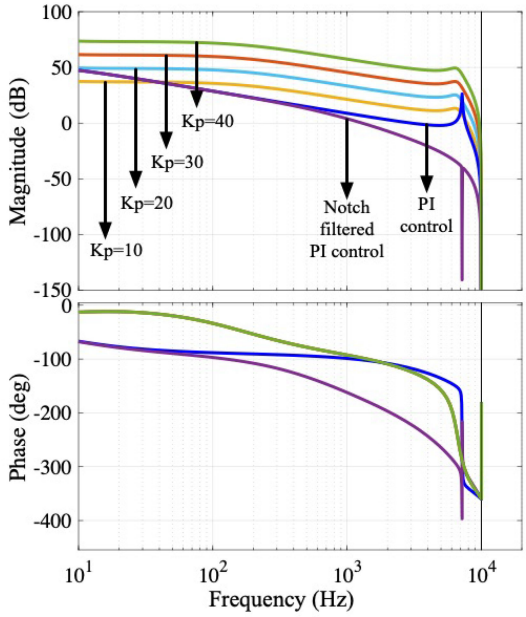
where f_{sw} and $\tau_{i,iLfg}$ are the switching frequency and integral time constant, respectively. The initial value for weighing factor can start from a typical range of 800–1000.

Second, based on the initial WF and K_p, the inner loop weighing factor is swept from 100 to 800. During the sweeping period, the bode plots of open loop transfer functions from $i_{Lfg,\mathrm{err}}$ to i_{Lfg} are derived in Fig. 14(a). Also, the step responses and zero-pole map of closed loop transfer functions from $i_{Lfg,\mathrm{err}}$ to i_{Lfg} are derived in Figs. 15(a) and 16(a), respectively. With the reduction of the weighing factor, the control bandwidth is increased in Fig. 14(a). And the response time is decreased with more overshoot in the transient period as is shown in Fig. 15(a). The sweeping check conditions of the inner loop MPC weighing factor are the overshoot percentage, response time, and poles magnitude. Since the outer loop K_p gain is kept in low level and has not been tuned yet, the overshoot is not a big issue in the sweeping process of the inner loop weighing factor. And the response time is largely determined by the outer loop K_p gain and has not been shortened yet in the inner loop sweeping process. Thus, for the sweeping procedure of the weighing factor, the overshoot check condition threshold can be configured smaller than the outer loop sweeping process. And the response time check condition threshold can be configured larger than the outer loop sweeping process. If the overshoot is larger than 5%, response time is smaller than 5 ms or poles are outside of the unit circle, the weighing factor sweeping is stopped to entering the outer loop PI gain sweeping procedure.

Third, the outer loop PI gain is swept from 10 to 40. During the sweeping period, the bode plots of open-loop transfer functions from $i_{Lfg,\mathrm{err}}$ to i_{Lfg} are also derived in Fig. 14(b). Also, the step responses and zero-pole map of closed loop transfer functions from $i_{Lfg,\mathrm{err}}$ to i_{Lfg} are derived in Figs. 15(b) and 16(b), respectively. With the increment of gain, the control bandwidth is increased in Fig. 14(b). And the response time is decreased with more overshoot in the transient period as is shown in Fig. 15(b). Same sweeping check items of the outer loop PI gain are configured as the overshoot percentage, response time, and poles magnitude with different thresholds. Compared with the inner loop weighing factor sweeping, the outer loop gain sweeping procedure addresses more on the tracking speed and less on overshoot issue, since the inner loop MPC has been proved to guarantee an active damping function for the whole LCL system stability to attenuate the resonance. If the overshoot is larger than 10%, response time is smaller than 1 ms or poles are outside of the unit circle, the weighing factor sweeping is stopped to finalize the outer loop PI gain sweeping procedure.



(a)



(b)

Fig. 14. Bode plots of the PI control, notch-filtered PI control, and cascaded MMPC methods transfer functions from $i_{Lfg,\mathrm{err}}$ to i_{Lfg} with the cascaded MMPC. (a) Weighing factor Q/R swept from 100 to 800 at the K_p gain of 10. (b) K_p gain swept from 10 to 40 at the Q/R of 400.

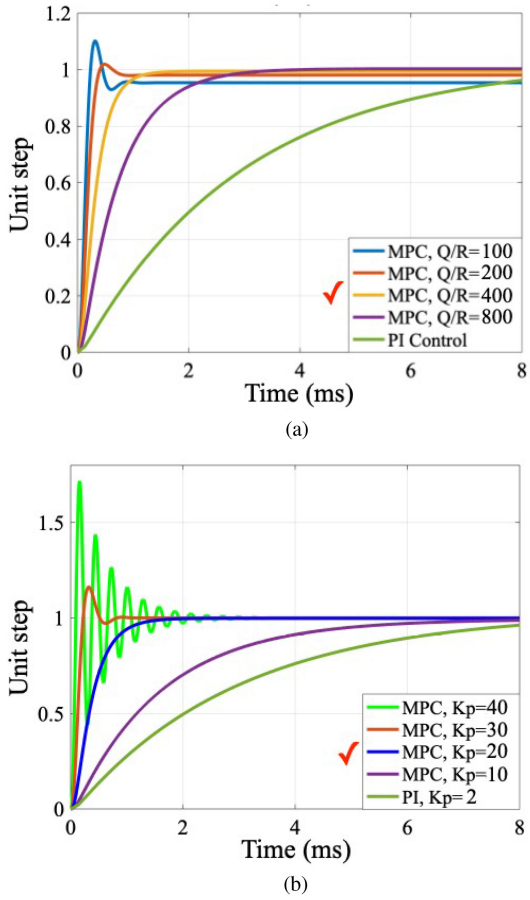


Fig. 15. Step responses of the cascaded MMPC close-loop transfer function from $i_{Lfg,\text{err}}$ to i_{Lfg} with (a) weighing factor Q/R swept from 100 to 800 and (b) K_p gain swept from 10 to 40.

TABLE I
SYSTEM PARAMETER CONFIGURATIONS

Parameter	Value
Grid voltage, $V_{grid,L-N}$	110V-120V
DC voltage, V_{dc}	400V-450V
Switching frequency	80kHz
Switch side inductor, L_{fs}	45μH
Grid side inductor, L_{fg}	450μH
Output Capacitor, C_f	12μF
MOSFET	C3M0021120K
Controller	LAUNCHXL-F28379D
Leakage current	$\leq$ 15mA

V. RESULTS

The proposed optimal control design method for resonance damping and dynamic performance improvement is validated experimentally on the modified nonisolated three-phase converter with a grid simulator. The testing parameters are 400–450V_{dc} to 110–120V_{L-N} with switching frequency of 80 kHz. The LCL filter parameters are 45 μH for L_{fs}, 12 μF for C_f, and 450 μH for L_{fg}. C3M0021120 K SiC from Cree and TMS320F28379D from TI are applied for switches and controller, respectively. The corresponding parameters have been shown in Table I.

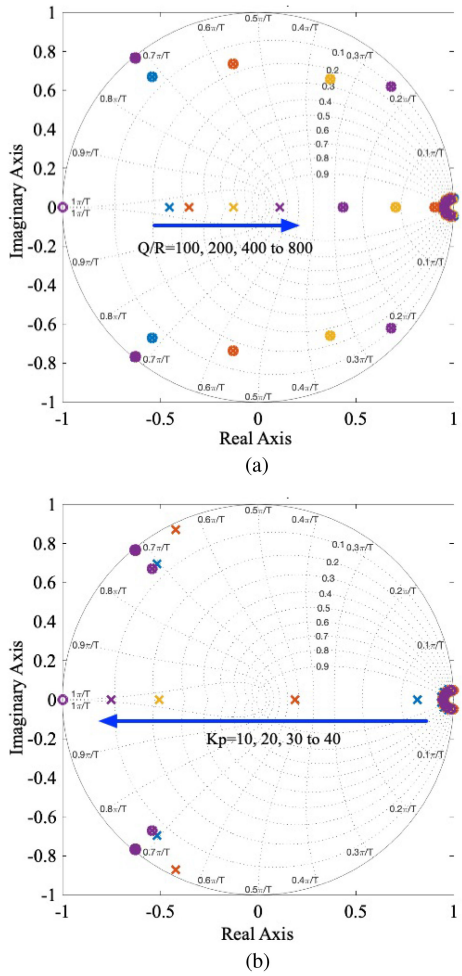


Fig. 16. Zeros and poles plots of the cascaded MMPC from $i_{Lfg,\text{err}}$ to i_{Lfg} with (a) weighing factor Q/R swept from 100 to 800 and (b) K_p gain swept from 10 to 40.

A. State Estimation Test

The state estimator combined with the MPC has been tested experimentally for the reduction of sensor count. Fig. 17(a)–(c) shows the captured ADC readings of estimation and measurement for switch-side inductor current, output capacitor voltage, and grid-side inductor current, respectively. The switch-side inductor current can be accurately estimated for the MPC purpose based on the measurement of output capacitor voltage and grid-side inductor current.

B. Steady-State Common-Mode Test

The steady-state performance of the cascaded MMPC is tested experimentally to show the stabilized zero-sequence grid voltage and reduced leakage current. Fig. 18 shows the switch-side inductor current, output capacitor voltage, grid-side inductor current, and dc bus voltage in steady state. The leakage current and zero-sequence grid voltage performances are shown in Fig. 19 with a 450-V dc bus. It can be seen from the bottom waveform that the zero-sequence grid voltage has been stabilized to be constant at half of the dc bus, 225 V. And the leakage current has been attenuated to be less than 15 mA. Thus, the developed

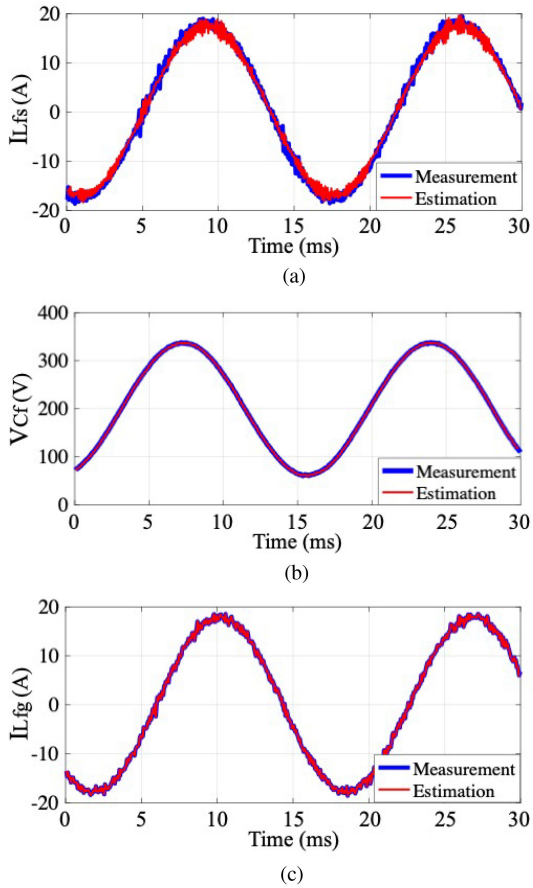


Fig. 17. Comparison of the experimentally captured estimation and measurement of (a) switch-side inductor current, (b) output capacitor voltage, and (c) grid-side inductor current.

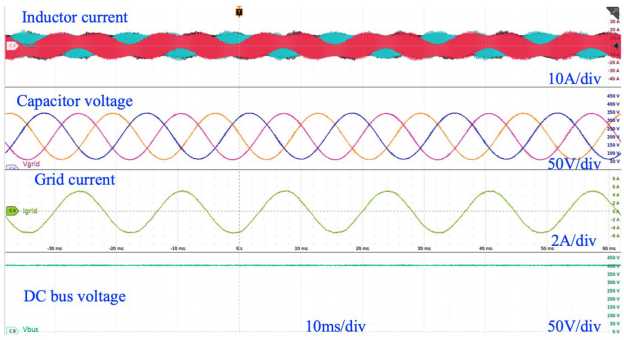


Fig. 18. Steady-state waveforms of switch-side inductor current, output capacitor voltage, grid-side inductor current, and dc bus voltage.

zero-sequence voltage MPC method is capable of reducing the leakage current in the modified nonisolated LCL inverter. The standard requirements of the leakage current in IEC and IET are also satisfied.

C. Dynamic and Stability Performance Test

The dynamic performance of the developed optimal control design method for cascaded MMPC is validated with step transient testing. Fig. 20 shows the transient waveforms of switch-side inductor current, output capacitor voltage, grid-side

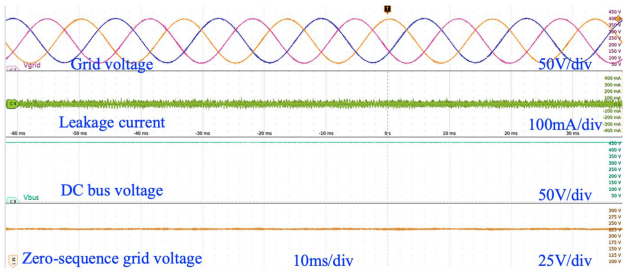


Fig. 19. Steady-state waveforms of three-phase grid voltage, leakage current, dc bus voltage, and zero-sequence grid voltage.

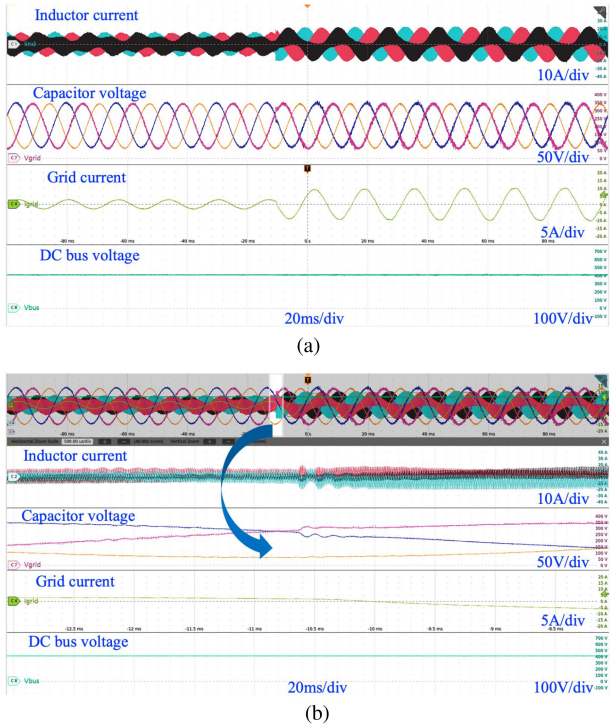


Fig. 20. (a) Transient and (b) zoomed transient waveforms of switch-side inductor current, output capacitor voltage, grid-side inductor current, and dc bus voltage with $i_{Lfg,q}$ from 3 to 10 A.

inductor current, and dc bus voltage with a current step of 7 A. The transient performance of control methods are evaluated by capturing the experimental ADC readings with current steps. Fig. 21(a) and (b) shows the $i_{Lfg,q}$ steps from 2 to 8 A and 8 to 2 A with different outer loop grid-side inductor current control gains of 10, 20, 30, and 40, respectively. Thus, the optimal gain is selected as 20 based on the control parameter design flow chart. For the dynamic performance comparison of PI control, notch-filtered PI control, cascaded MMPC, and cascaded PI methods, Figs. 22 and 23 show the $i_{Lfg,q}$ steps and zoomed waveforms from 2 to 8 A and 8 to 2 A under the following five testing cases: PI control with K_p gain of 20; notch-filtered PI control with K_p gain of 20; PI control with K_p gain of 2; MMPC with K_p gain of 20; and cascaded PI control with K_p gain of 2. It can be seen that the MMPC behaves more stable than either PI control or notch-filtered PI control at high K_p gain of 20 with less overshoot and oscillation. Even though the PI and cascaded PI methods can act stably with a smaller K_p gain of 2, the response time is much longer than MMPC. For a more intuitional

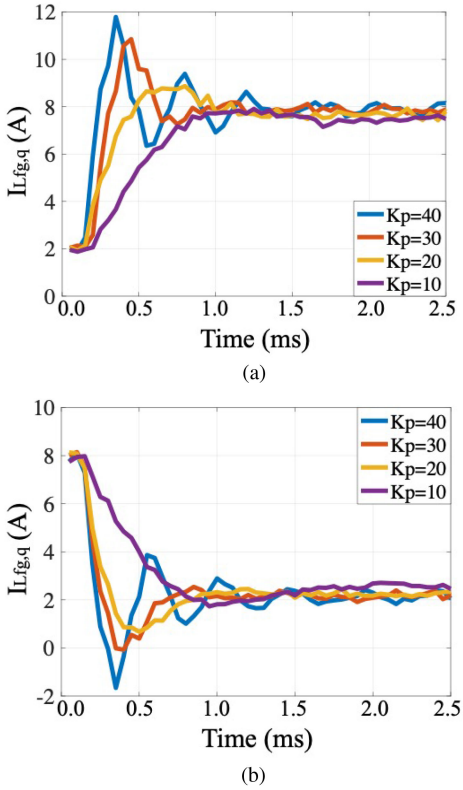


Fig. 21. Cascaded MMPC transient captured ADC readings of grid-side inductor current q component (a) from 2 A to 8 A and (b) from 8 A to 2 A with K_p gain of 10, 20, 30, and 40. (a) MMPC transient of $i_{Lfg,q}$ from 2A to 8A. (b) MMPC transient of $i_{Lfg,q}$ from 8A to 2A.

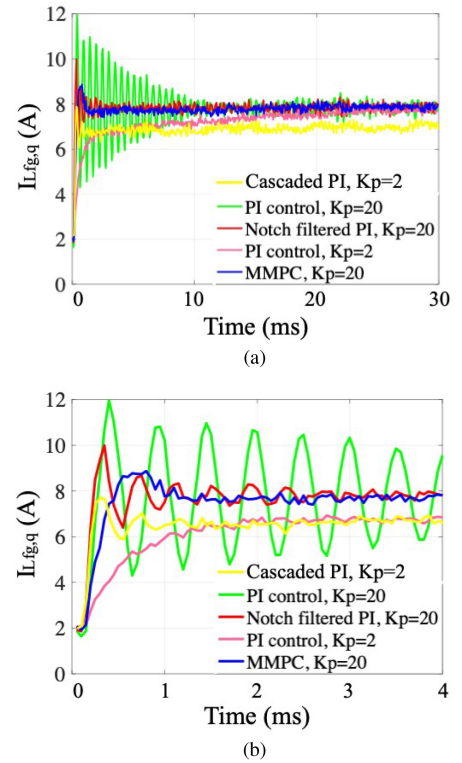


Fig. 22. Comparison of PI, notch-filtered PI, and MMPC transient captured ADC readings of (a) grid-side inductor current q component from 2 to 8 A and (b) zoomed waveforms.(a) Transient comparison of PI and MMPC. (b) Zoomed transient comparison of PI and MMPC.

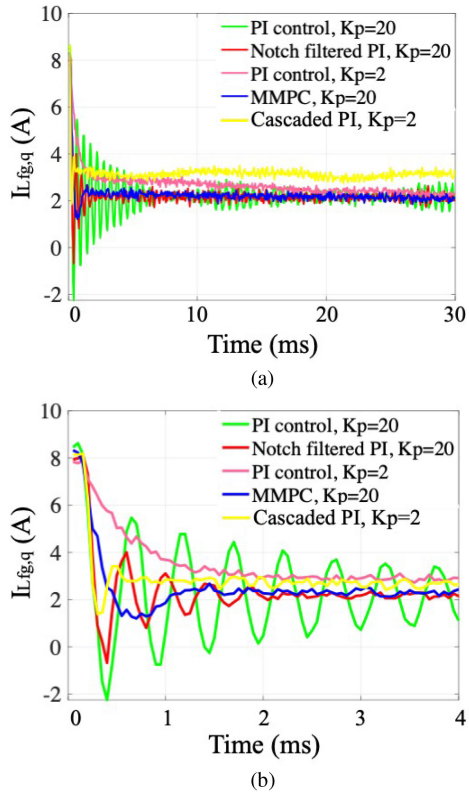


Fig. 23. Comparison of PI and MMPC transient captured ADC readings of (a) grid-side inductor current q component from 8 to 2 A and (b) zoomed waveforms. (a) Transient comparison of PI and MMPC. (b) Zoomed transient comparison of PI and MMPC.

TABLE II
CONTROL PARAMETERS OF DIFFERENT METHODS

	Q/R	K_p
PI	n/a	2, 20
Notch filtered PI	n/a	20
MMPC	400	10, 20, 30, 40

comparison, the inductor current, output capacitor voltage, grid current, and dc bus voltage waveforms of these five testing cases are shown in Fig. 24(a)–(e), respectively. The PI control has more oscillation than the MMPC method at the same high K_p gain condition of 20. Even with the notch filter, a high K_p gain of 20 could also oscillate the waveforms with slightly less ripple than pure PI. The cascaded PI has more oscillation than PI at a low K_p of 2. The cascaded PI will diverge faster than the PI method at higher K_p gain. The MMPC can operate at a K_p of 20 without oscillation and shorten the response time without the need of reducing the K_p gain as pure PI method. Thus, the experimental comparison of PI, notch-filtered PI, MMPC, and cascaded PI verifies that the optimal control design method for cascaded MMPC improves the dynamic performance with a shorter response time, less overshoot, and less oscillation. Based on the theoretical analysis in this article, the improvements of MMPC is resulted from the inner loop MPC, which has the function of active damping and attenuation of resonance in the LCL-filtered grid-connected inverter. The corresponding control parameters for the experiments have been summarized in Table II.

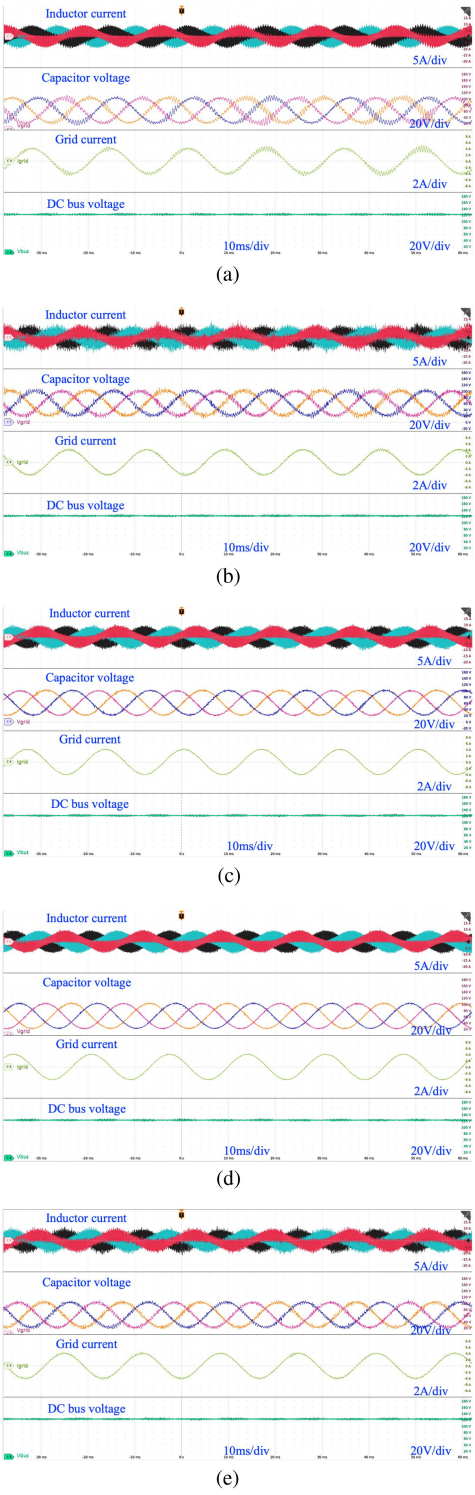


Fig. 24. Waveforms comparison of inductor current, output capacitor voltage, grid current and dc bus voltage for (a) PI control with K_p of 20, (b) notch-filtered PI control with K_p of 20, (c) PI control with K_p of 2, (d) MMPC with K_p of 20, and (e) cascaded PI control with K_p of 2.

D. Comparison With the State of the Art

The proposed active damping MMPC is compared with the state of art for the grid-connected LCL inverter MPC methods in this section. Chen *et al.* [30] proposed an observations-based FCS-MPC method with grid-side inductor current sensors for balanced and unbalanced grid voltage conditions. Falkowski and Sikorski [31] proposed two implementations of FCS-MPC methods to eliminate the low-order grid current harmonics and decrease the sensitivity to grid voltage distortion. The authors in [32] and [33] proposed also FCS-MPC methods to deal with the dynamic performance of the grid-connected LCL inverter in the $\alpha\beta$ reference frame. The advantages of the proposed MMPC can be concluded in the following three aspects:

1) The computation burden is low to be implemented explicitly on a low cost DSP instead of the expensive FPGA for the aforementioned references. The proposed MMPC is implemented in per phase switch-side LC of the abc reference frame instead of dq or $\alpha\beta$. Thus, the variable of the grid angular speed is not required in the state-space matrix and the order of the per phase LC state-space matrix is lower. The execution time for MMPC is within 4 μs at each control interrupt.
2) The proposed MMPC is combined with the modified inverter topology to stabilized the zero-sequence voltage and attenuate the leakage current. This function enables the non-isolated converter applications to satisfy the grid-connection standard requirements for common-mode behavior.
3) The size of offline generated piecewise affine function C code file is small to be fit into the DSP controller. Since the MMPC is implemented for per phase LC in theabc reference frame, the explicit solver function is largely simplified and the C file is within 5 kB. This size could be easily fit into the DSP memory.

VI. Conclusion

This article develops an optimal control design method for resonance damping and dynamic performance improvement of cascaded MMPC for a modified grid-connected LCL inverter. The LCL system is modeled to show the intrinsic resonance issue. Also, the common-mode circuit is analyzed for the modified nonisolated grid-connected inverter to manifest the leakage current bypassing and zero-sequence voltage stabilization functions. Three control strategies, including PI control, notch-filtered PI control, and cascaded MMPC, are studied with zero-sequence stabilization capabilities to explore the dynamic and stability performance. The cascaded MMPC is validated to have the active damping function by inserting an inner loop MPC cascaded with outer loop PI control. This cascaded control structure is capable of damping the resonance and increasing the control bandwidth to improve the system dynamic performance. A control parameter design method is finally proposed for the cascaded MMPC to derive the optimal weighing factor and gain. The experiments have validated the proposed method.

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