Integrated Maximum Power Point Tracking System for Photovoltaic Energy Harvesting Applications

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***Abstract*—The integrated circuits employed for power management in photovoltaic (PV) energy harvesting applications are required to perform an efficient maximum power point tracking (MPPT) process for maximizing the power production of the PV source during the continuously changing atmospheric conditions. Among the alternative MPPT methods, the perturbation and observation (P&O) technique has the advantages of operational and implementation simplicity. In this article, a novel PV MPPT control system for on-chip implementation of the P&O MPPT method is presented, which, compared to the past-proposed on-chip MPPT systems, has the advantage that it is implemented based on purely digital CMOS circuits without requiring the use of complex circuits, such as multipliers, sample and hold units, or analog-to-digital converters. Therefore, it can be easily implemented on-chip with low design complexity while simultaneously retaining the high-performance features of the P&O MPPT technique. The proposed PV MPPT system has been fabricated using the XFAB XH018 0.18-μm CMOS technology. The experimental results verify the successful operation of the on-chip PV MPPT control unit and its ability to achieve a high MPPT efficiency over a wide range of operating solar irradiation values.**

***Index Terms*—DC/DC converter, energy harvesting, integrated circuit (IC), maximum power point tracking (MPPT), photovoltaic (PV).**

I. Introduction

A SIGNIFICANT technological evolution of energy harvesting systems based on solar, thermal, and piezoelectric generators has been achieved during the decade. Their target is to cover the energy requirements of consumer-level smart devices in applications, such as Internet-of-Things [1], wireless sensor networks [2], and wearable computing [3]. These developments have also shaped the present form of application-specific integrated circuits (ASICs), which act as dedicated peripheral circuits for managing the aforementioned sources of power generation. Such ASICs may also include integrated sensors, switching converters, and passive elements (e.g., capacitors, inductors, etc.) fabricated on the same silicon substrate.

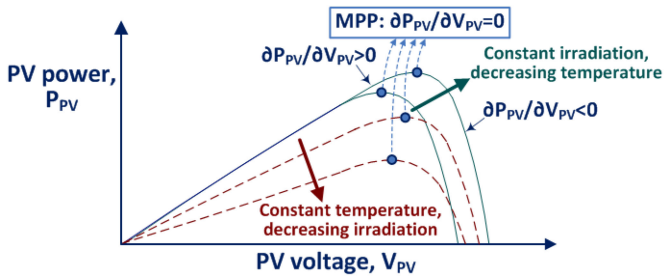

Fig. 1. Power–voltage curves of a PV power generator.

The research of energy harvesting systems that are targeted to cover such market needs has produced a plethora of implementations. The most traditional route includes implementations that are based solely on photovoltaic (PV) sources. Some of them focus on the PV string/panel level, but single solar cell integrations have also been studied since they are more suitable for low-power and small-footprint implementations. The power–voltage curves of a PV generator under different incident solar irradiation and ambient temperature conditions are illustrated in Fig. 1 [4]. It is observed that the position of the PV generator operating point where the produced power is maximized (i.e., maximum power point, MPP) depends on the solar irradiance and ambient temperature atmospheric conditions. In energy harvesting applications, a dc/dc converter is connected to the output of the PV source and it is controlled according to an appropriate MPP tracking (MPPT) process in order to ensure that the PV source always operates at the respective MPP during the continuously changing meteorological conditions of the PV system installation site. Such a power management system for PV energy harvesting applications is typically required to feature low power consumption, high accuracy of tracking the MPP (i.e., MPPT efficiency), as well as low complexity and implementation cost.

Various on-chip implementations of MPPT systems have been proposed till present. The ripple correlation control MPPT technique has been implemented on-chip in [5] and [6]. This MPPT method is based on purely analog circuits and depends on the use of a high switching frequency in order to reduce the

Manuscript received January 25, 2022; accepted February 24, 2022. Date of publication March 7, 2022; date of current version April 28, 2022. This work was supported in part by the European Regional Development Fund of the European Union and in part by the Greek National Funds through the Operational Program Competitiveness, Entrepreneurship and Innovation, under the call RESEARCH–CREATE–INNOVATE under Project T1EDK-01485. Recommended for publication by Associate Editor Y. Li. *(Corresponding authors: Eftichios Koutroulis.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3156400.

Digital Object Identifier 10.1109/TPEL.2022.3156400

size and cost of the passive components required for its implementation. The on-chip implementations of the perturbation and observation (P&O, also called "Hill-Climbing") MPPT algorithm presented in [7]–[9] aim to maximize the output power of low-power dc/dc converters based on charge-pump circuits. This is achieved by adjusting the switching frequency and conversion ratio based on measurements of the charge-pump output voltage, thus performing a two-dimensional MPPT operation. However, these implementations are not applicable in switching dc–dc converters that address higher power levels. In [10]–[22], various on-chip implementations inspired by the fractional open-circuit voltage (FOCV) method are presented. When applied to PV energy harvesting systems, the FOCV MPPT method has the disadvantage that the energy production is suspended during measurement of the PV source open-circuit voltage, which reduces the energy production efficiency. Furthermore, it requires knowledge of the open-circuit voltage of the PV source, which depends on both the manufacturing characteristics of the solar cells employed and their configuration in series and/or parallel for forming the PV generator in each application.

The MPPT technique in [23] has been implemented in an integrated circuit (IC) and it is based on changing the duty cycle and switching frequency of a dc/dc converter to ensure that the power conversion efficiency is maximized, and simultaneously, the input impedance of the power converter will always settle close to its optimal value, which should be known *a priori* (i.e., impedance matching). In [24], the MPPT process is performed on-chip by adjusting the power converter duty cycle such that the input impedance of the converter is equal to a previously known optimal value.

The MPPT method in [25] has also been implemented in an IC but it is applicable only in converterless energy harvesting systems with specific electrical and operational characteristics of the electronic load that is power-supplied. The MPPT process for converterless energy harvesting systems in [26] is based on the use of a negative feedback control loop for following a predefined voltage–frequency curve. In the time-based MPPT techniques [27]–[30], the power provided by the input source is estimated by measuring the charging time of a capacitor in the power converter circuit. However, although such an MPPT technique can be integrated on-chip, it is applicable only to specific configurations of the power converter circuit and, therefore, it cannot cover generic energy harvesting architectures.

In [1] and [31]–[36], on-chip designs of the P&O MPPT technique are presented, which are based on analog circuits. Among them, the MPPT circuit in [32] requires sample and hold (S/H) circuits while that in [35] is built based on a mixed-signal multiplier (requiring multiple capacitors) and an analog-to-digital (A/D) converter, all adding on the ASIC footprint size and complexity. The same is the case with [2], [37], [38], which require an analog multiplier and S/H circuits. In [39], a variation of the P&O MPPT method is implemented on-chip, which, however, requires the use of an analog power metering circuit and a complex digital core to ensure robustness under low irradiance conditions. Finally, the P&O methods in [33], [36], and [40]–[42] are all based on analog and mixed-signal circuitry (multiplexers, comparators, integrators, and/or electronic circuits), which increase the design and implementation complexity of the MPPT chip, due to the need of storing and processing the PV current and PV voltage measurements between consecutive sampling periods while keeping a high dynamic range with a chip of small footprint. In [43], a mixed-signal multiplier has been proposed recently for the calculation of power to implement the P&O method. The multiplier operation is based on internal analog circuits for producing pulse-signals with ON times proportional and inversely proportional, respectively, to the multiplier input voltages. Therefore, a special multiplier design is required for on-chip application of this MPPT technique.

Among the alternative MPPT methods described above for application in PV energy harvesting systems, the P&O technique has the advantages of universality, as well as operational and implementation simplicity. Also, it does not require knowledge of the operational characteristics of the PV source (e.g., PV source output impedance, locus of MPPs, open-circuit voltage, number of PV cells connected in series/parallel, etc.). Thus, it can be easily incorporated in commercial PV energy harvesting products, where the electrical specifications of the PV source are not known during the industrial manufacturing stage of the PV power management system since they are defined by the end-user depending on the application and installation site meteorological conditions [4].

According to the prior art review presented above, the existing on-chip implementations of the P&O MPPT technique are based on the use of complex electronic circuits such as analog PV current and voltage multipliers, S/Hs and A/D converters, which increase the implementation complexity and power consumption of the MPPT unit within an IC. Also, the commercially available chips either require the connection of external analog current and voltage sensors in order to perform the MPPT process according to the P&O technique (e.g., SM72445 and LT8490), or contain a microprocessor (e.g., MPT612 and PowerPSoC), which increases the complexity of MPPT system implementation on-chip, or they are not capable to operate with PV sources comprised of a single PV cell (e.g., MAX20800). Alternatively, the operation of commercial MPPT chips is based on the FOCV MPPT method (e.g., BQ24650, SPV1050, AEM10941, and CN3801), which, as discussed above, exhibits significant drawbacks in PV energy harvesting applications.

In this article, a novel MPPT control system for on-chip implementation of the P&O MPPT method is presented, which, compared to the on-chip MPPT solutions proposed till present at both the scientific and commercial levels, has the following advantages.

1) The use of complex circuits, such as multipliers, S/H units, A/D converters, or microprocessors, is not required.
2) The MPPT algorithm is implemented based on purely digital CMOS circuits, and therefore, its operation and performance do not depend on the chip fabrication technology.
3) *A priori* knowledge of the operational characteristics of the PV source is not required for its operation.
4) It is suitable for use over the entire spectrum of PV energy harvesting applications in combination with switching power converters of either low or high power rating.

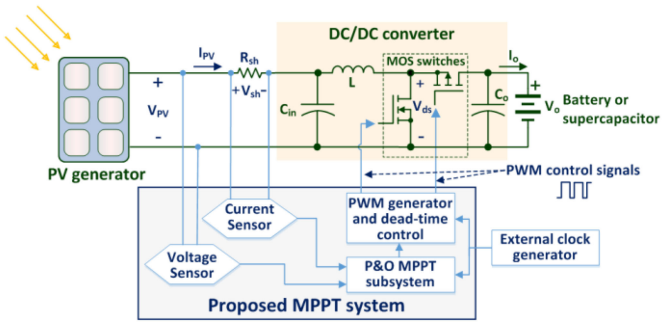


Fig. 2. Diagram of a PV energy harvesting system employing the proposed MPPT control unit.

Thus, the proposed MPPT system can be easily implemented on-chip with low design complexity while simultaneously retaining the high-performance features of the P&O MPPT technique. Additionally, its operation is not deteriorated by system noise, which is significant when controlling switching power converters and affects the operation of analog current and voltage sensing circuits. The proposed MPPT system has been fabricated using a 0.18-μm CMOS technology and its performance has been evaluated experimentally outdoors, under real operating conditions. Experimental results are presented in this article, which verify the successful operation of the fabricated MPPT chip and its ability to control in real time the MPPT operation of a dc/dc power converter in a PV energy harvesting system.

The rest of this article is organized as follows. The proposed MPPT system in terms of both the circuit-level design of the PV current and voltage sensors and the operation of the digital MPPT unit is described in Section II while the experimental results are presented in Section III. Finally, Section IV concludes this article.

II. Proposed MPPT System

A diagram of the PV energy harvesting system under study is shown in Fig. 2. It consists of a boost-type (step-up) dc/dc power electronic converter, the PV source output current and voltage sensors, and the MPPT circuit that produces the pulsewidth modulation (PWM) signals for driving the nMOS and pMOS power transistors of the dc/dc converter according to the P&O MPPT algorithm.

A. Circuit-Level Design of the PV Current and Voltage Sensors

To avoid the complexity and power consumption of A/D converters, the voltage and current sensor design in the proposed MPPT system was based on a voltage-to-frequency converter topology [44]. In order to generate the required input sensing signals for the digital MPPT block, the PV source output voltage is converted to a pulse train with a frequency $f_{V,\mathrm{pv}}$ (Hz), varying proportionally to the PV source output voltage (i.e., V_{PV} in Fig. 2), as follows:

$$f_{V,\mathrm{PV}} = k_V \cdot V_{\mathrm{PV}} \tag{1}$$

where k_V is the gain of the PV voltage sensor.

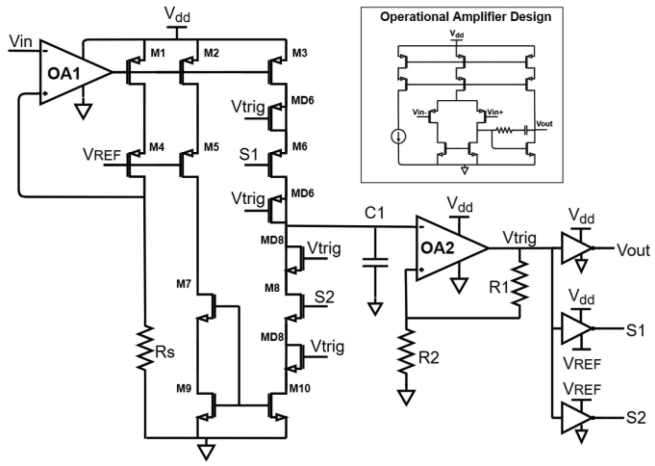


Fig. 3. Circuit diagram of the PV source voltage sensor of the proposed MPPT system.

The circuit diagram of the PV voltage sensor of the proposed MPPT system is depicted in Fig. 3. Initially, the input voltage is converted to the current through a voltage-to-current converter. This circuit block is based on an operational amplifier (OA1) utilizing resistive transistors, in order to achieve low-power operation. Furthermore, an additional cascode structure of pMOS transistors is placed under the supply voltage rail, to provide high power supply rejection ratio to the circuit. The resistor R_s, which is the key component for the voltage conversion, is selected at the value of 1 MΩ, to reduce the operating current and contribute to the further reduction of the power consumption. The produced current is mirrored through a cascode configuration in a scale of 4:1. The current charges and discharges C1 capacitor through pMOS switch M6 (charging) and nMOS switch M8 (discharging). A current-feedthrough and charge-injection cancelation technique is used [45], with the integration of two half-sized dummy switches (MDx) for each operational switch (M6 and M8) with short-circuited drain–source terminals, to reduce current spikes during ON and OFF operation. The voltage level of C1 changes between $V_{\mathrm{low}} = 0$ V and $V_{\mathrm{high}} = 1.4$ V. The V_{high} threshold is selected to the value that provides the best performance and linearity over process-voltage-temperature corners. The capacitor C1 voltage is controlled by a low-power op-amp based Schmitt Trigger (OA2) and two inverters, added to the output of the Schmitt Trigger to provide proper switching to the M6 and M8 switches (S1 and S2 signals). By selecting the C1 value at 100 pF, the output frequency range drops to hundreds of hertz to a few kilohertz, radically reducing the overall power consumption and the need of high-speed op-amp blocks implementation. Finally, a third inverter is added to act as a voltage buffer for the output that is fed to the digital MPPT control unit, which is described next. For the proper operation of the total sensor block, a voltage reference circuit (providing the voltage $\mathrm{V_{REF}}$ in Fig. 3) based on the work in [46] is designed, using transistors with different threshold voltages. Additionally, a current bank block is implemented, utilizing cascode transistors for robust operation. The overall simulated current consumption is 4.3 μA at 2.25 V.

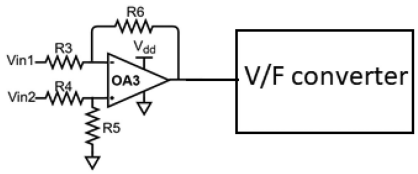


Fig. 4. Structure of the PV source current sensor of the proposed MPPT system.

The PV current sensor topology is presented in Fig. 4. An op-amp based voltage subtractor (OA3) senses the voltage difference at the terminals of the shunt resistor $R_{\rm sh}$ depicted in Fig. 2, which is equal to

$$\Delta V_{\rm shunt} = V_{\rm in,1} - V_{\rm in,2} = R_{\rm sh} \cdot I_{\rm PV} \tag{2}$$

where $V_{\rm in,1}$ $V_{\rm in,2}$ (V) are the voltages developed at the terminals of $R_{\rm sh}$ with respect to the ground level.

The output of OA3 is driving the input of a voltage-to-current converter with the same circuit as that shown in Fig. 3, thus producing a pulse train with frequency $f_{\rm I,pv}$ (Hz) that varies linearly with the PV source output current (i.e., $I_{\rm PV}$ in Fig. 2) according to

$$f_{I,\rm PV} = k_I \cdot R_{\rm sh} \cdot I_{\rm PV} \tag{3}$$

where k_I is the PV current sensor gain. The overall simulated current consumption is 5.6 μA at 2.25 V.

B. Digital MPPT Control Unit

The structural breakdown of the MPPT control unit and the interconnections between its subsystems are presented in Fig. 5. All modules contained in the proposed MPPT unit are implemented with digital circuits and their clock is provided by an external oscillator. The subsystems use clock dividers based on digital counters in order to adjust the sampling time $T_{\rm S\_CLK}$ (sec) and the shaping of the dc/dc converter PWM control signal as described in the following.

The operation of the proposed MPPT digital circuit is based on the P&O algorithm. As illustrated in Fig. 1, the derivative of the PV source output power with respect to its output voltage is positive at the left side of the MPP and negative at its right while the following condition holds at the MPP [4]:

$$\frac{\partial P_{\rm PV}}{\partial V_{\rm PV}} = 0 \tag{4}$$

where $P_{\rm PV}$ (W), and $V_{\rm PV}$ (V) are the output power and voltage, respectively, of the PV module/array.

In case that a boost-type dc/dc converter operating in the continuous conduction mode is connected to the output of the PV source, then its input $V_{\rm PV}$ and output V_o voltage levels are correlated as follows [47]:

$$\frac{V_o}{V_{\rm PV}} = \frac{1}{1-D} \tag{5}$$

where D is the duty cycle of the PWM control signal of the dc/dc converter's nMOS switch.

Furthermore, in PV energy harvesting applications, the dc/dc converter output is typically connected to an energy storage device (i.e., battery or supercapacitor). Thus, V_o remains constant during the short time interval required for convergence of the MPPT algorithm. Therefore, it is possible to change the operating point of the PV source, by changing the duty cycle of the PWM signal that drives the dc/dc converter, since according to (5), when the duty cycle is decreased, the operating point of the PV source shifts toward the right side of the PV power–voltage curve (i.e., higher voltages are developed at the PV source), else it moves toward the left side of that curve. When the boost-type dc/dc converter operates in the discontinuous-conduction mode, the nonlinear $D = g(V_{\rm PV})$ characteristic equation provided in [47] should be considered. In that case, since according to the current–voltage characteristic of a PV source it holds that $\frac{\partial I_{\rm PV}}{\partial V_{\rm PV}} < 0$ and as $V_o > V_{\rm PV}$, the following condition results:

$$\frac{\partial D}{\partial V_{\rm PV}} < 0. \tag{6}$$

Therefore, a similar operation with the continuous conduction mode, which has been described above, is also achieved in the discontinuous-conduction mode of the boost converter.

According to (1) and (3), the number of pulses of the PV current and voltage sensors during a sampling period $N_{I,\rm PV}$ and $N_{V,\rm PV}$, are proportional to $I_{\rm PV}$ and $V_{\rm PV}$, respectively

$$N_{I,\rm PV} = f_{I,\rm PV} \cdot T_{\rm S\_CLK} \tag{7}$$

$$N_{V,\rm PV} = f_{V,\rm PV} \cdot T_{\rm S\_CLK} \tag{8}$$

where $T_{\rm S\_CLK}$ (sec) is the sampling period. Therefore, the product $N_{P,\rm PV} = N_{I,\rm PV} \cdot N_{V,\rm PV}$ is proportional to $P_{\rm PV}$. By measuring the values of $N_{P,\rm PV}$ and $N_{V,\rm PV}$ in the proposed MPPT system, the condition for convergence to the MPP given by (4) is transformed as follows:

$$\frac{\partial P_{\rm PV}}{\partial V_{\rm PV}} = 0 \quad \Leftrightarrow \quad \frac{\partial N_{P,\rm PV}}{\partial N_{V,\rm PV}} = 0. \tag{9}$$

Thus, in the proposed P&O MPPT unit the need for incorporating analog multipliers, S/Hs, A/D converters, or other analog circuitry is eliminated. In order to control the dc/dc power converter, the duty cycle, $D(k)$, of the dc/dc converter PWM control signal at time step k is modified as follows:

$$D(k) = D(k-1) - \alpha \cdot \text{sign}\left(\frac{\partial N_{P,\rm PV}}{\partial N_{V,\rm PV}}(k)\right) \tag{10}$$

where $\alpha > 0$ is a constant and the function sign$(\cdot)$ is defined as follows:

$$\text{sign}(x) = \begin{cases} 1, & \text{if } x > 0 \\ -1, & \text{if } x < 0. \end{cases} \tag{11}$$

The digital values of $N_{P,\rm PV}$ and $N_{V,\rm PV}$ in (7)–(10) are stored in registers of 40 and 20 b, respectively. The value of $T_{\rm S\_CLK}$ should be higher than the time required by the dc/dc power converter to reach steady state after a duty cycle perturbation according to (10). The latter can be calculated according to the power converter circuit design in each target PV application based on [47]. A high value of α in (10) enables faster convergence to the MPP [48]. This is suitable for PV applications where the incident

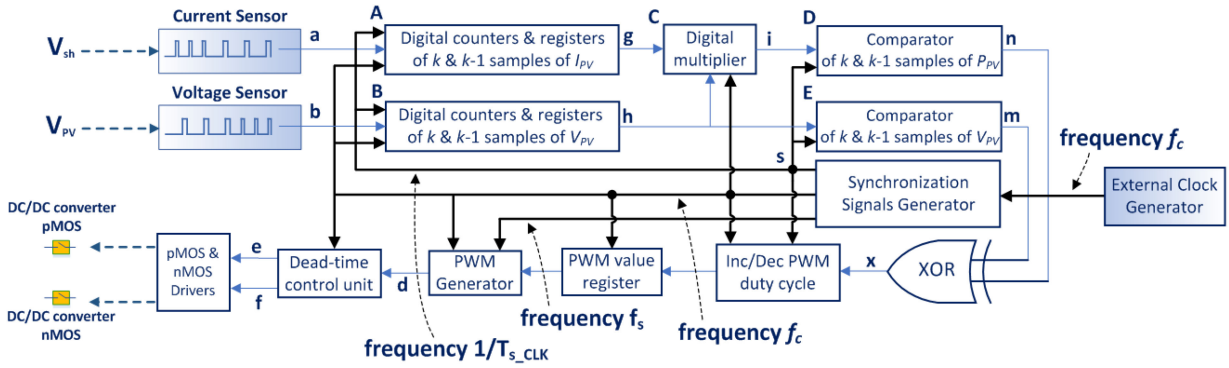


Fig. 5. Block diagram of the proposed MPPT unit.

solar irradiation changes frequently (e.g., due to shading when the PV system is installed in an urban environment, or on moving surfaces/vehicles, etc.). However, the amplitude of oscillations around the MPP after convergence of the tracking process is also increased in this case.

In order to implement the MPPT control law described by (10), the pulse-rate modulated digital outputs of the PV output current and voltage sensors (signals "a" and "b" in Fig. 5) trigger the corresponding digital counters (blocks A and B in Fig. 5), which sum the received events per sampling period and produce the binary values of $N_{I,\mathrm{PV}}$ and $N_{V,\mathrm{PV}}$, respectively. The registers in blocks A and B store the samples of $N_{I,\mathrm{PV}}$ and $N_{V,\mathrm{PV}}$ during the sampling periods k and $k-1$. In block C, the corresponding values of $N_{I,\mathrm{PV}}$ and $N_{V,\mathrm{PV}}$ are digitally multiplied to obtain the values of $N_{P,\mathrm{PV}}$ at the k and $k-1$ sampling periods, i.e., $N_{P,\mathrm{PV}}(k)$ and $N_{P,\mathrm{PV}}(k-1)$, respectively. Then, the pairs $[N_{P,\mathrm{PV}}(k-1), N_{V,\mathrm{PV}}(k-1)]$ and $[N_{P,\mathrm{PV}}(k), N_{V,\mathrm{PV}}(k)]$ are processed by digital comparators (blocks D and E), which raise their output to a logic "1" in case that $\Delta N_{P,\mathrm{PV}}(k) = N_{P,\mathrm{PV}}(k) - N_{P,\mathrm{PV}}(k-1) > 0$ or $\Delta N_{V,\mathrm{PV}}(k) = N_{V,\mathrm{PV}}(k) - N_{V,\mathrm{PV}}(k-1) > 0$, else, they output a logic "0." Therefore, since (10) is implemented through comparison of successive samples of $N_{P,\mathrm{PV}}$ and $N_{V,\mathrm{PV}}$, knowledge of the exact values of the sensors gains k_V and k_I in (1) and (3) is not required for the development (e.g., for adjustment of circuit parameters) and operation of the proposed on-chip MPPT unit. The outputs of the comparators are applied to a two-input XOR logic gate, which guarantees that when $\Delta N_{P,\mathrm{PV}}(k)$ and $\Delta N_{V,\mathrm{PV}}(k)$ have the same polarity the output will signal a duty cycle decrement, i.e., $0 \oplus 0 = 0$ and $1 \oplus 1 = 0$ according to (10), where "$\oplus$" is the Boolean symbol of the XOR operation. Similarly, when $\Delta N_{P,\mathrm{PV}}(k)$ and $\Delta N_{V,\mathrm{PV}}(k)$ have the inverse polarity, then the output will signal a duty cycle increment (i.e., $1 \oplus 0 = 1$ and $0 \oplus 1 = 1$). The XOR output is routed to a digital subsystem that increases or decreases by an amount equal to α [as dictated by (10)] the digital output of a counter that corresponds to the duty cycle value of the final PWM control signal of the dc/dc converter. The resulting output of the "Inc/Dec PWM duty cycle" block, is input to the "PWM Generator" module, which is implemented according to the work in [49] and includes the digital logic that creates a square-wave PWM control signal with the desired duty cycle for driving the power switches of the dc/dc converter. The resulting PWM signal is then routed (through signal "d" in Fig. 5) to the dead-time control unit, which introduces small delays to avoid cross-conduction of the nMOS and pMOS power switches of the dc/dc converter due to their non-zero turn-ON/OFF delay times.

In order to double the number of distinct duty cycle values that can be produced, a special module was embedded in the "PWM Generator" block that uses two counters where the first one is triggered on the rising edge of the clock and the second one is triggered on the falling edge of the clock. Therefore, the PWM frequency of the dc/dc converter f_s, the frequency of the global clock f_c, and the duty cycle range DR are related according to the following equation:

$$\mathrm{DR} = 2 \cdot \frac{f_c}{f_s}. \tag{12}$$

In order to implement a PV MPPT system using the proposed chip design, the value of f_s should initially be chosen by the designer of the dc/dc converter such that 1) the switching speed limit of the power switches employed (see Fig. 2, e.g., MOSFETs, IGBTs, etc.) is not exceeded and 2) the resulting switching power losses and volume of the inductive and capacitive components of the dc/dc converter satisfy the desired specifications, as described in [47]. Then, the value of f_c should be selected according to the specifications of the chip fabrication technology used, such that the power consumption of the digital circuits is kept to a low level.

The simulated waveforms of the principal MPPT logic signals presented in Fig. 5 are displayed in Fig. 6. This simulation includes the main clock, the current sensor output (signal "a"), and the voltage sensor output (signal "b"). The vector signals "g" and "h" are the outputs of the current and voltage registers, respectively, which hold the counter values of the number of digital pulses per sampling period, presented in a decimal format. The vector signal "i" corresponds to the product of "g" and "h" and holds the samples of the input power. The signal "s" contains the sampling triggering pulses. The signals "m" and "n" correspond to the result of the comparators of two consecutive samples of the voltage and the power, respectively. These comparators output a logic "1" when $\Delta N_{V,\mathrm{PV}}(k) > 0$ and $\Delta N_{P,\mathrm{PV}}(k) > 0$, else they output a logic "0." The signal "x" is the result of the XOR operation of signals "m" and "n." Its waveform confirms

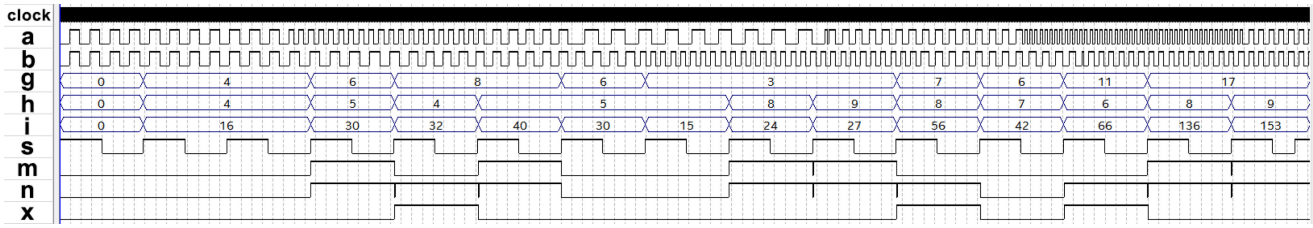


Fig. 6. Simulated waveforms of principal logic signals of the proposed MPPT control unit.

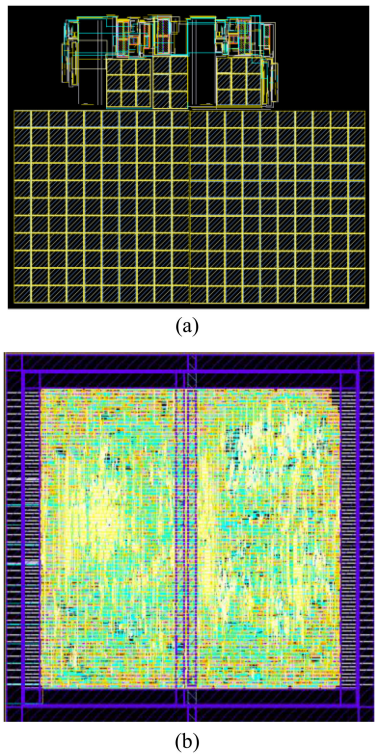
the desired outcome, which is to increase the duty cycle when $\Delta N_{P,\mathrm{PV}}(k)$ / $\Delta N_{V,\mathrm{PV}}(k) < 0$, else the duty cycle is decreased.

The proposed on-chip MPPT unit is based on the implementation of the P&O technique in a digital subsystem while analog circuit design is only required for the PV current and voltage sensors. The major advantage of this feature is that the proposed digital P&O subsystem can be designed using a Hardware Description Language (e.g., VHDL) independently of the final fabrication technology of the chip, which demands a low chip design effort. In contrast, its analog counterpart would require detailed circuit design (e.g., for calculation of components values, adjustment of voltage thresholds, extensive simulations, such as corner and/or Monte Carlo analyses), which depends on the target fabrication technology of the chip and needs re-design if another chip fabrication technology is selected. Also, in the proposed on-chip MPPT unit, the IC noise does not affect the major part of the overall MPPT system since it is based on digital circuits, while in a fully analog MPPT system the entire circuit would be vulnerable to noise.

III. Experimental Results

The proposed MPPT system was fabricated using the XFAB XH018 0.18-μm mixed-signal CMOS technology. The PV current/voltage sensors and the MPPT control unit, respectively, were fabricated in two different chips, which were interconnected during the experimental validation process, but this does not affect the operation of the overall MPPT system. The digital MPPT control unit has been built using the VHDL language, while the Cadence Virtuoso digital implementation software suite was used for the synthesis of the final chip. The physical design of the PV source current and voltage sensors is depicted in Fig. 7(a). Special techniques, such as cross-coupling and interdigitation, were employed for the transistors matching. Additionally, dummy devices were incorporated to improve the overall circuit performance. The 100-pF capacitors of the sensors were fully integrated on chip using metal–insulator–metal (MIM) capacitors. Guard rings were added to protect the sensor blocks from noise generated by other circuits of the chip. The total sensors' physical layout implementation area is 640 μm $\times$ 520 μm. The physical design of the P&O MPPT control unit is presented in Fig. 7(b). The occupied area is 465 μm $\times$ 465 μm and its power consumption has been measured experimentally equal to 141.5 μW.

The performance of the fabricated chips of the proposed MPPT system was tested outdoors under real operating conditions by synthesizing a PV array comprised of four PV modules



(a)

(b)

Fig. 7. Physical design of the (a) PV current and voltage sensors and (b) P&O MPPT control unit.

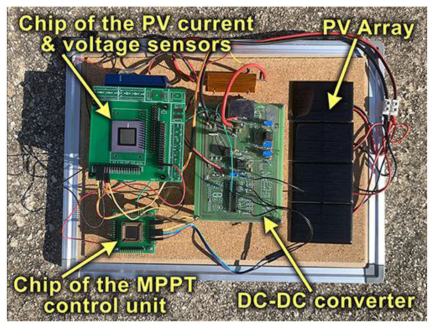


Fig. 8. Experimental setup used for evaluating the performance of the fabricated chips of the proposed MPPT system.

connected in parallel. Also, a dc/dc converter operating with a PWM switching frequency of 31.25 kHz was designed according to the work in [47]. The overall experimental setup is illustrated in Fig. 8, while the parameters of the PV modules under standard test conditions (STC) and dc/dc converter, respectively, are listed

TABLE I
PV MODULE AND DC/DC CONVERTER PARAMETERS VALUES IN THE EXPERIMENTAL SETUP

PV MODULES	
Short-circuit current under STC	0.24 A
Open-circuit voltage under STC	2.4 V
MPP power under STC	0.4 W
DC/DC CONVERTER	
PWM switching frequency	31.25 kHz
Inductance, L	150 μH
Input capacitance, C_{in}	1000 μF
Output capacitance, C_o	4700 μF
Nominal output voltage, V_o	6 V

in Table I. The PWM output of the MPPT chip drives, through a MOSFET driver IC, the dc/dc converter circuit, which has been built using discrete electronic components. The output of the dc/dc converter is connected to a 6-V rechargeable battery, which also provides power to the MPPT chip through a 2.4-V voltage regulator. Also, a shunt resistor of $R_{\text{sh}} = 0.1\Omega$ has been used for sensing the PV array output current, as analyzed in Section II-A. In order to experimentally test the operation of the fabricated chips, the values of f_s, f_c, $T_{\text{S\_CLK}}$, and α were selected as described in Section II-B. Considering the values of the dc/dc converter parameters shown in Table I, the switching frequency of the PWM control signals, which are produced by the P&O MPPT unit, has been set to $f_s = 31.25\,\text{kHz}$. A signal generator has been used to provide the $f_c = 2\,\text{MHz}$ clock pulses of the digital subsystems of the MPPT control unit, which results in DR = 128 according to (12). Finally, (10) is implemented with $\alpha = 4$ and $T_{\text{S\_CLK}} = 0.5$ (sec) in order to achieve adequate performance in terms of MPPT convergence speed and accuracy for the typical PV applications as analyzed in Section II-B.

The experimentally measured PV array output voltage and current during operation of the proposed MPPT chip in case that the incident solar irradiation intensity and ambient temperature are equal to 1000 W/m^2 and 26 °C, respectively, are shown in Fig. 9(a). At that operating point of the PV source, it holds that $V_{\text{PV}} = 1.75\,\text{V}$ and $I_{\text{PV}} = 800\,\text{mA}$. The corresponding oscilloscope waveforms of the output signals of the PV array output voltage and current sensing circuits of the proposed MPPT system are presented in Fig. 9(b). According to these results, it is concluded that the experimental gains of the PV voltage and current sensors in (1) and (3) are equal to $k_V = 899.43\,\text{Hz/V}$ and $k_I = 872.91\,\text{Hz/V}$. These values deviate by 0.71% and 3.82%, respectively, from the corresponding values derived by circuit post-layout simulations performed after the physical design of the proposed MPPT chip. These deviations are due to the chip fabrication process. The resulting waveforms of the pMOS transistor gate voltage that is produced by the PV MPPT system for PWM control in this test case, as well as the corresponding drain–source voltage of the dc/dc converter nMOS transistor

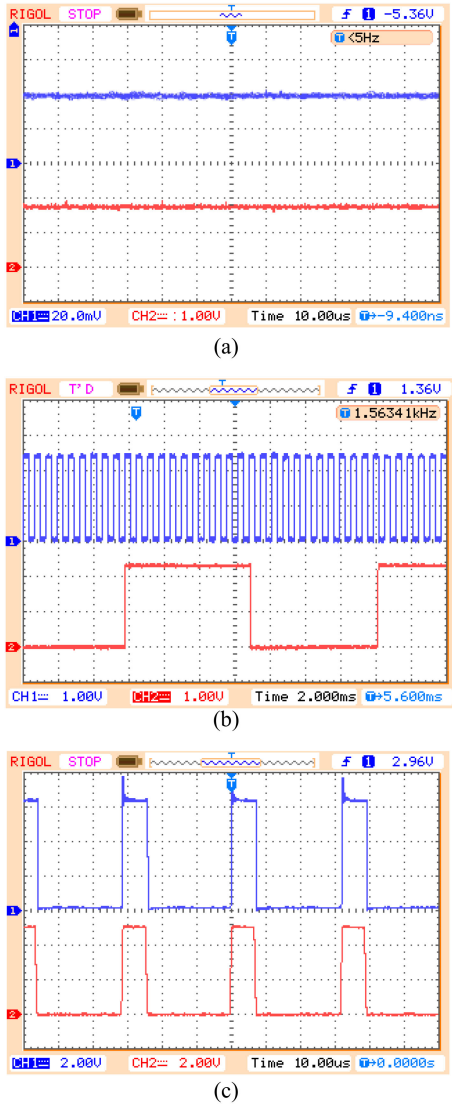


Fig. 9. Oscilloscope waveforms at 1000 W/m^2 and 26 °C of (a) PV array output current (channel 1: 400 mA/div) and voltage (channel 2: 1 V/div), (b) output voltage of the sensing circuits of the PV array output voltage (channel 1: 1V/div) and current (channel 2: 1 V/div), (c) dc/dc converter nMOS drain–source voltage (channel 1: 2 V/div), and PWM control signal (channel 2: 2V/div).

(i.e., V_{ds} in Fig. 2), are depicted in Fig. 9(c). It is observed that the PWM signal produced by the fabricated MPPT chip is capable to control the switching operation of the dc/dc converter as expected, in order to perform the MPPT process.

The operation of the proposed MPPT system was evaluated for incident solar irradiance values in the range of 100–1000 W/m^2. The corresponding experimentally measured current–voltage and power–voltage characteristics of the PV array are presented in Fig. 10. The corresponding MPP of the PV source as well as the final operating point after convergence of the P&O process that is executed by the proposed MPPT system are also depicted in that figure. Due to the inherent oscillation of the operating point of the PV array around the MPP, which is imposed by the P&O algorithm according to (10), the average power produced by the PV array after convergence of the MPPT system for each

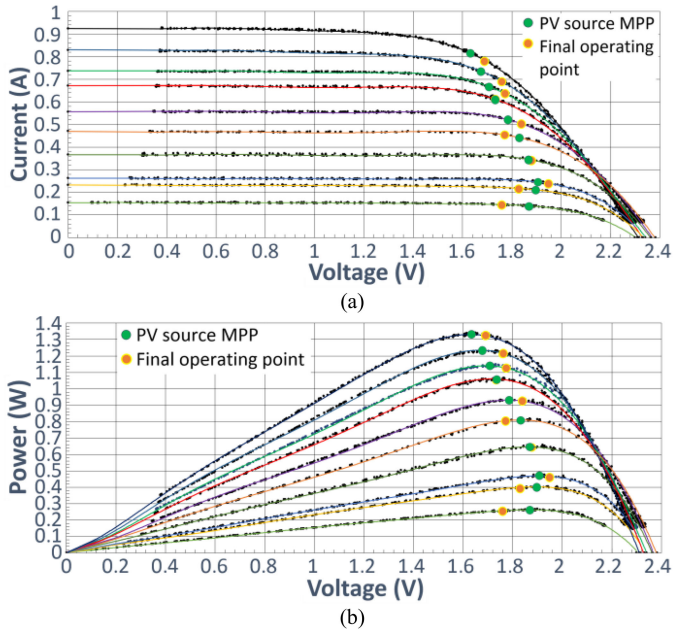


Fig. 10. Experimental results for incident solar irradiance values in the range of 100–1000 W/m^2. (a) PV array current–voltage characteristics. (b) PV array power–voltage characteristics.

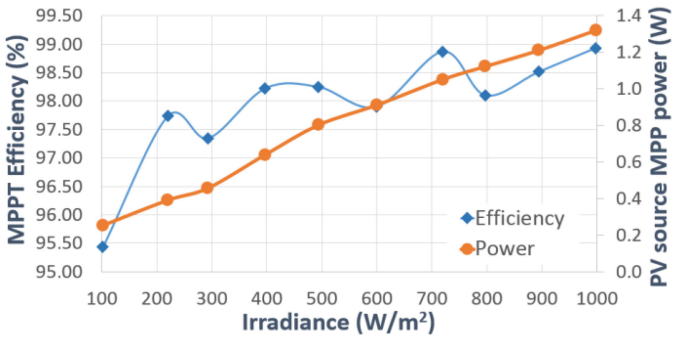


Fig. 11. Experimentally measured MPP power of the PV array and the MPPT efficiency of the proposed system for incident solar irradiance values in the range of 100–1000 W/m^2.

solar irradiance value was calculated. In order to quantify the accuracy of convergence to the actual MPP of the PV array, the MPPT efficiency η_{MPP} (%) of the proposed MPPT system has been calculated as follows:

$$\eta_{\text{MPP}} = \frac{P_{\text{MPP},r}}{P_{\text{MPP},a}} \cdot 100\% \tag{13}$$

where $P_{\text{MPP},r}$ (W) is the average value of the PV-generated power after convergence of the MPPT system and $P_{\text{MPP},a}$ (W) is the power at the actual MPP point of the PV source according to the experimental results displayed in Fig. 10.

The resulting values of η_{MPP} at various incident solar irradiance levels are presented in Fig. 11, demonstrating that the proposed on-chip MPPT control unit achieves a high MPPT efficiency over a wide range of solar irradiance values. The deviations from the actual MPP of the PV source are due to 1) the small-scale offset and nonlinearity exhibited by the PV array output voltage and current sensing circuits in the fabricated

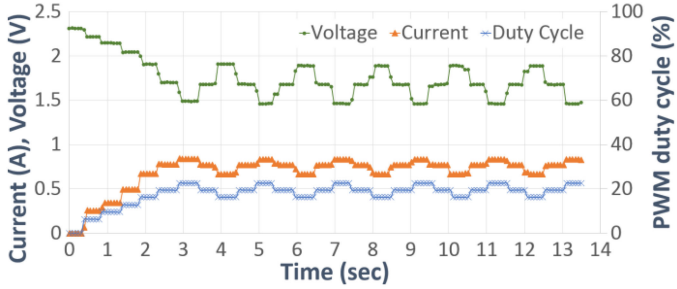


Fig. 12. Experimental waveforms of the PV source output current and voltage and the duty cycle of the dc/dc converter control signal, during operation of the proposed MPPT system under transient conditions, when the incident solar irradiance is 1000 W/m^2.

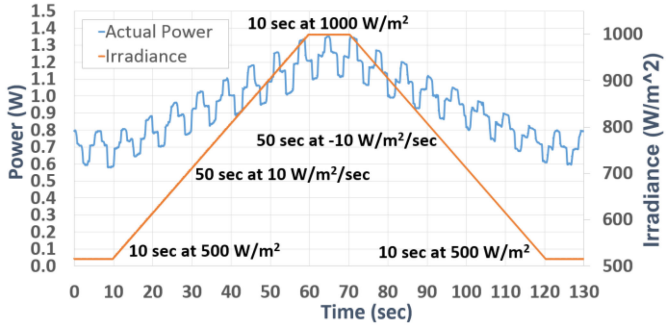


Fig. 13. Experimentally measured power that is produced by the dc input source during dynamic operation of the proposed MPPT chip when the incident solar irradiance follows a sequential ramp.

chip and 2) the size of the duty cycle perturbation step [i.e., parameter α in (10)]. These results verify that since the duty cycle calculation according to (10) is based on comparison of successive samples of $N_{P,\text{PV}}$ and $N_{V,\text{PV}}$ and not on their absolute values, as analyzed in Section II-B, any deviation of the simulated and experimental values of k_V and k_I in (1) and (3) does not affect significantly the operation of the proposed on-chip MPPT unit.

The dynamic operation of the proposed MPPT system is illustrated in Fig. 12, which displays the variation of the PV source output current and voltage, as well as the duty cycle of the dc/dc converter control signal, during the execution of the MPPT process in case that the incident solar irradiance is 1000 W/m^2 and the duty cycle value was initially set equal to 0 %. The time required for convergence to the MPP of the PV source under transient conditions depends on the P&O algorithm iteration period [i.e., parameter $T_{\text{S\_CLK}}$ in (7) and (8)], which must be set to be longer than the response time of the dc/dc converter.

The dynamic operation of the fabricated MPPT chips was additionally evaluated experimentally by applying ramps of irradiance variation as analyzed in [50] based on the EN 50530 standard. For that purpose, by adjusting the tilt angle of the PV array with respect to the horizontal plane, the incident solar irradiance was set to follow a sequential ramp between 500 W/m^2 and 1000 W/m^2 with a rate of $\pm$10 W/m^2/s and a pause of 10 s on each irradiance level, as shown in Fig. 13. The power produced by the PV array during the operation of the proposed MPPT chip

under these conditions is also illustrated in Fig. 13. It is observed that the proposed on-chip MPPT system follows successfully the changes of incident solar irradiance that appear in typical PV applications and its performance is not affected by the time delay of the internal digital circuits. Also, the power produced at each operating point is in accordance with the results presented in Figs. 10 and 12. The power oscillations observed are an inherent characteristic of the P&O MPPT algorithm according to (10), as also mentioned above.

The experimental results demonstrate that, compared to the integrated MPPT system presented recently in [43], the proposed on-chip MPPT control unit operates successfully by employing only CMOS digital units, without requiring the implementation of analog circuits. Furthermore, it is capable to operate in combination with PV current and voltage sensors with a pulse-frequency modulated output that is connected externally to the chip of the proposed MPPT control unit, in order to adapt to any target PV energy harvesting system requirements (e.g., in high-power PV systems).

IV. Conclusion

The use of power management ICs is required in PV energy harvesting applications, which implement an efficient MPPT process for maximizing the power production of the PV source during the continuously changing atmospheric conditions. Among the alternative MPPT techniques, the P&O method has the advantages of operational and implementation simplicity. In this article, a novel PV MPPT control system has been presented, which is suitable for on-chip implementation of the P&O MPPT method. Compared to the past-proposed on-chip MPPT implementations at both the scientific and commercial levels, the proposed MPPT system has the advantage that it is implemented based on purely digital CMOS circuits without requiring the use of complex circuits, such as multipliers, S/H units, A/D converters, or microprocessors. Also, its operation does not require *a priori* knowledge of the operational characteristics of the PV source and it can be used in combination with switching power converters of any power rating. Therefore, it can be easily implemented on-chip with low design complexity while simultaneously retaining the high-performance features of the P&O MPPT technique. The proposed PV MPPT system has been fabricated using the XFAB XH018 0.18-μm CMOS technology. The experimental results that were obtained under real operating conditions verified the successful operation of the proposed on-chip PV MPPT control unit and its ability to achieve a high MPPT efficiency over a wide range of operating solar irradiation values. The proposed MPPT system design is universal and its operation does not depend on the chip fabrication technology. Finally, it can also be used for performing the MPPT process of thermoelectric generators, which are frequently employed in ambient energy harvesting applications [23].

Acknowledgment

The authors would like to thank Prof. V. Paliouras, Mr. K. Papachatzopoulos, and Mr. E. Kavvousanos (Electrical and Computer Engineering Department, University of Patras, Greece) for their contribution in the synthesis of the physical design of the digital MPPT control unit.

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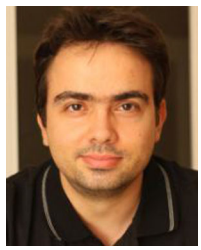

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