High-Efficiency Low-EMI Buck Converter Using Multistep PWL and PVT Insensitive Oscillator

Hong-Yi Huang, *Member, IEEE*, Harreez M. Villaruz, and Nieva M. Mapula

***Abstract*—This article presents a high-efficiency buck converter with electromagnetic interference (EMI) reduction. The proposed buck converter employs a simple method of piecewise linear (PWL) modulation to mitigate EMI significantly. Since EMI reduction tradesoff with efficiency and ripple content, this work also integrates the design of process, voltage, and temperature (PVT) insensitive crystal-less oscillator. This technique limits the modulated switching frequency to remain within range across all process corners, supply voltage. and operating temperatures, thereby limiting the range of efficiencies and ripple content that the buck converter will incur throughout its operation. As a result, the tradeoff between efficiency and ripple content is optimized while maintaining lower output voltage spurious noise tone. The chip was implemented using the 0.18 μm 1p6m CMOS process. The measured results show that the power spectrum's peak noise is at −60.37 dBm, and the minimum efficiency is 93% with a ripple content of less than 43.7 mV for worst-case considering PVT variations at 2.2 V input, 1.7 V output with 100 mA load current.**

***Index Terms*—Buck converter, electromagnetic interference (EMI), EMI mitigation, EMI reduction, modulation profile, oscillator, piecewise linear (PWL), process, voltage, and temperature (PVT) insensitive oscillator, pulsewidth modulation (PWM).**

I. Introduction

THE emergence of 5G network encouraged any physical object's transformation into an IoT device, where inanimate objects became smarter, while electronic devices gain connectivity [1]. This surge of demands on IoT devices, specifically on wireless sensor nodes (WSN), necessitated the additional need for efficient power converters. A typical WSN consists of application-specific integrated circuit, power management unit (PMU), sensing circuitry, clocking modules, and radio frequency (RF) blocks [2]. Since all these blocks are integrated into a single chip for more functionality, the undesired spurious noise of the PMU usually degrades the performance of the noise-sensitive RF blocks [3]. As such, most buck converters impose electromagnetic interference (EMI) reduction techniques.

The pulsewidth modulation (PWM) switch control scheme provides the most flexible and practical approach to solve the EMI problem [4]. These control schemes include delta-sigma modulation (DSM), frequency hopping technique, and periodic PWM modulation. DSM is a frequency-variation control system that has low harmonic and switching frequency noise. It can shape the frequency noise to high band frequencies. However, it exhibits clock-feedthrough and charges injection error signal that affects system operation [5]. Moreover, it requires a high-frequency clock input and complex combinations of counters and accumulators as waveform shapers.

On the other hand, the frequency hopping technique allows random selection of ramp frequencies to decrease spur noise and reduce EMI effectively. However, the random frequencies produce unexpected ripple signals. A low hopping rate is ineffective in reducing the spur noise while a high hopping rate is challenging to design [6] and may cause duty-cycle errors and high power loss.

With periodic PWM modulation, the frequency of the gate signal is modulated. One of its important advantages is that it introduces lower unwanted low-frequency harmonics than other modulation schemes [4]. This simple structure eliminated the spike in the frequency domain because the energy is not any more accumulated at a fixed switching frequency but is spread to a range of frequencies. The most common profiles used in periodic PWM modulation are sinusoidal signal, triangular signal, and exponential signal [4]. The exponential or onion wave modulation profile is not linear, but it gives the most considerable EMI reduction; thus, its implementation is complex. On the other hand, triangular modulation has the simplest implementation, but its EMI reduction is lower [7].

In order not to sacrifice complexity with EMI reduction, this article aims to propose a multistep piecewise linear (PWL) modulation profile consisting of several linear signals as a simple method to approximate the onion wave to achieve higher EMI reduction. Moreover, this article also proposes a way to maintain the switching frequency range by integrating a process, voltage, and temperature (PVT) insensitive crystal-less oscillator to the multistep PWL modulator. This method will help reduce frequency variations due to process, voltage, and temperature variations that may compromise the buck converter's efficiency. This will ensure that the buck converter's range of efficiencies throughout its operation stays within the desired range.

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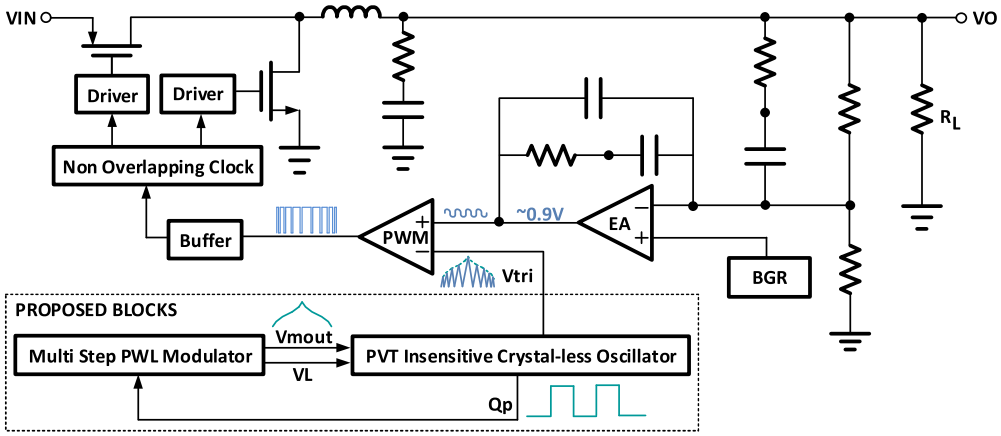

Fig. 1. Proposed high-efficiency low EMI buck converter.

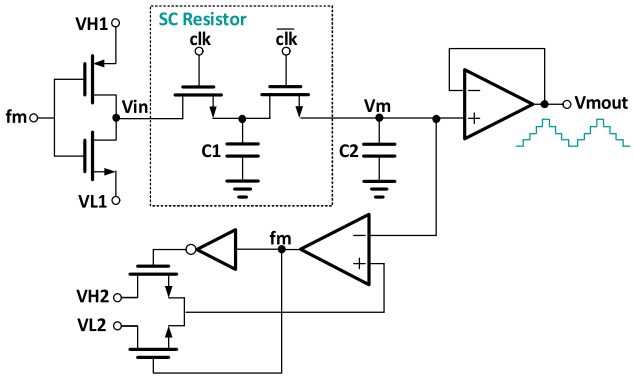

Fig. 2. Switched-capacitor frequency modulator circuit.

The enhanced buck converter architecture with the proposed blocks is shown in Fig. 1. Section II discusses the new multistep PWL and the PVT-insensitive oscillator design. Section III presents the measurement results. Finally, Section IV concludes this article.

II. Circuit Design and Analysis

A. Multistep PWL Frequency Modulator

EMI peak reduction can be calculated from its direct relationship with modulation index m_f as shown in (1). As such, to have larger attenuation, m_f is increased. This can be done by increasing the spreading ratio δ or by decreasing modulating frequency f_m. Since δ dictates the desired range of switching frequency f_{sw}, it is best to increase m_f by decreasing f_m. In the current controlled or thermometer coded capacitor technique, f_m is decreased by increasing the counters that drive the switches. To alleviate problems with large counters, [8] presented a jitter function using switched-capacitor (SC) scheme as shown in Fig. 2, which is similar to the sample and hold concept. It generates a triangular waveform by transferring charges between C_1 and C_2, where the switched capacitor acts as a resistor. Therefore, the current that flows from nodes V_{in} to V_m can be derived following (2) to (5).

Due to exponential charging and discharging characteristics of the capacitor as shown in (6) and (7), the output triangular waveform of [8] is found to be nonlinear and nonsymmetric which degrades its EMI reduction. To address this concern, this article, equated (6) and (7) to ensure 50% duty cycle and then set the time constant τ, to be longer than the time period t_m, to make the waveform linear. Equation (8) shows τ due to the SC resistor and C_2. Substituting resistance in (4) to (8), τ is simplified to (9). Equation (10), on the other hand, shows the time period t_m, of the triangular waveform V_m, which is the sum of charging and discharging time. Substituting (5) to (10) and assuming $\Delta V = V_m$, $f_{sw} = Q_p$ since this is the frequency of the clock from the oscillator, $V_{H1} >> V_m$ and $V_{L1} >> V_m$, t_m can then be rewritten into (11).

$$\mathrm{EMI_{reduction}} \propto 10\log m_f \propto 10\log \frac{\delta * f_{sw}}{f_m} \tag{1}$$

$$Q = CV = IT \tag{2}$$

$$V/I = T/C \tag{3}$$

$$R = \frac{T}{C} = \frac{t_{sw}}{C_1} = \frac{1}{f_{sw}\cdot C_1} \tag{4}$$

$$I = \frac{V}{R} = \frac{V_{in}-V_m}{(1/f_{sw}\cdot C_1)} = f_{sw}\cdot C_1\cdot (V_{in}-V_m) \tag{5}$$

where $V_{in} = V_{H1}$ when $f_m = 0$.
$V_{in} = V_{L1}$ when $f_m = 1$.

$$V_m = \Delta V\cdot[1-e^{(-tm/\tau)}] \tag{6}$$

$$V_m = \Delta V\cdot e^{(-tm/\tau)} \tag{7}$$

where $V_m =$ is the amplitude of the output triwave.
$t_m =$ is the frequency of the output triwave $= 1/f_m$.
$\Delta V = V_{H2} - V_{L2}$.
$\tau =$ is the time constant of the integrator RC.

$$\tau = RC \tag{8}$$

$$\tau = \frac{C_2}{f_{sw}\cdot C_1} \tag{9}$$

$$t_m = t_c + t_d = \frac{C_2\cdot\Delta V}{I} + \frac{C_2\cdot\Delta V}{I} \tag{10}$$

$$t_m = \frac{C_2\cdot V_m}{C_1\cdot Q_p\cdot V_{H1}} + \frac{C_2\cdot V_m}{C_1\cdot Q_p\cdot V_{L1}} \tag{11}$$

From (11), since it is best to attain more EMI reduction by decreasing f_m or increasing t_m, one can decide for the values

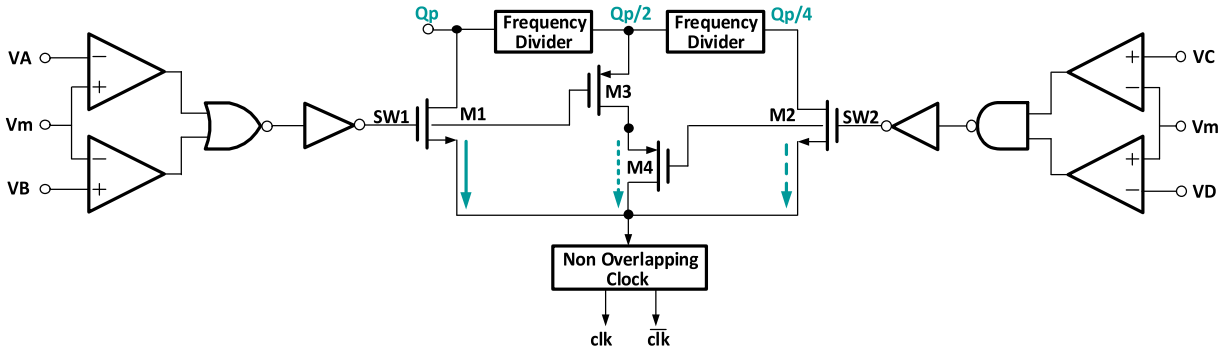

Fig. 3. Frequency selector circuit for proposed multi step PWL modulator.

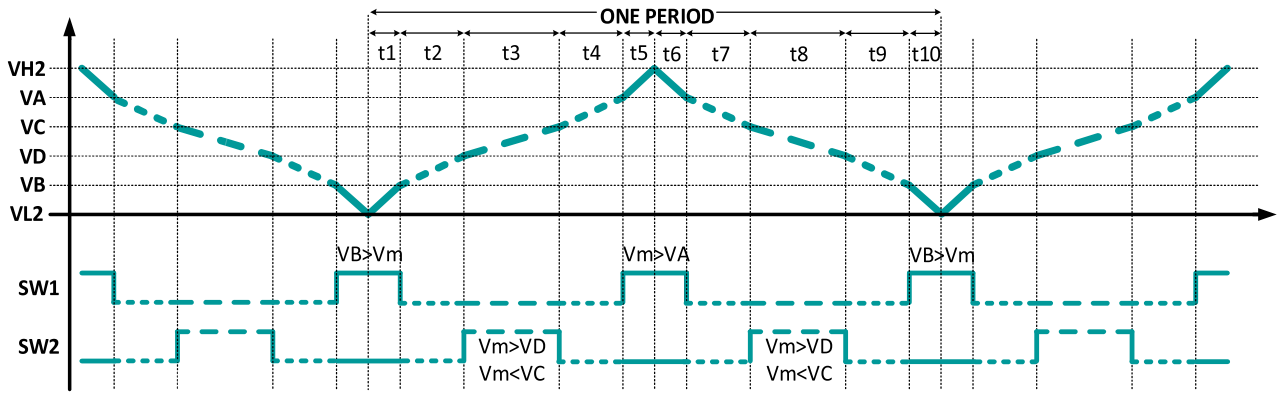

Fig. 4. PWL onion wave profile.

of C_1 and C_2. But to consume less area, C_1 is small as possible. But it cannot be smaller than around 100FF for it not to be dominated by parasitic capacitances. Thus, it is the area of C_2 that would limit the choice of t_m. This is the limitation of the architecture in [8].

In this article, for more reduction of EMI peak, t_m is further increased by varying the frequency f_{sw} of the clk and $\overline{clk}$ of the SC resistor of [8] at certain voltage levels to approximate an onion waveform. The triangular profile is modified by using the multistep PWL modulation idea presented in [7]. But instead of modifying the step increment at different time intervals, it is the frequency that is varied at different voltage levels. This further simplifies the idea of [7], as the high-frequency input clock, accumulators, and number of counters are also eliminated.

Fig. 3 shows the frequency selector circuit that is added to the frequency modulator circuit of [8] in Fig. 2 to enhance the EMI reduction. This circuit varies the frequency of the clk and $\overline{clk}$ at different voltage levels within V_{H2} and V_{L2} approximating an onion wave. It is composed of four comparators to compare voltage levels; two frequency dividers to divide the oscillator output Q_p by two and four; and four frequency selector switches M1, M2, M3, and M4 to decide which among frequencies Q_p, $Q_p/2$, or $Q_p/4$ goes through the nonoverlapping clock generator. The output of the comparators at different voltage levels decides the control signals SW1 and SW2, which will turn ON or OFF transistors M1, M2, M3, and M4. In effect, this gives different frequencies to the clk and $\overline{clk}$ instead of just constant Qp.

Fig. 4 shows the PWL onion wave profile and control switches SW1 and SW2. At time period one (t_1) and ten (t_{10}), $V_m<V_B$ and $V_m<V_A$, thus SW1 is 1. Moreover, since $V_m<V_C$ and $V_m<V_D$, thus, SW2 is 0. With SW1 $=$ 1, M1 is turned ON and M3 is turned OFF. While with SW2 $=$ 0 M2 is turned OFF. Therefore, clk and $\overline{clk}$ will receive a clock frequency of Q_p.

At time period two (t_2) and nine (t_9), $V_m>V_B$ and $V_m<V_A$, thus SW1 is 0. Moreover, since $V_m<V_C$ and $V_m<V_D$, thus, SW2 is 0. With SW1 $=$ 0, M1 is turned OFF and M3 is turned ON. While with SW2 $=$ 0 M2 is turned OFF and M4 is turned ON. Therefore, clk and $\overline{clk}$ will receive a clock frequency of $Q_p/2$.

At time period three (t_3) and eight (t_8), $V_m>V_B$ and $V_m<V_A$, thus SW1 is 0. Moreover, since $V_m<V_C$ and $V_m>V_D$, thus, SW2 is 1. With SW1 $=$ 0, M1 is turned OFF and M3 is turned ON. While with SW2 $=$ 1 M2 is turned ON and M4 is turned OFF. Therefore, clk and $\overline{clk}$ will receive a clock frequency of $Q_p/4$.

At time period four (t_4) and seven (t_7), $V_m>V_B$ and $V_m<V_A$, thus SW1 is 0. Moreover, since $V_m>V_C$ and $V_m>V_D$, thus, SW2 is 0. With SW1 $=$ 0, M1 is turned OFF and M3 is turned ON. While with SW2 $=$ 0 M2 is turned OFF and M4 is turned ON. Therefore, clk and $\overline{clk}$ will receive a clock frequency of $Q_p/2$.

At time period five (t_5) and six (t_6), $V_m>V_B$ and $V_m>V_A$, thus SW1 is 1. Moreover, since $V_m>V_C$ and $V_m>V_D$, thus, SW2 is 0. With SW1 $=$ 1, M1 is turned ON and M3 is turned OFF. While with SW2 $=$ 0 M2 is turned OFF. Therefore, clk and $\overline{clk}$ will receive a clock frequency of Q_p.

Table I summarizes the conditions of SW1 and SW2 at different voltage levels of V_m and the corresponding switching

TABLE I
SWITCH CONTROL OUTPUT FREQUENCY

V_m Voltage Level	SW1	SW2	f_{sw}
V_A to V_{H2}	1	0	Q_p
V_C to V_A	0	0	$Q_p/2$
V_D to V_C	0	1	$Q_p/4$
V_B to V_D	0	0	$Q_p/2$
V_{L2} to V_B	1	0	Q_p

frequency f_{sw} of the input clocks clk and $\overline{\text{clk}}$ of Fig.2. Note that selecting the fastest switching frequency at time periods t_5, t_6 and t_1, t_{10} will further increase the signal slopes at maximum and minimum points, respectively.

$$t_m = t_1 + t_2 + t_3 + t_4 + t_5 + t_6 + t_7 + t_8 + t_9 + t_{10} \quad (12)$$

$$\begin{aligned} t_m = {} & \frac{C_2(V_B - V_{L2})}{C_1 Q_p V_{H1}} + \frac{C_2(V_D - V_B)}{C_1 \frac{Q_p}{2} V_{H1}} + \frac{C_2(V_C - V_D)}{C_1 \frac{Q_p}{4} V_{H1}} \\ & + \frac{C_2(V_A - V_C)}{C_1 \frac{Q_p}{2} V_{H1}} + \frac{C_2(V_{H2} - V_A)}{C_1 Q_p V_{H1}} + \frac{C_2(V_{H2} - V_A)}{C_1 Q_p V_{L1}} \\ & + \frac{C_2(V_A - V_C)}{C_1 \frac{Q_p}{2} V_{L1}} + \frac{C_2(V_C - V_D)}{C_1 \frac{Q_p}{4} V_{L1}} + \frac{C_2(V_D - V_B)}{C_1 \frac{Q_p}{2} V_{L1}} \\ & + \frac{C_2(V_B - V_{L2})}{C_1 Q_p V_{L1}}. \end{aligned} \quad (13)$$

In addition, by selecting the slowest frequency at t3 and t8 the slopes at the zero-crossing points will decrease. This will help evenly distribute the energy within the frequency band. Hence, with just a simple PWL, the magnitude of EMI reduction is increased as compared to that of [8]. The modulation period in (11) can then be modified by substituting different voltage levels and different frequencies to get the modulation time t_m of the multistep PWL. Doing the same steps in (10) and (11) on how to solve the $_{tm}$ for the triangular wave, the t_m of the multistep PWL can then be shown as that of (12) and (13).

B. PVT Insensitive Crystal Less Oscillator

Equation (14) shows the output frequency of an oscillator. The frequency of an oscillator can be made less sensitive to process, voltage supply and temperature if (i) V_H and V_L are from the same bandgap reference circuit which gives the same voltage difference (V_H-V_L) in all process corners, voltage and temperature; (ii) capacitor C can be made less sensitive to process, which is made possible by using NMOSCAP which has $\pm 4\%$ variation as compared to the $\pm 15\%$ variation of MIMCAP and (iii) current I_{ref} can be made constant throughout supply, process, and temperature variations.

$$Q_p = \frac{I_{ref}}{C \cdot (V_H - V_L)}. \quad (14)$$

However, most current references are from a constant Gm (CGM) circuit, where current is only voltage and temperature independent. This is because of the $\pm 15\%$ process variation of its resistor component. To improve I_{ref}, the resistor less CMOS current reference idea of [9] was applied to the voltage to current (VtoI) converter of [10]. But instead of using one transistor operating in a linear region to replace the resistor, the VtoI converter produces an output current which is the sum of currents from two transistors operating in saturation and a linear region as shown in (15). Since the current is proportional to carrier mobility, its variation due to process will still be about 15%.

$$I_{ref} = \beta \cdot [(V_{GS} - V_{th}) - V_{ref}] \quad (15)$$

$$I_{ref} = 2 \cdot V_{ref} \cdot C \cdot F_{ref}. \quad (16)$$

In [11], the circuit in [10] was modified to make it a low voltage V to I converter. It reduced the elements in series to reduce the minimum voltage required. Moreover, [11] replaced the resistor with an SC claiming that the SC equivalent resistor when coupled with high accuracy bandgap voltage will have low variation as shown in (16). However, it can be seen that aside from the process variation due to the capacitor, an accurate external clock F_{ref} is required by the circuit to drive the switched capacitors.

In this article, as shown in Fig. 5, the structure in [11] is further improved by replacing SC with a single linear MOS resistor. Since in linear MOS, current is dependent on β and V_{th} variation, MN3 a cascade NMOS in saturation is added to make V_{th} variation negligible. Moreover, to cater β variation to temperature, the constant voltage bandgap reference is replaced by a PTAT voltage bandgap reference circuit. Since device MN3 is in saturation, the current in MN3 is equal to (17). From (17), V_{GS} of MN3 is calculated through (18) and (19).

$$I_{MN3} = \frac{1}{2}\beta_{MN3}(V_{GSMN3} - V_{thMN3})^2 \quad (17)$$

$$\sqrt{\frac{2I_{MN3}}{\beta_{MN3}}} = V_{GSMN3} - V_{thMN3} \quad (18)$$

$$V_{GSMN3} = \sqrt{\frac{2I_{MN3}}{\beta_{MN3}}} + V_{thMN3} \quad (19)$$

$$V_{GSMN3} \approx V_{thMN3}. \quad (20)$$

Since transistor MN3 is a device with a large W/L ratio biased by a small current source, (19) can be simplified into (20). Therefore, V_{GSR} can be solved as follows:

$$V_{GSR} \approx V_{GSMN3} + V_{DSR} \quad (21)$$

$$V_{GSR} \approx V_{thMN3} + V_{DSR}. \quad (22)$$

Transistor MR is in linear region; therefore, the current through MR is as shown in (23). Substituting, (22) to (23) gives the PVT insensitive current (24).

$$I_{MR} = \frac{1}{2}\beta_R[2(V_{GSR} - V_{thMR})V_{DSR} - V_{DSR}^2] \quad (23)$$

$$I_{MR} = \frac{1}{2}\beta_R[2(V_{DSR} + V_{thMN3} - V_{thMR})V_{DSR} - V_{DSR}^2] = I_{ref}. \quad (24)$$

Since MR and MN3 are both NMOS, it can be assumed that they have the same V_{th} variation. With this, process variation in linear resistor MOS is canceled. Moreover, since V_{DSR} is forced by the OP to be equal to PTAT V_{ref}, the increasing

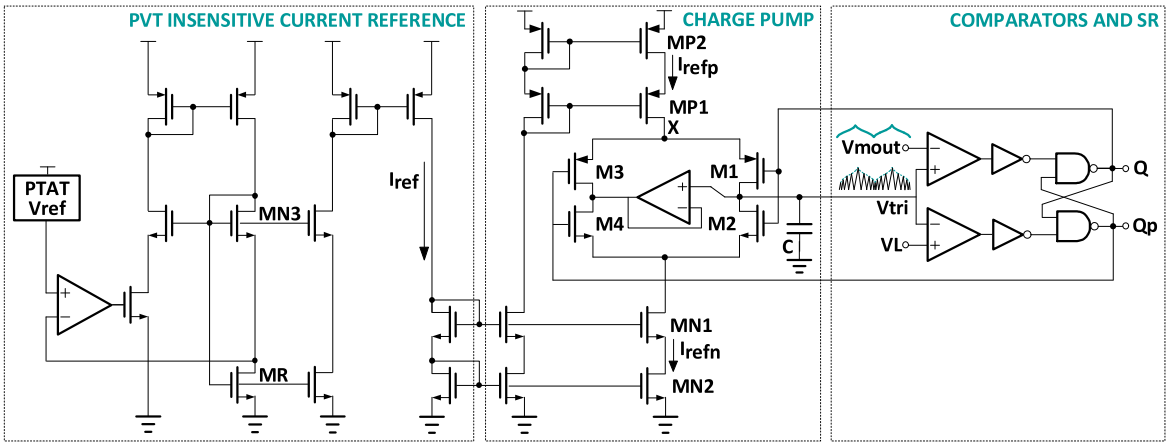

Fig. 5. PVT insensitive oscillator circuit.

V_{ref} as temperature increases compensates the decreasing β. In addition, since there is no V_{DD} term in (24), the derived current can be said to be supply independent. Thus, (24) shows a PVT insensitive current.

1) Charge Pump: Transistors MP1, MP2, MN1, and MN2 of the charge pump, mirrors the PVT insensitive current from the proposed VtoI converter. When Q = 0, M1 charges the capacitor at V_{tri}. When Q = 1, M2 discharges the capacitor. Switching transistors M3 and M4 are added to provide an alternative path of the mirrored current I_{refp} during capacitor discharging time. When Q = 1, I_{refp} flows thru the ground thru the OP, maintaining the voltage at node X. Therefore, MP1 and MP2 always operate in the saturation region, mirroring exact current at all times.

2) Comparators and SR Latch: The comparators used are PMOS and NMOS input single-stage differential comparators which compares V_{tri} with V_{mout} and V_L, respectively. When V_{tri} is higher than V_{mout}, Q is set to 1 and when V_{tri} is lower than V_L, Q is reset to 0. Recall that V_{mout} is the output of the multistep PWL modulator. Traditionally, it is just a constant V_H, but here V_{mout} is designed to vary between V_{H2} and V_{L2}. This varying amplitude of the triangular wave will vary the output frequency of the crystal-less oscillator. The delays of the comparators and the NAND gates are designed to be small enough not to cause additional delay to the delay designed to be mainly dominated by the capacitor at the charge pump.

3) Triangular Versus PWL Modulated Oscillator: The cycle time of an oscillator can be calculated from the sum of its charging and discharging time shown in (25). Since charging and discharging currents are equal, oscillator frequency Q_p can be simplified into (26). The oscillation frequency of [8] is maximum when V_{mout} is at its lowest which is V_{L2}. While it is oscillation frequency is minimum when V_{mout} is at its highest which is V_{H2}. These equations are shown in (27) and (28), respectively. The difference of which gives the frequency variation, ΔQ_p, shown in (29). On the other hand, the cycle time of the modulator shown in (11) can be rewritten into its equivalent modulation frequency as shown in (30). Substituting (29) and (30) to (1), mf of a triangular wave modulated oscillator can be written in (31). With PWL onion wave, f_m in (30) is further decreased by simply changing the frequency at different voltage levels in between

TABLE II
MODULATED FREQUENCY USING ICGM AT DIFFERENT CORNERS

	TT	SS	FF
Resistor	R	R+0.15R	R-0.15R
Capacitor	C	C+0.15C	C-0.15C
Current	I=V/R	I=V/1.15R=0.87I	I=V/0.85R=1.18I
Frequency	F=I/CV	F=0.87I/1.15CV =0.76F	F=1.18I/0.85CV =1.39F
fsw	2.5MHz	1.9MHz	3.47MHz
fmodulated	2.3 to2.7 MHz	1.7 to 2.1MHz	3.27 to 3.67MHz

V_{H2} and V_{L2}. From (13), the cycle time of the PWL onion wave modulator can be written into its equivalent modulation frequency in (32).

$$t = t_c + t_d = \frac{C \cdot \Delta V}{I_{charge}} + \frac{C \cdot \Delta V}{I_{discharge}} \tag{25}$$

$$Q_p = \frac{1}{t} = \frac{I}{2C \cdot \Delta V} = \frac{I}{2C \cdot (V_{mout} - V_L)} \tag{26}$$

$$Q_{p,max} = \frac{I}{2C \cdot (V_{L2} - V_L)} \tag{27}$$

$$Q_{p,min} = \frac{I}{2C \cdot (V_{H2} - V_L)} \tag{28}$$

$$\Delta Q_p = \frac{Q_{p,min} + Q_{p,max}}{2} = \frac{I}{4C}\left[\frac{V_{H2} - V_{L2}}{(V_{H2} - V_L)(V_{L2} - V_L)}\right] \tag{29}$$

$$f_m = \frac{C_1 \cdot Q_p \cdot (V_{H1} \cdot V_{L1})}{C_2 \cdot (V_{H2} - V_{L2}) \cdot (V_{L1} + V_{H1})} \tag{30}$$

$$m_f = \frac{I}{4C}\left[\frac{(V_{H2} - V_{L2})^2}{(V_{H2} - V_L)(V_{L2} - V_L)}\right] \cdot \left[\frac{C_2 \cdot (V_{H1} + V_{L1})}{C_1 \cdot Q_p \cdot (V_{H1} \cdot V_{L1})}\right]. \tag{31}$$

Since the sum of the voltage levels in between V_{H2} and V_{L2} is simply V_{H2}-V_{L2} as shown in (33), (32) can be simplified into (34). Comparing (34) with (30), it can be concluded that the f_m of PWL onion wave is lower than that of the triangular wave. Therefore, mf of a PWL onion wave shown in (35) is higher than

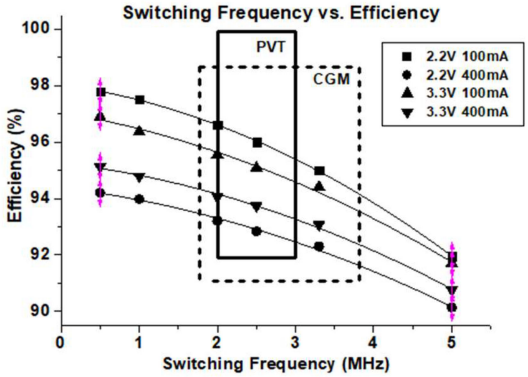

Fig. 6. Efficiency of the buck converter at different switching frequencies.

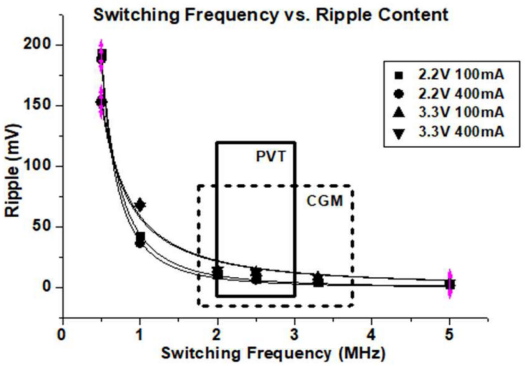

Fig. 7. Output ripple of the buck converter at different switching frequencies.

the mf of the triangular wave in (31). Thus, peak reduction is further improved.

III. Experimental Results

PWL modulation allows the switching frequency to deviate from its center frequency to reduce the EMI peak. However, with process variations, switching frequency may deviate more than desired which affects the efficiency. In this article, possible frequency deviation due to process variations is calculated beforehand. Tables II and III present the modulated frequency when process variations of different devices are considered.

Table II presents the fsw when CGM current is used in the oscillator circuit. At the TT corner, where R and C are as designed, an ideal current I and frequency F are achieved. However, at SS corner, the resistor and capacitor increased by $+15\%$. Thereby, I is reduced to 0.87I, in effect, F becomes 0.76

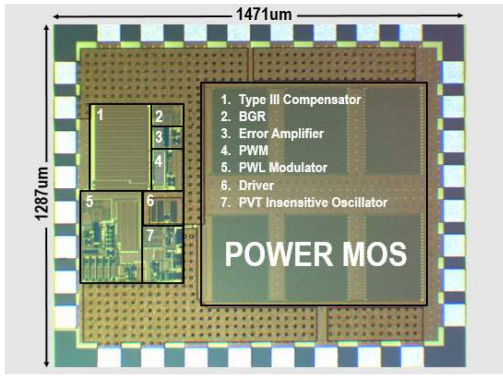

Fig. 8. Proposed buck converter chip micrograph.

TABLE III
Modulated Frequency Using IPVT at Different Corners

	TT	SS	FF
Resistor	R	R+0.06R	R-0.06R
Capacitor	C	C+0.04C	C-0.04C
Current	I=V/R	I=V/1.06R=0.94I	I=V/0.94R=1.06I
Frequency	F=I/CV	F=0.94I/1.04CV =0.90F	F=1.06I/0.96CV =1.10F
fsw	2.5MHz	2.25MHz	2.75MHz
fmodulated	2.3 to 2.7MHz	2.05 to 2.45MHz	2.55 to 2.95MHz

F. In addition, at FF corner, R and C decreased by -15%. Thus, I is increased to 1.18I, making F increase to 1.39F. Considering fsw of 2.5MHz, which is allowed to be modulated from 2.3 to 2.7 MHz, at SS corner, the modulated frequency can go as low as 1.7 to 2.1 MHz. While at FF corner, the modulated frequency can go as high as 3.27 to 3.67 MHz.

This wide frequency deviation can cause the serious effects on efficiency. Thus, with the use of PVT insensitive current at the oscillator, this deviation is minimized as shown in Table III. Using PVT insensitive current in the oscillator circuit where the resistor is replaced by a linear MOS resistor MR and cascade MOS MN3, resistor variation is reduced to $+6\%$ at SS corner. Thus, I is reduced to 0.94I. Also, the use of NMOSCAP rather than MIMCAP, reduced the C variation to $+4\%$, allowing frequency F to reduce to 0.9F. While at FF corner, the -6% variation of R causes I to increase to 1.06I and the -4% variation of C causes the increase of F to 1.1F. In effect, modulated frequency using PVT insensitive current at the oscillator may have frequencies of 2.05 to 2.95 MHz only, as opposed to 1.7 to 3.67 MHz.

The simulated buck converter efficiency at different frequencies is shown in Fig. 6. Since using CGM current results in

$$f_m = \frac{C_1 \cdot Q_p \cdot (V_{H1} \cdot V_{L1})}{C_2\left[(V_B - V_{L2}) + 2(V_D - V_B) + 4(V_C - V_D) + 2(V_A - V_C) + (V_{H2} - V_A)\right] \cdot (V_{H1} + V_{L1})} \tag{32}$$

$$V_{H2} - V_{L2} = (V_B - V_{L2}) + (V_D - V_B) + (V_C - V_D) + (V_A - V_C) + (V_{H2} - V_A) \tag{33}$$

$$f_m = \frac{C_1 \cdot Q_p \cdot (V_{H1} \cdot V_{L1})}{C_2\left[(V_{H2} - V_{L2}) + (V_D - V_B) + 3(V_C - V_D) + (V_A - V_C)\right] \cdot (V_{H1} + V_{L1})} \tag{34}$$

$$m_f = \frac{I}{4C}\left[\frac{(V_{H2} - V_{L2})^2}{(V_{H2} - V_L)(V_{L2} - V_L)}\right] \cdot \left[\frac{C_2\left[(V_D - V_B) + 3(V_C - V_D) + (V_A - V_C)\right] \cdot (V_{H1} + V_{L1})}{C_1 \cdot Q_p \cdot (V_{H1} \cdot V_{L1})}\right] \tag{35}$$

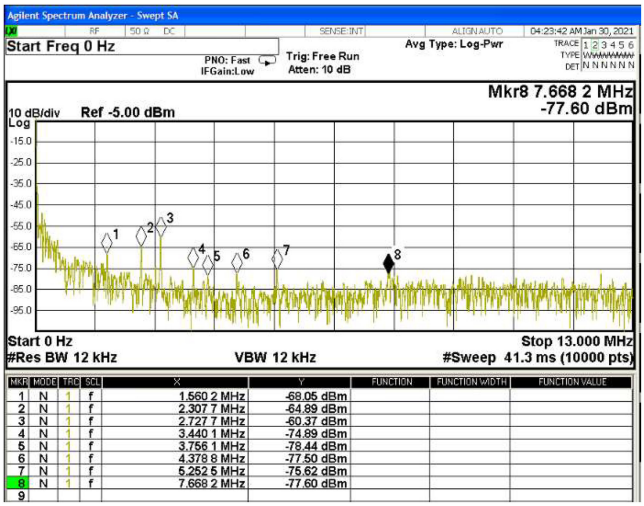

Fig. 9. Measured output spectrum of the buck converter.

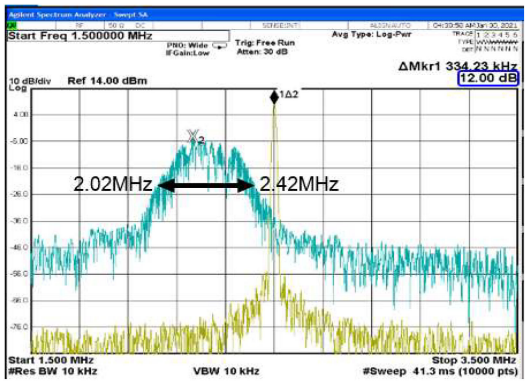

Fig. 10. Measured output spectrum of PWL modulated oscillator.

a wider frequency range, if the converter operates at these higher frequencies, efficiency may be degraded significantly. This scenario is avoided using PVT insensitive current since its frequency range is narrowed. Moreover, in Fig. 7, the ripple content of the buck converter output at different frequencies is shown. At lower frequencies, ripple content goes higher. Since using CGM current allows even lower frequencies, the buck converter ripple output may also be higher than designed. This scenario is again avoided by using the PVT insensitive current, where allowed frequencies are narrower.

Fig. 8 shows the chip micrograph of the proposed buck converter which was fabricated using a 0.18 μm CMOS process. The overall area of the chip is 1287 $\times$ 1471 μm^2. The chip is sealed onto a 32pin SB32 package.

With PWL, a peak emission of -60.37 dBm is measured at the output spectrum of the buck converter, as shown in Fig. 9. If just the output spectrums of the unmodulated oscillator and PWL onion wave modulated oscillator are compared, it can be observed that after PWL modulation, the peak emission is reduced by 12 dB, as shown in Fig. 10. Fig. 11 shows the worst-case measured output voltage of the buck converter which is 1.694 V and the largest Vpp ripple content which is 43.4 mV when V_{in} is 2.2 V and output load current is 100 mA. Fig. 12 shows the efficiency of the buck converter at different input voltages and

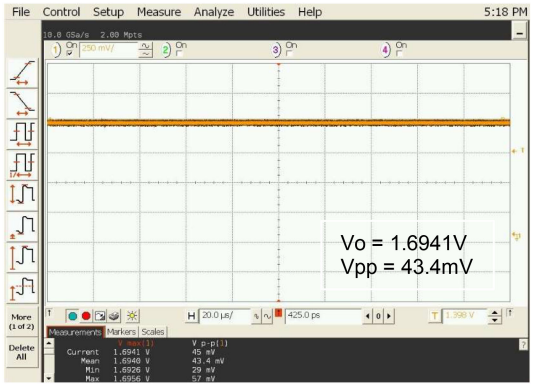

Fig. 11. Measured output voltage and ripple of buck converter.

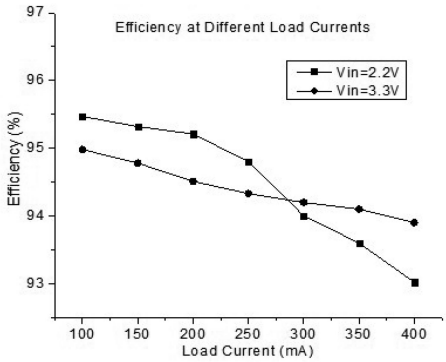

Fig. 12. Efficiency of the buck converter at different load current.

load currents of 100 to 400 mA. These measurements coincide with the simulated efficiency in Fig. 6.

Table IV presents the performance comparison table. With regards to the main objective of this work, which is efficiency, this work was able to achieve efficiency as high as 95.4%. Moreover, assuming that other references display their highest efficiency, it can be seen that even the lowest efficiency of this work, which is 93%, is even higher than the highest efficiency of other publications. As for the peak noise, [6] has lower peak noise because its switching frequency is spread as wide as 2.26 MHz whereas this work is only spread by 0.4 MHz. Also, for architectures with EMI reduction, [2] and [5] were able to measure lower ripple because their operating frequencies are higher and their output capacitors are bigger.

IV. Conclusion

A buck converter with high-efficiency and low EMI peak is successfully implemented in this article. With the introduction of a new and simple PWL onion wave modulator, the EMI peak is reduced further as compared to the triangular wave modulator. Moreover, the use of a new and simple PVT insensitive current generator in the oscillator circuit ensures that switching frequencies stays within desired range to maintain high-efficiency and low ripple content.

MOS resistor and NMOSCAP at the oscillator allow $\pm 10\%$ frequency variation only, whereas, with CGM current, frequency variation can reach to -24% to $+39\%$. This wide range of

TABLE IV
PERFORMANCE COMPARISON TABLE

Reference	[2] TCASII	[3] TPE	[5] TIE	[6] VLSI	[12] JSSC	[13] TPE	[14] JSSC	[15] JSSC	This work
Year	2019	2017	2018	2016	2011	2018	2015	2019	2021
Technology	0.18μ	0.13μ	0.35μ	0.35μ	0.045μ	0.055μ	0.18μ	0.065μ	0.18μ
Efficiency(%)	88.2	92.4	91.6	88.5	87.4	91.5	94	94.9	93-95.4
Fsw(MHz)	8.1-11	2-3	5	0.3-2.56	2	2	10-25	10	2.0-2.4
ΔFsw (MHz)	2.9	1.0	Not shown	2.26	N/A	N/A	N/A	N/A	0.4
Vi (V)	2.8-4.2	2.2-3.3	3.3-3.6	3.6-5	2.8-4.2	1.5-3	1.8	1.8	2.2-3.3
Vo (V)	1.3-2.2	1.7	1-2.5	1-3	0.4-1.2	1.2	0.6-1.5	0.15-1.69	1.7
Io (mA)	40-200	0.01-20	50-600	30-500	0.02-100	1-10	100-600	100-600	100-400
EMI Comp	SS	SSCG	CTDSM	DSM	None	None	None	None	PWL
L/C (uH/nF)	1/1	3/3	4.7/10	4.7/4.7	10/2	3/3	0.22/4.7	0.22/4.7	1.7/0.68
Ripple (mV)	19	N/A	<40	62	20	20	3.5	N/A	43.4
Peak Noise (dBm)	-39	-57.55	-67.5	-64	N/A	N/A	N/A	N/A	-60.37
Chip Area (mm2)	Not shown	Not shown	2.25	2.209	2.25	Not shown	5.0	2.118	1.893

frequencies can lead to higher ripple content at lower frequencies and lower efficiency at higher frequencies. This problem was eliminated using PVT insensitive current to narrow the frequency range. Consequently, this maintains ripple content as well as efficiency.

The proposed buck converter chip is implemented using a 0.18 μm CMOS process with an overall area of 1287 $\times$ 1471 μm^2. It accepts input voltages within the range of 2.2 to 3.3 V and outputs 1.7 V. At a switching frequency of 2.0 to 2.4 MHz, its lowest efficiency is 93% with a peak noise of -60.37 dBm and output ripple of 43.4 mV. Moreover, since it is primarily designed for IoT devices, the design of the type III compensator to be on-chip and the small off-chip components, such as 1.7 μH inductor and 0.68 μF capacitor, are advantageous.

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