Design and Multiobjective Optimization of an Auxiliary Wireless Power Transfer Converter in Medium-Voltage Modular Conversion Systems

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***Abstract*—This article proposes an optimized design for a wireless power transfer converter serving as an auxiliary power supply in a medium-voltage, high $\mathrm{d}v/\mathrm{d}t$ modular conversion system. A *CLLC-CL* circuit topology is implemented to generate a load-independent output voltage with a coupling-coefficient-independent resonant frequency. The output voltage of the circuit can be tuned by changing one pair of resonant *LC* parameters, which decouples the circuit gain from the coil design. Essential parameters of coil and magnet are extracted analytically or numerically to avoid time-consuming 3-D finite element analysis simulations for the subsequent optimization. After the design of the circuit and coil, a multiobjective optimization is carried out with objectives being efficiency, isolation capacitance, and insulation rating of the converter. Finally, experiments demonstrate a 48- to 48-V dc–dc converter with 100 W output power, 92.78% efficiency, 2.78 pF isolation capacitance, and 27 kV insulation rating to validate the optimization result.**

***Index Terms*—Auxiliary power supply (APS), magnetics, multiobjective optimization, resonant converter, wireless power transfer (WPT).**

Nomenclature

V_{in}	Converter input voltage.
V_{o}	Converter output voltage.
v_{AB}	Input voltage of the primary side resonant tank.
i_1	Primary side coil current.
i_{const}	Secondary side coil current.
C_1	Primary side series resonant capacitor.
C_2	Resonant capacitor for reactive power compensation.
C_{r}	Resonant capacitor for output voltage tuning.
L_{r}	Resonant inductor for output voltage tuning.
L_{M}	Mutual inductance of the coil pair.
v_{OP}	Input voltage of the diode bridge.
r_{i}	Inner radius of the coil.
r_{o}	Outer radius of the coil.
r_{w}	Radius of the coil winding.
d	Distance between two coils.
d_{f}	Distance between one coil and its adjacent ferrite.
E_{max}	Maximum electric field around the coil.
V_{max}	Maximum partial-discharge free insulation voltage.
C_{p}	Isolation capacitance of the coil pair.
N	Turn number the coil.
k	Coupling coefficient of the coil pair.
η	Efficiency of the WPT converter.
N_{s}	Litz wire strand number.

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I. Introduction

MEDIUM-VOLTAGE (MV) power converters are widely used in areas of traction system, industrial motor drive, and power distribution system of microgrid, thanks to the superior characteristics of wideband-gap devices such as silicon-carbide (SiC) MOSFETs [1]–[5]. Auxiliary power supply (APS) plays an essential role in providing stable and reliable power for control, driving, and sensing circuitry, which guarantees the normal operation of main power converter. In an MV modular conversion system, of which the basic power cell units are operating at different MV potentials, the APS can be fed either from an external source with a reference ground connected to the earth, or from the local MV dc-link inside each power cell. For an APS powered by the local dc-link, a high-step-down converter is required such as different flyback converters [6], [7] or switched-capacitor converters [8], [9]. In this case, the auxiliary system is typically disabled when the dc-link voltage is lower than a wake-up voltage, e.g., during the start-up or fault conditions. However, if fed from an external source with a grounded reference point, the APS ensures reliable power for the gate drivers and controllers regardless of the dc-link voltage status, although the required insulation rating of an externally fed APS increases with the number of stacked power cells. Admittedly, an externally fed APS may not be practical in applications like HVdc because of the limitation of insulation capability; still,

it is manageable and beneficial for MV applications that range around 1–35 kV [10], [11].

To design an externally fed APS, the most critical part is to build the galvanic isolation between the earth and power cells. The galvanic isolation barrier can be established by optical coupling, mechanical coupling, or magnetoelectric coupling, etc. The power-over-fiber (PoF) technology provides a solution with theoretically infinite insulation strength and zero coupling capacitance [12], [13]. However, the efficiency, power rating, and cost performance are all quite limited at this moment. The isolation can also be provided through mechanical coupling using a piezoelectric transformer [14], [15]. However, the system operating frequency (usually in the range of tens of kilohertz) is determined by piezoelectric material per se and limits the converter power density. For isolated dc–dc converters, most of the designs are still utilizing magnetoelectric coupling to provide galvanic isolation. One typical externally fed APS uses a traditional type of transformer with a ferrite core and cable winding to provide galvanic isolation between primary and secondary side [16]–[19]. To drive multiple loads with one primary side, a current transformer with multiple secondary sides is explored to reduce system complexity [20]–[24]. For the transformer windings, PCB-based windings are used to replace handmade windings for higher power density and consistent and reliable manufacturing [25]–[29]. Nevertheless, the physical connection between winding and core complicates the mechanical design and impairs hot-swap configurations.

On the other hand, wireless power transfer (WPT) converters have been explored and implemented in the APS system by leveraging their inherent creepage-free feature and flexible mechanical structure. Marxgut *et al.* [30] proposed a PCB-embedded coil solution to power gate drivers. The design in [31] gave a highly compact example by utilizing ferrite material as a shielding shell. Similarly, [32] and [33] proposed to use WPT converters as APS for modular converters with insulation capability up to 90 kV. WPT with one transmitter and multiple receivers as a gate driver power supply is proposed in a three-phase system [34], although the total efficiency is limited due to the low coupling coefficient. Recently, very high-frequency APS with PCB winding and coreless transformer also provides a competitive solution to build APS with high insulation capability [35]–[38], less weight, and low system complexity. Nguyen *et al.* [39] proposed a special asymmetrical coil structure to minimize the coupling capacitance. However, the PCB windings and shielding-free design make it hard to reach a power rating in the hundred-watt range and the EMI to the system remains a concern. In summary, while that WPT converters serve as an APS with various insulation requirements has been demonstrated in the literature, systematic design and multiobjective optimization for a WPT converter with magnetic shielding in MV APS applications are still missing.

The concerned exemplary converter configuration in this article is a modular multilevel converter (MMC) with four power cells in series per arm working in a switching-cycle control (SCC) mode [40] and an integrated-capacitor-blocked-transistor (ICBT) mode [41] (see Fig. 1). As opposed to the conventional

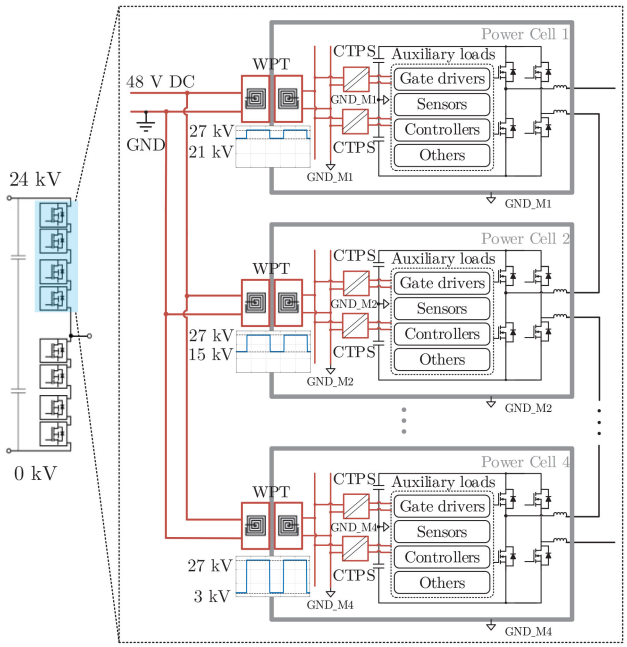

Fig. 1. System configurations of WPT converters for a MMC with four power cells in series.

MMC controls, both SCC and ICBT allow extremely low arm inductance and enable switching-cycle capacitor voltage balancing. Each power cell, as a modular design unit, contains a WPT converter, multiple current-transformer-based power supplies (CTPS) [22], a SiC-MOSFET full-bridge, dc-link capacitors, load inductors, and different auxiliary loads. Auxiliary loads include gate drivers, sensors, and controllers, etc. The rated dc-link voltage of each cell is 6 kV, with 10 kV SiC MOSFET module in use. Therefore, the maximum voltage difference between the receiver coil and the grounded transmitter coil for the upper arm is 27 kV, as indicated in Fig. 1. The voltage across the APS also contains switching components, whose duty cycle and equivalent frequency are associated with the MMC's operation mode. With this two-stage APS solution [42], the first-stage WPT primarily deals with the high insulation voltage without feedback control, while the second-stage CTPS focuses on voltage regulation and protection.

Pursuing a partial-discharge-free galvanic isolation, insulation design criterion and electric field distribution under different coil geometries have been analyzed, compared, and validated [11]. A comprehensive insulation design including the influence of ferrite shielding layer has also been addressed previously [11]. Therefore, the insulation design part is summarized concisely with only important conclusions listed in this article. The primary purpose of this article is to present the complete procedure including design, multiobjective optimization, and test of the auxiliary WPT converter in the MV system, and its main contributions include the following aspects. First, a *CLLC-CL* topology is analyzed, unveiling its advantages including load independent output voltage, reactive power compensation, and load-/input-independent soft-switching characteristics. Second, analytical, numerical, and empirical equations are derived and

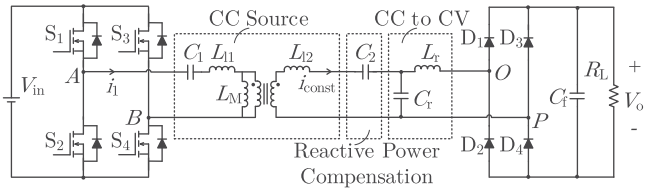

Fig. 2. *CLLC-CL* topology for wireless power transfer converter.

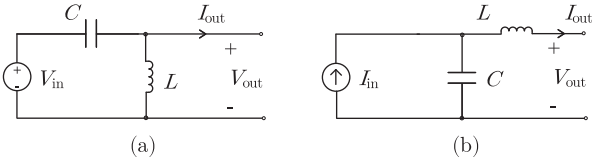

Fig. 3. LC resonant tanks generating (a) CC source and (b) CV source.

summarized for parameter extraction of the coil without the FEA simulation. Third, the multiobjective optimization procedure is implemented providing design guidelines for WPT converter with high efficiency, low coupling capacitance, and high insulation capability simultaneously. The remaining sections of this article are organized as follows. Section II presents the analysis of the *CLLC-CL* topology. Sections III and IV present the analysis and parameter extraction for the coil pair with and without ferrite shielding respectively. In Section V, a multiobjective optimization methodology has been done to explore the WPT converter performance. Section VI presents the experimental validations including circuit operation test, insulation test, and other measurements. Finally, Section VII concludes this article.

II. Circuit Topology

As an APS for the MMC, the circuit topology of WPT should provide the following characteristics. First, a load-independent gain is necessary. The auxiliary load power may vary because of different operation modes of the power cell, different operating temperatures, or even different configurations of controllers and sensors. Adding a closed-loop control for WPT will not only meet difficulties for the feedback signal isolation with MV rating but also can be interfered with the high $\mathrm{d}v/\mathrm{d}t$ environment. Therefore, it is necessary to have an open-loop design, relying on the topology impedance matching, for a constant output voltage. Second, the excessive reactive power of the WPT converter should be compensated to reduce conduction loss, while a proper amount of inductive current should be left to achieve zero-voltage-switching (ZVS) for MOSFETs reducing the switching loss. Third, the converter gain (or the output voltage) should be tunable by the circuit components alone for any given shape and size of the coil. As mentioned before, the coil design of WPT is complicated since many aspects like coupling coefficient, coupling capacitance, and electric field intensity under high voltage need to be considered simultaneously. To simplify the problem, the circuit gain of the WPT should be decoupled from the coil design so that the circuit parameters can be designed after the optimization of the coil instead of being considered at the same time. Last but not the least, because of the nonideality of the coil pair such as the alignment mismatch and distance tolerance, a coupling-independent resonant frequency can increase the system consistency and reduce the effort of retuning primary side resonant capacitor. In this section, parameters with a hat mark represents its peak value, and the bold letter represents complex scalar variables. Important parameters are all labeled in Fig. 2.

A. CLLC-CL Topology

The *CLLC-CL* topology (see Fig. 2) is a mirrored implementation of the *LCCL-LC* topology [43]. While the latter converts a constant-voltage (CV) source to a constant-current (CC) source, *CLLC-CL* is implemented in this work to ensure that the WPT's output generates a CV source. For a conventional series–series *CLLC* resonant circuit, capacitor C_1 resonates with the self-inductance of the primary side coil L_1 (note $L_1 = L_{l1} + L_M$), and the current through the secondary inductor L_{l2} behaves as a CC source. The capacitor C_2 is used to adjust the load impedance of the full-bridge inverter to reduce reactive power and achieve ZVS for primary-side MOSFETs. The $C_r L_r$ pair appended to the *CLLC* circuit can convert the CC source to a load-independent CV source. Detailed analysis is as follows.

1) CV & CC Source: A pair of LC components can switch the source type between CV source and CC source [44]. From CV to CC source as shown in Fig. 3(a)

$$I_{out} = j\omega C \cdot V_{in} - \left(\frac{1}{j\omega L} + j\omega C\right) \cdot V_{out} \tag{1}$$

where

$$\omega = \frac{1}{\sqrt{LC}}. \tag{2}$$

When LC resonate, the output is a CC source that

$$I_{out} = j\omega C \cdot V_{in} = -\frac{1}{j\omega L} \cdot V_{in}\,. \tag{3}$$

As a duality shown in Fig. 3(b), from CV to CC

$$V_{out} = \frac{1}{j\omega C} \cdot I_{in} - \left(j\omega L + \frac{1}{j\omega C}\right) \cdot I_{out}\,. \tag{4}$$

When LC resonate, the output is a CV source, so

$$V_{out} = \frac{1}{j\omega C} \cdot I_{in} = -j\omega L \cdot I_{in}\,. \tag{5}$$

2) Series Compensation as a CC Source: As shown in Fig. 2, the primary side C_1, L_{l1}, and L_M together form a CC source with same topology in Fig. 3(a), where the angular resonant frequency

$$\omega_s = \frac{1}{\sqrt{(L_{l1} + L_M)\, C_1}} = \frac{1}{\sqrt{L_1 C_1}}. \tag{6}$$

The amplitude of the fundamental output constant current wave $\widehat{i}_{const}$ should be

$$\widehat{i}_{const} = \frac{4}{\pi} \frac{V_{in}}{\omega_s L_M}. \tag{7}$$

Accordingly, (7) is always true when C_1 is in resonance with L_1. Inductance L_1 is the self-inductance of the primary side coil which is not a function of the coupling coefficient k. Unlike the case when series capacitance is in resonance with leakage inductance, C_1 does not need to be readjusted when k is changed.

3) L_rC_r Resonant Tank: In Fig. 2, the C_rL_r resonant tank can transfer the CC source to CV output. Based on the circuit diagram of Fig. 3(b), under the resonant angular frequency

$$\omega_{\mathrm{s}} = \frac{1}{\sqrt{L_{\mathrm{r}}C_{\mathrm{r}}}} \tag{8}$$

the output voltage amplitude is

$$\widehat{v}_{\mathrm{OP}} = \widehat{i}_{\mathrm{const}} \cdot \omega_{\mathrm{s}} L_{\mathrm{r}} = \widehat{i}_{\mathrm{const}} \cdot \frac{1}{\omega_{\mathrm{s}} C_{\mathrm{r}}} \tag{9}$$

$$V_{\mathrm{o}} = \frac{L_{\mathrm{r}}}{L_{\mathrm{M}}} V_{\mathrm{in}} \,. \tag{10}$$

Equation (10) is always true when (6) and (8) are met. Therefore, V_{o} can be tuned by changing L_{r} and C_{r} pair without changing the coil structure. This characteristic decouples the optimization of the coil from the gain of the circuit which simplifies the design and provides additional flexibility for changing the output voltage of the WPT converter.

B. Reactive Power Compensation and Soft-Switching

Besides the CV output, the load impedance of the full-bridge inverter should be adjusted to reduce the reactive power thus increase the system efficiency. At the same time, some amount of inductive power is required so that the primary side switching current can help charge and discharge the output capacitance of the MOSFETs to achieve ZVS. The amount of inductive current should be determined by the resonant current, dead time, and output capacitance of MOSFET. With the fundamental frequency approximation, the source voltage of the resonant tank

$$v_{\mathrm{AB}} = \frac{4V_{\mathrm{in}}}{\pi} \sum_{n=1,3,5,\ldots} \frac{1}{n} \sin\left(n\omega t\right) \approx \frac{4V_{\mathrm{in}}}{\pi} \sin\left(\omega t\right) \,. \tag{11}$$

The load resistor can be reflected before the diode bridge as

$$R_{\mathrm{eq}} = \frac{8}{\pi^2} R_{\mathrm{L}} \,. \tag{12}$$

Therefore, the input current

$$\begin{aligned} \boldsymbol{I_1} &= \boldsymbol{V}_{\mathrm{AB}} / Z_{\mathrm{eq}} = \boldsymbol{V}_{\mathrm{AB}} \cdot Y_{\mathrm{eq}} \\ &= \boldsymbol{V}_{\mathrm{AB}} \cdot \left(\frac{{L_{\mathrm{r}}}^2}{{L_{\mathrm{M}}}^2 R_{\mathrm{eq}}} + j \cdot \frac{C_2\omega^2 \left(L_{\mathrm{l2}} + L_{\mathrm{M}} - L_{\mathrm{r}}\right) - 1}{C_2 {L_{\mathrm{M}}}^2 \omega^3} \right) \\ &= \boldsymbol{V}_{\mathrm{AB}} \cdot A \angle \varphi \end{aligned} \tag{13}$$

where

$$\begin{cases} A = \sqrt{\left(\dfrac{{L_{\mathrm{r}}}^2}{{L_{\mathrm{M}}}^2 R_{\mathrm{eq}}} \right)^2 + \left(\dfrac{C_2\omega^2 \left(L_{\mathrm{l2}} + L_{\mathrm{M}} - L_{\mathrm{r}}\right) - 1}{C_2 {L_{\mathrm{M}}}^2 \omega^3} \right)^2} \\ \varphi = \arctan\left(\dfrac{\left[C_2\omega^2 \left(L_{\mathrm{l2}} + L_{\mathrm{M}} - L_{\mathrm{r}}\right) - 1\right] R_{\mathrm{eq}}}{C_2 L_{\mathrm{r}}^2 \omega^3} \right) \,. \end{cases} \tag{14}$$

Therefore, the turn-OFF current of the switch is

$$I_{\mathrm{off}} = \frac{4V_{\mathrm{in}}A}{\pi} \sin(\pi + \varphi) \,. \tag{15}$$

To simplify the representation, assume

$$\begin{cases} G = C_2\omega^2 \left(L_{\mathrm{l2}} + L_{\mathrm{M}} - L_{\mathrm{r}}\right) - 1 \\ H = C_2 {L_{\mathrm{M}}}^2 \omega^3 \,. \end{cases} \tag{16}$$

Then

$$I_{\mathrm{off}} = \frac{4V_{\mathrm{in}}A}{\pi} \sin(\pi + \varphi) = -\frac{4V_{\mathrm{in}}}{\pi} \frac{G}{H} \,. \tag{17}$$

Thus

$$C_2 = \frac{4V_{\mathrm{in}}}{\pi I_{\mathrm{off}} {L_{\mathrm{M}}}^2 \omega^3 + 4V_{\mathrm{in}} \left(L_{\mathrm{l2}} + L_{\mathrm{M}} - L_{\mathrm{r}}\right) \omega^2} \,. \tag{18}$$

Equation (17) proves one of the critical advantages of this topology, that is the turn-OFF current of the MOSFET is not related to the load resistance. Once the coil inductance and resonant frequency are fixed, soft-switching can be achieved by tuning the capacitor C_2 according to the requirement turn-OFF current. In order to have ZVS operation of the full-bridge, turn-OFF current should be large enough to fully charge/discharge the MOSFET output capacitance C_{oss} during the dead time t_{d} that

$$I_{\mathrm{off}} \geq \frac{2Q_{\mathrm{oss}}}{t_{\mathrm{d}}} \approx \frac{2C_{\mathrm{oss}}V_{\mathrm{in}}}{t_{\mathrm{d}}} \,. \tag{19}$$

Combining (18) and (19) gives

$$C_2 = \frac{2t_{\mathrm{d}}}{\pi C_{\mathrm{oss}} {L_{\mathrm{r}}}^2 \omega^3 + 2t_{\mathrm{d}} \left(L_{\mathrm{l2}} + L_{\mathrm{M}} - L_{\mathrm{r}}\right) \omega^2} \tag{20}$$

which is neither a function of V_{in} nor R_{L}. As a brief summary, with the *CLLC-CL* topology, the WPT circuit can have a load-independent output voltage, a load-independent soft-switching design, and the output voltage can be tuned by circuit parameters alone with any given optimized coil.

III. Coil Design

With the designed *CLLC-CL* circuit topology, the next step is to analyze the coil of WPT extracting parameters like inductance, capacitance, and electric-field intensity for the later multiobjective optimization.

A. Coil Insulation Design

Detailed insulation design guidelines and considerations for the WPT coil have been presented in [11], for the conciseness of this article, only important conclusions are summarised in this section. First of all, for two common types of coil shape (see Fig. 4), the flat-spiral shape is selected because of its more evenly distributed electric field compared with the solenoid one (see Fig. 5). Moreover, the coils are selected to be symmetrical (same size and structure for primary and secondary side) which fully utilizes the space area to improve the high voltage insulation performance and simplifies the optimization procedure. Second, litz wire is used as the coil winding. Compared with hollow wire [32], [45], litz wire of the same winding radius has much lower ac resistance, better mechanical performance,

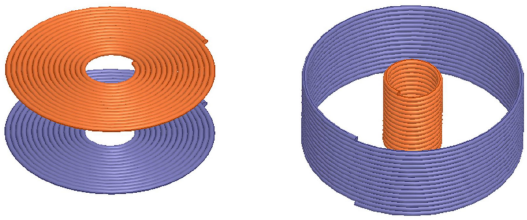

Fig. 4. Coil shape of flat spiral and solenoid.

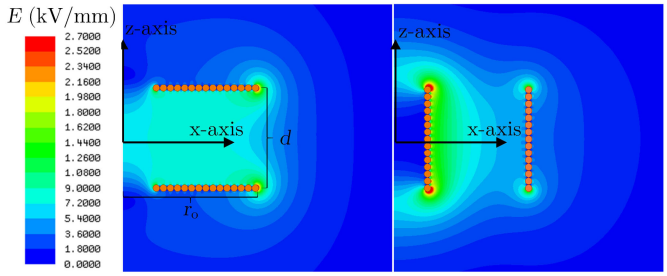

Fig. 5. E-field simulation result of coil with flat spiral and solenoid shape.

and is proved to have comparable insulation capability if the strand number is high [11]. Third, the maximum E-field intensity of the coil $E_{\max}$ is a parameter that should be included in the optimization process. As shown in Fig. 5, for a flat-spiral shape coil, the maximum E-field is near the edge of the coil. From FEA result and curve fitting, a derived numerical equation below can be used for $E_{\max}$ calculation

$$E_{\max} = 0.8 \cdot V_{\text{insu}} \cdot r_{\text{o}}^{-0.21} \cdot r_{w}^{-0.28} \cdot d^{-0.39}\,. \tag{21}$$

The insulation voltage between two coils V_{insu}, outer radius r_{o}, distance between coils d, and radius of the cable of each turn r_{w} will all affect the maximum electric field, where the unit of d, r_{o}, r_{w} are mm, the unit of V_{insu} is kV, and the unit of $E_{\max}$ is kV/mm. From the result, larger r_{o}, d, and r_{w} can help to reduce $E_{\max}$ thus increase the coil high voltage insulation capability. However, a larger size coil will lead to lower power density and higher isolation capacitance. Therefore, a multiobjective optimization will be done to determine the geometry of the coil.

B. Inductance and Isolation Capacitance of Coil

1) Inductance and Coupling Coefficient: The inductance of multiturn coil structure can be calculated from an equivalent lumped one-turn disk structure times the square of turn number N [46]. Analytical equations for flat spiral structure inductance [47], [48] are shown as follows:

$$L = L(r_{\text{i}}, r_{\text{o}}, N) = \frac{\mu_0 N^2}{(r_{\text{o}} - r_{\text{i}})^2} \int_0^{\pi} \int_{r_{\text{i}}}^{r_{\text{o}}} \int_{r_{\text{i}}}^{r_{\text{o}}} \frac{xy\cos\theta}{\sqrt{x^2 + y^2 - 2xy\cos\theta}} dx dy d\theta \tag{22}$$

$$M = M(r_{\text{i}}, r_{\text{o}}, N, d) = \frac{\mu_0 N^2}{(r_{\text{o}} - r_{\text{i}})^2} \int_0^{\pi} \int_{r_{\text{i}}}^{r_{\text{o}}} \int_{r_{\text{i}}}^{r_{\text{o}}} \frac{xy\cos\theta}{\sqrt{d^2 + x^2 + y^2 - 2xy\cos\theta}} dx dy d\theta \tag{23}$$

where μ_0 is the vacuum permeability, r_{i} is the inner radius, and N is the turn number. The triple integral calculation can be evaluated by the $integral3$ function in MATLAB numerically. Further analytical simplification of these multiple integrals can also be found in [49]. For a symmetric coil pair, the coupling coefficient

$$k = M/L\,. \tag{24}$$

2) Isolation Capacitance: For an ideal parallel plate capacitor, the capacitance can be calculated by

$$C_{\text{p}} = \varepsilon S/d \tag{25}$$

where S is the plate area, d is the distance between two plates, and ε is the dielectric permittivity. However, this equation is not accurate since it assumes that the electric charge density on the plates is uniform and neglects the fringing field of the edges. A numerical method with high accuracy of calculating isolation capacitance C_{p} between primary and secondary side coil for flat spiral structure has been proposed in [50] which requires discussion for different parameters. This article proposes a calculation equation for isolation capacitance for flat spiral structure as shown as follows:

$$C_p = \frac{5\varepsilon_0}{3\pi} \frac{\left(r_{\text{o}}^2 - r_{\text{i}}^2\right)^2}{X} \tag{26}$$

where

$$X = \int_0^{\pi} \int_{r_{\text{i}}}^{r_{\text{o}}} \int_{r_{\text{i}}}^{r_{\text{o}}} \frac{xy}{\sqrt{x^2 + y^2 - 2xy\cos\theta}} dx dy d\theta - \int_0^{\pi} \int_{r_{\text{i}}}^{r_{\text{o}}} \int_{r_{\text{i}}}^{r_{\text{o}}} \frac{xy}{\sqrt{d^2 + x^2 + y^2 - 2xy\cos\theta}} dx dy d\theta\,. \tag{27}$$

Fig. 6 shows the comparison of C_{p} result between Maxwell 3-D FEA simulation results and calculation results from (26) by sweeping different geometry parameters. The blue curves are calculation results from (26), and the red dots are FEA simulation results. From this figure, the equation can accurately present the isolation capacitance value. The capacitance drops when the distance between two coils is larger but the slope of the curve is decreasing which means keeping increasing distance will not help too much to reduce C_{p}. The capacitance increases when the coil outer radius increases which is similar to a normal planar capacitor. In addition, increasing inner radius can also reduce the C_{p}, but the effect is weak when $r_{\text{i}}/r_{\text{o}}$ is smaller than $1/3$.

C. Analysis of a Normalized Coil Pair

To analyze the effect of different coil parameters to the inductance and capacitance of the coil pair, coils with different

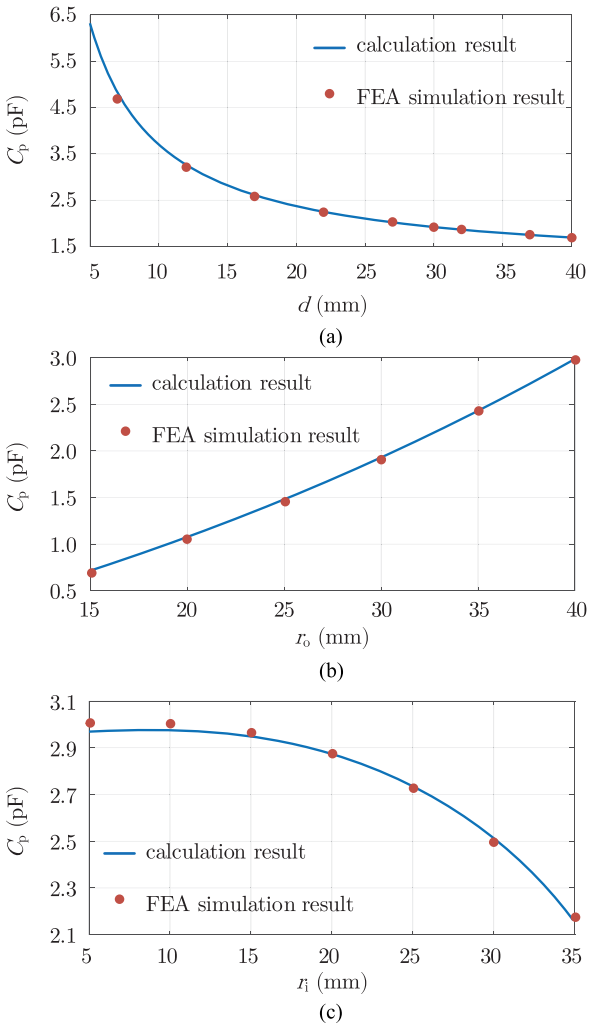

Fig. 6. Calculation and simulation results comparison of the isolation capacitance C_p when sweeping (a) distance d, (b) outer radius r_o, and (c) inner radius r_i. (a) $r_\mathrm{o} = 30\,\mathrm{mm}$, $r_\mathrm{i} = 10\,\mathrm{mm}$. (b) $r_\mathrm{i} = 10\,\mathrm{mm}$, $d = 30\,\mathrm{mm}$. (c) $r_\mathrm{o} = 40\,\mathrm{mm}$, $d = 30\,\mathrm{mm}$.

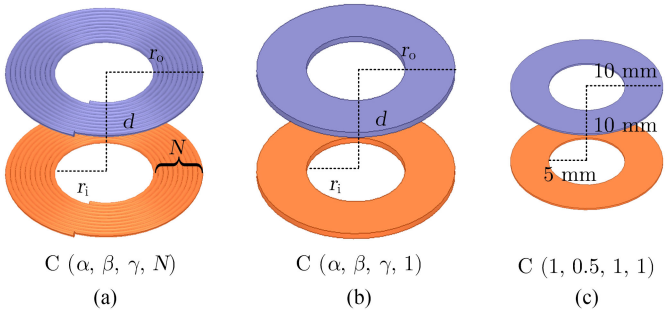

Fig. 7. Standardized presentation of the WPT coil pair. (a) Multiturn coil pair. (b) Single-turn coil pair. (c) Example coil pair with standardized form.

parameters are presented by a standardized form with dimensionless ratios $C(\alpha, \beta, \gamma, N)$ as shown in Fig. 7 where $\alpha = r_\mathrm{o}/d$, $\beta = r_\mathrm{i}/r_\mathrm{o}$, $\gamma = d/(10\,\mathrm{mm})$, and N is the turn number. First, parameters of the multiturn coil structure can be derived from the single turn disk structure. Second, γ is used to describe the size of the coil pair, where the reference distance value is set to

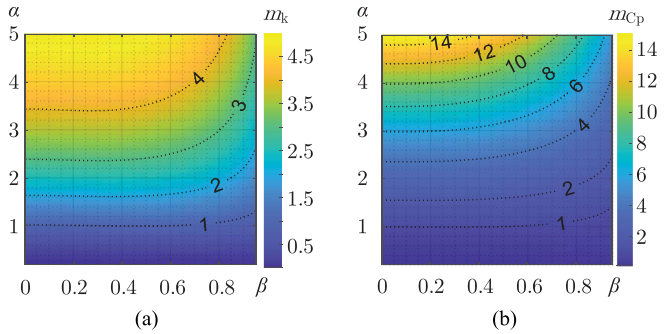

Fig. 8. (a) Correlation between coupling coefficient and coil shape. (b) Correlation between isolation capacitance and coil shape.

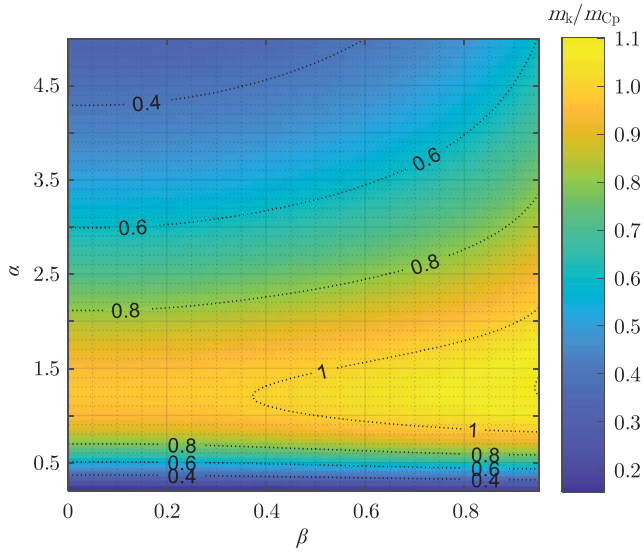

Fig. 9. Coil pair figure of merit under different geometries.

be 10 mm. From (22), (23), and (26), there is

$$\begin{cases} L_{C(\alpha,\beta,\gamma,N)} = \gamma N^2 \cdot L_{C(\alpha,\beta,1,1)} \\ M_{C(\alpha,\beta,\gamma,N)} = \gamma N^2 \cdot M_{C(\alpha,\beta,1,1)} \\ k_{C(\alpha,\beta,\gamma,N)} = k_{C(\alpha,\beta,1,1)} \\ C_{\mathrm{p},C(\alpha,\beta,\gamma,N)} = \gamma \cdot C_{\mathrm{p},C(\alpha,\beta,1,1)}. \end{cases} \tag{28}$$

Since the effect of turns number N, and size of coil γ can both be calculated through (28), only the characteristics of the normalized coil $C(\alpha, \beta, 1, 1)$ are required to be analyzed. The effect of coil shape (i.e., α and β) to k and C_p are shown in Fig. 8, where $m_\mathrm{k} = k_{C(\alpha,\beta,1,1)}/k_{C(1,0.5,1,1)}$, and $m_\mathrm{Cp} = C_{\mathrm{p},C(\alpha,\beta,1,1)}/C_{\mathrm{p},C(1,0.5,1,1)}$.

For coil design, higher coupling coefficient k and lower isolation capacitance C_p are required to increase system efficiency while reducing common mode current generated by high $\mathrm{d}v/\mathrm{d}t$. Therefore, a figure of merit $m_\mathrm{k}/m_\mathrm{Cp}$ is calculated to quantify the performance of the coil. From results shown in Fig. 9, the coil pair has the highest figure of merit, which means both high efficiency and low isolation capacitance, when the outer radius of the coil is similar to the distance between two coils (α around

1.2). At the same time, the inner radius to outer radius ratio (β) will not affect the figure of merit too much when β is smaller than 0.5.

D. Other Parameters

1) Length of Coil Cable: Length of the coil cable l is used in both of the calculations for ac resistance and self-resonant frequency. For this Archimedean spiral coil shape, the length of the cable can be calculated by

$$l = \int_0^{2\pi \cdot N} \sqrt{\left(r_{\mathrm{i}} + \frac{r_w}{\pi}\theta\right)^2 + \left(\frac{r_w}{\pi}\right)^2}\, \mathrm{d}\,\theta\,. \tag{29}$$

2) Self-Resonant Frequency: The self-resonant frequency of the coil f_{sr} should be much larger than the switching frequency f_{s} of the converter so that the power is transmitted between coils. Analytical analysis of the flat-spiral coil self-resonant frequency is given in [51], while a simplified equation [52] can be used that

$$f_{\mathrm{sr}} = \frac{c}{2l}(0.9923 - 8.6494 r_{\mathrm{i}} + 48.869 {r_{\mathrm{i}}}^2 + 0.0728\ln(p) + 132.896 r_{\mathrm{w}} + 0.1484\ln(N))\,. \tag{30}$$

where c is the light velocity, and p is the turn spacing.

3) AC Resistance: Ac resistance of flat-spiral coil using litz wire is fully analyzed in [53] with both skin effect and proximity effect considered.

IV. Coil With Ferrite Shielding

Section III analyzed the effect of different parameters of the coil pair. For the designed WPT converter, two coils will be sandwiched by two ferrite shielding layers to increase the inductance of the coil pair thus increase system efficiency and limit EMI interference to the external space around the coil. This section will analyze the case when the ferrite shieldings are included in the system. Since the ferrite works as shielding instead of the path of main magnetic flux as in a traditional transformer and the power level of the converter is low, the ferrite magnetic is considered working only in the linear magnetic region for the following part of this section.

A. Inductance Calculation With Ideal Ferrite Shielding

Coil inductance calculation with ferrite shielding is a difficult part of WPT design. Besides the coil pair itself, the inductance value is affected by many different factors of the shielding including the permeability, thickness, area, and position, etc. To simplify the problem, an ideal shielding is first considered for inductance calculation, and the factors of nonideality will be considered later. In the ideal case, the ferrite shielding has infinite thickness and permeability. The analytical calculation of self-inductance and mutual-inductance of the flat circle coil with ferrite is first solved in [54], and extended to flat-spiral multiturn structure in [55] with high accuracy. However, these analytical works contain complicated calculation procedures which increase the difficulty for the later optimization procedure.

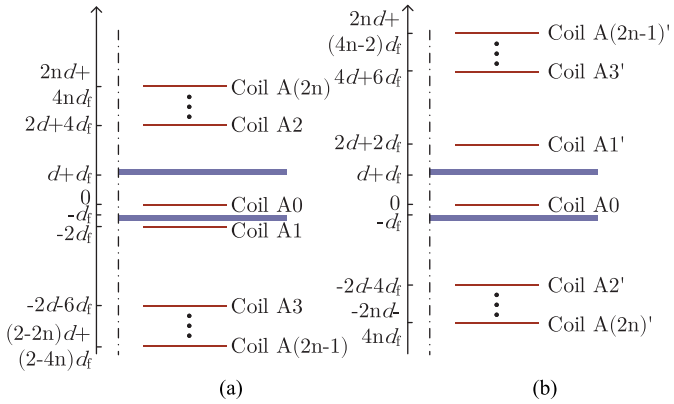

Fig. 10. Coil and mirror coils for self-inductance calculation. (a) Mirror coils start the reflection from the bottom ferrite. (b) Mirror coils start the reflection from the top ferrite.

At the same time, using pure FEA method for parameters extraction will take longer computation time and more data collection effort. Therefore, this article proposes a mirror coil method for self-inductance and mutual-inductance calculation using only two equations of (22) and (23).

From the static electromagnetic field analysis point of view, the ideal ferrite layer changes the boundary condition for this inductance calculation problem and the field can be equivalently presented by the original coil and its mirror coils. Since the coil structure has rotational symmetry, the coil and its mirror coils are shown in a 2-D format in Fig. 10, which can rotate around the z-axis to get the full 3-D structure, where d is the distance between two coils, and d_f is the distance between the coil and its adjacent ferrite. In Fig. 10, Coil A0 is the original coil sandwiched by two ferrite shielding layers. Fig. 10(a) presents the mirror coils series which start the reflection from the bottom ferrite including Coil A1, Coil A2,..., Coil A$(2\mathrm{n}-1)$, Coil A$(2\mathrm{n})$ and their positions. Fig. 10(b) presents the mirror coils series which start the reflection from the top ferrite including Coil A1′, Coil A2′,..., Coil A$(2\mathrm{n}-1)'$, Coil A$(2\mathrm{n})'$ and their positions. These two series of mirror coils are separated for a clearer presentation. Therefore, the self-inductance of coil considering the effect of ideal ferrite shielding layers can be calculated by

$$L_{\mathrm{A\_f}} = L_{\mathrm{A0}} + \sum_{n=1}^{\infty} M_{\mathrm{A0An}} + \sum_{n=1}^{\infty} M_{\mathrm{A0An'}} \tag{31}$$

where $L_{\mathrm{A\_f}}$ is the self-inductance of Coil A with ferrite shielding, L_{A0} is the self-inductance of Coil A without ferrite shielding, M_{A0An} is the mutual inductance between Coil A0 and mirror coil Coil An, n is an integer equal to or greater than 1. L and M can be calculated by (22) and (23).

Fig. 11(a) presents the position of Coil B0, Coil A0, and all the mirror coils of Coil A0. Fig. 11(b) presents the position of Coil A0, Coil B0, and all the mirror coils of Coil B0. With a similar principle, the mutual inductance of the coil pair with

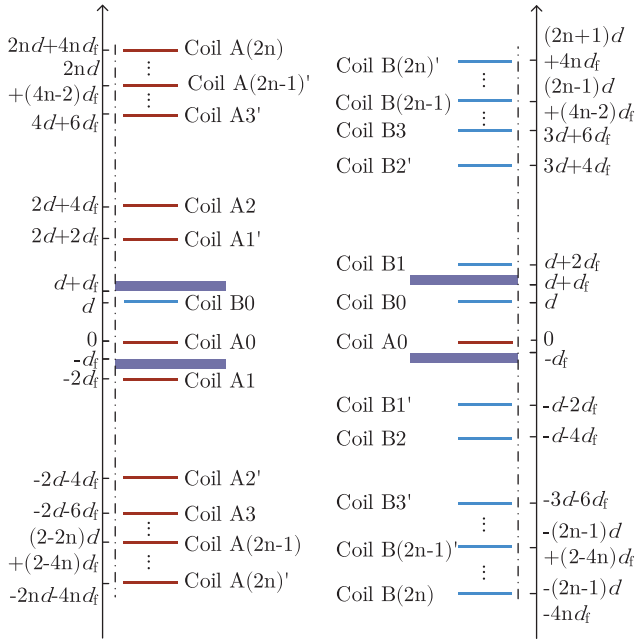

Fig. 11. Coil and mirror coils for mutual-inductance calculation. (a) Coil B, Coil A and its mirror coils. (b) Coil A, Coil B and its mirror coils mirror coils.

ferrite shielding can be calculated by

$$M_{\mathrm{AB\_f}} = M_{\mathrm{A0B0}} + \sum_{n=1}^{\infty} M_{\mathrm{A0Bn}} + \sum_{n=1}^{\infty} M_{\mathrm{A0Bn'}} = M_{\mathrm{A0B0}} + \sum_{n=1}^{\infty} M_{\mathrm{B0An}} + \sum_{n=1}^{\infty} M_{\mathrm{B0An'}} \quad (32)$$

where $M_{\mathrm{AB\_f}}$ is the mutual-inductance of the coil pair with ferrite shielding, M_{A0B0} is the mutual-inductance of the coil pair without ferrite shielding, M_{A0Bn} is the mutual inductance between Coil A0 and mirror coil Coil Bn, L and M can be calculated by (22) and (23). When calculating inductance value by (31) and (32), with increasing n, the mutual inductance of M_{A0An}, M_{A0Bn} will keep decreasing because the distance between the original coil to the mirror coil will become larger, and finally negligible compared to the inductance without ferrite shielding layers. To reduce calculation duration while keeping the accuracy, the series is calculated until $n = 4$, so the equations can be simplified to be

$$\begin{aligned} L_{A\_f} &= L_{A0} + M_{A0A1} + M_{A0A1'} + M_{A0A2} + M_{A0A2'} \\ &\quad + M_{A0A3} + M_{A0A3'} + M_{A0A4} + M_{A0A4'} \\ &= M(0) + M(2d_{\mathrm{f}}) + M(2d + 2d_{\mathrm{f}}) + M(2d + 4d_{\mathrm{f}}) \\ &\quad + M(2d + 4d_{\mathrm{f}}) \\ &\quad + M(2d + 6d_{\mathrm{f}}) + M(4d + 6d_{\mathrm{f}}) + M(4d + 8d_{\mathrm{f}}) \\ &\quad + M(4d + 8d_{\mathrm{f}}) \end{aligned} \quad (33)$$

$$\begin{aligned} M_{AB\_f} &= M_{A0B0} + M_{A0B1} + M_{A0B1'} + M_{A0B2} + M_{A0B2'} \\ &\quad + M_{A0B3} + M_{A0B3'} + M_{A0B4} + M_{A0B4'} \\ &= M(d) + M(d + 2d_{\mathrm{f}}) + M(d + 2d_{\mathrm{f}}) + M(d + 4d_{\mathrm{f}}) \\ &\quad + M(3d + 4d_{\mathrm{f}}) \\ &\quad + M(3d + 6d_{\mathrm{f}}) + M(3d + 6d_{\mathrm{f}}) + M(3d + 8d_{\mathrm{f}}) \\ &\quad + M(5d + 8d_{\mathrm{f}}) \end{aligned} \quad (34)$$

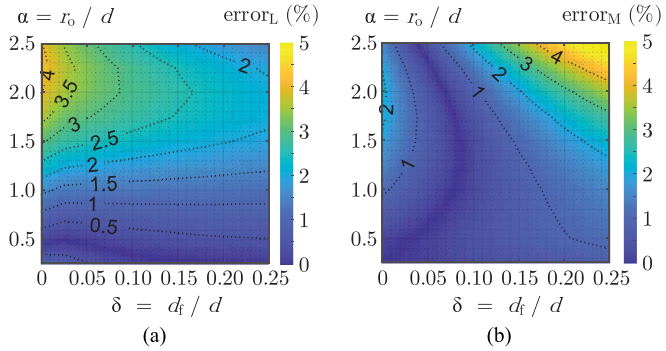

Fig. 12. Error of the simplified equations for numerical calculation of coil pair with ideal magnetic shielding. (a) Self-inductance. (b) Mutual inductance.

where the parameter in the bracket is the distance between the original coil and mirror coil for each mutual-inductance calculation. Fig. 12 summarized the percentage error of calculation results from (33) and (34) compared with FEA simulation. From this figure, the error of the calculation is less than 5%, for parameter sweeping of α and δ (d_{f}/d), for both self-inductance and mutual-inductance calculation. For author's computer with Intel i7-8700 CPU, if 3-D FEA method is used extracting mutual inductance with 3-D coil model, the simulation duration for each structure takes around 60 min. Considering the coils' rotational symmetry, 2-D cross-sectional model can be used for simplification which can drastically reduce the simulation time for each data point to around 5 min. As a comparison, it takes only around 0.3 s in MATLAB for calculation from (33) or (34) when the accuracy of the $integral3$ is set to be 0.0001. Considering more than thousands of data points to collect, the saved time is enormous.

B. *Factors From Nonidealities of Ferrite Layer*

With the mirror image method, the inductance of the coil pair sandwiched by ferrite shielding layers can be calculated by the numerical method. However, the result is based on the assumption that ferrite shielding is ideal. In this section, nonidealities of the ferrite shielding layers will be discussed to illustrate their effect on inductance calculation.

1) Permeability and Thickness of the Ferrite Shielding: Multiple magnetic shielding sheets with different thickness h, permeability μ_{r}, flexibility, and the manufacturer have been tested with the same coil. Self-inductance measurement results from impedance analyzer are shown in Table I. From this table, several conclusions can be drawn. First, although a flexible magnetic sheet is convenient for special shape applications, the permeability is usually much lower since it uses small magnetic particles and glue to mix them together. Second, the inductance will increase when the product of permeability and thickness increases

TABLE I
SELF-INDUCTANCE OF COIL WITH DIFFERENT MAGNETIC SHIELDING

	L (μH)	h (mm)	μ_r	Flexibility	Manufacturer
1	13.95	0.5	140	Yes	KEMET
2	13.60	0.3	160	Yes	KEMET
3	15.12	1.1	540	No	Laird
4	15.13	1.1	2500	No	Laird
5	12.38	0.1	220	Yes	TDK
6	12.95	0.18	135	Yes	TDK
7	15.33	5	3000	No	TDK
8	14.09	0.3	230	Yes	Würth
9	14.61	0.5	220	Yes	Fair-Rite
0	9.90	no magnetic shielding			

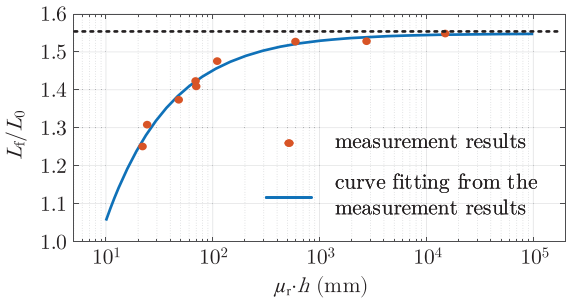

Fig. 13. Ratio of coil self-inductance with and without magnetic shielding with different product of permeability and thickness.

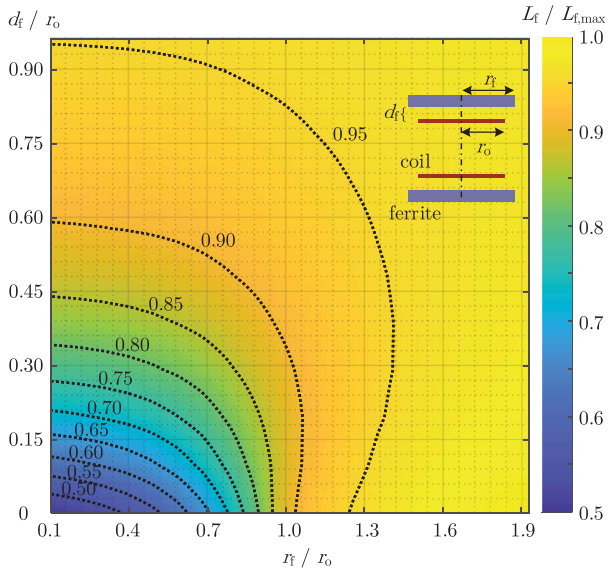

Fig. 14. Effect of the size and position of the magnetic shielding layer to the self-inductance of the coil pair.

because a higher product of permeability and thickness means higher shielding capability of the magnetic layer, which reduces leakage field and increase magnetic field between coils. Third, the inductance increases with the product, but the increasing speed becomes slower. Note that compared with sample number 3, sample number 7 has 25 times higher product but only 1.014 times higher self-inductance. As shown in Fig. 13, the x-axis is the product of the μ_r and h and the y-axis is the self-inductance of the coil with magnetic shielding L_f over the self-inductance of the coil without magnetic shielding L_0. The red dots are measurement results with samples from Table I, and the blue curve is the curve fitting result from those measurements. The dashed line shows the maximum L_f/L_0 it can achieve, i.e., the ideal case with infinite ferrite thickness and permeability. From the figure, the ferrite can be considered ideal if the product of h and μ_r is larger than 1000 mm since the difference between this L_f and the L_f with ideal ferrite is less than 3%. Therefore, choosing a proper magnetic shielding sheet helps to increase the inductance of the coils and keep a reasonable size of magnetics which matches the result in [56].

2) Size and Position of the Ferrite Shielding: Besides the thickness and permeability, the size and position of the ferrite shielding will also affect its performance. An ideal ferrite shielding with infinite radius is not practical in the real application. Since the coil discussed in this article is a flat spiral shape, so the ferrite shielding is designed in the shape of a circular disk. The radius of the ferrite shielding is r_f and the distance between the shielding to the coil is d_f. Fig. 14 presents the effect of ferrite shielding size. In this figure, the x-axis is r_f/r_o which presents the size of the ferrite shielding; y-axis is d_f/r_o which presents different positions of the shielding; the color of the figure is $L_f/L_{f,max}$ which is the ratio of the coil self-inductance with the specific size ferrite and coil self-inductance with the infinitely large ferrite. From this figure, it can be claimed that when the radius of the ferrite is larger than 1.05 of the radius of the coil, the shielding effect to coil self-inductance will be more than 90% compared with an ideal infinite large ferrite. As for the coupling coefficient k, an empirical equation is derived through parameter sweeping in FEA simulation. Note that this equation is accurate (5% error) only within a specific parameter range as shown as follows:

$$k = (0.3074\alpha - 0.1171) \cdot \lambda^{-0.45} \cdot \kappa^{0.21} \tag{35}$$

where

$$\begin{cases} \alpha \in (0.75, 2) \\ \lambda = (d + 2d_f)/d \in (1, 2) \\ \kappa = r_f/r_o \in (0.75, 2)\,. \end{cases} \tag{36}$$

As a brief summary, the coil self- and mutual-inductance can be calculated by (33) and (34) numerically for the ideal shielding case. For the nonideal condition, the thickness and permeability effect can be negligible if the product of them is higher than 1000 mm; the effect of shielding size to self-inductance can be negligible if κ is higher than 1.05. At the same time, the coupling coefficient k for coils with nonideal ferrite can be calculated through (35). Therefore, the self-and mutual-inductance of coil pair with nonideal shielding layers can both be calculated numerically without FEA simulation.

C. AC Resistance of Coil With Magnetic Shielding

AC resistance of litz wire coil with magnetic shielding can be calculated through [57] accurately.

TABLE II
VARIABLES OF THE MULTIOBJECTIVE OPTIMIZATION

d	10 - 50 mm	r_o	10 - 50 mm
f_s	200 - 2000 kHz	d_f	0 - 10 mm
r_w	0.6 - 1.5 mm	N_s	255 - 2700
d_{cj}	AWG 44 - 48		

V. MULTIOBJECTIVE OPTIMIZATION AND CONVERTER PROTOTYPE

A. Multiobjective Optimization

For the WPT designed specifically as an MV APS, three design requirements should be met at the same time. First, the efficiency η of the converter should be high. Compared to losses of the megawatt power rating MV converter, losses from APS contributed to the total system are negligible. However, the space of the power cell is very limited due to the highly compact design requirements. Therefore, the high efficiency can help APS shrink the size without having thermal dissipation issues. Second, the coil pair should have low isolation capacitance C_p between transmitter and receiver. For SiC-based power cell, the switching node of the half-bridge can have dv/dt as high as 100 V/ns. The coupling capacitance should be minimized to reduce the induced common-mode current since this electromagnetic interference (EMI) problem can ruin the performance of controllers and sensors. Third, the coil should have adequate insulation capability considering MV converter applications. Therefore, a multiobjective optimization process taking all the requirements into consideration is necessary.

For the multiobjective optimization, sweeping variables are summarized in Table II, including the distance between the two coils d, outer radius the coil r_o, switching frequency f_s, distance between the coil and its neighboring ferrite d_f, and different types of litz wire (radius of litz wire r_w, strand number N_s, and diameter of each strand d_{cj}). Parameters of litz wire come from the datasheet of New England Wire. Based on the E-field design criterion, the E_{max} should be lower than 2.4 kV/mm [11] to avoid partial-discharge (PD) of coil under high voltage excitation. From (21), the PD-free maximum allowed insulation voltage V_{max} for different coil geometry can be calculated as

$$V_{max} = \frac{E_{max}(2.4\,kV/mm)}{0.8 \cdot r_o^{-0.21} \cdot r_w^{-0.28} \cdot d^{-0.39}}. \quad (37)$$

The multiobjective optimization result is shown in Fig. 15 with converter efficiency η, coupling capacitance C_p, power density of the coil ρ, and the maximum allowed PD-free isolation voltage V_{max}. From the optimization space with solutions shown in Fig. 15, the effect of different parameters is clearly shown. For the outer radius r_o, each "layer" of dots in Fig. 15 represents solutions with the same coil outer radius. Larger r_o means lower ρ, larger C_p, higher η, and higher V_{max}. For the distance between two coils d, within the same "layer" of dots in the optimization space, each vertical line represents solutions with the same coil distance. Larger d means lower ρ, lower C_p, lower η, and higher V_{max}. Dots within each vertical line of the optimization space shows the effect of other parameters include different litz wire,

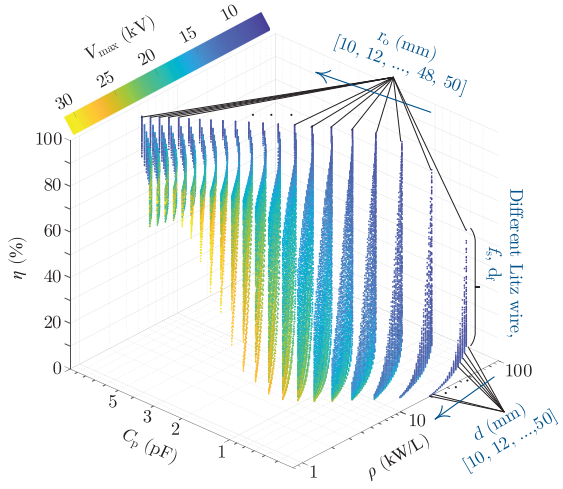

Fig. 15. Parameters sweeping result with variables presented in Table II.

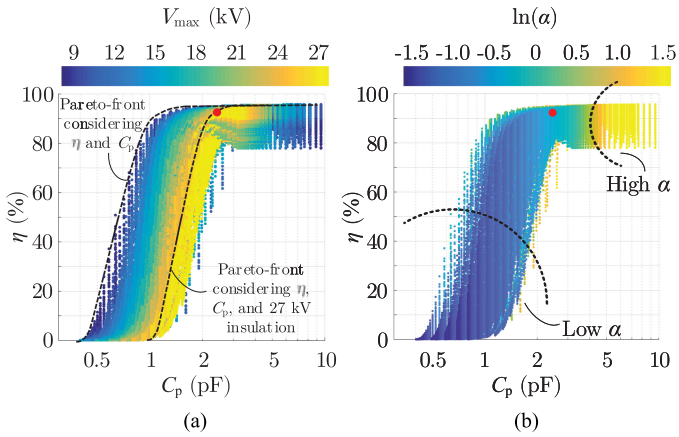

Fig. 16. Multiobjective optimization result of the WPT converter. (a) Maximum PD-free insulation voltage is included. (b) Ratio of outer radius to coil distance is included.

switching frequency, and distance between coil and ferrite. From Fig. 15, those parameters will not affect the ρ and C_p, but will affect η, and V_{max}.

Since the power density is not the key optimization goal in the application, the problem is simplified to be multiobjective optimization among η, C_p, and V_{max} as described in Fig. 16(a). For a 100-W WPT converter, if the converter efficiency is the only factor under consideration, η can be as high as 96%. However, if both the converter efficiency and isolation capacitance are considered, the optimal design cases reside on the fundamental Pareto-front of the optimization result, which is the envelope of the dark blue dots marked by the left black dashed line. From the coil construction point of view, in order to minimize C_p, those possible designs with a small distance d between the coils or large radius r_o should be excluded. Furthermore, if the insulation capability is also considered at the same time, the possible design regions will move toward the right from the fundamental Pareto-front line. For the 27-kV insulation requirement, the final possible design points are along with the

TABLE III
OPTIMIZED PARAMETERS FOR COIL IN WPT CONVERTER

r_i	1 mm	r_o	40 mm
d	34 mm	d_f	5 mm
r_w	1.2 mm	N	16
N_s	1725	d_{cj}	AWG 46
f_s	1 MHz	V_{max}	27 kV
η	93.19%	C_p	2.65 pF
P_o	100 W	V_o	48 V

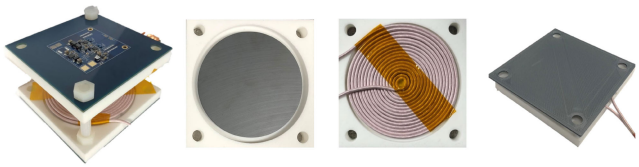

Fig. 17. Hardware prototype of the WPT converter, ferrite, coil, bobbin, and coil cover.

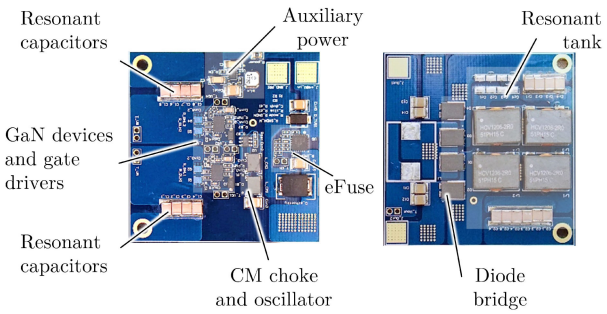

Fig. 18. Primary and secondary side PCB with 50 × 50 mm size.

envelope of all the light yellow dots marked by the right black dashed line in Fig. 16(a). Thus, the litz wire cable radius r_w can not be too small; otherwise, the maximum E-field intensity is too large to meet the design criterion. Therefore, from the viewpoint of insulation, there is a lower limit for the litz wire radius, although it seems over-designed for the circuit power rating. Instead of using color to present the insulation voltage, Fig. 16(b) utilizes color to present α in logarithm scale which proves the conclusion presented in Fig. 9 that the best shape for both high k (thus η) and low C_p can be achieved if α is near 1. Too large α will lead to high C_p while too small α will lead to low η. The final optimized solution is selected at the knee point along the right dashed line in Fig. 16(a), and the coil parameters of the selected design are summarized in Table III.

B. Converter Prototype

The converter prototype, coil, ferrite, and bobbin are all shown in Fig. 17. Important components on the primary side PCB and secondary side PCB are marked in Fig. 18. The primary side converter includes the low voltage APS, oscillator for driving signal, GaN device gate driver, eFuse (TPS16630 for protection and soft start-up), GaN-based full-bridge inverter, and compensation capacitors. The secondary side includes the resonant tank, diode rectifier, and output filter. A dc–dc converter is used to

TABLE IV
COMPARISON OF OPTIMIZATION RESULT AND MEASUREMENT RESULT OF COIL PARAMETERS

	Optimization Result	Measurements Result
L_1	12.04 µH	11.37 µH
L_M	2.16 µH	2.01 µH
C_p	2.65 pF	2.76 pF
R_{ac}	236 mΩ	247 mΩ
η	93.19%	92.78%

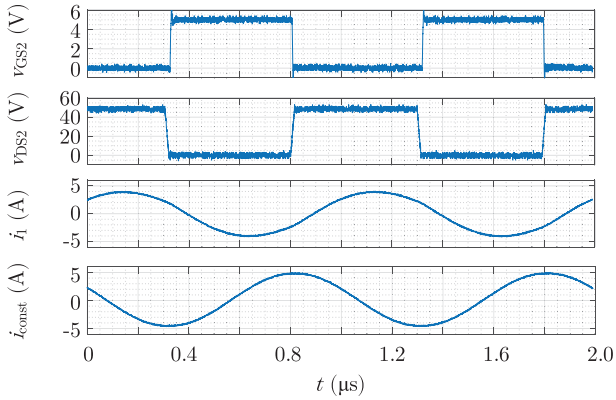

Fig. 19. Operating waveforms of the WPT converter.

transfer the input 48–5 V supplying voltage and power for the silicone oscillator and GaN device gate driver. The LTC6908 oscillator generates the gate PWM signal to the gate driver with a 50% duty cycle and 1 MHz frequency. The LMG1210 from TI is used as the GaN device gate driver with a bootstrap circuit and tunable deadtime. The EPC2016 C is selected to be the GaN device with 100 V_{DS}, 16 m $R_{DS(ON)}$, and 210 pF output capacitance. For the resonant capacitor, C0G/NP0 type capacitors are used since their capacitance is accurate and stable under different temperatures and voltages. The converter PCB size is 50 mm × 50 mm for both sides. From Table IV, the optimization result and the measurement result match accurately which proves the validity of the design and optimization process.

VI. EXPERIMENTAL VALIDATIONS

A. Circuit Operation

1) Operating Waveforms: Fig. 19 shows the normal operating waveforms of the WPT converter including the gate signal and drain to source voltage of the MOSFET S_2, v_{GS2}, v_{DS2}, primary side coil current i_1, and secondary side coil current i_{const}. The gate signal is 1 MHz, 5 V pulse generated from the GaN gate driver. The device drain to source voltage is 48 V, 50% duty cycle. Also, when comparing v_{GS2} and v_{DS2}, ZVS is achieved. Current i_1 is not in phase with v_{DS2} perfectly, so the inductive current is used to charge and discharge the output capacitance of the GaN devices. Fig. 20 shows the efficiency and output voltage of the WPT converter under different load conditions. Since perfect resonance of all LC parameters is not realistic, the output voltage is not exactly the same under different loads for an uncontrolled open-loop system. From the 10 to 100 W

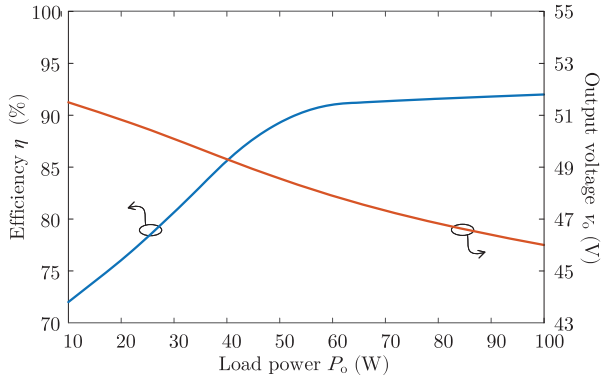

Fig. 20. Efficiency and output voltage of WPT with different load.

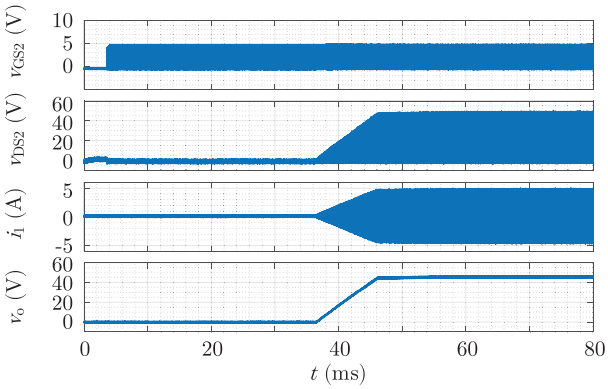

Fig. 21. Soft start-up procedure of the WPT converter.

case, the output voltage will have +8% to -4% output voltage difference. For efficiency, the peak efficiency is 92.78% under full load. Most of the losses come from the ac losses of the coil and the secondary side full-bridge diode rectifier. Since the WPT secondary side coil is working as a constant current source, the loss from i_{const} always exists which causes an efficiency drop in the light load condition.

2) Soft Start-Up: Since there is no feedback control and variable frequency control implemented for this converter, an eFuse TPS16630 from TI is implemented in the main power path functioning overcurrent protection, UVLO, OVLO, and soft-startup by limiting the current passing through it. Fig. 21 shows the soft-startup procedure of the WPT converter. When the 48 V is fed in the system, the oscillator and gate driver start to work so v_{GS2} appears. After tens of milliseconds, the eFuse is on but the current flowing through it is limited to the maximum allowed value. Using a constant current to charge the output capacitor will make the output voltage increase linearly from 0 to 48 V without overshoot.

3) Value of C_2: As analyzed before, capacitor C_2 is used to tune the loading impedance of the full-bridge inverter, which should compensate for the excessive reactive power but leave some inductive current for soft-switching of the MOSFETs as shown in Fig. 19. Besides the case when $C_2 = 2.547\text{nF}$, the other two cases where C_2 is either too large or too small are also tested with coil current and zoomed-in turn-OFF transient

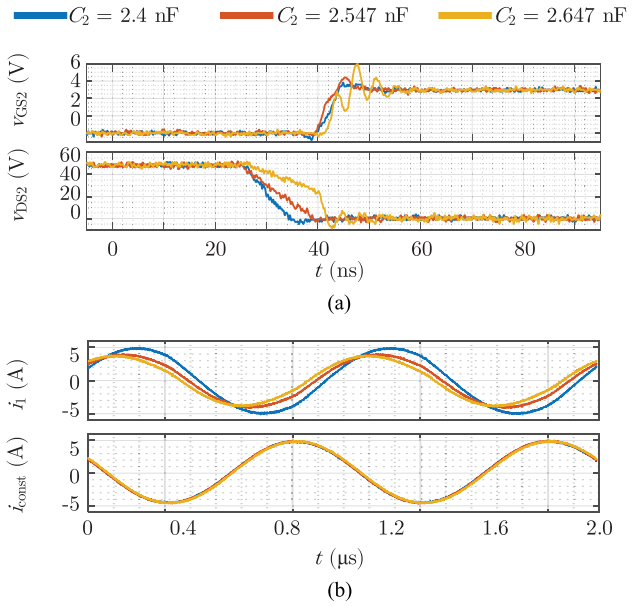

Fig. 22. For different C_2 values. (a) Voltage waveforms during turn-OFF transient. (b) Coil current waveforms.

presented in Fig. 22. The blue curves present the test waveforms and zoomed-in switching transient when $C_2 = 2.4\text{nF}$. In this case, although ZVS can be achieved, too much reactive power will increase the primary side current i_1. Peak value of i_1 is 4.85 A while the peak value of i_1 in Fig. 19 is 3.85 A. This circulating current will cause more conduction losses on the coil and GaN devices. On the contrary, yellow curves present the test waveforms and zoomed-in switching transient when $C_2 = 2.647\,nF$. In this case, the loading impedance from the full-bridge inverter is almost pure resistive. Although the peak value of i_1 is as small as 3.60 A, ZVS cannot be achieved which increases the switching loss. In this case, hard switching also causes higher spikes and ringing of v_{GS} and v_{DS} which can cause overvoltage and shoot-through problems. Therefore, a fine-tuned C_2 value is required to have a tradeoff between switching loss and conduction loss. Going back to (20), considering deadtime t_d of 12 ns, C_{oss} of 210 pF, and all the other parameters of the coil and converter, the calculated C_2 should be 2.52 nF which matches the testing result accurately.

B. Insulation Tests

The first set of tests are done to prove the assumption that the e-field condensed area for the coil is around its outer edge. As shown in Fig. 23, both the nondestructive PD test and destructive flashover test have proved that the weak point, i.e., the E-field condensed area, is at the outer edge of the coil. The final insulation of the transmitter and receiver coils is then validated by PD experiments. Under a distance of 34 mm, no discharge events are captured until around 33 kV dc. Similarly, no detectable PD between the coils can be captured under line frequency ac excitation with a peak value of 33 kV. As a summary, the PD-free voltage level for the designed coil is at least 33 kV, which is about 20 % higher than our insulation design target detailed test setup

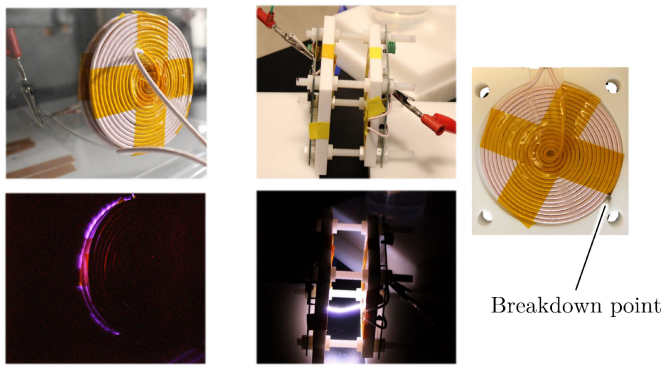

Fig. 23. Insulation verification tests. (a) PD happened around the edge of the coils. (b) Flashover happened at the edge of the coils.

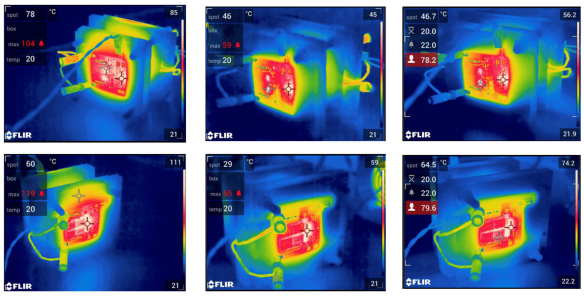

Fig. 24. Thermal map of the WPT converter. (a) 160 W output power with natural air cooling. (b) 160 W output power with forced air cooling. (c) 200 W output power with forced air cooling.

and result and also be found in [11]. In order to further increase the insulation system reliability and insulation capability, a coil cover can be added as a barrier which can push the flashover voltage much higher, to more than 40 kV.

C. Thermal Performance and Isolation Capacitance

To test the thermal performance and limitation of the designed WPT converter, continuous tests with output power more than required and are done as shown in Fig. 24. From the steady-state thermal map, the hottest spot on the primary side is the eFuse, and the hottest spot on the secondary side PCB is the rectifier diode. With 160 W output power, the diode rectifier temperature can be as high as 119 °C for natural air cooling and drops to 65 °C with forced air cooling. With forced-air cooling, the output power can even be pushed higher to 200 W with 80 °C temperature for the diode rectifier.

The isolation capacitance is measured through an impedance analyzer. For WPT without a coil cover, the measured C_{p} value is 2.78 pF. For WPT with a coil cover, the measured C_{p} value is 3.02 pF.

VII. Conclusion

This article proposes an analytical design and optimization process for coil and magnetics in WPT converter for APS. The calculation equation for isolation capacitance for flat spiral structure is given. In addition, mirror method is used to calculate the self- and mutual-inductance of coil with magnetic shielding so that the parameters can be calculated without using FEM simulation. An efficiency, isolation capacitance, insulation capability multiobjective optimization is done to optimize the coil specifically for APS application. A GaN-based 100-W dc–dc converter is used as prototype to validate the design and optimization of the coil and magnetic.

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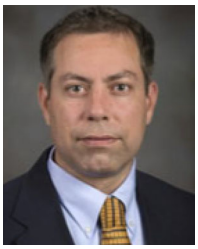

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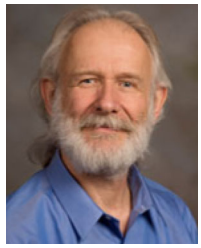

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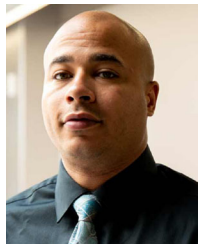

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