Design and Control of a Decoupled Multichannel Wireless Power Transfer System Based on Multilevel Inverters

Yuxin Liu, *Student Member, IEEE*, Chunhua Liu, *Senior Member, IEEE*, Xingran Gao, and Senyi Liu, *Member, IEEE*

***Abstract*—Traditional multichannel wireless power transfer (WPT) systems suffer from the complex system structure and cross-interference among receivers. To solve such problems, this article presents the design and control methods of a decoupled multichannel WPT system based on multilevel inverters. A single-phase multilevel inverter is utilized to drive the transmitter circuit with a voltage waveform consisting of multiple components. Particularly, these components are independent in the frequency spectrum, and their amplitudes can be controlled independently. Moreover, primary compensation is used to offer multiple frequencies for the primary circuit. Additional damping filters are used in the secondary circuits to reduce the cross-interference between the receivers. In addition, the features of the system topology are analyzed, and an exact parameter design method is presented. Furthermore, combined with the neutral point voltage balance strategy, a simple vector-based control method is proposed to regulate the transmitted power in each power channel. As a result, the power can be transferred to loads through the designed power channels simultaneously without mutual interference. Finally, both simulation and experiment of a 1-kW experimental prototype with SIC-MOSFET are given to verify the feasibility of the proposed multichannel WPT system and the control strategy.**

***Index Terms*—Compensation network, multilevel inverter (MLI), multiple power channel, wireless power transfer (WPT).**

I. Introduction

Wireless power transfer (WPT) has been widely used in various applications, such as electric vehicles (EVs), unmanned aerial vehicles, and portable electronics, due to its convenience, safety, and better user experience [1]–[3]. Recently, the multichannel WPT has attracted more and more attention for its advantage over single-channel WPT in delivering power to multiple loads simultaneously. Multichannel WPT can be realized using multiple transmitters [4], [5] or only one transmitter. Particularly, the way of using one transmitter and many receivers is also known as one-to-multiple WPT (O2M-WPT) [12].

O2M-WPT has been applied in applications of EV charging systems [7], wireless motors [8], [9], and inductive heating [10]. In an O2M-WPT system, the power allocation of multiple loads is usually achieved by multifrequency channels [6]. To enhance the efficiency of O2M-WPT, compensated capacitor switchers [9] or multiple-frequency resonating compensation (MFRC) [12], [17] can be used to offer multiple resonant frequencies for the transmitter circuit. Different resonant frequencies are set for loads, and when a specific frequency is selected, the corresponding load is activated [6]–[8]. Commonly, the output power can be regulated by adjusting the amplitude of the corresponding frequency components [10]–[12].

Although O2M-WPT has broad application prospects, there are still some issues that need to be handled. One issue is about the cross-interference, which affects the independence of each channel and reduces the efficiency [15], [16]. In [7], dc–dc circuits are placed for the receivers of a dual-pickup wireless EV charging system to allocate power to each load accurately. However, the system structure is complex due to the additional dc–dc circuits. In [13], auxiliary circuits are added to receiver circuits and relay circuits to reduce the cross-interference. However, the use of relay circuits complicates the system. Fu *et al.* [14] proposed a compensation method to lessen the influence of cross-interference by calculating the derived optimal load reactances. However, this method is challenging to apply when the loads change frequently. Narayanamoorthi *et al.* [15] used a frequency bifurcation approach to realize O2M-WPT with reduced cross-interference. However, the system parameters are difficult to design, especially when the number of receivers increases. In [16], three types of compensation networks with damping filters are introduced into receivers, and the cross-interference among multiple receivers can be reduced flexibly. However, the cross-interference can be further reduced by enhanced control.

The multifrequency superposition is another issue of OWPT, which superimposes multiple power components to drive the transmitter [12]. Many attempts have been made to realize

---

Manuscript received July 12, 2021; revised October 28, 2021 and January 12, 2022; accepted March 3, 2022. Date of publication March 15, 2022; date of current version April 28, 2022. This work was supported in part by the Science Technology and Innovation Committee of Shenzhen Municipality, Shenzhen, China, under Project JCYJ20180307123918658, in part by the Innovation and Technology Commission, Hong Kong SAR under Project ITP/027/19AP, and in part by the Collaboration Research Fund from Research Grants Council, Hong Kong SAR, under Project CRF: C1052-21GF. Recommended for publication by Associate Editor C. K. Lee. *(Corresponding author: Chunhua Liu.)*

The authors are with the School of Energy and Environment, City University of Hong Kong, Hong Kong, China, and also with the Shenzhen Research Institute, City University of Hong Kong, Shenzhen 518057, China (e-mail: yuxin.liu@my.cityu.edu.hk; chunliu@cityu.edu.hk; xingran.gao@cityu.edu.hk; senyiliu2-c@my.cityu.edu.hk).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3159129.

Digital Object Identifier 10.1109/TPEL.2022.3159129

multifrequency superposition for O2M-WPT. Liu *et al.* [11] used a transformer to combine all the power components from multiple inverters. However, the primary part still has only one resonant frequency, which prevents the system from operating in high efficiency. To solve this problem, Huang *et al.* [12] introduced resonant tanks to the topology presented in [11] and, therefore, employed different resonant frequencies to the transmitter. However, multiple inverters and additional transformers are still required. In [10], a family of power converters is proposed to provide two simultaneous frequencies for dual-frequency inductive heating. However, many passive components are required in the proposed topologies, which makes the system structure complex. In [30], a hybrid sinusoidal pulse width modulation (SPWM) method is proposed to realize multifrequency superposition with only one full-bridge inverter, where the modulation wave contains components with multiple frequencies. However, the power switches are required to operate at a frequency much larger than the transmission frequency, which increases switching losses and adds cost to power switches and digital controllers. Therefore, the hybrid SPWM method is more suitable for applications with low transmission frequencies. Multilevel inverters (MLIs) can generate more voltage levels than two-level inverters, which makes MLIs have the potential to realize multifrequency superposition with a simple system structure and a relatively low switching frequency.

In addition, MLIs surpass traditional two-level inverters in various applications because of the advantages such as lower voltage stress on power switches, better power quality, and smaller EMI [18]–[20]. Several topologies of MLIs have been proposed, such as neutral point clamped (NPC), flying capacitor, and cascaded H-bridge. As the number of voltage levels increases, MLIs can offer O2M-WPT with more possible solutions to superimpose multiple power components and regulate power allocation in each power channel. However, as more power switches are utilized in MLIs, the control of MLIs is more challenging [18], [19]. Moreover, the problem of neutral point (NP) voltage imbalance reduces the reliability of MLIs, which may lead to increased voltage stress of power switches, distorted output voltage, and additional losses [20]–[22].

Driven by combining the advantages of MLIs with O2M-WPT, this article proposes a decoupled multichannel WPT system based on MLIs. The main contributions of this article are listed as follows.

1) The multiple voltage levels of the MLIs can generate voltage waveforms with multiple frequency components, which naturally realize multifrequency superposition without additional transformers. The power components have no overlap in the frequency spectrum and can therefore be regulated independently.
2) MFRC with multiple resonant frequencies is applied in the transmitter circuit, which enhances the efficiency. Damping filters are used in the receiver circuits to reduce the cross-interference between two power channels.
3) Detailed parameter design methods for both transmitter circuit and receiver circuit are proposed as the flowcharts.
4) A simple vector-based control method with NP voltage balancing and third harmonic reduction is proposed to regulate the transmitted power in each power channel.

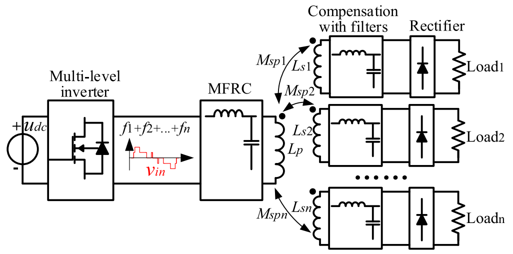


Fig. 1. Proposed multichannel WPT system based on an MLI.

TABLE I
SWITCHING STATES OF THE SINGLE-PHASE TNPC INVERTER

V_j	S_1	S_2	S_3	S_4	u_{in}	i_o	Category
V_1	1	0	0	1	u_{dc}	0	Large
V_2	1	0	0	0	$0.5u_{dc}$	$-i_{in}$	Medium
V_3	0	0	0	1	$0.5u_{dc}$	i_{in}	Medium
V_4	1	0	1	0	0	0	Zero
V_5	0	0	0	0	0	0	Zero
V_6	0	1	0	1	0	0	Zero
V_7	0	1	0	0	$-0.5u_{dc}$	$-i_{in}$	Medium
V_8	0	0	1	0	$-0.5u_{dc}$	i_{in}	Medium
V_9	0	1	1	0	$-u_{dc}$	0	Large

II. SYSTEM CONFIGURATION AND MODEL

The proposed multichannel WPT system is shown in Fig. 1, which composes one transmitter part and *n* receiver parts. The primary part contains a dc voltage source (u_{dc}), a single-phase MLI, an MFRC network, and a transmitter coil (L_P). Each secondary part has a receiver coil (L_{si}, $i = 1,\ldots,n$), a compensation network with damping filters, rectifier, and load. The voltage levels of the MLI can work at different frequencies. Therefore, a voltage waveform containing components with frequencies of f_i ($i = 1,\ldots,n$) can be generated, corresponding to the resonant frequencies of *n* receiver circuits. The MFRC network provides the primary circuit with multiple resonant frequencies [12], [17]. The damping filters used in the receiver circuits can produce a high impedance at nontargeted frequencies, which helps in reducing the cross-interference [16].

Generally, more power channels can be built by increasing the number of the voltage level of the MLI and the number of resonant frequencies of the MFRC network. Therefore, no additional transformer is needed to realize multifrequency superposition, and no additional inverter and dc voltage source are needed to regulate the power allocation among each load. In this article, a typical dual-channel WPT system based on a T-type NPC (TNPC) inverter is used as a representative example to illustrate the design and control method, and the circuit configuration is shown in Fig. 2.

In the case of neutral voltage balance, the two dc-link capacitors (C_1 and C_2) share the dc-link voltage equally as $u_{c1} = u_{c2} = 0.5u_{\mathrm{dc}}$, where u_{dc} is the voltage of the dc link. As shown in Table I, nine switching states (V_j, $j = 1,\ldots,9$) of the eight SIC-MOSFETs (S_n and $\overline{S_n}$, $n \in \{1, 2, 3, 4\}$) are available to generate five levels of inverter output voltage. Based on the

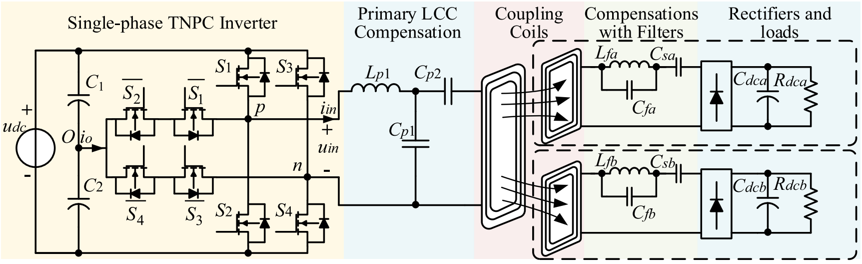


Fig. 2. Example of dual-channel WPT system based on TNPC inverter.

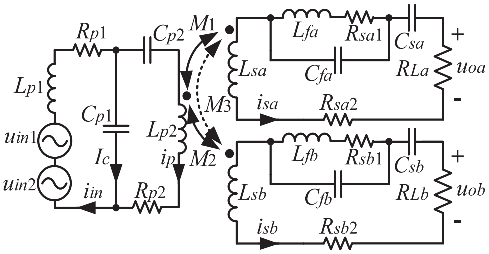


Fig. 3. Equivalent topology of the proposed dual-channel WPT system.

absolute value of the inverter output voltage, the nine switching states can be categorized as large, medium, and zero. The value of neutral line current i_o is also subject to the switching states according to Table I. V_2 and V_3 and V_7 and V_8 are two pairs of redundant medium switching states with the same inverter output voltage but the different neutral line current direction. The direction of i_o can affect the balance of the voltages across the two dc-link capacitors, and this principle will be explained in detail in Section IV.

In the proposed dual-channel WPT system, the transmitter coil transfers energy to the two receiver coils through two separated channels with different operating frequencies (ω_1 and ω_2). Therefore, the TNPC inverter is designed to generate a voltage waveform of two components $u_{\text{in}1}$ and $u_{\text{in}2}$. $u_{\text{in}1}$ has the fundamental frequency of ω_1, and $u_{\text{in}2}$ has the fundamental frequency of ω_2. ω_1 and ω_2 have the relation as

$$\omega_2 = 2\omega_1. \tag{1}$$

It is worth mentioning that with the proposed control method, $u_{\text{in}1}$ and $u_{\text{in}2}$ do not contain even order harmonics. Therefore, $u_{\text{in}1}$ does not have the harmonic with a frequency of ω_2, and $u_{\text{in}2}$ does not have the harmonic with a frequency of ω_1. The purpose of this setting is to reduce the mutual interference between the two power channels. The output voltage of the TNPC inverter can be expressed as

$$\begin{aligned} u_{\text{in}} &= \frac{u_{\text{dc}}}{2}\left(S_1 - S_2 - S_3 + S_4\right) \\ &= u_{\text{in}1} + u_{\text{in}2}. \end{aligned} \tag{2}$$

Fig. 3 is the equivalent circuit of the proposed dual-channel system. L_{p2} is the inductance of the transmitter coil. L_{p1}, C_{p1}, and C_{p2} form the *LCC* network, which can be tuned with two resonant frequencies. R_{p1} and R_{p2} are the equivalent series resistances (ESRs) of the primary part. A series compensation network with a damping filter is used in each secondary part. L_{sx}, C_{sx}, L_{fx}, and C_{fx} ($x = a$, b) are the inductances of the secondary coils, the capacitances of series compensated capacitors, the inductances of the damping filters, and the capacitances of the damping filters, respectively. R_{sx1} and R_{sx2} are the ESRs of the secondary parts. M_1 and M_2 denote two mutual inductances between the primary coil and secondary coils. M_3 is the mutual inductance of the two secondary coils. R_{La} and R_{Lb} are the converted equivalent resistances of loads of the two channels, where $R_{La} = 8R_{dca}/\pi^2$ and $R_{Lb} = 8R_{dcb}/\pi^2$ [12].

Compared to a conventional series and parallel resonant topology with a single natural resonant frequency, the *LCC* compensation can provide two natural resonant frequencies [10], [12]. The primary *LCC* compensation is prevalently used to naturally achieve constant voltage (CV) and constant current (CC) output [27], [28]. However, in this application, the primary *LCC* network is tuned with resonant frequencies of ω_1 and ω_2, which cannot realize nature CV and CC operation. However, the CV and CC ability can still be obtained by feedback control methods [29]. Meanwhile, series compensation with damping filter is used in two secondary parts with different resonant frequencies. ω_1 is the resonant frequency of Receiver *A*, and ω_2 is the resonant frequency of Receiver *B*. The *LC* parallel resonant circuit of the filters can generate high impedance at nontargeted frequency, which damps the component of nontargeted frequency [16]. For example, ω_1 is the resonant frequency of Receiver *A*, and the filter helps to damp the component of ω_2 in Receiver *A*. The quality factor of the *LC* parallel resonant circuit can affect the damping performance [24], [25]. Higher quality factors can lead to better decoupling ability and higher system efficiency. With Litz wires, the inductors of the filters can be made with a quality factor of a few hundred in case of several hundred kHz operation frequencies [26], which can achieve a desirable decoupling ability.

Based on Fig. 3, the total impedance of each secondary part can be calculated by

$$\begin{aligned} Z_{sx} = R_{Lx} + R_{sx2} &+ \frac{R_{sx1}}{1 - \omega^2 C_{fx} L_{fx} + j\omega C_{fx} R_{sx1}} \\ &+ j\left(\omega L_{sx} + \frac{\omega L_{fx}}{1 - \omega^2 C_{fx} L_{fx} + j\omega C_{fx} R_{sx1}} - \frac{1}{\omega C_{sx}}\right) \end{aligned} \tag{3}$$

where $x = a, b$. Based on the aforementioned operating principle of the damping filters, the following simple tuning equations for receiver parts, where the ESRs are neglected, can be obtained:

$$\begin{cases} \omega_1 L_{sa} + \frac{\omega_1 L_{fa}}{1-\omega_1^2 C_{fa} L_{fa}} - \frac{1}{\omega_1 C_{sa}} = 0 \\ 1-\omega_2^2 C_{fa} L_{fa} = 0 \\ \omega_2 L_{sb} + \frac{\omega_2 L_{fb}}{1-\omega_2^2 C_{fb} L_{fb}} - \frac{1}{\omega_2 C_{sb}} = 0 \\ 1-\omega_1^2 C_{fb} L_{fb} = 0 \end{cases}. \tag{4}$$

The model of the whole proposed system can be derived as

$$\begin{bmatrix} U_{\text{in}} \\ 0 \\ 0 \\ 0 \end{bmatrix} = \begin{bmatrix} R_{p1} + j\omega L_{p1} & Z_p & j\omega M_1 & j\omega M_2 \\ \frac{1}{j\omega C_{p1}} & -Z_p - \frac{1}{j\omega C_{p1}} & -j\omega M_1 & -j\omega M_2 \\ 0 & j\omega M_1 & Z_{sa} & j\omega M_3 \\ 0 & j\omega M_2 & j\omega M_3 & Z_{sb} \end{bmatrix} \begin{bmatrix} I_{\text{in}} \\ I_p \\ I_{sa} \\ I_{sb} \end{bmatrix} \tag{5}$$

where Z_p is expressed as

$$Z_p = j\omega L_{p2} + \frac{1}{j\omega C_{p2}} + R_{p2}. \tag{6}$$

The effect of the two secondary parts can be expressed as total reflected impedance (Z_r), which is the sum of the reflected impedance of the Receiver *A* (Z_{ra}) and Receiver *B* (Z_{rb}) [17] as

$$\begin{cases} Z_{ra}(\omega) = \frac{\omega^2 M_1^2 Z_{sb}(\omega) - j\omega^3 M_1 M_2 M_3}{\omega^2 M_3^2 + Z_{sa}(\omega) Z_{sb}(\omega)} \\ Z_{rb}(\omega) = \frac{\omega^2 M_2^2 Z_{sa}(\omega) - j\omega^3 M_1 M_2 M_3}{\omega^2 M_3^2 + Z_{sa}(\omega) Z_{sb}(\omega)} \\ Z_r(\omega) = Z_{ra}(\omega) + Z_{rb}(\omega) \end{cases}. \tag{7}$$

The value of $Z_r(\omega)$ is subject to the operating frequency. Particularly, when the system operates in ω_1, due to the damping filter of Receiver *B*, based on (3) and (4), $Z_{sb}(\omega_1)$ is at a very high value. The value of $|Z_{sa}(\omega_1)Z_{sb}(\omega_1)|$ is far larger than the values of $|\omega_1^3 M_1 M_2 M_3|$, $|\omega_1^2 M_3^2|$, and $|\omega_1^2 M_2^2 Z_{sa}(\omega_1)|$, which make $Z_{rb}(\omega_1)$ neglectable and $Z_r(\omega_1)$ is dominated by $Z_{ra}(\omega_1)$ as

$$Z_r(\omega_1) \approx Z_{ra}(\omega_1) \approx \frac{\omega_1^2 M_1^2}{R_{La}}. \tag{8}$$

Similarly, the total reflected impedance at ω_2 are expressed as

$$Z_r(\omega_2) \approx Z_{ra}(\omega_2) \approx \frac{\omega_2^2 M_2^2}{R_{Lb}}. \tag{9}$$

Equations (8) and (9) indicate that two receiver parts can receive power through two separate channels with little cross-interference.

The value of $I_{\text{in}}, I_p, I_{sa}$, and I_{sb} can be obtained from (5). Also, according to (5) and (6), the total impedance at the ac source can be derived as

$$Z_T = j\omega L_{p1} + R_{p1} + \frac{1}{j\omega C_{p1}} || \left(j\omega L_{p2} + \frac{1}{j\omega C_{p2}} + R_{p2} + Z_r \right). \tag{10}$$

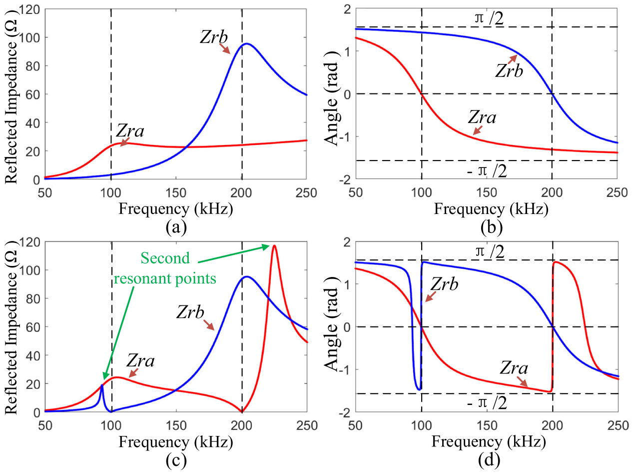


Fig. 4. Curves of the reflected impedance. (a) Absolute values of the reflected impedance without damping filter. (b) Angles of the reflected impedance without damping filter. (c) Absolute values of the reflected impedance with damping filter. (d) Angles of the reflected impedance with damping filter.

Based on the total impedance of the primary part (Z_T), the phase difference between the inverter output voltage and current can be calculated as

$$\varphi = \arctan\left[\frac{\mathrm{Im}(Z_T)}{\mathrm{Re}(Z_T)}\right]. \tag{11}$$

Then, the system efficiency can be expressed as

$$\eta = \frac{|I_{sa}|^2 R_{La} + |I_{sb}|^2 R_{Lb}}{|U_{\text{in}}|\,|I_{\text{in}}|\cos\varphi}. \tag{12}$$

III. PARAMETER DESIGN FOR THE PROPOSED WPT SYSTEM

Due to the high order and complexity of the model of the system, it is not easy to find the proper system parameters by analytical calculation. In this section, the features of the system topology will be analyzed, and the numerical calculation method will be used to design the parameters. The detailed design procedures of the secondary circuit and the primary circuit will be given in the form of flowcharts.

A. Features of System Topology

Fig. 4(c) and (d) illustrates the curves of absolute value and angles of the reflected impedance of the system. The parameters of the secondary circuits are listed as follows: $M_1 = M_2 = 31\ \mu$H, $M_3 = -2.9\ \mu$H, $L_{sa} = L_{sb} = 64.5\ \mu$H, $R_{La} = R_{Lb} = 16.21\ \Omega$, $R_{sa2} = R_{sb2} = 0.03\ \Omega$, $C_{fa} = 50$ nF, $C_{fb} = 100$ nF, $L_{fa} = 12.67\ \mu$H, $L_{fb} = 25.33\ \mu$H, $R_{sa1} = 0.01\ \Omega$, $R_{sb1} = 0.02\ \Omega$, $C_{sa} = 31.12$ nF, and $C_{sb} = 11.3$ nF. All the parameters are designed by the method introduced in Section III-B. With these parameters, Receiver *A* has a resonant frequency of $\omega_1 = 2\pi \times 10^5$, and Receiver *B* has a resonant frequency of $\omega_2 = 4\pi \times 10^5$. Fig. 4(a) and (b) shows the curves of the absolute values and angles of the reflected impedance of traditional series compensation (without damping filters) with the same resonant frequencies.

According to Fig. 4, by introducing damping filter into the receiver circuit, $|Z_{ra}|$ at ω_2 and $|Z_{rb}|$ at ω_1 are nearly equal to

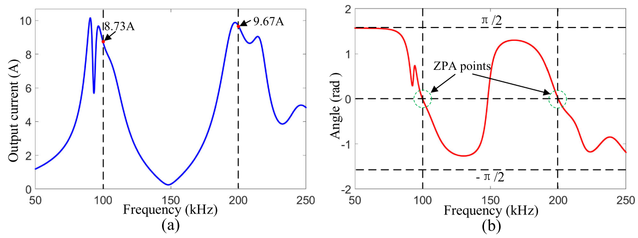


Fig. 5. Parameter sweeping results of the proposed WPT system. (a) Absolute value of the inverter output current. (b) Impedance angle of Z_T.

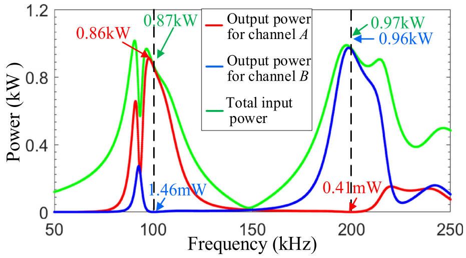


Fig. 6. Sweeping results of total input power and output power in each channel.

zero, whereas $|Z_{ra}|$ at ω_1 and $|Z_{rb}|$ at ω_2 are large. Compared to traditional series compensation, the reflected impedance at the required resonant frequency is nearly the same, whereas the reflected impedance at the damped frequency is much smaller. This feature ensures the decoupling of the two power channels.

Based on the receiver circuits parameters, a set of transmitter circuits parameters can be obtained by the design method proposed in Section III-C as: $L_{p1} = 43.05$ μH, $C_{p1} = 18.2$ nF, $C_{p2} = 11.6$ nF, $L_{p2} = 163.34$ μH, $R_{p1} = 0.03$ Ω, and $R_{p2} = 0.05$ Ω. With the rms value of the input voltage equaling 100 V, the absolute value of the inverter output current and the impedance angle of Z_T are shown in Fig. 5(a) and (b), respectively. Fig. 5(b) illustrates that Z_T has two zero phase angle (ZPA) points, one with a frequency of $\omega_1 = 2\pi \times 10^5$, and another with a frequency of $\omega_2 = 4\pi \times 10^5$. In this case, the two resonant frequencies of Z_T are ω_1 and ω_2. From Fig. 5(a), the absolute value of the inverter output current is 8.73 A at ω_1 and 9.67 A at ω_2. Fig. 6 shows the sweeping results of the output power and total input power. When the frequency of the input voltage is 100 kHz, the output power for Channel *A* is 0.86 kW, and the output power for Channel *B* is 1.46 mW. When the input voltage frequency is 200 kHz, the output power for Channel *A* is 0.41 mW, and the output power for Channel *B* is 0.96 kW.

B. Design of Secondary Parts

Compared to the traditional series compensation, the damping filters generate an additional resonant point in each receiver circuit, as shown in Fig. 4(c). If the additional resonant points are not handled well, the two power channels may affect each other. To better realize the decoupling of the two power channels, the frequency of the additional resonance point of one power channel should avoid being the odd multiples of the operating frequency of another power channel.

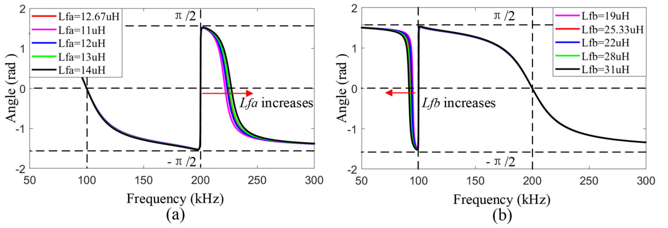


Fig. 7. Angles of the reflected impedance for different L_{fa} and L_{fb}. (a) Impedance angle of Z_{ra} for different L_{fa}. (b) Impedance angle of Z_{rb} for different L_{fb}.

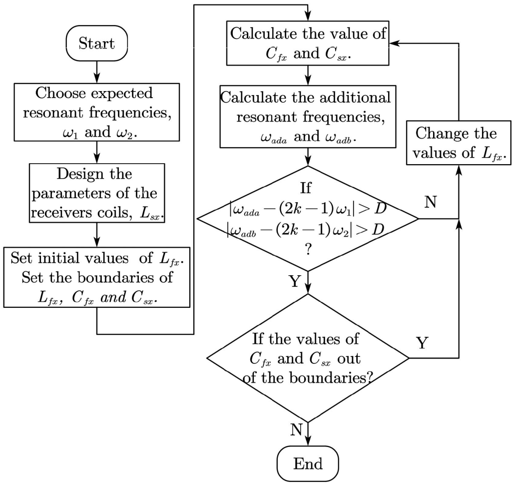


Fig. 8. Flowchart of the parameter design of receiver circuit.

Changing the values of L_{fa} and L_{fb} under the premise of satisfying equation (4), the frequencies of the additional resonant points will also change accordingly, as illustrated in Fig. 7. Therefore, the parameter design procedure can be obtained as Fig. 8.

First, the expected operating frequencies (ω_1 and ω_2) should be decided, which are also the resonant frequency and damping frequency of the receiver circuits. Then, L_{sx} ($x = a$ or b) are determined by the fabrication of the receiver coils. Next, the boundaries of L_{fx}, C_{fx}, and C_{sx} are defined, and all the selected values should be within the boundaries. Once L_{fx} are set to certain values, C_{fx} and C_{sx} will be calculated according to (4). Then, the additional resonant frequencies will be calculated and tested. L_{fx} will be set to new values unless all the parameters meet the requirements.

C. Design of Primary Part

As for the primary circuit design, the research work presented in [11] offers a parameter design method based on numerical calculations to find out the suitable parameters of the primary circuit. This method ensures that the frequencies corresponding to the ZPA points are the resonant frequencies required by the receiver circuit. Similarly, a parameter design method for the primary circuit is proposed to find suitable parameters.

When the value of L_{p1} keeps constant, changing the value of C_{p1} and C_{p2} will change the ZPA points of the primary circuit,

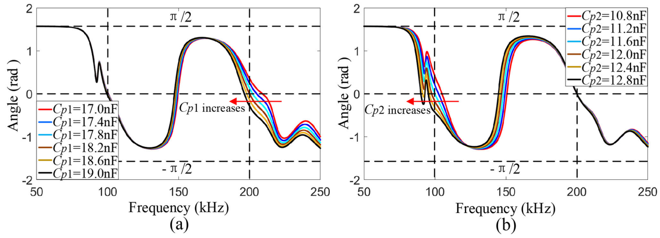


Fig. 9. Angles of Z_T for different C_{p1} and C_{p2}. (a) Angles of Z_T with the change of C_{p1}. (b) Angles of Z_T with the change of C_{p2}.

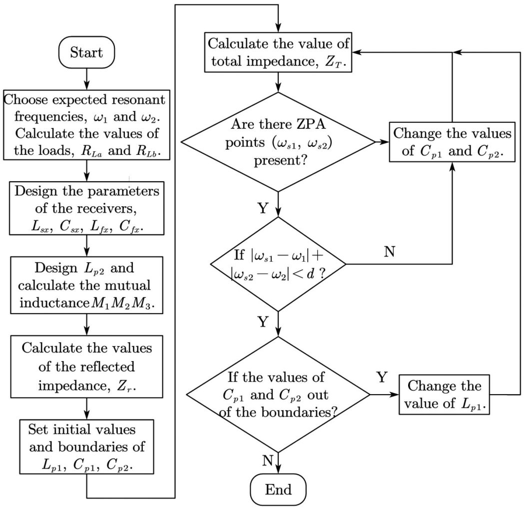


Fig. 10. Flowchart of the parameter design procedure of the primary circuit.

as shown in Fig. 9. As illustrated in Fig. 9, when the first ZPA point lies around 100 kHz, and the second ZPA point lies around 200 kHz, increasing the value of C_{p1} will decrease the frequency of the second ZPA point, whereas the frequency of the first ZPA point changes a little; increasing the value of C_{p2} will decrease the frequency of the first ZPA point, whereas the frequency of the second ZPA point changes a little. Therefore, the values of the frequencies of each ZPA point can be regulated separately by changing the values of C_{p1} and C_{p2}. Based on this principle, a detailed parameter design procedure of the primary circuit can be derived, as shown in Fig. 10.

First, the equivalent resistances of loads (R_{La} and R_{Lb}) can be calculated from the actual loads (R_{dca} and R_{dcb}). Then, L_{p2} is determined by the fabrication of the primary coil, and the mutual inductance (M_1, M_2, and M_3) can be measured. Next, based on the designed parameters of the receiver circuits, Z_r can be calculated. After that, the initial values and boundaries will be set for L_{p1}, C_{p1}, and C_{p2}. By changing the value of C_{p1} and C_{p2}, the ZPA points will shift, as shown in Fig. 9. L_{p1} will be assigned a new value if C_{p1} and C_{p2} are out of boundaries.

IV. CONTROL METHOD FOR THE PROPOSED WPT SYSTEM

A triangular carrier-based control method is used to regulate the output voltage of the inverter. The whole system can operate in three modes. For Mode I, the inverter generates both $u_{\text{in}1}$ and $u_{\text{in}2}$; therefore, both secondary loads can receive energy. For Mode II, the inverter only generates $u_{\text{in}1}$, and the only load in Receiver A can receive energy. In Mode III, only $u_{\text{in}2}$ is generated by the inverter, so the only load in Receiver B can receive energy.

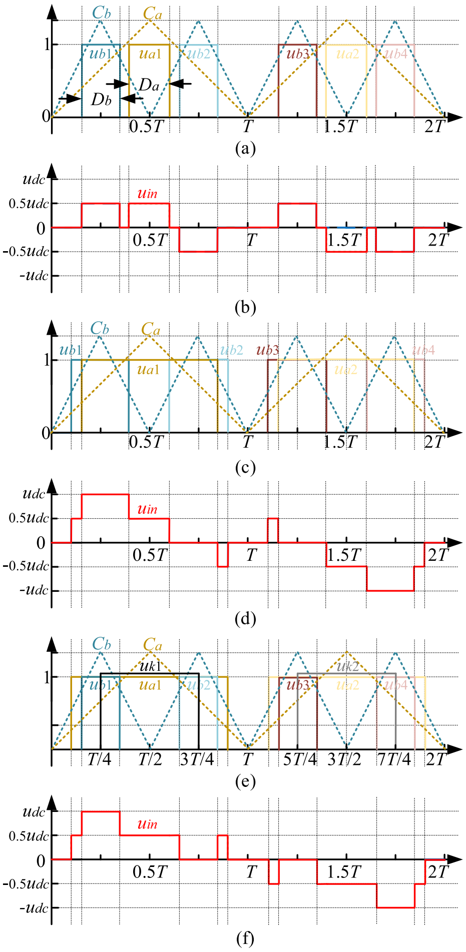


Fig. 11. Control waveforms of Mode I. (a) Pulses generation in Zone 1. (b) Inverter output voltage in Zone 1. (c) Pulses generation in Zone 2. (d) Inverter output voltage in Zone 2. (e) Pulses generation in Zone 3. (f) Inverter output voltage in Zone 3.

A. Control Method of Mode I

Fig. 11 shows the control process of Mode I in the time range from 0 to 2T, where $T = 2\pi/\omega_2$. As shown in Fig. 11(a), two triangular carriers are used to generate the control signals. One carrier (C_a) has the frequency of ω_1/2, and another carrier (C_b) has the frequency of ω_2/2. By setting two corresponding comparison values to the two sets of pulses (u_{am} and u_{bn}, $m\in\{1, 2\}$, $n\in\{1, 2, 3, 4\}$) can be achieved. u_{am} has a pulsewidth of D_a ($0\leq D_a\leq T$), and u_{bn} has a pulsewidth of D_b ($0\leq D_b\leq T/2$). Based on the value of D_a and D_b, three zones can be divided in Mode I, as shown in Fig. 12.

For Zone 1, all pulses have no overlap, and $D_b\leq 0.5T-D_a$; for Zone 2, overlaps occur in u_{am} and u_{bn}, $D_b>0.5T-D_a$, and $D_b> D_a-0.5T$; for Zone 3, overlaps occur in u_{am} and u_{bn}, and $D_b\leq D_a$-0.5T. The inverter output voltage has a different shape in each zone. Fig. 11(a), (c), and (e) shows the generation process of the pulses in Zones 1, 2, and 3, respectively. The control signals of each SIC-MOSFET can be obtained by doing logic operations to u_{am} and u_{bn}. Then, the inverter output voltage in

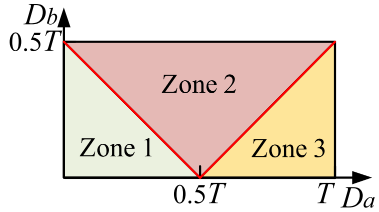


Fig. 12. Zone division in Mode I.

TABLE II
CONTROL SEQUENCE IN MODE I WITHOUT NP VOLTAGE BALANCE STRATEGY

Zone	Switching sequence
1	V_5-V_3-V_5-V_2-V_5-V_8-V_5-V_3-V_5-V_7-V_5-V_8-V_5
2	V_5-V_3-V_1-V_2-V_4-V_8-V_5-V_3-V_6-V_7-V_9-V_8-V_5
3	V_5-V_2-V_1-V_2-V_4-V_2-V_5-V_7-V_6-V_7-V_9-V_7-V_5

Zones 1–3 can be generated as shown in Fig. 11(b), (d), and (f), respectively. Two components of the inverter output voltage can be described as

$$\begin{cases} u_{\text{in1\_mode1}} = \frac{u_{\text{dc}}}{2}\left(u_{a1} - u_{a2}\right) \\ u_{\text{in2\_mode1}} = \frac{u_{\text{dc}}}{2}\left(u_{b1} - u_{b2} + u_{b3} - u_{b4}\right) \end{cases}. \tag{13}$$

The Fourier decomposition of u_{in} can be expressed as

$$u_{\text{in\_mode1}} = \sum_{k=1}^{\infty} \left\{ \underbrace{\left[1-(-1)^k\right]\frac{u_{\text{dc}}}{\pi k}\cos\left[k\pi\left(0.5-\frac{D_a}{2T}\right)\right]\sin\left(\frac{k\pi t}{T}\right)}_{u_{\text{in1}}} + \underbrace{\left[1-(-1)^k\right]\frac{U_{\text{dc}}}{\pi k}\cos\left[k\pi\left(0.5-\frac{D_b}{T}\right)\right]\sin\left(\frac{2k\pi t}{T}\right)}_{u_{\text{in2}}} \right\}. \tag{14}$$

From (14), it can be known that u_{in1} and u_{in2} do not contain even harmonics. u_{in1} only have the components with frequencies of $(2k-1)\omega_1$ ($k = 1,2,3,\ldots,$), and u_{in2} only have the components with frequencies of $(2k+1)\omega_1$. Thus, u_{in1} and u_{in2} have no overlap in the frequency spectrum. A simple way to meet (13) is to set $S_1 = u_{a1}$, $S_2 = u_{a2}$, $S_3 = u_{b2}+u_{b4}$, and $S_4 = u_{b1}+u_{b3}$. So, the value of u_{in1} is controlled by S_1 and S_2, and the value of u_{in2} is controlled by S_1 and S_2. In this way, the switching sequence for each zone is shown in Table II. However, regardless of the NP voltage, a specific switching sequence is applied in each zone, and the redundant medium switching states are not used to adjust the NP voltage balance. The voltages of two dc-link capacitors are prone to be imbalanced during operation, which will be discussed later.

The net charge injected to the NP in the time from 0 to $2T$ can be expressed as

$$\Delta Q_{NP} = -\int_0^{2T} i_o dt. \tag{15}$$

From Table I, i_o of medium switching states V_2, V_3, V_7, and V_8 do not equal zero. V_2 and V_3 have the same value of inverter output voltage but have opposite *io* directions; V_7 and V_8 have the same value of inverter output voltage but have opposite output voltage. By assigning appropriate medium switching states to each zone, adjusting the difference of dc-link capacitor voltage can be achieved.

The inverter output current can be regarded as the sum of two sinusoidal currents (one with a frequency of ω_1, and another with a frequency of ω_2) because ω_1 and ω_2 are the resonant frequency of the proposed system. Therefore, the inverter output current can be written as

$$\begin{cases} i_{\text{in1}} = I_{m1}\sin\left(\frac{\pi}{T}t - \varphi_1\right) \\ i_{\text{in2}} = I_{m1}\sin\left(\frac{2\pi}{T}t - \varphi_2\right) \\ i_{\text{in}} = i_{\text{in1}} + i_{\text{in2}} \end{cases} \tag{16}$$

where i_{in1} is the current with a frequency of ω_1 and an amplitude of I_{m1}, and φ_1 ($-\pi/2<\varphi_1<\pi/2$) is the phase difference between i_{in1} and u_{in1} in a real situation; i_{in2} is the current with a frequency of ω_2 and an amplitude of I_{m2}, and φ_2 ($-\pi/2<\varphi_2<\pi/2$) is the phase difference between i_{in2} and u_{in2} in a real situation.

Based on (15), (16), and Table I, in Zone 1, the net charge injected to the NP in the time from 0 to $2T$ can be calculated as

$$\Delta Q_{\text{NP\_zone1}} = -\int_0^{2T} i_o dt = - \left(k_{11}\int_{\frac{T}{4}-\frac{D_b}{2}}^{\frac{T}{4}+\frac{D_b}{2}} i_{\text{in}}dt + k_{12}\int_{\frac{T}{2}-\frac{D_a}{2}}^{\frac{T}{2}+\frac{D_a}{2}} i_{\text{in}}dt + k_{13}\int_{\frac{3T}{4}-\frac{D_b}{2}}^{\frac{3T}{4}+\frac{D_b}{2}} i_{\text{in}}dt + k_{14}\int_{\frac{5T}{4}-\frac{D_b}{2}}^{\frac{5T}{4}+\frac{D_b}{2}} i_{\text{in}}dt + k_{15}\int_{\frac{3T}{2}-\frac{D_a}{2}}^{\frac{3T}{2}+\frac{D_a}{2}} i_{\text{in}}dt + k_{16}\int_{\frac{7T}{4}-\frac{D_b}{2}}^{\frac{7T}{4}+\frac{D_b}{2}} i_{\text{in}}dt \right) \tag{17}$$

where k_{1x} (x$\in\{1, 2, 3, 4\}$) denote the relation between i_o and i_{in} and $k_{1x}\in\{1, -1\}$. For example, if V_2 is selected for the time from $T/4-D_b/2$ to $T/4-D_b/2$, $k_{11} = -1$, whereas if V_3 is selected for the time from $T/4-D_b/2$, $k_{11} = 1$. By assigning each value of k_{1x}, the medium switching states are selected for each time interval.

When no NP balance strategy is applied, [k_{11}, k_{12}, k_{13}, k_{14}, k_{15}, k_{16}] = [1, −1, 1, 1, −1, 1], and $\Delta Q_{\text{NP·zone1}}$ can be calculated as

$$\Delta Q_{\text{NP\_zone1\_1}} = \frac{2I_{m2}T\sin\left(\frac{D_a\pi}{T}\right)\sin\left(\varphi_2\right)}{\pi}. \tag{18}$$

In (18), depending on the value of φ_2, $\Delta Q_{\text{NP·zone1·1}}$ can be positive or negative. Moreover, in every period of $2T$, the net charge flowing into the NP will accumulate, which causes the imbalance of the NP voltage.

However, for [k_{11}, k_{12}, k_{13}, k_{14}, k_{15}, k_{16}] = [1, 1, 1, −1, −1, −1], $\Delta u_{\text{dc·zone1}}$ can be calculated as

$$\Delta Q_{\text{NP\_zone1\_2}} = -\frac{4I_{m1}T\cos\left(\varphi_1\right)\left[\sin\left(\frac{D_a\pi}{2T}\right)+\sqrt{2}\sin\left(\frac{D_b\pi}{2T}\right)\right]}{\pi}. \tag{19}$$

In this case, based on the boundaries of φ_1, D_a, and D_b, and their relations in Zone 1, $\Delta Q_{\text{NP·zone1·2}}\leq 0$, which should be

TABLE III
CONTROL SEQUENCE IN MODE I WITH NP VOLTAGE BALANCE

Zone	Condition	Switching sequence	Control signal
1	$u_{c1} \leq u_{c2}$	V_5-V_3-V_5-V_3-V_5-V_8-V_5-V_2-V_5-V_7-V_5-V_7-V_5	$S_1 = u_{b3}$, $S_2 = u_{a2} + u_{b4}$, $S_3 = u_{b2}$, $S_4 = u_{a1} + u_{b1}$.
	$u_{c1} > u_{c2}$	V_5-V_2-V_5-V_2-V_5-V_7-V_5-V_3-V_5-V_8-V_5-V_8-V_5	$S_1 = u_{a1} + u_{b1}$, $S_2 = u_{b2}$, $S_3 = u_{a2} + u_{b4}$, $S_4 = u_{b3}$.
2	$u_{c1} \leq u_{c2}$	V_5-V_3-V_1-V_3-V_5-V_8-V_5-V_2-V_5-V_7-V_9-V_7-V_5	$S_1 = u_{a1}u_{b1} + u_{b3}\overline{u_{a2}}$, $S_2 = u_{a2}\overline{u_{b3}} + u_{b4}$, $S_3 = u_{b2}\overline{u_{a1}} + u_{a2}u_{b4}$, $S_4 = u_{a1}\overline{u_{b2}} + u_{b1}$.
	$u_{c1} > u_{c2}$	V_5-V_2-V_1-V_2-V_5-V_7-V_5-V_3-V_5-V_8-V_9-V_8-V_5	$S_1 = u_{a1}\overline{u_{b2}} + u_{b1}$, $S_2 = u_{b2}\overline{u_{a1}} + u_{a2}u_{b4}$, $S_3 = u_{a2}\overline{u_{b3}} + u_{b4}$, $S_4 = u_{a1}u_{b1} + u_{b3}\overline{u_{a2}}$.
3	$u_{c1} \leq u_{c2}$	V_5-V_2-V_1-V_3-V_5-V_2-V_5-V_8-V_5-V_7-V_9-V_8-V_5	$S_1 = (u_{a1}\overline{u_{k1}}+u_{b1})\overline{u_{b2}}$, $S_2 = u_{k2}\overline{u_{b3}} + u_{b4}$, $S_3 = (u_{a2}\overline{u_{k2}}+u_{b4})\overline{u_{b3}}$, $S_4 = u_{k1}\overline{u_{b2}} + u_{b1}$.
	$u_{c1} > u_{c2}$	V_5-V_3-V_1-V_2-V_5-V_3-V_5-V7-V_5-V_8-V_9-V_7-V_5	$S_1 = u_{k1}\overline{u_{b2}} + u_{b1}$, $S_2 = (u_{a2}\overline{u_{k2}}+u_{b4})\overline{u_{b3}}$, $S_3 = u_{k2}\overline{u_{b3}} + u_{b4}$, $S_4 = (u_{a1}\overline{u_{k1}}+u_{b1})\overline{u_{b2}}$.

applied in the condition of $u_{c1} \leq u_{c2}$ to balance the NP voltage. Alternately, for $[k_{11}, k_{12}, k_{13}, k_{14}, k_{15}, k_{16}] = [-1, -1, -1, 1, 1, 1]$, $\Delta Q_{\text{NP }\dot{}\text{zone1}\dot{}2} \geq 0$, which should be applied in the condition of $u_{c2} > u_{c1}$. Thus, different switching sequences with opposite net charges injected into the NP can be applied to each SIC-MOSFET based on the condition of NP voltage, as shown in Table III.

Using the same method, we can also know that in Zones 2 and 3, when no NP balance strategy is applied, the net charge ΔQ_{NP} does not equal zero. Therefore, the NP voltage balance is not controllable. Also, suitable switching sequences for Zones 2 and 3 can be deduced to maintain NP voltage balance. The detailed derivation process can be found in Appendix.

As all the suitable switching sequences for Mode I have been obtained, the control signals of S_m ($m \in \{1, 2, 3, 4\}$) can be generated by doing logic operations to pluses in Fig. 11(a), (c), and (e). The control signals for each condition with NP voltage balance strategy are listed in Table III. It is noted that for Zone 3, two addition pluses (u_{k1} and u_{k2}) are required to generate S_m, as shown in Fig. 11(e). u_{k1} is a pulse with a value of 1 in the time range from $T/4$ to $3T/4$, and u_{k2} is a pulse with a value of 1 in the time range from $5T/4$ to $7T/4$.

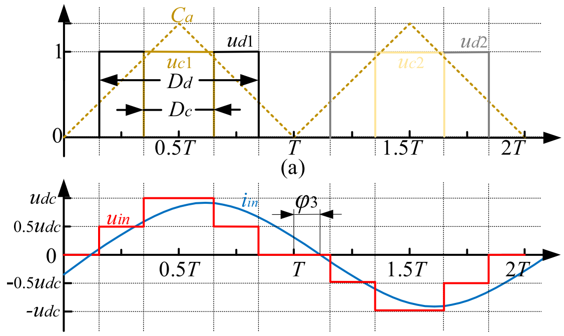


Fig. 13. Control for Mode II. (a) Pulses generation. (b) Inverter output voltage and current.

TABLE IV
CONTROL SEQUENCE IN MODE II AND MODE III WITHOUT NP VOLTAGE BALANCE STRATEGY

Mode	Switching sequence	Control signal
II	V_5-V_3-V_1-V_3-V_5-V_8-V_9-V_8-V_5	$S_1 = u_{c1}$, $S_2 = u_{c2}$, $S_3 = u_{d2}$, $S_4 = u_{d1}$.
III	V_5-V_3-V_1-V_3-V_5-V_8-V_9-V_8-V_5	$S_1 = u_{c1}$, $S_2 = u_{c2}$, $S_3 = u_{d2}$, $S_4 = u_{d1}$.

B. Control Method of Mode II and Mode III

For Mode II, $u_{\text{in2}} = 0$, and all the five-level voltages are used to generate u_{in1}. As shown in Fig. 13(a), two comparison values together with triangular carrier C_a are used to generate two sets of pulses u_{cm} and u_{dm} ($m \in \{1, 2\}$). u_{cm} have a pulsewidth of D_c, and u_{dm} have a pulsewidth of D_d. $0 \leq D_c \leq T$, $0 \leq D_d \leq T$, and $D_c \leq D_d$. Fig. 13(b) shows the inverter output voltage and current in Mode II, where φ_3 is the phase difference between u_{in} and i_{in}. In this case, u_{in} can be expressed as

$$u_{\text{in\_mode2}} = \frac{u_{\text{dc}}}{2}\left(u_{c1} + u_{d1} - u_{c2} - u_{d2}\right). \tag{20}$$

The Fourier decomposition of the inverter output voltage in Mode II can be expressed as

$$u_{\text{in\_mode2}} = \sum_{k=1}^{\infty}\left\{\left[1-(-1)^k\right]\frac{u_{\text{dc}}}{\pi k}\left\{\cos\left[k\pi\left(0.5-\frac{D_d}{2T}\right)\right]\right.\right.$$
$$\left.\left.+\cos\left[k\pi\left(0.5-\frac{D_c}{2T}\right)\right]\right\}\sin\left(\frac{k\pi}{T}t\right)\right\}. \tag{21}$$

When no NP voltage balance strategy is applied, the control signals can be set as $S_1 = u_{c1}$, $S_2 = u_{c2}$, $S_3 = u_{d2}$, and $S_4 = u_{d1}$, and the switching sequence is shown in Table IV.

The output current in Mode II can be written as

$$i_{\text{in}} = I_{m3}\sin\left(\frac{\pi}{T}t - \varphi_3\right). \tag{22}$$

In Mode II, the net charge injected to the NP in the time from 0 to $2T$ can be calculated as

$$\Delta Q_{\text{NP\_mode2}} = -$$
$$\int_0^{2T} i_o dt = -\left(k_{41}\int_{\frac{T}{2}-\frac{D_d}{2}}^{\frac{T}{2}-\frac{D_c}{2}} i_{\text{in}}dt + k_{42}\int_{\frac{T}{2}+\frac{D_c}{2}}^{\frac{T}{2}+\frac{D_d}{2}}\right.$$
$$\left. i_{\text{in}}dt + k_{43}\int_{\frac{3T}{2}-\frac{D_d}{2}}^{\frac{3T}{2}-\frac{D_c}{2}} i_{\text{in}}dt + k_{44}\int_{\frac{3T}{2}+\frac{D_c}{2}}^{\frac{3T}{2}+\frac{D_d}{2}} i_{\text{in}}dt\right). \tag{23}$$

TABLE V
CONTROL SEQUENCE IN MODE II AND MODE III WITH NP VOLTAGE BALANCE STRATEGY

Mode	Condition	Switching sequence	Control signal
II	$u_{c1} \leq u_{c2}$	V_5-V_3-V_1-V_3-V_5-V_7-V_9-V_7-V_5	$S_1 = u_{c1}$, $S_2 = u_{d2}$, $S_3 = u_{c2}$, $S_4 = u_{d1}$.
	$u_{c1} > u_{c2}$	V_5-V_2-V_1-V_2-V_5-V_8-V_9-V_8-V_5	$S_1 = u_{d1}$, $S_2 = u_{c2}$, $S_3 = u_{d2}$, $S_4 = u_{c1}$.
III	$u_{c1} \leq u_{c2}$	V_5-V_3-V_1-V_3-V_5-V_7-V_9-V_7-V_5	$S_1 = u_{e1}$, $S_2 = u_{f2}$, $S_3 = u_{e2}$, $S_4 = u_{f1}$.
	$u_{c1} > u_{c2}$	V_5-V_2-V_1-V_2-V_5-V_8-V_9-V_8-V_5	$S_1 = u_{f1}$, $S_2 = u_{e2}$, $S_3 = u_{f2}$, $S_4 = u_{e1}$.

When no NP balance strategy is applied, $[k_{41}, k_{42}, k_{43}, k_{44}] = [1, 1, 1, 1]$. $\Delta Q_{\mathrm{NP\cdot mode2}}$ can be calculated as

$$\Delta Q_{\mathrm{NP\_mode2\_1}} = 0. \tag{24}$$

From (24), we can know that when the system operates in Mode II, the net charge injected to the NP in every period of $2T$ is zero. Therefore, unlike the situation in Mode I, the net charge injected to NP will not accumulate even if no NP voltage balance strategy is applied in Mode II. However, the mismatch of the two dc-link capacitors can also lead to the imbalance of the NP voltage [17]. In this case, the NP voltage balance strategy in Mode II is still necessary.

For $[k_{41}, k_{42}, k_{43}, k_{44}] = [1, 1, -1, -1]$, $\Delta Q_{\mathrm{NP\cdot mode2}}$ can be calculated as

$$\Delta Q_{\mathrm{NP\_mode2\_2}} = \frac{4 I_{m3} T \cos(\varphi_3)\left[\sin\left(\frac{D_c\pi}{2T}\right) - \sin\left(\frac{D_d\pi}{2T}\right)\right]}{\pi}. \tag{25}$$

Because $D_c \leq D_d$ and $\Delta Q_{\mathrm{NP\cdot mode2\cdot 2}} \leq 0$, it should be applied in the condition of $u_{c1} \leq u_{c2}$ to balance the NP voltage. Alternately, for $[k_{41}, k_{42}, k_{43}, k_{44}] = [1, 1, -1, -1]$, $\Delta Q_{\mathrm{NP\cdot mode2\cdot 2}} \geq 0$, which should be applied in the condition of $u_{c2} > u_{c1}$. Therefore, with the NP voltage balance strategy, the suitable switching sequences and control signals in Mode II can be found as shown in Table V.

As for Mode III, $u_{\mathrm{in1}} = 0$. As shown in Fig. 14(a), two comparison values together with triangular carrier C_b are used to generate two sets of pulses u_{em} and u_{fm} ($m \in \{1, 2\}$). u_{em} have a pulsewidth of D_e, and u_{fm} have a pulsewidth of D_f. $0 \leq D_e \leq T/2$, $0 \leq D_f \leq T/2$, and $D_e \leq D_f$. As shown in Fig. 15(b), the shape of the inverter output voltage and current are similar to those in Mode III, despite their frequency becoming ω_2. φ_4 is the phase difference between u_{in} and i_{in}. The Fourier decomposition of the inverter output voltage in Mode III can be expressed as

$$u_{\mathrm{in\_mode3}} = \sum_{k=1}^{\infty}\left\{\left[1-(-1)^k\right]\frac{u_{\mathrm{dc}}}{\pi k}\left\{\cos\left[k\pi\left(0.5-\frac{D_f}{T}\right)\right] + \cos\left[k\pi\left(0.5-\frac{D_e}{T}\right)\right]\right\}\sin\left(\frac{k\pi}{T}t\right)\right\}. \tag{26}$$

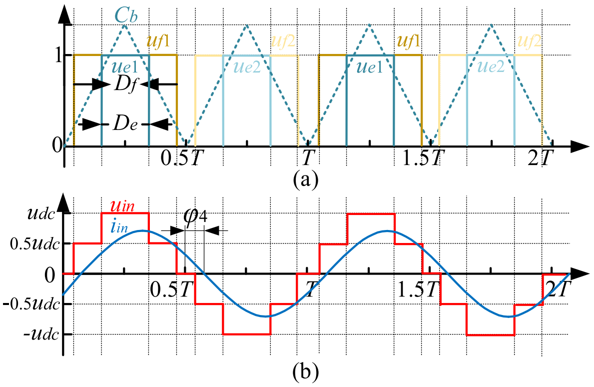


Fig. 14. Control for Mode III. (a) Pulses generation. (b) Inverter output voltage and current.

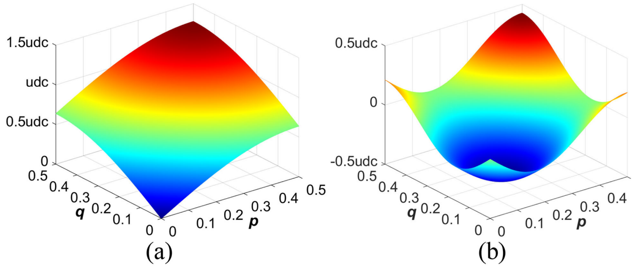


Fig. 15. Value of the first-order harmonic component and the third-order harmonic component. (a) First-order harmonic component. (b) Third-order harmonic component.

By applying the same analysis method used in Mode II, the switching sequences and control signals with or without NP voltage balance strategy can be obtained, as listed in Tables IV and V. The detailed derivation process can be found in Appendix.

C. *Third Harmonic Reduction Strategy*

According to (21) and (26), the amplitude of the first harmonic (m_1) of $u_{\mathrm{in\cdot mode2}}$ and $u_{\mathrm{in\cdot mode3}}$ can be expressed as

$$m_1 = \frac{2u_{\mathrm{dc}}}{\pi}\left[\sin(\pi p) + \sin(\pi q)\right] \tag{27}$$

where $p = D_d/2T$ and $q = D_c/2T$ for Mode II; $p = D_f/T$ and $q = D_e/T$, for Mode III; and $0 \leq p \leq 0.5$ and $0 \leq q \leq 0.5$.

From (27), it can be seen that the value of m_1 is subject to p and q. Taking the output power as a control object, the controller needs to control m_1. But, the same value of m_1 may correspond to countless combinations of values of p and q. The relation of p and q should be defined. The damping filters in the receivers can only deal with the cross-interference from the fundamental frequencies ω_1 and ω_2. However, their odd multiple can also cause cross-interference. It can be known from

(26) that $u_{\text{in}\cdot\text{mode2}}$ and $u_{\text{in}\cdot\text{mode3}}$ only have odd multiples. The third harmonic is the closest to the fundamental component in frequency. Due to the selectivity of the WPT system, the third harmonics are more likely to cause cross-interference between the two power channels than other odd harmonics. The third harmonics may also introduce additional losses and EMI issues. Therefore, a third harmonic reduction strategy is proposed to minimize the proportion of the third harmonic in Modes II and III.

The amplitude of the third harmonic (m_3) of $u_{\text{in}\cdot\text{mode2}}$ and $u_{\text{in}\cdot\text{mode3}}$ can be expressed as

$$m_3 = \frac{2u_{\text{dc}}}{3\pi}\left[\sin\left(3\pi p\right) + \sin\left(3\pi q\right)\right]. \tag{28}$$

The amplitudes of m_1 and m_3 in the case of p and q are shown in Fig. 15(a) and (b), respectively. m_1 and m_3 will vary with the change of p and q. The goal is to regulate the first harmonic amplitude and reduce the proportion of the third harmonic as much as possible. This is an optimization problem for solving the minimum absolute value of m_3. On minimizing the absolute value of (28) with (27), we can get the following results:

$$[p,q] = \begin{cases} \left[0.5 - \frac{1}{\pi}\cos^{-1}\left(\frac{\pi m_1}{2u_{dc}}\right), 0\right] \quad 0 \le m_1 \le \frac{\sqrt{3}}{\pi}u_{\text{dc}} \\ \left[\frac{2}{3} - \frac{1}{\pi}\cos^{-1}\left(\frac{\pi m_1}{2\sqrt{3}u_{dc}}\right), \frac{1}{3} - \frac{1}{\pi}\cos^{-1}\left(\frac{\pi m_1}{2\sqrt{3}u_{dc}}\right)\right] \\ \frac{\sqrt{3}}{\pi}u_{\text{dc}} < m_1 \le \frac{3}{\pi}u_{\text{dc}} \\ \left[\frac{1}{3} + \frac{1}{\pi}\cos^{-1}\left(\frac{\pi m_1}{2\sqrt{3}u_{dc}}\right), \frac{1}{3} - \frac{1}{\pi}\cos^{-1}\left(\frac{\pi m_1}{2\sqrt{3}u_{dc}}\right)\right] \\ \frac{3}{\pi}u_{\text{dc}} < m_1 \le \frac{2\sqrt{3}}{\pi}u_{\text{dc}} \\ \left[0.5 - \frac{1}{\pi}\cos^{-1}\left(\frac{\pi m_1}{4u_{dc}}\right), 0.5 - \frac{1}{\pi}\cos^{-1}\left(\frac{\pi m_1}{4u_{dc}}\right)\right] \\ \frac{2\sqrt{3}}{\pi}u_{\text{dc}} < m_1 \le \frac{4}{\pi}u_{\text{dc}} \end{cases}. \tag{29}$$

In (29), when $\sqrt{3}u_{\text{dc}}/\pi \leqslant m_1 \leqslant 2\sqrt{3}u_{\text{dc}}/\pi$, the selected combination of p and q can fully eliminate the third harmonic in u_{in}, which is $m_3 = 0$; when $0 \leqslant m_1 \leqslant \sqrt{3}u_{\text{dc}}/\pi$ or $2\sqrt{3}u_{\text{dc}}/\pi \leqslant m_1 \leqslant 4u_{\text{dc}}/\pi$, the selected combination of p and q can minimize $|m_3|$.

V. SIMULATION AND EXPERIMENT RESULTS

To verify the effectiveness of the proposed WPT system, simulations are conducted in MATLAB/Simulink. Also, a 1-kW prototype is established for experiments. As shown in Table VI, the parameters for simulations and experiments are identical, designed by the proposed methods in Section III.

A. Simulation Results

Fig. 16 shows the simulation results of the proposed WPT system in Mode I. Fig. 16(a), (c), and (e) shows the input and output waveforms of current (i_{in}, i_{sa}, and i_{sb}) and voltage (u_{in}, $u_{\text{out}\,a}$, and $u_{\text{out}\,b}$) in Zone 1 ($D_a = 0.2T$, $D_b = 0.2T$), Zone 2 ($D_a = 0.5T$, $D_b = 0.2T$), and Zone 3 ($D_a = 0.8T$, $D_b = 0.2T$), respectively. The dc-link voltage (u_{dc}) is 150 V and the proposed NP voltage balance strategy is applied. It can be known that the inverter output voltage and current are consistent with the previous analysis in Section IV. In these three figures, D_b keeps constant at $0.2T$, and only D_a is changed. Consequently, the output voltage of Receiver B ($u_{\text{out}\,b}$) keeps at 53 V, and the output voltage of Receiver A ($u_{\text{out}\,a}$) increases as D_a increases.

TABLE VI
PARAMETERS FOR SIMULATIONS AND EXPERIMENTS

Items	Value
Coil turns (n_p, n_{s1}, n_{s2})	17, 13.5, 13.5N
Coil inductance (L_{p2}, L_{sa}, L_{sb})	163.34, 63.81, 65.11μH
Primary compensation inductance (L_{p1})	43.05μH
Primary compensation capacitance (C_{p1}, C_{p2})	18.13, 11.31nF
Compensation capacitance for Receiver A (C_{fa}, C_{sa})	50.17, 31.39nF
Compensation inductance for Receiver A (L_{fa})	12.67μH
Compensation capacitance for Receiver B (C_{fb}, C_{sb})	99.87, 11.21nF
Compensation inductance for Receiver B (L_{fb})	25.33μH
Load resistance (R_{dca}, R_{dcb})	20, 20Ω
DC-link capacitance (C_1, C_2)	941, 946μF
Output capacitance (C_{dca}, C_{dcb})	472, 475μF
Mutual inductance of coils (M_1, M_2, M_3)	30.58, 31.81, -2.91μH
Operating frequency (f_1, f_2)	100, 200kHz

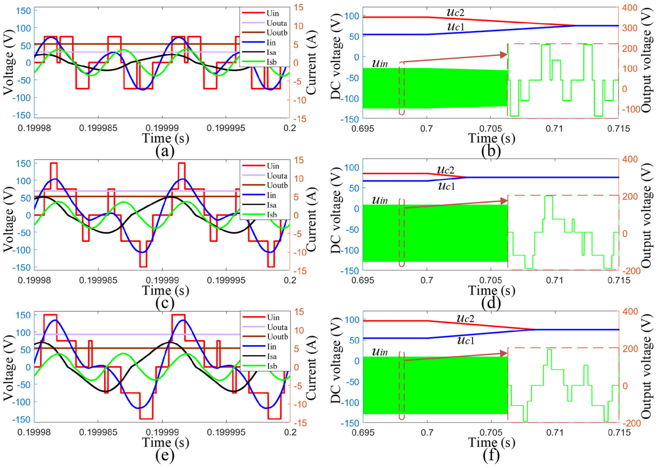


Fig. 16. Simulation results of the proposed WPT system in Mode I. (a) Input and output waveforms of current and voltage in Zone 1. (b) Comparison of control methods with and without NP balance strategy in Zone 1. (c) Input and output waveforms of current and voltage in Zone 2. (d) Comparison of control methods with and without NP balance strategy in Zone 2. (e) Input and output waveforms of current and voltage in Zone 3. (f) Comparison of control methods with and without NP balance strategy in Zone 3.

Fig. 16(b), (d), and (f) shows the comparisons of control methods with and without NP balance strategy in Zones 1, 2, and 3, respectively. The NP voltage balance strategy is added at the time of 0.7 s. When no NP voltage balance strategy is applied, the net charge injected to the NP will accumulate, which leads to the imbalance of the NP voltage. As shown in the simulation results, the voltage difference of the two dc-side capacitors is 41.5 V in Zone 1, 18.2 V in Zone 2, and 41.6 V in Zone 3. Because of the imbalance of the NP voltage, the inverter output voltage is distorted compared to the waveforms in Fig. 16(a), (c), and (e). However, after the NP voltage balance strategy is applied, the imbalance of the NP voltage can be eliminated in 0.015 s. This indicates the effectiveness of the NP voltage balance strategy in three operation zones of Mode I.

Fig. 17 shows the simulation results of the proposed WPT system in Mode II and Mode III. Fig. 17(a) and (c) shows the input and output waveforms of current (i_{in}, i_{sa}, and i_{sb})

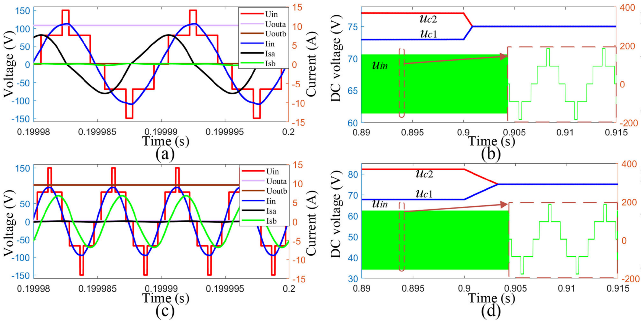


Fig. 17. Simulation results of proposed WPT system in Mode II and Mode III. (a) Input and output currents and voltages in Mode II. (b) Comparison of control methods with and without NP balance strategy in Mode II. (c) Input and output currents and voltages in Mode III. (d) Comparison of control methods with and without NP balance strategy in Mode III.

and voltage (u_{in}, $u_{\text{out}\,a}$, and $u_{\text{out}\,b}$) in Mode II and Mode III, respectively. The dc-link voltage (u_{dc}) is 150 V. The NP voltage balance strategy and the third harmonic reduction method are applied with $m_1 = 0.7u_{\text{dc}}$. In Fig.17(a), all the five voltage levels are used to generate $u_{\text{in}1}$ with a frequency of 100 kHz, and therefore, the output voltage of Receiver B ($u_{\text{out}\,b}$) is nearly equal to zero. Similarly, in Fig. 17(b), the output voltage of Receiver A ($u_{\text{out}\,a}$) is nearly equal to zero, which indicates that there is nearly no mutual interference between the two power channels. Besides, in both cases, fast Fourier transform (FFT) tests of u_{in} are conducted in MATLAB, which shows that the third-order harmonic of u_{in} is fully eliminated because of the proposed third harmonic reduction method.

Fig. 17(b) and (d) shows the comparisons of control methods with and without NP balance strategy in Mode II and Mode III. According to (24) and (38), when no NP balance strategy is applied, the net charge injected to the NP in every control period is zero. Therefore, when the parameters of the dc-link capacitors are identical, the NP voltage will keep balance. However, the imbalance of NP voltage can still come from the mismatch of the two dc-link capacitors. The capacitance tolerance of an aluminum electrolytic capacitor can be as high as ±20%, which makes the NP voltage balance strategy still necessary in Mode II and Mode III. To make the influence of the capacitance mismatch obvious, an additional 222 μF capacitor is connected parallelly to C_2. In this case, $C_1 = 941$ μF and $C_2 = 1168$ μF. The NP voltage balance strategy is added at the time of 0.9 s. When no NP voltage balance strategy is applied, the voltage difference of two dc-side capacitors is 4.1 V in Mode II and 14.4 V in Mode III. After the NP voltage balance strategy is applied, the imbalance of the dc-link voltage can be eliminated within 0.005 s. This indicates the effectiveness of the proposed NP voltage balance strategy in Mode II and Mode III.

B. Experimental Results

To demonstrate the proposed WPT system and verify the control methods, a 1-kW SIC-MOSFET testbed is established, as shown in Fig. 18. CREE discrete SIC-MOSFETs (C3M0060065K) are used as power switches (S_n and $\bar{S}_n$, $n \in \{1, 2, 3, 4\}$). The oscilloscope, current probe, and voltage probe are all from Tektronix, whose models are TPS 2024B, TCP A300, and P5200A. All the parameters in Table VI are measured by the LCR meter, KEYSIGHT E4980AL.

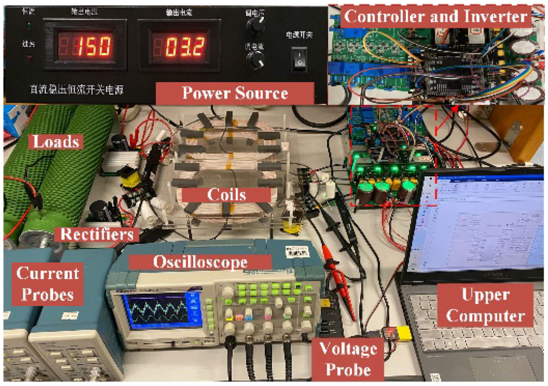


Fig. 18. 1-kW SIC-MOSFET testbed of the proposed WPT system.

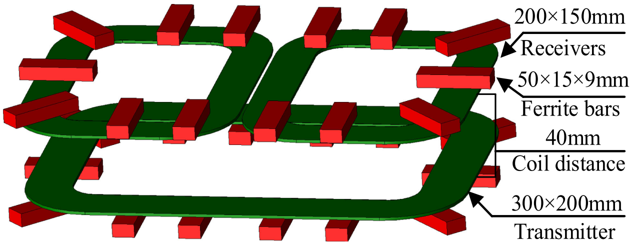
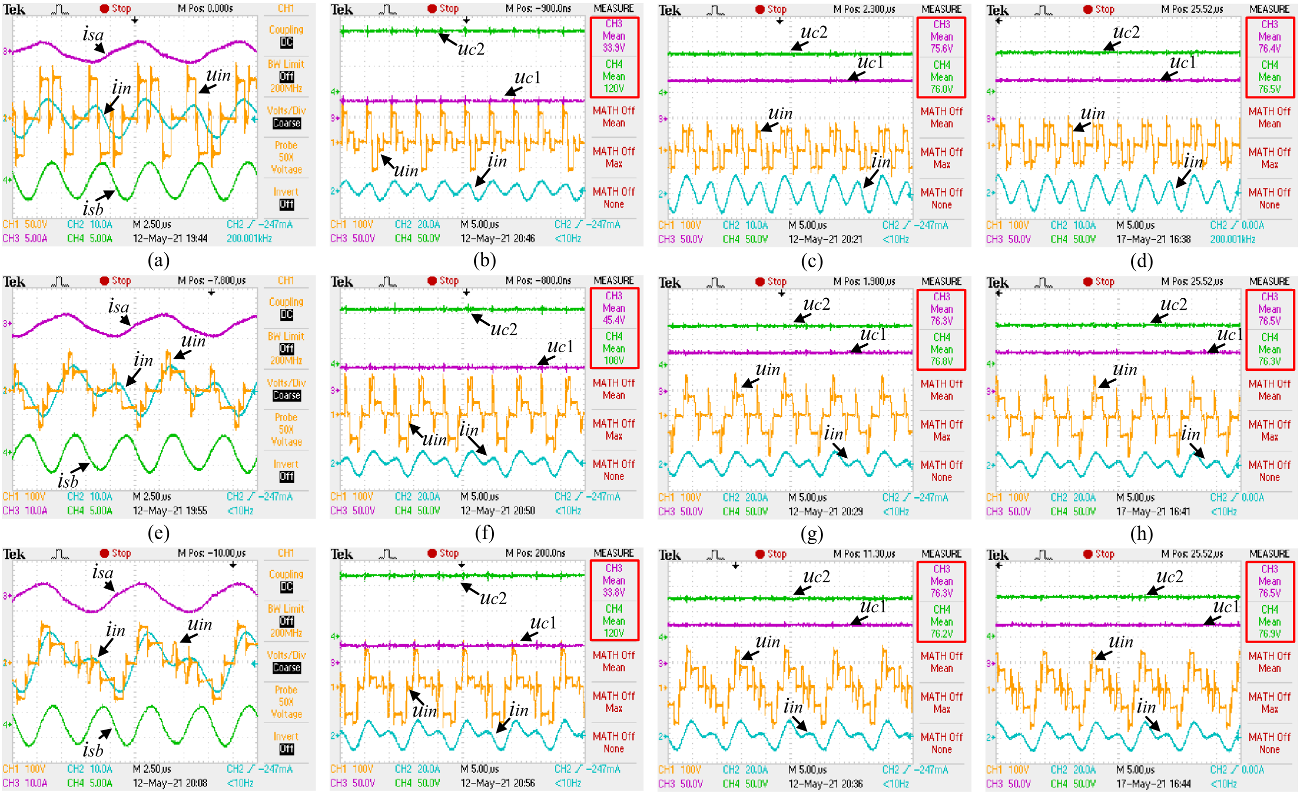


Fig. 19. 3-D coil structure of the proposed WPT system.

The controllers are DSP TMS320F28379D from TI and FPGA XC6LX25 from XILINX. The DSP is used to calculate the pulse width, while the FPGA is used to generate the control signals of each SIC-MOSFET by logic operations. Fig. 19 shows the 3-D coil structure of the proposed WPT system, where the size of the transmitter coil and receiver coils are marked. The dc-to-loads efficiency of the prototype is 84.1% at full load (500 W for each channel).

Fig. 20 shows the experimental results when the system operates in Mode I. When NP voltage balance strategy is applied, the inverter output voltage (u_{in}), inverter output current (i_{in}) and receiver coil currents (i_{sa} and i_{sb}) in Zone 1 ($D_a = 0.2T$, $D_b = 0.2T$), Zone 2 ($D_a = 0.5T$, $D_b = 0.2T$), and Zone 3 ($D_a = 0.8T$, $D_b = 0.2T$) are shown in Fig. 20(a), (e), and (i), respectively. The voltage and current waveforms are consistent with those in the simulation results. Besides, when D_b keeps constant, D_a increases, i_{sb} keeps almost constant and i_{sa} increases, which indicates that the two power channels are well-decoupled.

Fig. 20(b), (f), and (j) shows the waveforms of the inverter output voltage (u_{in}), inverter output current (i_{in}), and voltages of the dc-link capacitors (u_{c1} and u_{c2}) in the three operating zones without NP voltage balance strategy. According to the measurement values (marked in the red boxes) of the oscilloscope, the difference of u_{c1} and u_{c2} is 86.1 V in Zone 1, 62.6 V in Zone 2, and 86.2 V in Zone 3. The inverter output voltages are distorted compared with those in Fig. 20(a), (e), and (i), due to the imbalance of the NP voltage. Therefore, when the system operates in Mode I, the NP voltage is prone to be imbalanced, which conforms to the analysis in Section IV and the previous simulation results.



(a) (b) (c) (d)

(e) (f) (g) (h)

(i) (j) (k) (l)

Fig. 20. Experimental results of the proposed WPT system in Mode I. (a) u_{in}, i_{in}, i_{sa}, and i_{sb} in Zone 1. (b) u_{in}, u_{c1}, u_{c2}, and i_{in} in Zone 1 without NP voltage balance. (c) u_{in}, u_{c1}, u_{c2}, and i_{in} in Zone 1 with NP voltage balance. (d) u_{in}, u_{c1}, u_{c2}, and i_{in} in Zone 1 with NP voltage balance and capacitance mismatch. (e) u_{in}, i_{in}, i_{sa}, and i_{sb} in Zone 2. (f) u_{in}, u_{c1}, u_{c2}, and i_{in} in Zone 2 without NP voltage balance. (g) u_{in}, u_{c1}, u_{c2}, and i_{in} in Zone 2 with NP voltage balance. (h) u_{in}, u_{c1}, u_{c2}, and i_{in} in Zone 2 with NP voltage balance and capacitance mismatch. (i) u_{in}, i_{in}, i_{sa}, and i_{sb} in Zone 3. (j) u_{in}, u_{c1}, u_{c2}, and i_{in} in Zone 3 without NP voltage balance. (k) u_{in}, u_{c1}, u_{c2}, and i_{in} in Zone 3 with NP voltage balance. (l) u_{in}, u_{c1}, u_{c2}, and i_{in} in Zone 3 with NP voltage balance and capacitance mismatch.

Fig. 20(c), (g), and (k) are the waveforms of u_{in}, i_{in}, u_{c1}, and u_{c2} in the three operating zones with NP voltage balance strategy. When the proposed NP voltage balance strategy is applied, the difference of u_{c1} and u_{c2} in each operating zone can be reduced to within 0.5 V. This result proves the effectiveness of the proposed NP voltage balance strategy in Mode I.

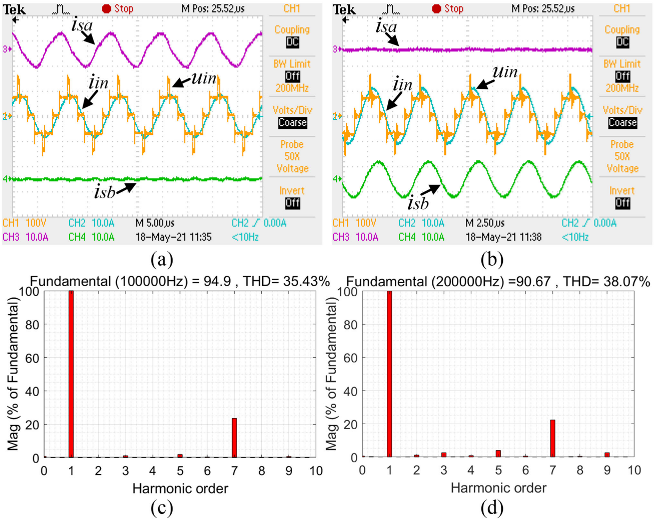
To demonstrate the performance of the proposed WPT system under the condition of dc-link capacitance mismatch, an additional 222 μF electrolytic capacitor is added to C_2. In this case, the measured capacitance of C_1 is 941 μF, and the measured capacitance of C_2 is 1168 μF. The waveforms of u_{in}, i_{in}, u_{c1}, and u_{c2} in the three operating zones with NP voltage balance strategy are shown in Fig. 20(c), (g), and (k). The difference between u_{c1} and u_{c2} can be controlled within 0.5 V in all three operating zones. Therefore, the proposed NP voltage balance strategy is still effective even under the condition of dc-link capacitance mismatch.

Fig. 21 shows the experimental results of the proposed WPT system in Modes II and III with NP voltage balance strategy and the third harmonic reduction method. m_1 is set as $0.7u_{\text{dc}}$ for both cases. As shown in Fig. 21(a) and (b), when the system operates in Mode II, i_{sb} is close to zero, and nearly no power is transferred to Receiver B. When the system operates in Mode III, i_{sa} is close to zero, and nearly no power is transferred to Receiver A.

By importing experimental data to MATLAB, FFT tests are conducted for u_{in} in Mode II and Mode III. Fig. 21(c) and (d) shows the FFT test results of u_{in} in Mode II and Mode III, respectively. According to the FFT test results, the third harmonic of u_{in} in each case is relatively small because of the proposed third harmonic reduction method. Also, the fundamental component of u_{in} in Mode III is a little smaller than that in Mode II because as the operating frequency increases, the influence of the dead time becomes greater.

Based on the analysis in Section IV, when the parameters of the two dc-link capacitors (C_1 and C_2) are identical, the NP voltage can keep balance in Mode II and Mode III even if no NP voltage balance strategy is applied.

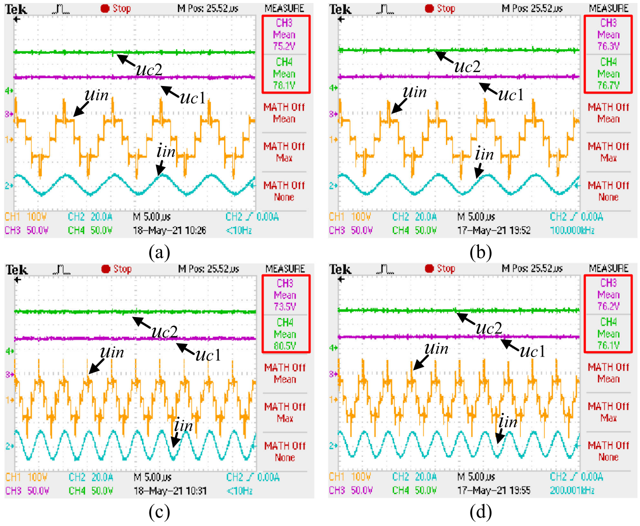
Because the net charge injected to NP in every cycle time is zero. Experiments are conducted in the condition of dc-link capacitance mismatch to verify the effectiveness of the proposed NP voltage balance strategy in Mode II and Mode III. With $C_1 = 941$ μF and $C_2 = 1168$ μF, the experimental waveforms of u_{in}, u_{c1}, u_{c2}, and i_{in} in Mode II and Mode III without NP voltage balance strategy are shown in Fig. 22(a) and (c). According to measurement results of the oscilloscope, the difference of u_{c1} and u_{c2} is 2.9 V in Fig. 22(a) and 7 V in Fig. 22(b), which is much smaller than that in Mode I. Fig. 22(b) and (d) shows the waveforms of u_{in}, u_{c1}, u_{c2}, and i_{in} in Mode II and Mode III with



(a) (b)

(c) (d)

Fig. 21. Experimental results of the proposed WPT system in Mode II and Mode III. (a) u_{in}, u_{c1}, u_{c2}, and $i_{\rm in}$ in Mode II. (b) $u_{\rm in}$, u_{c1}, u_{c2}, and $i_{\rm in}$ in Mode III. (c) FFT test result of $u_{\rm in}$ in Mode II. (d) FFT test result of $u_{\rm in}$ in Mode III.



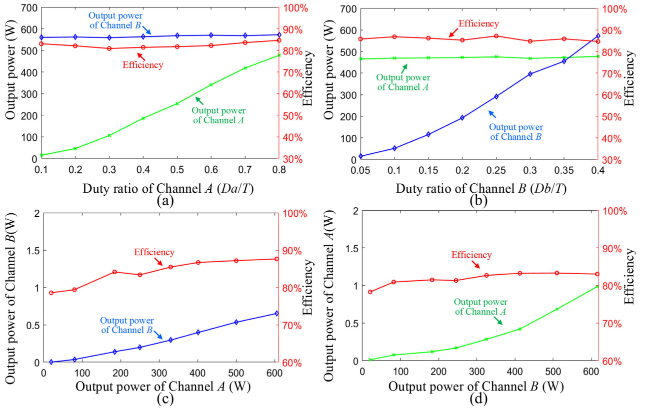
(a) (b)

(c) (d)

Fig. 22. Comparison of experimental results of the control methods with and without NP voltage balance strategy in Mode II and Mode III. (a) $u_{\rm in}$, u_{c1}, u_{c2}, and $i_{\rm in}$ in Mode II with capacitance mismatch and no NP voltage balance strategy. (b) $u_{\rm in}$, u_{c1}, u_{c2}, and $i_{\rm in}$ in Mode II with capacitance mismatch and NP voltage balance strategy. (c) $u_{\rm in}$, u_{c1}, u_{c2}, and $i_{\rm in}$ in Mode III with capacitance mismatch and no NP voltage balance strategy. (d) $u_{\rm in}$, u_{c1}, u_{c2}, and $i_{\rm in}$ in Mode III with capacitance mismatch and NP voltage balance strategy.

NP voltage balance strategy, where the difference of u_{c1} and u_{c2} is reduced to less than 0.5 V. Thus, in Mode II and Mode III, the proposed NP voltage balance strategy is effective and suitable for the condition of dc-link capacitance mismatch.

Some summarized plots of the output power and efficiency of the proposed system from experiments are shown in Fig. 23. Fig. 23(a) and (b) shows the results of Mode I. When the duty ratio of Channel B (D_b/T) keeps constant at 0.4, and the duty ratio of Channel A (D_a/T) varies from 0.1 to 0.8, the values of received power of two loads and the total efficiency (Total received power divide input power from dc power supply) are shown in Fig. 23(a). When the duty ratio of Channel A varies from 0.1 to 0.8, the variation of the received power of Channel B can keep below 2.6%. When the duty ratio of Channel A (D_a/T) keeps constant at 0.8, and the duty ratio of Channel B (D_b/T) varies from 0.1 to 0.4, the values of received power of two loads and the total efficiency are shown in Fig. 23(b). When the duty ratio of Channel B varies from 0.1 to 0.4, the variation of the received power of Channel A can keep below 2.4%. Fig. 23(a) and (b) indicates a good decoupling ability of the system operating in Mode I.



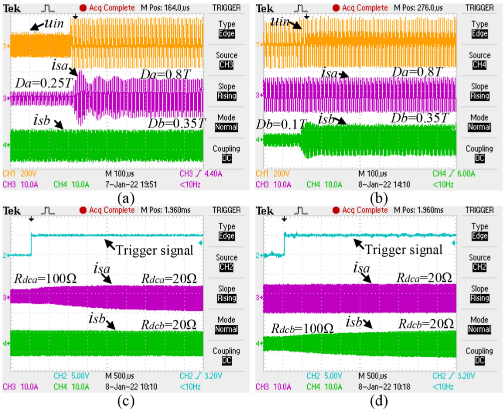
(a) (b)

(c) (d)

Fig. 23. Experimental results of output power and efficiency. (a) Output power and efficiency with variation of the duty ratio of Channel A in Mode I. (b) Output power and efficiency with the variation of the duty ratio of Channel B in Mode I. (c) Output power of Channel B and efficiency with the variation of the output power of Channel A in Mode II. (d) Output power of Channel A and efficiency with the variation of the output power of Channel B in Mode III.

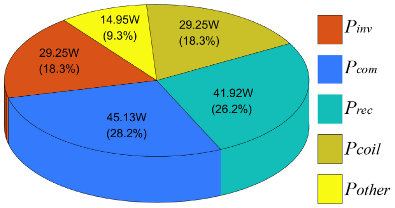
Fig. 23(c) and (d) shows the results of Mode II and Mode III. When the output power of Channel A changes from 20 to 600 W, the value of output power of Channel B and the efficiency (output power of Channel A divide input power from dc power supply) are shown in Fig. 23(c). When the output power of Channel B changes from 20 to 600W, the value of output power of Channel A and the efficiency (output power of Channel B divide input power from dc power supply) are shown in Fig. 23(d). Fig. 23(c) and (d) shows that when only one channel is targeted, another power channel can only receive less than 1/600 value of the power of the targeted channel, which indicates a good decoupling ability of the system operating in Mode II and Mode III.

To further demonstrate the dynamic performance and independent regulation ability of the proposed WPT system, experimental transient waveforms with duty ratio variation and load variation are exhibited, as shown in Fig. 24. Fig. 24(a) shows the waveforms of $u_{\rm in}$, i_{sa}, and i_{sb} when the duty ratio of Channel A (D_a) changes from $0.25T$ to $0.8T$, while the duty ratio of Channel B (D_b) constantly remains at $0.35T$. Fig. 24(a) indicates that after D_a changes, i_{sa} reaches a new steady-state after a transient process, and the amplitude of i_{sb} keeps constant. Similarly, in Fig. 24(b), when D_b changes from $0.1T$ to $0.35T$, and D_a constantly remains at $0.8T$, the amplitude of i_{sa} is not affected. Fig. 23(c) and (d) shows the waveforms of the secondary currents with load variation from Channel A and Channel B, respectively. Fig. 23(c) and (d) indicates that in the proposed WPT system, the transmitted power in a receiver is not influenced by the load change from other receivers.



(a) (b) (c) (d)

Fig. 24. Experimental transient waveforms. (a) Duty ratio variation for Channel *A*. (b) Duty ratio variation for Channel *B*. (c) Load variation for Channel *A*. (d) Load variation for Channel *B*.



Total losses: 160W DC to loads efficiency: 84.1%

Fig. 25. Power losses distribution.

The power loss distribution [11] for the prototype is calculated, shown in Fig. 25. The calculation is conducted with both power channels activated and reaches the maximum designed transmitted power (500 W for each power channel). The system losses consist of inverter losses P_{inv}, rectifier losses P_{rec}, compensation networks losses P_{Com}, coils losses P_{Coil}, and other losses P_{other}. Fig. 25 shows that the losses from compensation networks and rectifiers account for a large proportion of the system losses. Therefore, the fabrication of compensation networks and rectifiers is essential in improving system efficiency.

In Table VII, the proposed WPT system is compared with the existing O2M-WPT systems from the literature. The advantages of MLIs are incorporated into the proposed system. Therefore, the multifrequency superposition with independent power regulation ability is naturally realized without transformers and multiple inverters. Besides, the switching frequencies of the power switches are the same as the transmission frequencies. The efficiency of the prototype reaches 84.1%, which is relatively higher than the listed O2M-WPT systems.

VI. CONCLUSION

In this article, a decoupled multichannel WPT system based on MLIs is proposed to enable power transfer through independent channels with a simple system structure. The key contributions of the work are listed as follows.

1) A single-phase MLI is used to generate a voltage waveform that contains multiple frequency components. Thus, multifrequency superposition can be realized without a complex system structure, and each power channel can be regulated independently.
2) MFRCs are used to offer a primary circuit with multiple resonant compensations, which enhance the system efficiency. Damping filters are used in the receiver circuits to minimize the cross-interference issue.
3) Based on a dual-channel WPT system with a TNPC inverter, the topology features of the proposed system are studied with detailed parameter design procedures.
4) A control method with NP voltage balance and third harmonic reduction is proposed for a dual-channel WPT system.
5) Finally, both simulations and experiments indicate the effectiveness of the proposed WPT system and control methods.

APPENDIX

A. *Calculation of Control Method for Mode I*

For Zone 2, the net charge injected to the NP in the time from 0 to $2T$ can be calculated as

$$\Delta Q_{\text{NP\_zone2}} = -\int_0^{2T} i_o dt = - \left(k_{21}\int_{\frac{T}{4}-\frac{D_b}{2}}^{\frac{T}{2}-\frac{D_a}{2}} i_{\text{in}}dt + k_{22}\int_{\frac{T}{4}+\frac{D_b}{2}}^{\frac{3T}{4}-\frac{D_b}{2}} i_{\text{in}}dt + k_{23}\int_{\frac{T}{2}+\frac{D_a}{2}}^{\frac{3T}{4}+\frac{D_b}{2}} i_{\text{in}}dt + k_{24}\int_{\frac{5T}{4}-\frac{D_b}{2}}^{\frac{3T}{2}-\frac{D_a}{2}} i_{\text{in}}dt + k_{25}\int_{\frac{5T}{4}+\frac{D_b}{2}}^{\frac{7T}{4}-\frac{D_b}{2}} i_{\text{in}}dt + k_{26}\int_{\frac{3T}{2}+\frac{D_a}{2}}^{\frac{7T}{4}+\frac{D_b}{2}} i_{\text{in}}dt \right). \tag{30}$$

When no NP balance strategy is applied, based on Table II, $[k_{21}, k_{22}, k_{23}, k_{24}, k_{25}, k_{26}] = [1, -1, 1, 1, -1, 1]$. So, $\Delta Q_{\text{NP·zone2}}$ can be calculated as

$$\Delta Q_{\text{NP\_zone2\_1}} = \frac{2I_{m2}T\sin\left(\frac{D_a\pi}{T}\right)\sin\left(\varphi_2\right)}{\pi}. \tag{31}$$

Therefore, in Zone 2, when no NP balance strategy is applied, the NP voltage is prone to be imbalance. For $[k_{21}, k_{22}, k_{23}, k_{24}, k_{25}, k_{26}] = [1, 1, 1, -1, -1, -1]$, $\Delta Q_{\text{NP·zone2}}$ can be calculated as

$$\Delta Q_{\text{NP\_zone2\_2}} = \frac{4I_{m1}T\cos\left(\varphi_1\right)\left[\sin\left(\frac{D_a\pi}{2T}\right) - \sqrt{2}\cos\left(\frac{D_b\pi}{2T}\right)\right]}{\pi}. \tag{32}$$

Because $0 \leq D_a \leq T$, $0 \leq D_b \leq T/2$, and $-\pi/2 < \varphi_1 < \pi/2$, $\Delta Q_{\text{NP·zone2·2}} \leq 0$, which is suitable for the condition of $u_{c1} \leq u_{c2}$. Alternately, for $[k_{21}, k_{22}, k_{23}, k_{24}, k_{25}, k_{26}] = [-1, -1, -1, 1, 1, 1]$, $\Delta Q_{\text{NP·zone2·2}} \geq 0$, which is suitable for the condition of $u_{c1} > u_{c2}$.

Similarly, for Zone 3, the net charge injected to the NP in the time from 0 to $2T$ can be calculated as

$$\Delta Q_{\text{NP\_zone3}} = -\int_0^{2T} i_o dt = - \left(k_{31}\int_{\frac{T}{2}-\frac{D_a}{2}}^{\frac{T}{4}-\frac{D_b}{2}} i_{\text{in}}dt + k_{32}\int_{\frac{T}{4}+\frac{D_b}{2}}^{\frac{3T}{4}-\frac{D_b}{2}} i_{\text{in}}dt + k_{33}\int_{\frac{3T}{4}+\frac{D_b}{2}}^{\frac{T}{2}+\frac{D_a}{2}} i_{\text{in}}dt + k_{34}\int_{\frac{3T}{2}-\frac{D_a}{2}}^{\frac{5T}{4}-\frac{D_b}{2}} i_{\text{in}}dt + k_{35}\int_{\frac{5T}{4}+\frac{D_b}{2}}^{\frac{7T}{4}-\frac{D_b}{2}} i_{\text{in}}dt + k_{36}\int_{\frac{7T}{4}+\frac{D_b}{2}}^{\frac{3T}{2}+\frac{D_a}{2}} i_{\text{in}}dt \right). \tag{33}$$

When no NP balance strategy is applied, $[k_{31}, k_{32}, k_{33}, k_{34}, k_{35}, k_{36}] = [-1, -1, -1, -1, -1, -1]$. So, $\Delta Q_{\text{NP·zone3}}$ can be calculated as

$$\Delta Q_{\text{NP\_zone3\_1}} = \frac{2I_{m2}T\sin\left(\frac{D_a\pi}{T}\right)\sin\left(\varphi_2\right)}{\pi}. \tag{34}$$

Therefore, in Zone 3, when no NP balance strategy is applied, the NP voltage is prone to be imbalance. For $[k_{31}, k_{32}, k_{33}, k_{34}, k_{35}, k_{36}] = [-1, 1, -1, 1, -1, 1]$, $\Delta Q_{\text{NP·zone3}}$ can be calculated as

$$\Delta Q_{\text{NP\_zone3\_2}} = \frac{4I_{m1}T\cos\left(\varphi_1\right)\left[\sin\left(\frac{D_a\pi}{2T}\right) - \sqrt{2}\cos\left(\frac{D_b\pi}{2T}\right)\right]}{\pi}. \tag{35}$$

In this case, $\Delta u_{\text{dc·zone3}} \leq 0$, which is suitable for the condition of $u_{c1} \leq u_{c2}$. Alternately, for $[k_{31}, k_{32}, k_{33}, k_{34}, k_{35}, k_{36}] = [1, -1, 1, -1, 1, -1]$, $\Delta u_{\text{dc·zone3}} \geq 0$, which is suitable for the condition of $u_{c1} > u_{c2}$.

B. Calculation of Control Method for Mode III

The output current in Mode III can be written as

$$i_{in} = I_{m4}\sin\left(\frac{2\pi}{T}t - \varphi_4\right). \tag{36}$$

In Mode III, the net charge injected to the NP in the time from 0 to T can be calculated as

$$\begin{aligned} \Delta Q_{\text{NP\_mode3}} &= -\int_0^T i_o dt = \\ &- \left(k_{51}\int_{\frac{T}{4}-\frac{D_f}{2}}^{\frac{T}{4}-\frac{D_e}{2}} i_{\text{in}} dt + k_{52}\int_{\frac{T}{4}+\frac{D_e}{2}}^{\frac{T}{4}+\frac{D_f}{2}} \right. \\ &\left. i_{\text{in}} dt + k_{53}\int_{\frac{3T}{4}-\frac{D_f}{2}}^{\frac{3T}{4}-\frac{D_e}{2}} i_{\text{in}} dt + k_{54}\int_{\frac{3T}{4}+\frac{D_e}{2}}^{\frac{3T}{4}+\frac{D_f}{2}} i_{\text{in}} dt \right). \end{aligned} \tag{37}$$

When no NP balance strategy is applied, $[k_{51}, k_{52}, k_{53}, k_{54}] = [1, 1, 1, 1]$. $\Delta Q_{\text{NP·mode3}}$ can be calculated as

$$\Delta Q_{\text{NP\_mode3\_1}} = 0. \tag{38}$$

Therefore, the net charge injected to NP will not be accumulated during normal operation in Mode III.

For $[k_{51}, k_{52}, k_{53}, k_{54}] = [1, 1, -1, -1]$, $\Delta Q_{\text{NP·mode3}}$ can be calculated as

$$\Delta Q_{\text{NP\_mode3\_2}} = \frac{2I_{m4}T\cos\left(\varphi_4\right)\left[\sin\left(\frac{D_e\pi}{T}\right) - \sin\left(\frac{D_f\pi}{T}\right)\right]}{\pi}. \tag{39}$$

Because $D_e \leq D_f$, $\Delta Q_{\text{NP·mode3·2}} \leq 0$, it should be applied in the condition of $u_{c1} \leq u_{c2}$ to balance the NP voltage. Alternately, for $[k_{51}, k_{52}, k_{53}, k_{54}] = [-1, -1, 1, 1]$, $\Delta Q_{\text{NP·mode3·2}} \geq 0$, which should be applied in the condition of $u_{c2} > u_{c1}$. Therefore, with the NP voltage balance strategy, the suitable switching sequences and control signals in Mode III can be found as shown in Table V.

REFERENCES

[1] X. Lu, P. Wang, D. Niyato, D. I. Kim, and Z. Han, “Wireless charging technologies: Fundamentals, standards, and network applications,” *IEEE Commun. Surv. Tut.*, vol. 18, no. 2, pp. 1413–1452, Apr.–Jun 2016.

[2] Z. Zhang, H. Pang, A. Georgiadis, and C. Cecati, “Wireless power transfer—An overview,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 2, pp. 1044–1058, Feb. 2019.

[3] J. Pries, V. P. N. Galigekere, O. C. Onar, and G. Su, “A 50-kW three-phase wireless power transfer system using bipolar windings and series resonant networks for rotating magnetic fields,” *IEEE Trans. Power Electron.*, vol. 35, no. 5, pp. 4500–4517, May 2020.

[4] C. Zhao and D. Costinett, “GaN-based dual-mode wireless power transfer using multifrequency programmed pulse width modulation,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9165–9176, Nov. 2017.

[5] X. Zhang, F. Liu, and T. Mei, “Multifrequency phase-shifted control for multiphase multiload MCR WPT system to achieve targeted power distribution and high misalignment tolerance,” *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 991–1003, Jan. 2021.

[6] Y. Zhang, T. Lu, Z. Zhao, F. He, K. Chen, and L. Yuan, “Selective wireless power transfer to multiple loads using receivers of different resonant frequencies,” *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6001–6005, Nov. 2015.

[7] Y. Huang, C. Liu, Y. Zhou, Y. Xiao, and S. Liu, “Power allocation for dynamic dual-pickup wireless charging system of electric vehicle,” *IEEE Trans. Magn.*, vol. 55, no. 7, Jul. 2019, Art no. 8600106.

[8] C. Jiang, K. T. Chau, W. Liu, C. Liu, W. Han, and W. H. Lam, “An LCC-compensated multiple-frequency wireless motor system,” *IEEE Trans. Ind. Inform.*, vol. 15, no. 11, pp. 6023–6034, Nov. 2019.

[9] C. Jiang, K. T. Chau, C. Liu, and W. Han, “Design and analysis of wireless switched reluctance motor drives,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 245–254, Jan. 2019.

[10] H. Sarnago, O. Lucía, and J. M. Burdio, “Multiresonant power converter for improved dual-frequency induction heating,” *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2097–2103, Mar. 2019.

[11] F. Liu, Y. Yang, Z. Ding, X. Chen, and R. M. Kennel, “A multifrequency superposition methodology to achieve high efficiency and targeted power distribution for a multiload MCR WPT system,” *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 9005–9016, Oct. 2018.

[12] Y. Huang, C. Liu, Y. Xiao, and S. Liu, “Separate power allocation and control method based on multiple power channels for wireless power transfer,” *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9046–9056, Sep. 2020.

[13] W. Zhong and S. Y. R. Hui, “Auxiliary circuits for power flow control in multifrequency wireless power transfer systems with multiple receivers,” *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5902–5910, Oct. 2015.

[14] M. Fu, T. Zhang, X. Zhu, P. C. Luk, and C. Ma, “Compensation of cross coupling in multiple-receiver wireless power transfer systems,” *IEEE Trans. Ind. Inform.*, vol. 12, no. 2, pp. 474–482, Apr. 2016.

[15] R. Narayanamoorthi, A. V. Juliet, and B. Chokkalingam, “Cross interference minimization and simultaneous wireless power transfer to multiple frequency loads using frequency bifurcation approach,” *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10898–10909, Nov. 2019.

[16] F. Liu, Y. Yang, Z. Ding, X. Chen, and R. M. Kennel, “Eliminating cross interference between multiple receivers to achieve targeted power distribution for a multifrequency multi-load MCR WPT system,” *IET Power Electron.*, vol. 11, no. 8, pp. 1321–1328, 2018.

[17] Z. Zhang, X. Li, H. Pang, H. Komurcugil, Z. Liang, and R. Kennel, “Multiple-frequency resonating compensation for multichannel transmission of wireless power transfer,” *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5169–5180, May 2021.

[18] T. T. Davis and A. Dey, “A neutral point voltage balancing scheme with improved transient performance for 5-level ANPC and TNPC inverters,” *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12513–12523, Dec. 2019.

[19] K. Wang, L. Xu, Z. Zheng, and Y. Li, “Capacitor voltage balancing of a five-level ANPC converter using phase-shifted PWM,” *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1147–1156, Mar. 2015.

[20] W. Ding, L. Ming, C. Yin, M. Chen, and P. C. Loh, “Differential-mode filters with common-mode neutral-point-balancing accelerators for single-phase symmetrical five-level converters,” *IEEE Trans. Power Electron.*, vol. 36, no. 8, pp. 9209–9220, Aug. 2021.

[21] K. Chen, W. Jiang, and P. Wang, “An extended DPWM strategy with unconditional balanced neutral point voltage for neutral point clamped three-level converter,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8402–8413, Nov. 2019.

[22] S. Wang, J. Ma, B. Liu, N. Jiao, T. Liu, and Y. Wang, "Unified SVPWM algorithm and optimization for single-phase three-level NPC converters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7702–7712, Jul. 2020.
[23] G. A. Covic, J. T. Boys, M. L. G. Kissin, and H. G. Lu, "A three-phase inductive power transfer system for roadway-powered vehicles," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 3370–3378, Dec. 2007.
[24] J.-H. Cheng and A. F. Witulski, "Simple design of selected 3-element converters by scaling the solution of the LC parallel resonant converter," in *Proc. Appl. Power Electron. Conf.*, 1996, vol. 1, pp. 284–290.
[25] W. Gao and W. M. Snelgrove, "A linear integrated LC bandpass filter with Q-enhancement," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 45, no. 5, pp. 635–639, May 1998.
[26] Q. Deng *et al.*, "Frequency-dependent resistance of litz-wire square solenoid coils and quality factor optimization for wireless power transfer," *IEEE Trans. Ind. Electron.*, vol. 63, no. 5, pp. 2825–2837, May 2016.
[27] W. Li, H. Zhao, J. Deng, S. Li, and C. C. Mi, "Comparison study on SS and double-sided LCC compensation topologies for EV/PHEV wireless chargers," *IEEE Trans. Veh. Technol.*, vol. 65, no. 6, pp. 4429–4439, Jun. 2016.
[28] C. Xiao, D. Cheng, and K. Wei, "An LCC-C compensated wireless charging system for implantable cardiac pacemakers: Theory, experiment, and safety evaluation," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 4894–4905, Jun. 2018.
[29] Q. Deng *et al.*, "Modeling and control of inductive power transfer system supplied by multiphase phase-controlled inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 9303–9315, Sep. 2019.
[30] C. Xia, N. Wei, H. Zhang, S. Zhao, Z. Li, and Z. Liao, "Multifrequency and multiload MCR-WPT system using hybrid modulation waves SPWM control method," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12400–12412, Nov. 2021.

Yuxin Liu (Student Member, IEEE) received the B.Eng. degree in electrical engineering and automation from Tongji University, Shanghai, China, in 2017, and the M.Eng. degree in electrical engineering from South China University of Technology, Guangzhou, China, in 2020. He is currently working toward the Ph.D. degree in electrical and electronic engineering from City University of Hong Kong, Hong Kong.

His main research interests include power electronics, wireless power transmission, and control of power converters.

Chunhua Liu (Senior Member, IEEE) received the B.Eng. and M.Eng. degrees in automatic control from Beijing Institute of Technology, Beijing, China, in 2002 and 2005, respectively, and the Ph.D. degree in electrical and electronic engineering with The University of Hong Kong, Hong Kong, in 2009.

He is currently an Associate Professor in electrical and electronic engineering with the School of Energy and Environment, City University of Hong Kong, Hong Kong. In addition, he is a Distinguish Lecturer of IEEE Vehicular Technology Society and World's Top 2% Scientists according to metrics compiled by Stanford University. His research interests include electric machines and drives, electric vehicles and aircrafts, electric robotics and ships, renewables and microgrids, power electronics, and wireless power transfer. In these areas, he has authored or coauthored more than 250 refereed papers.

Dr. Liu is currently an Associate Editor for the IEEE TRANSACTION ON INDUSTRIAL ELECTRONICS, Editor of the IEEE TRANSACTIONS ON VEHICULAR TECHNOLOGY, Editor of the IEEE TRANSACTIONS ON ENERGY CONVERSION, and Editor of the IEEE POWER ENGINEERING LETTERS. Also, he is an Editor of Energies, a Subject Editor of *IET – Renewable Power Generation*, an Associate Editor of *Open Journal of the Industrial Electronics Society*, an Associate Editor of the IEEE CHINESE JOURNAL OF ELECTRICAL ENGINEERING, and an Editor of the IEEE TRANSACTIONS ON MAGNETICS – CONFERENCE. In addition, he is the Chair & Founder for both Hong Kong Chapter, IEEE Vehicular Technology Society, and Hong Kong & Guangzhou Joint Chapter, IEEE Industrial Electronics Society, respectively.

Xingran Gao received the B.S. degree in automation and the Ph.D. degree in mechatronics from Wuhan University, Wuhan, China, in 2013 and 2019, respectively.

He is currently a Postdoctoral Researcher in electrical and electronic engineering with the City University of Hong Kong, Hong Kong. His main research interests include power electronics, wireless power transmission, electric vehicle technology, and motor driving technologies.

Senyi Liu (Member, IEEE) received the B.Eng. and M.Eng. degrees in vehicle engineering from Tongji University, Shanghai, China, in 2015 and 2018, respectively, and the Ph.D. degree in electrical and electronic engineering from City University of Hong Kong (CityU), Hong Kong, in 2021.

He is currently a postdoctoral fellow in CityU. His main research interests include advanced control of motor drive systems, electric servo system, and wireless power transmission.