# Common High-Frequency Bus-Based Cascaded Multilevel Solid-State Transformer With Ripple and Unbalance Power Decoupling Channel

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***Abstract*—A novel three-port cascaded multilevel solid-state transformer (CM-SST) is proposed in this article, which is based on modular multilevel converter submodules (SM) interconnected by high-frequency link (HFL), forming a decoupling channel to SMs and a low-voltage dc port. The common high-frequency bus in HFL helps to reduce the numbers of secondary full bridges in the form of multiplexing. The decoupling channel achieves the automatic balancing of capacitors voltage and natural elimination of SM ripple power, so the arms second-order circulating current can be eliminated from the root cause. Therefore, the CM-SST can simultaneously realize the switches decreasing, capacitance size reducing, arms circulating current elimination, and control simplification. In this article, the topology, equivalent model, HFL design, ripple-power decoupling, power loss, and control scheme are analyzed in detail. In addition, an evaluation of CM-SST compared with the traditional methods is provided, including sizing, components count, control, and efficiency. Finally, the correctness and effectiveness of the proposed scheme are verified by the simulation and experiment.**

***Index Terms*—High-frequency link (HFL), modular multilevel converter (MMC), ripple power, solid-state transformer (SST), voltage balance.**

NOMENCLATURE

| | |
|---|---|
| SST | Solid-state transformer. |
| MMC | Modular multilevel converter. |
| SM | Submodule. |
| CM-SST | Cascaded multilevel SST. |
| HFL | High-frequency link. |
| DAB | Dual-active bridge. |
| TAB | Triple-active bridge. |
| CHFB | Common high-frequency bus. |
| FB | Full-bridge. |
| FBL | FB and phase-shift inductor $L_r$. |
| CDM$^2$C-SST | SST based on MMC MVdc bus cascading centralized DABs. |
| DDM$^2$C-SST | SST based on MMC SMs dc bus cascading distributed DABs. |
| MVac | Medium-voltage alternating current. |
| MVdc | Medium-voltage direct current. |
| LVdc | Low-voltage direct current. |

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## I. INTRODUCTION

OVER the past decade, the increase in the proportion of renewable energy and dc load, as well as users' demand for the high quality of power supply, has promoted the development of power interface technology. Solid-state transformer (SST) is a typical representative, which is claimed by many scholars that it will replace the bulky traditional power–frequency transformer in multiple application fields in the future [1]–[3]. The advantages of SST are that it can actively control power flow, integrate energy storage, limit fault current, improve power quality, realize networked communication, and many others [3]–[6].

In the medium- and high-voltage power conversion system, SST based on multilevel converter cascading isolated dc/dc converters is the current typical scheme. The multilevel converter mainly includes cascaded H-bridge (CHB) and modular multilevel converter (MMC) [7]–[9], and the dual-active bridge (DAB) is the main method for isolated dc/dc converter [10]. In order to expand the working range of the energy router in the dc microgrid, a CHB-DAB SST topology was proposed in [11], and the power multidirectional exchange mechanism between medium-voltage alternating current (MVac) port and clustered low-voltage direct current (LVdc) ports was discussed. In order to optimize the operation capability of SST under three-phase unbalance, a three-stage SST topology of CHB-DAB-buck/boost was proposed in [12] in which the LVdc port of each phase outputs separately, and an unbalance compensation scheme was discussed, which achieves good unbalance control effect. Others, such as high-frequency transformer (HFT) design [13], voltages balancing control [14], ripple-power suppression [15], active power limitation [16], and so on for CHB-SST, were also widely discussed. The future medium-voltage power distribution network presents the characteristics of multiport and multibus. MMC is the preferred solution in the discussion of medium-voltage multiport SST topology due to its MVdc bus and high module scalability.

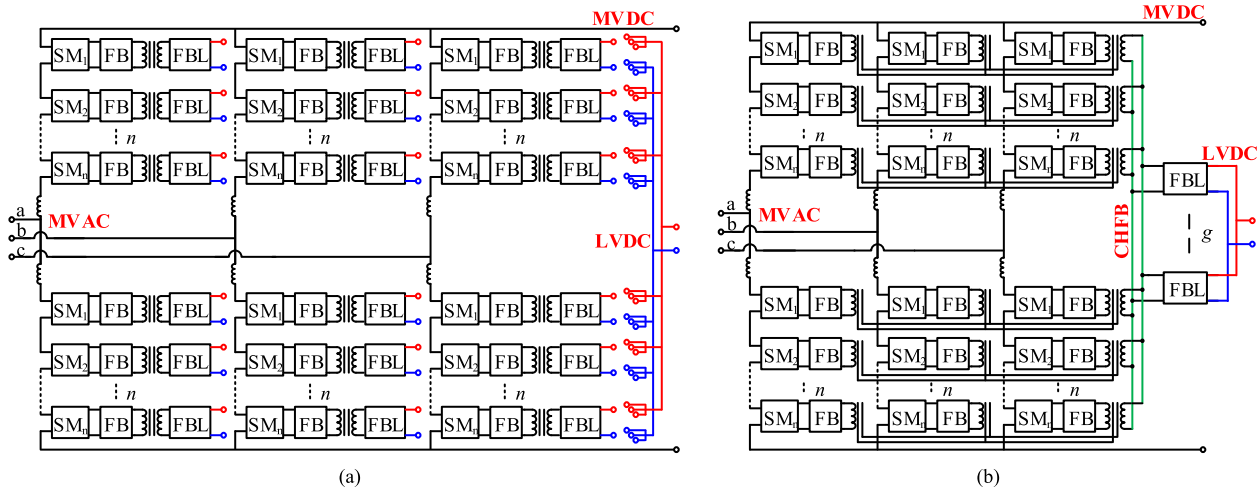


Fig. 1. Two types of MMC-based SST topologies. (a) DDM$^2$C-SST in [23]–[29]. (b) Proposed CM-SST.

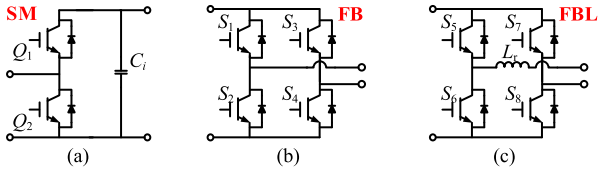


Fig. 2. Module circuits. (a) SM. (b) FB. (c) FBL.

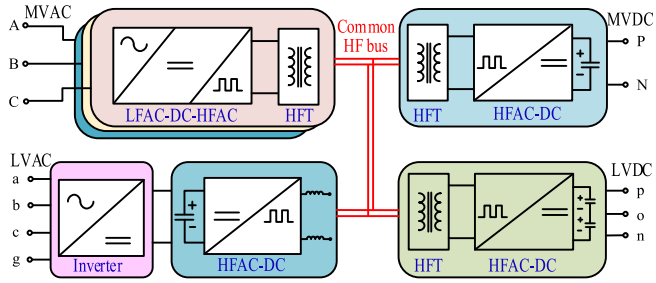


Fig. 3. Multiplexing scheme based on common high-frequency ac bus.

There have been several topology schemes suggested for MMC hybrid dc/dc-based SST. An SST (CDM$^2$C-SST) topology in which MMC MVdc bus and input-series-output-parallel (ISOP) centralized DABs are cascaded was first proposed in [17] and [18]. While realizing medium-voltage ac and dc power conversion, renewable energy systems can be connected through low-voltage ports. The parameters design principle [19], power flow control scheme [20], power quality improvement [21], etc., of CDM$^2$C-SST in the application of hybrid ac and dc low-voltage power transmission have been continuously studied. The advantage of CDM$^2$C-SST is that the ISOP isolation stage can be flexibly configured according to voltage level, while the disadvantages are that it needs more dc capacitors and power balance control, and high DAB cell power capacity is required [22].

Therefore, to cope with the above issues, the SST based on MMC submodules (SMs) dc bus cascading distributed DABs (DDM$^2$C-SST) is further proposed [23]–[31], as shown in Fig. 1(a). The full-bridge (FB), FB and phase-shift inductor $L_r$ (FBL), as shown in Fig. 2, and the HFT form a DAB unit. Briz *et al.* [23], [24] discussed the application potential of DDM$^2$C-SST in distributed energy storage, proposed the corresponding energy management control scheme, and discussed the required hardware and software configuration. Bayat and Yazdani [25], [26] proposed a DDM$^2$C-SST applied to distributed photovoltaic and energy storage management system and analyzed the control scheme of power balance between MMC arms and phase units by configuring a few energy storage units in arms. Xu *et al.* [27]–[29] analyzed the fault tolerance capability of DDM$^2$C-SST and the dc side short-circuit fault ride-through capability, and the influence of the fault on instantaneous power of the MMC arms and SM capacitor voltage was estimated with mathematical deduction. Aiming at the demand of high power density in SST system, the size optimization of SM capacitor is realized from the perspective of software [30] and hardware [31] by virtue of the natural advantages of DDM$^2$C-SST topology. The above research articles fully demonstrate that DDM$^2$C-SST has great potential in the medium- and low-voltage multiport conversion system, but it still has problems, such as large SM capacitance, too many FBs and HFTs, and complicated drive.

As shown in Fig. 3, an SST topology scheme based on a common high-frequency ac bus is proposed in [32]–[34], which is an idea of FB modules multiplexing. In multistage transformation, the number of FB modules is reduced by reducing the number of transformation stages and effectively reducing the cost and size of the system. In the context of multiport applications, the bidirectional dc/dc converter, such as triple/quad/multi-active bridge with a multiterminal transformer, is another FB multiplexing solution and can achieve the decreasing of HFTs number [35], [36]. The above two multiplexing schemes provide theoretical support for the research of this article.

Aiming at the application of hybrid medium- and low-voltage multibus multiport distribution network, this article proposes a cascaded multilevel solid-state transformer (CM-SST), as shown

in Fig. 1(b), which is composed by MMC stage and high-frequency link (HFL) stage based on a common high-frequency ac bus common high-frequency bus (CHFB). The CHFB in HFL helps to reduce the numbers of secondary FBs in the form of multiplexing, and the decoupling channel achieves the natural elimination of SM ripple power and automatic balancing of capacitors voltage. Therefore, the CM-SST can simultaneously realize the switches decreasing, capacitance size reducing, arms circulating current elimination, and control simplification.

The rest of this article is organized as follows. In Section II, the topology, equivalent model, and power flow of CM-SST are introduced. Section III analyzes the clamped characteristic of SMs voltage in detail, which helps to achieve the automatic balancing of SMs voltage, and the natural elimination of SMs ripple power and arms circulating current. Section IV provides the design and evaluation results of CM-SST compared with the existing representative MMC-SST, including the sizing, efficiency, and control. Section V gives the simulation and experimental verification results. Finally, Section VI concludes this article.

## II. Cascaded Multilevel Solid-State Transformer

### A. CM-SST Topology

Focusing on the application of hybrid medium- and low-voltage multibus multiport distribution network, the CM-SST topology proposed in this article is shown in Fig. 1(b), and the module circuits are shown in Fig. 2. Based on the conventional MMC, triple-active bridge (TAB) composed of three FB modules and a four-terminal HFT in HFL is cascaded with the horizontal three SMs, and the secondary windings of all HFT are in parallel, so a CHFB can be formed, which provides a power channel between SMs. The FBL modules are in parallel connection to realize active power interaction between LVdc bus and CHFB.

In addition to power transmission among the three ports of CM-SST, TAB has realized the interconnection of horizontal three SMs. In addition, TAB does not have phase-shifting inductors and exists low impedance under synchronous-switching modulation. Therefore, SMs capacitor voltages are clamped to each other, showing switched capacitors' characteristics. All TABs are interconnected to provide an unbalanced power transfer channel between vertical SMs.

### B. Equivalent Model and Power Flow

CM-SST can realize power interaction among three ports, and the power flow direction of each port is bidirectional. The equivalent model of CM-SST is shown in Fig. 4, where $U_{\mathrm{mvdc}}$ and $I_{\mathrm{mvdc}}$ represent the voltage and current of MVdc bus, while $U_{\mathrm{lvdc}}$ and $I_{\mathrm{lvdc}}$ represent the voltage and current of LVdc bus. $u_x$ and $i_x$ represent the MVac bus voltage and current, respectively (where $x$ means $a$, $b$, and $c$), $u_{ux}$ and $i_{ux}$ represent the upper arm voltage and current, respectively, $u_{dx}$ and $i_{dx}$ represent the lower arm voltage and current, respectively, $F_{ux}$ and $F_{dx}$ represent the average switching function of upper and lower arm SMs, respectively, $n$ is the number of SMs on the arm, $L_g$ is the arm

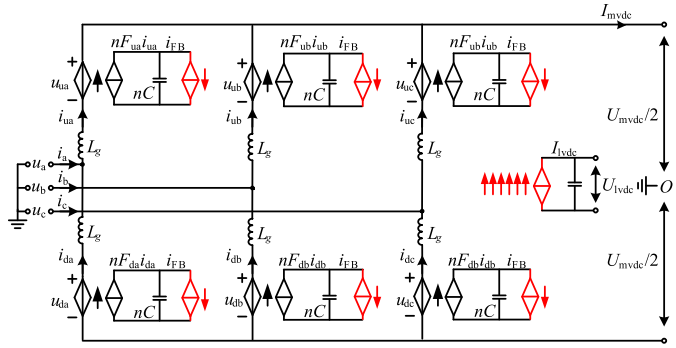


Fig. 4. Equivalent model of CM-SST.

inductance, $C$ is the SM capacitor, and $i_{\mathrm{FB}}$ is the current flowing into FB.

Taking phase-$a$ as an example, assuming that the phase angle of phase-$a$ is zero, the voltage and current are

$$\begin{cases} u_a = U_{\mathrm{mvac}} \sin(\omega t) \\ i_a = I_{\mathrm{mvac}} \sin(\omega t + \varphi) \end{cases} \tag{1}$$

where $U_{\mathrm{mvac}}$ and $I_{\mathrm{mvac}}$ represent the line-to-neutral voltage and current amplitudes, respectively, $\omega$ is the angular frequency of the grid, and $\varphi$ is the power factor angle. Then, the voltage and current of the upper arm can be obtained as

$$\begin{cases} u_{ua} = \frac{1}{2}U_{\mathrm{mvdc}} - U_{\mathrm{mvac}} \sin(\omega t) \\ i_{ua} = \frac{I_{\mathrm{mvdc}}}{3} + \frac{I_{\mathrm{mvac}}}{2} \sin(\omega t + \varphi) + I_{2a} \sin(2\omega t + \theta_{2a}) \end{cases} \tag{2}$$

where $I_{2a}$ is the amplitude of second-order frequency circulating current and $\theta_{2a}$ is the phase angle. When the voltage modulation ratio is defined as $m$, the switching function is

$$F_{ua} = \frac{u_{ua}}{U_{\mathrm{mvdc}}} = \frac{1}{2} - \frac{m}{2} \sin(\omega t). \tag{3}$$

As shown in Fig. 4, the current of SMs, that is, the current defined between SM half-bridge and capacitor, can be obtained from (2) and (3) as

$$\begin{aligned} i_{\mathrm{sm}ua} &= F_{ua} i_{ua} = I_{\mathrm{sm}ua\_\mathrm{dc}} + I_{\mathrm{sm}ua\_\mathrm{ac}} \\ &= \underbrace{\frac{I_{\mathrm{mvdc}}}{6} - \frac{I_{\mathrm{mvac}}}{8} m \cos(\varphi)}_{\mathrm{DCcurrent}:I_{\mathrm{sm}ua\_\mathrm{dc}}} \\ &\underbrace{+\frac{I_{\mathrm{mvac}}}{4} \sin(\omega t + \varphi) - \frac{I_{\mathrm{mvdc}}}{6} m \sin(\omega t) - \frac{I_{2a}}{4} m \cos(\omega t + \theta_{2a})}_{\mathrm{Fundamentalcurrent}:I_{\mathrm{sm}ua\_f1}} \\ &\underbrace{-\frac{I_{\mathrm{mvac}}}{8} m \cos(2\omega t + \varphi) + \frac{I_{2a}}{2} \sin(2\omega t + \theta_{2a})}_{\mathrm{second-ordercurrent}:I_{\mathrm{sm}ua\_f2}} \\ &\underbrace{+\frac{I_{2a}}{4} m \cos(3\omega t + \theta_{2a})}_{\mathrm{Third-ordercurrent}:I_{\mathrm{sm}ua\_f3}}. \end{aligned} \tag{4}$$

It can be known from (4) that the SM current includes dc part and ac part, which contains the fundamental, second-order, and third-order frequency components. The dc part, also known as active current, is responsible for the active power exchange

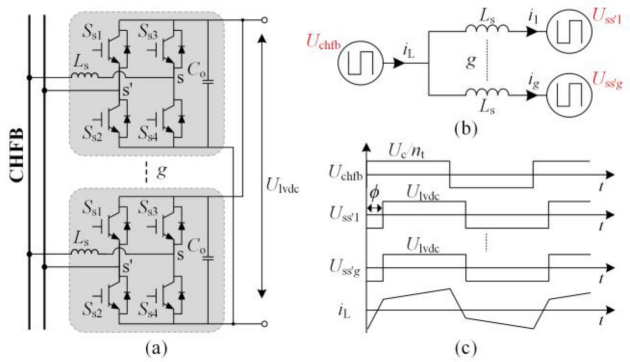


Fig. 5. Power interaction diagram between CHFB and LVdc. (a) Equivalent circuit. (b) Equivalent model. (c) Modulation method.

between SM and CHFB. Therefore, on the premise of SMs voltage equalization, the power balance expression among MVac, MVdc, and CHFB is

$$\frac{3}{2}U_{\mathrm{mvac}}I_{\mathrm{mvac}}\cos\varphi = U_{\mathrm{mvdc}}I_{\mathrm{mvdc}} + 6nU_cI_{\mathrm{smdc}} \tag{5}$$

where $U_c$ is the voltage of the SM capacitor.

The equivalent circuit of power interaction between CHFB and LVdc bus is shown in Fig. 5(a), which includes $g$ FBLs, and the number of FBLs can be flexibly determined based on the power level of the LVdc and the current stress of switches. The equivalent model and modulation method are shown in Fig. 5(b) and (c), respectively. $U_{\mathrm{chfb}}$ is the voltage of CHFB, the amplitude of which is $U_c/n_t$, $U_{ss'1}$, $U_{ss'2}$, …, $U_{ss'g}$ are the modulated voltages of FBLs, and $i_L$ is the inductor current. The voltage of CHFB is clamped by SMs capacitor voltage $U_c$ due to the synchronous modulation of all TABs, and the magnitude and direction of power flow between CHFB and FBLs are controlled by the phase-shift angle $\phi$. The power flow between CHFB and LVdc can be obtained from [37]

$$P_{\mathrm{lvdc}} = \frac{gU_{\mathrm{lvdc}}U_c}{2\pi n_t f_1 L_r}\phi\left(1-\frac{|\phi|}{\pi}\right). \tag{6}$$

## III. Operation Characteristics of Switched Capacitors Based Power Channel

### A. SMs Voltage Clamped Characteristic Based on Switched Capacitors Loop

As shown in Fig. 1(b), the MMC horizontal three SMs are interconnected by TAB, and the vertical SMs are interconnected by CHFB, so the power channel among all SMs can be formed. The equivalent impedance model of the power channel is shown in Fig. 6 in which all TABs adopt synchronous-switching signals. It should be noted that phase-shift inductors are no longer needed in TAB, and $L_{pa}$, $L_{pb}$, and $L_{pc}$ are the primary leakage inductances of four-terminal HFT. $R_{pa}$, $R_{pb}$, and $R_{pc}$ are the equivalent resistances of TAB primary side, including the ON-state resistance of switches and winding resistance of HFT. $L_s$ and $R_s$ are the secondary leakage inductance and winding resistance of

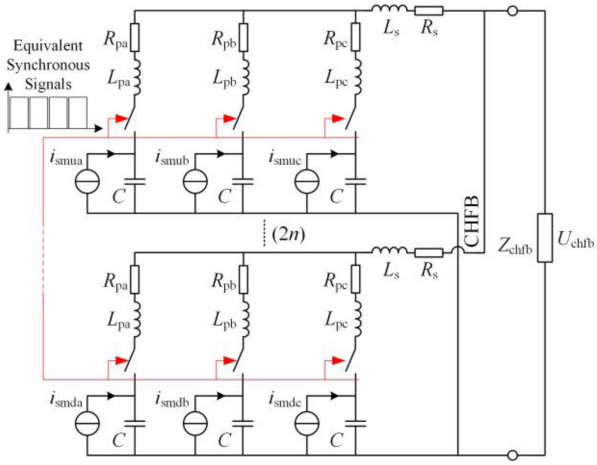


Fig. 6. Equivalent impedance model of power channel.

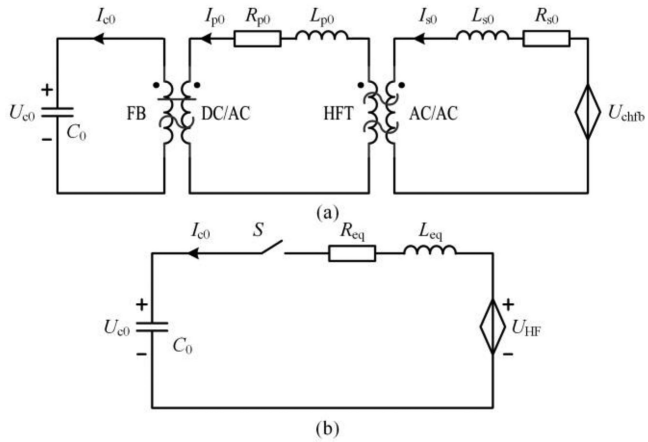


Fig. 7. Equivalent model of one switched-capacitor circuit cell. (a) Detailed. (b) Simplified.

HFT, respectively, and $Z_{\mathrm{chfb}}$ is the output impedance of CHFB, which represents the equivalent impedance of FBLs side.

In the process of synchronous switching of TAB, the impedance between SMs' capacitors is composed of leakage inductances and parasitic resistances, which have relatively low values. Therefore, the switching capacitors' characteristics will exist between SMs' capacitors, then all the SMs' capacitors clamp each other with the same voltage. And after the synchronous switching of all FBs, a stable voltage CHFB is formed with the amplitude of approximate SMs' capacitors average voltage, that is, $U_{\mathrm{HF}} \approx U_{\mathrm{mvdc}}/n$. The detailed and simplified equivalent model of one switched-capacitor circuit cell is shown in Fig. 7, where $U_{\mathrm{chfb}}$ is the voltage of CHFB and $U_{\mathrm{HF}}$ is the amplitude; $R_{\mathrm{eq}}$ and $L_{\mathrm{eq}}$, as shown in Fig. 7(b), represent the equivalent resistance and inductance of switched-capacitor loop, as shown in Fig. 7(a).

In order to simplify the analysis, suppose the transformation ratio of HFT is 1. In half of the switching cycle, when the voltage $U_{c0}$ of $C_0$ is inconsistent with the voltage amplitude

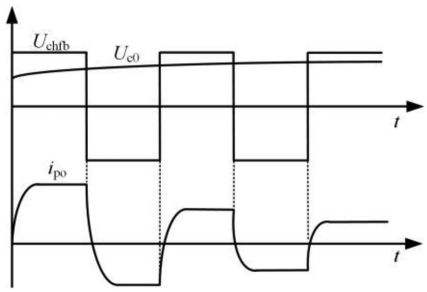


Fig. 8. Power flow curves of the switching-capacitor loop.

$U_c$ of CHFB, it can be obtained from Kirchhoff's voltage law

$$U_{c0} + i_{c0}R_{eq} + L_{eq}\frac{di_{c0}}{dt} = \frac{U_{lvdc}}{n} \tag{7}$$

where $i_{c0} = C_0 \cdot (dU_{c0}/dt)$, so (7) can be rewritten as

$$U_{c0} + R_{eq}C_0\frac{dU_{c0}}{dt} + L_{eq}C_0\frac{d^2U_{c0}}{dt^2} = \frac{U_{lvdc}}{n}. \tag{8}$$

In order to prevent the switching devices from being damaged by current spikes during the switching process, the switched-capacitor loop should work in an overdamped state. The characteristic roots of the characteristic equation in (8) are

$$s_{1,2} = -\frac{R_{eq}}{2L_{eq}} \pm \sqrt{\left(\frac{R_{eq}}{2L_{eq}}\right)^2 - \frac{1}{L_{eq}C_0}}. \tag{9}$$

In actual engineering practice, the equivalent resistance $R_{\rm eq}$ is in the $10^{-1}\ \Omega$ level, so the equivalent inductance $L_{\rm eq}$ is two orders of magnitude smaller than the SM capacitor $C_0$. By solving the general solution of the second-order overdamped system in (8), the charging current of SM capacitor is

$$\begin{aligned} i_{c0}(t) &= A_1 s_1 e^{s_1 t} + A_2 s_2 e^{s_2 t} \\ &\quad + \left(U_{lvdc}/n + A_1 e^{s_1 t} + A_2 e^{s_2 t}\right)/U_{eq}. \end{aligned} \tag{10}$$

The power flow diagram of the switched-capacitor loop is shown in Fig. 8, and the current flows in the form of overdamping during the switching process. The characteristics of switched capacitors of power decoupling channel between SMs' capacitors help to achieve SMs voltage automatic balancing and ripple-power natural elimination.

### *B. Natural Elimination of SMs Ripple Power*

The ac part in formula (4) is also known as low-frequency ripple current, which will flow into SM capacitor in DDM$^2$C-SST to generate ripple voltage due to the high impedance of DAB within the control bandwidth [30], that is, $Z_c << Z_{\rm dab} + Z_{\rm lvdc}$, and the SM current flow path is shown in Fig. 9.

In addition, the SM capacitor current can be obtained as

$$\begin{cases} i_{cua} \approx i_{{\rm sm}ua\_{\rm ac}} \\ i_{cub} \approx i_{{\rm sm}ub\_{\rm ac}} \\ i_{cuc} \approx i_{{\rm sm}uc\_{\rm ac}}. \end{cases} \tag{11}$$

In practical engineering case, the SM capacitance value ranges from $10^0$ to $10^1$ mF, which severely limits the power density of

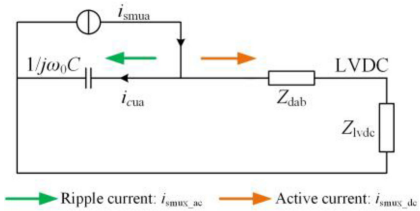


Fig. 9. Power flow diagram of SM in the traditional DDM$^2$C-SST.

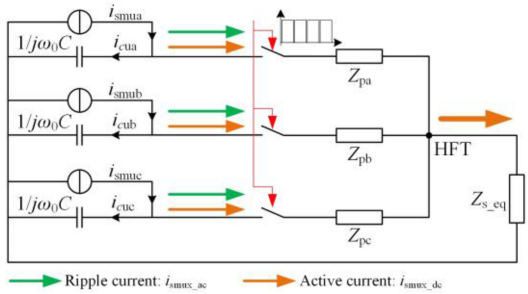


Fig. 10. Power flow diagram of horizontal three SMs in CM-SST.

DDM$^2$C-SST, and the SM capacitance can also be obtained as

$$C = \frac{1}{3}\frac{U_{\rm mvdc}I_{\rm mvdc}}{nm\omega\varepsilon {U_c}^2\cos(\varphi)}\left[1 - \left(\frac{m\cos(\varphi)}{2}\right)^2\right]^{3/2}. \tag{12}$$

Therefore, if the low-frequency ripple current does not flow into the SM capacitor, then its size will be significantly reduced.

Due to the synchronous modulation of all TABs, CM-SST can utilize the switched capacitors' characteristics of the power channel to realize decoupling and cancellation of the ripple power based on their three-phase symmetry. From the analysis of SM current in Section II-B, it can be seen that in (4), the phase characteristic of the three-phase SMs current is

$$\begin{cases} i_{{\rm sm}ua\_{\rm ac}} = i_{f1}\angle 0 + i_{f2}\angle 0 + i_{f3}\angle 0 \\ i_{{\rm sm}ub\_{\rm ac}} = i_{f1}\angle -\frac{2}{3}\pi + i_{f2}\angle\frac{2}{3}\pi + i_{f3}\angle 0 \\ i_{{\rm sm}uc\_{\rm ac}} = i_{f1}\angle\frac{2}{3}\pi + i_{f2}\angle -\frac{2}{3}\pi + i_{f3}\angle 0. \end{cases} \tag{13}$$

It can be known from (13) that the fundamental and second-order frequency components of the SMs' currents are in three-phase symmetry, which are the basis of cancellation in the decoupling channel. What needs a special explanation is that although the third-order frequency presents a zero order in (13), it belongs to the secondary fluctuation of the fundamental and second-order components. It will disappear with the elimination of the first two, which will be analyzed in detail in Section III-C.

The active- and ripple-power flow diagram of horizontal three SMs is shown in Fig. 10, where $\omega_0$ is the equivalent angular frequency of ripple current, and the TAB equivalent primary impedance $Z_{px} = j\omega_0 L_{px} + R_{px}$. Assuming that the voltages of the vertical SMs are balanced, the ripple-current transfer expression of one group of horizontal three SMs can be obtained

as

$$\begin{cases} i_{cua} = i_{\mathrm{sm}ua\_\mathrm{ac}} \frac{Z_{a2}}{Z_{a1}+Z_{a2}} + \frac{i_{\mathrm{sm}ub\_\mathrm{ac}}}{2} \frac{Z_{b1}}{Z_{b1}+Z_{b2}} + \frac{i_{\mathrm{sm}uc\_\mathrm{ac}}}{2} \frac{Z_{c1}}{Z_{c1}+Z_{c2}} \\ i_{cub} = \frac{i_{\mathrm{sm}ua\_\mathrm{ac}}}{2} \frac{Z_{a2}}{Z_{a1}+Z_{a2}} + i_{\mathrm{sm}ub\_\mathrm{ac}} \frac{Z_{b1}}{Z_{b1}+Z_{b2}} + \frac{i_{\mathrm{sm}uc\_\mathrm{ac}}}{2} \frac{Z_{c1}}{Z_{c1}+Z_{c2}} \\ i_{cuc} = \frac{i_{\mathrm{sm}ua\_\mathrm{ac}}}{2} \frac{Z_{a2}}{Z_{a1}+Z_{a2}} + \frac{i_{\mathrm{sm}ub\_\mathrm{ac}}}{2} \frac{Z_{b1}}{Z_{b1}+Z_{b2}} + i_{\mathrm{sm}uc\_\mathrm{ac}} \frac{Z_{c1}}{Z_{c1}+Z_{c2}} \end{cases} \tag{14}$$

where

$$\begin{cases} Z_{a1} = Z_c = 1/j\omega_0 C \\ Z_{a2} = Z_{pa} + (Z_{pb} + Z_c)//(Z_{pc} + Z_c). \end{cases} \tag{15}$$

The calculation of $Z_{b1}$, $Z_{b2}$ and $Z_{c1}$, $Z_{c2}$ is similar to (15). From the judgment condition for overdamping in the second-order system shown in (10), it can be seen that the leakage inductance $j\omega_0 L_{px}$ is much smaller than the SM capacitor $1/j\omega_0 C_0$, that is

$$Z_c >> Z_{pa} \approx Z_{pb} \approx Z_{pc}. \tag{16}$$

The equivalent impedance of the power decoupling channel, including leakage inductances and parasitic resistances, is much smaller than the SMs capacitance, so the inconsistency of impedance parameters of different turns ratios on HFT does not affect the transmission of ripple current. Therefore, (14) can be rewritten as

$$\begin{cases} i_{cua} \approx \frac{1}{3}(i_{\mathrm{sm}ua\_\mathrm{ac}} + i_{\mathrm{sm}ub\_\mathrm{ac}} + i_{\mathrm{sm}uc\_\mathrm{ac}}) = 0 \\ i_{cub} \approx \frac{1}{3}(i_{\mathrm{sm}ua\_\mathrm{ac}} + i_{\mathrm{sm}ub\_\mathrm{ac}} + i_{\mathrm{sm}uc\_\mathrm{ac}}) = 0 \\ i_{cuc} \approx \frac{1}{3}(i_{\mathrm{sm}ua\_\mathrm{ac}} + i_{\mathrm{sm}ub\_\mathrm{ac}} + i_{\mathrm{sm}uc\_\mathrm{ac}}) = 0. \end{cases} \tag{17}$$

The transmission of low-frequency ripple components of SM current is shown in Fig. 10. It can be known from the above analysis that the ripple current will cancel each other out based on their three-symmetry characteristic. Therefore, the natural elimination of SMs ripple power can be achieved, which significantly decreases the size of SM capacitance.

In this case, the SM capacitor parameter design only needs to consider filtering out the high-frequency switch ripples. As a result, TAB switching frequency is higher, so the switching ripples in TAB compared with half-bridge modules can be ignored. The SM capacitor in each switching cycle of charging energy can be obtained by referring boost circuit

$$E_c = C\varepsilon U_c = i_{ux\mathrm{ac\_max}} D_{\mathrm{sm}} / f_{\mathrm{sm}} \tag{18}$$

where $f_{\mathrm{sm}}$ is the frequency of SM half-bridge switches, $\varepsilon$ is the high-frequency ripple rate of SM capacitor voltage, and $D_{\mathrm{sm}}$ is the duty ratio of SM half-bridge switch and its maximum value is equal to the voltage modulation ratio $m$. The constraint of SM capacitance can be obtained from (4) and (18) as

$$C_i = \left((\frac{I_{\mathrm{mvac}}}{8} - \frac{I_{\mathrm{mvdc}}}{6})m^2 + \frac{I_{\mathrm{mvac}}}{4}m\right) \Big/ 6 f_{\mathrm{sm}} \varepsilon U_{\mathrm{mvdc}}. \tag{19}$$

### C. Natural Elimination of Arms Circulating Current

In the MMC-type topology, the arms circulating current will increase the power loss and current of switching devices. The low-frequency ripple components of SMs capacitor voltage are the root causes of the arms circulating current. In the traditional MMC, the arm voltage can be obtained from the SMs capacitor voltage and the switching function as

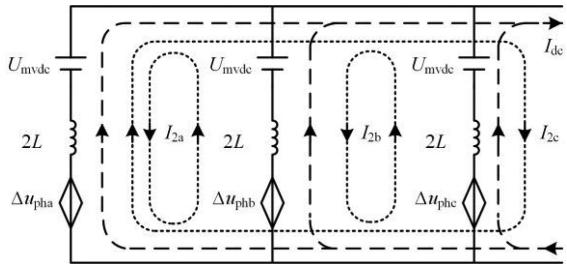


Fig. 11. Diagram of arms circulating current.

$$\begin{cases} u_{ux} = nF_{ux}u_{\mathrm{sm}ux} = nF_{ux}\frac{1}{C}\int i_{\mathrm{sm}ux}dt \\ u_{dx} = nF_{dx}u_{\mathrm{sm}dx} = nF_{dx}\frac{1}{C}\int i_{\mathrm{sm}dx}dt \end{cases} \tag{20}$$

where $u_{dx}$, $F_{dx}$, $u_{\mathrm{sm}\,dx}$, and $i_{\mathrm{sm}\,dx}$ are the lower arm voltage, switching function, SM voltage, and SM current, respectively. Taking phase-$a$ as an example and by referring to the research work in [38], the dominant second-order ripple voltage $\Delta u_{pha}$ can be obtained from (3), (4), and (20) as

$$\begin{aligned} \Delta u_{pha} &= u_{ux} + u_{dx} - U_{\mathrm{mvdc}} \\ &= \frac{n}{2\omega C}[\frac{1}{6}g^2 I_{\mathrm{mvdc}} sin(2\omega t) - \frac{1}{3}gI_{\mathrm{mvac}} sin(2\omega t + \varphi) \\ &\quad + \frac{1}{6}(2g^2+3)I_{2a} sin(2\omega t + \theta_{2a})]. \end{aligned} \tag{21}$$

The ripple voltages in phase-$a$ and phase-$b$ can be obtained in the same way, and the three-phase ripple voltages are in negative sequence, which will generate a second-order circulating current among the three phases, as shown in Fig. 11. Therefore, eliminating the low-frequency ripple voltage of the SMs capacitor will avoid the generation of the second-order frequency circulating current of arms at the root.

It can be seen from (4) that the third-order component in the SM current is generated by the second-order circulating current of arms, and from the article presented in [38] and (16), it can be seen that the second-order circulating current is generated by the fundamental and second-order components of the SM capacitor voltage ripples. Therefore, the third-order component in the SM low-frequency ripple current is the secondary fluctuation of the fundamental and the second-order components, and the former will automatically disappear with the suppression of the latter two.

## IV. Design and Evaluation of CM-SST

### A. Sizing and Cost

In order to further demonstrate the practicability of the proposed topology, a detailed comparative analysis of DDM$^2$C-SST in [23]–[29] [see Fig. 1(a)] and the proposed CM-SST [see Fig. 1(b)] is conducted from the perspective of sizing. The parameters of the two SST systems are given in Table I.

It is difficult to estimate the influence of the structure, layout, and peripheral control circuit of the actual system on sizing, so refer to the calculation method in [30], [39], and [40], taking

TABLE I
PARAMETERS OF DDM$^2$C-SST IN [23]–[29] AND PROPOSED CM-SST

| Parameters | DDM$^2$C-SST | CM-SST |
|---|---|---|
| MVAC power / $P_{\text{mvac}}$ | 10MVA | 10MVA |
| MVDC power / $P_{\text{mvdc}}$ | 5MW | 5MW |
| LVDC power / $P_{\text{lvac}}$ | 5MW | 5MW |
| MVAC voltage / $U_{\text{mvac}}$ | 10kV | 10kV |
| MVDC voltage / $U_{\text{mvdc}}$ | 20kV | 20kV |
| LVDC voltage / $U_{\text{lvdc}}$ | 800V | 800V |
| Number of SMs per arm/ $n$ | 25 | 25 |
| Capacitance of SM/ $C$ | 3.4mF | 150μF |
| Fundamental AC frequency/ $f$ | 50Hz | 50Hz |
| SM switching frequency/ $f_{\text{sm}}$ | 2kHz | 2kHz |
| DC/DC switching frequency/ $f_{\text{t}}$ | 10kHz | 10kHz |
| Transformer turns ratio/ $n_{\text{t}}$ | 1:1 | 1:1 |

TABLE II
MODULES NUMBER OF DDM$^2$C-SST AND CM-SST

| Modules | DDM$^2$C-SST | CM-SST |
|---|---|---|
| SM | 150 | 150 |
| FB | 150 | 150 |
| FBL | 150 | 50 |
| HFT | 150 | 50 |

sizing of the main module components as the comparison object, including all SMs, FBs, FBLs, and HFTs. Therefore, this article, respectively, designs, selects, and evaluates the switching devices, capacitors, and high-frequency magnetic elements. At first, the numbers of modules are listed in Table II. According to the principle that the switches current stresses in FB and FBL are consistent, the number of FBL is determined to be 50 by formulae (4)–(6).

*1) Switching Devices:* The MMC half-bridge switching devices can be selected according to arm current and SM capacitor voltage. According to (2) and ignoring the circulating current, this article selects the dual-IGBT module FF400R12KT3 of Infineon Technologies, with the rated parameter of 1200 V/400 A, volume of about 0.202 dm$^3$, and cost of 184.54USD.

The formulae (4) and (6) are the basis of the switches selection of dc/dc stage. For the tube's selection of FB and FBL in CM-SST, FF150R12RT4 dual-IGBT module with rating power of 1.2 kV/150 A, volume of 0.097 dm$^3$, and cost of 72.55USD is selected. For the tubes in DDM$^2$C-SST, FF50R12RT4 dual-IGBT module with rating power of 1.2 kV/50 A, volume of 0.097 dm$^3$, and cost of 53.26USD is selected.

*2) SM Capacitors:* Assuming that the allowable capacitor voltage fluctuation is 10%, the SM capacitor of DDM$^2$C-SST can be calculated as 3.4 mF [41]. For unified comparison and analysis, the high-voltage dc capacitors from TDK are adopted. Two B25680B1198K103 of 1.1 kV/1.9 mF in parallel are adopted, with a unit volume of 3.699 dm$^3$ and cost of 140.85USD.

The SM capacitor of CM-SST does not need to deal with low-frequency ripples. From the perspective of inhibiting high-frequency switching ripple, it only needs a 150 $\mu$F capacitor,

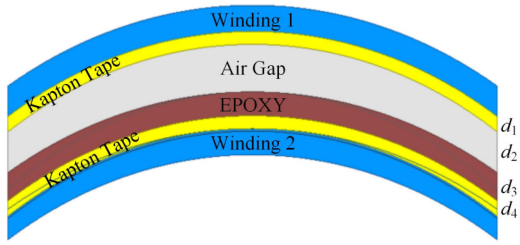


Fig. 12. Insulation design between windings [44].

according to (15). B25680B1237K101 of 1.1 kV/230 $\mu$F is selected, with a unit of 0.562 dm$^3$ and cost of 57.80USD.

*3) High-Frequency Transformers:* For the design of HFT, the magnetic core, insulation material, and the windings interlayer distances are the key factors. The medium-voltage, high-power, and high-frequency transformer has been extensively researched in [42]–[46], which are the basis of the design and calculation in this article.

Among many magnetic materials suitable for high-frequency applications, ferromagnetic materials are more suitable than ferrites because of their higher saturation flux densities [42]. In addition, the amorphous and nanocrystalline are typical representatives. Therefore, Vitroperm500F series from VAC is selected as the magnetic materials of HFTs both in DDM$^2$C-SST and CM-SST.

The HFT in the two types of SST topologies has the same insulation voltage level, which is the line-to-line voltage on the ac side. Guo *et al.* [44] provide a detailed HFT insulation design process, and under the insulation voltage of this article, EPOXY with a dielectric constant of 16 kV/mm is selected as the insulation material. The insulation structure between windings is shown in Fig. 12, which includes insulation material, air gap, and two layers of insulation tape. The insulation voltage can be calculated as

$$U_{\text{ins}} = d_1 E_{\text{tape1}} + d_2 E_{\text{air}} + d_3 E_{\text{EPOXY}} + d_4 E_{\text{tape2}} \quad (22)$$

where $U_{\text{ins}}$ is the insulation voltage between two windings, and $E$ and $d$ represent the electric field and thickness, respectively. According to the design and selection in this article and reference to the cases in the existing research, the sizing and cost of the HFT can be calculated as 4.348 dm$^3$, 109.33USD in DDM$^2$C-SST and 12.196 dm$^3$, 222.54USD in CM-SST.

According to the contents above, the design and selection results are summarized in Table III, and the volume and cost comparisons of two types of SST can be obtained, as shown in Figs. 13 and 14. It can be seen from the histogram that the volumes of switches, heat sinks, and high-frequency magnetic elements in CM-SST are almost the same with DDM$^2$C-SST, because the volume calculations of heat sinks and HFTs are mainly determined by the power capacity. But the reduction in the number of HFTs and switches will bring some cost reductions.

The significant reduction in the volume and cost of SM capacitors is the main advantage of CM-SST. Since the low-frequency ripple power among the horizontal three SMs can

TABLE III
DESIGN AND MAIN COMPONENTS FOR 10 MW DDM$^2$C-SST AND CM-SST

| | Component | Manufacture | Type | Features | Number | Volume(dm$^3$) | Cost(kUSD) |
|---|---|---|---|---|---|---|---|
| MMC side | SM tubes | Infineon | FF400R12KT3 | 1.2kV/400A | 150 | 30.3 | 28.1 |
| | Heat sinks | Delta | FHS-A7015B62 | 0.3°C/W | 150 | 165.8 | -- |
| DDM$^2$C-SST | SM capacitors | TDK | B25680B1198K103 | 1.1kV/1.9mF | 2*150 | 1109.7 | 42.3 |
| | FB/FBL tubes | Infineon | FF50R12RT4 | 1.2kV/50A | 300/300 | 29.1/29.1 | 40.0 |
| | FB/FBL heat sinks | Delta | FHS-A7015B62 | 0.3°C/W | 150/150 | 244.6 | -- |
| | HFT | VAC | Vitroperm500F | 35kW/10kHz | 150 | 652.2 | 16.4 |
| CM-SST | SM capacitors | TDK | B25680B1237K101 | 1.1kV/230uF | 1*150 | 84.3 | 8.7 |
| | FB/FBL tubes | Infineon | FF150R12RT4 | 1.2kV/150A | 300/100 | 29.1/9.7 | 29.0 |
| | FB/FBL heat sinks | Delta | FHS-A7015B62 | 0.3°C/W | 150/50 | 278.4 | -- |
| | HFT | VAC | Vitroperm500F | 100kW/10kHz | 50 | 609.8 | 11.1 |

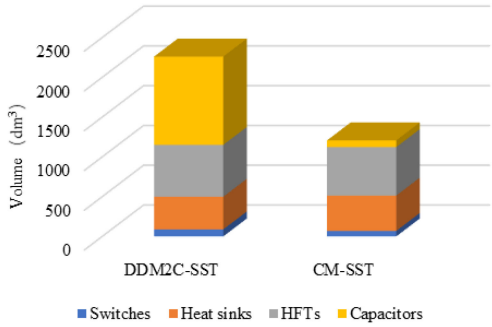


Fig. 13. Comparison results of volume.

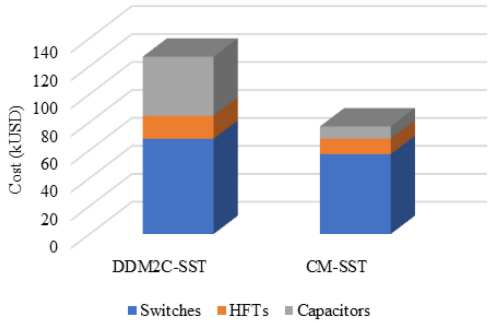


Fig. 14. Comparison results of cost.

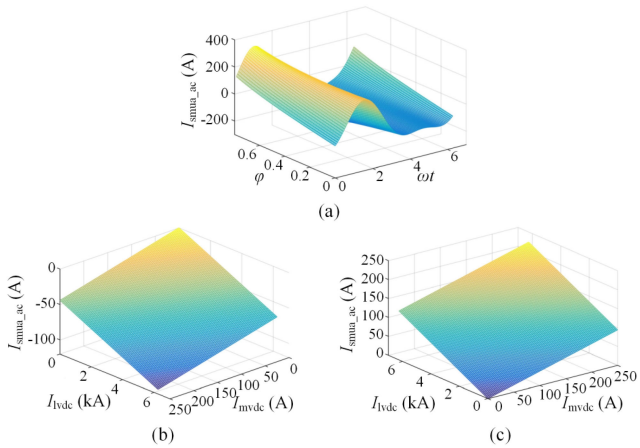


Fig. 15. SM ripple-current diagram. (a) Ripple current at full load. (b) Minimum and (c) maximum ripple currents at different MVdc and LVdc currents.

cancel each other out, the SM capacitor only needs to absorb the switching harmonics, which is reduced from 2.3 mF to 150 $\mu$F in the studied case, and the cost and volume are significantly reduced. The CM-SST sizing decreases by about 46.6% and cost decreases by about 39.4% compared with DDM$^2$C-SST.

### B. Efficiency

According to the analysis in Section III-B, FBs and HFTs in the power channel not only realize the active power transmission between SMs and LVdc but also transmit ripple power, which will bring additional power loss. In addition, according to the analysis in Section III-C, the natural elimination of arms second-order frequency circulating current will decrease the power loss on the SMs' switches. This section analyzes the power loss of CM-SST, and the SM current can be rewritten from (4)–(6) as

$$\begin{cases} I_{\mathrm{sm}ua\_\mathrm{dc}} = I_{\mathrm{lvdc}}/6n \\ I_{\mathrm{sm}ua\_\mathrm{ac}} = \frac{nI_{\mathrm{mvdc}}+I_{\mathrm{lvdc}}}{3mn\cos\varphi}\sin(\omega t+\varphi) - \frac{mI_{\mathrm{mvdc}}}{6}\sin(\omega t) \\ \quad -\frac{nI_{\mathrm{mvdc}}+I_{\mathrm{lvdc}}}{8n\cos\varphi}\cos(2\omega t+\varphi). \end{cases} \tag{23}$$

The ripple current in the above formula is expressed by the MVdc current and LVdc current. Based on the case parameters in Table I, the relationship diagram of the ripple current with respect to $\omega t$ and $\varphi$ under full load can be obtained, as shown in Fig. 15(a). According to (23) and Fig. 15(a), it can be seen that the minimum value of ripple current is at $\omega t = 5\pi/4$, and the maximum value is at $\omega t = \pi/2$. Then, the minimum and maximum values of ripple current can be obtained at different MVdc and LVdc currents on the condition that $\varphi = 0$, as shown in Fig. 15(b) and (c).

The SM currents at different loads are shown in Fig. 16. Because the SM half-bridge and FB and FBL in HFL in this article are all IGBT modules, the conduction loss and switching loss can be obtained from [47] shown at the bottom of the next to next page where $P_{\mathrm{con}\_T}$ and $P_{\mathrm{con}\_D}$ are the average conduction loss of IGBT and diode, respectively, $P_{\mathrm{sw}\_T}$ and $P_{\mathrm{sw}\_D}$ are the average switching loss of IGBT and diode, respectively, $u_{\mathrm{con}\_T}$ and $u_{\mathrm{con}\_D}$ are the conduction voltages of IGBT modules, which

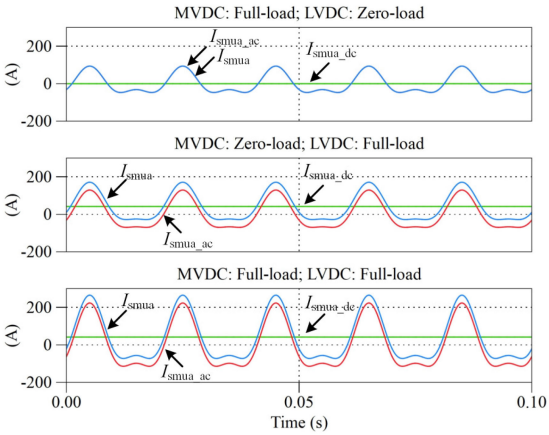


Fig. 16. SM current at different loads.

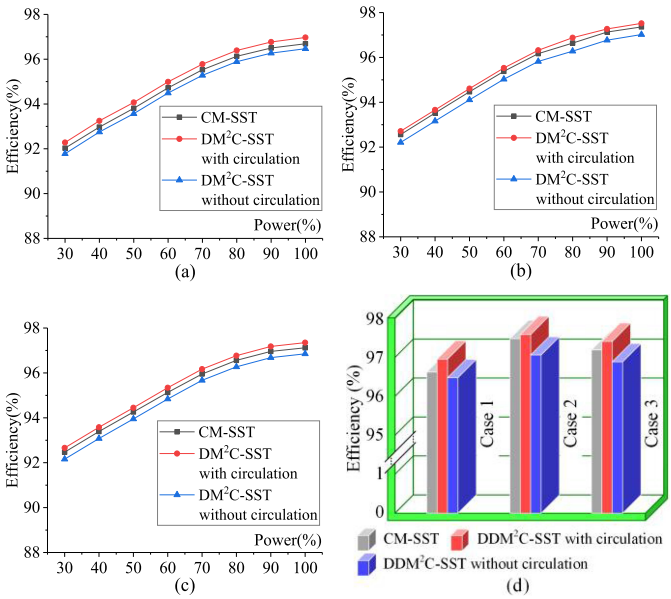


Fig. 17. Efficiency comparison results between CM-SST and DDM$^2$C-SST. (a) Case 1. (b) Case 2. (c) Case 3. (d) Efficiency values at full load in three cases.

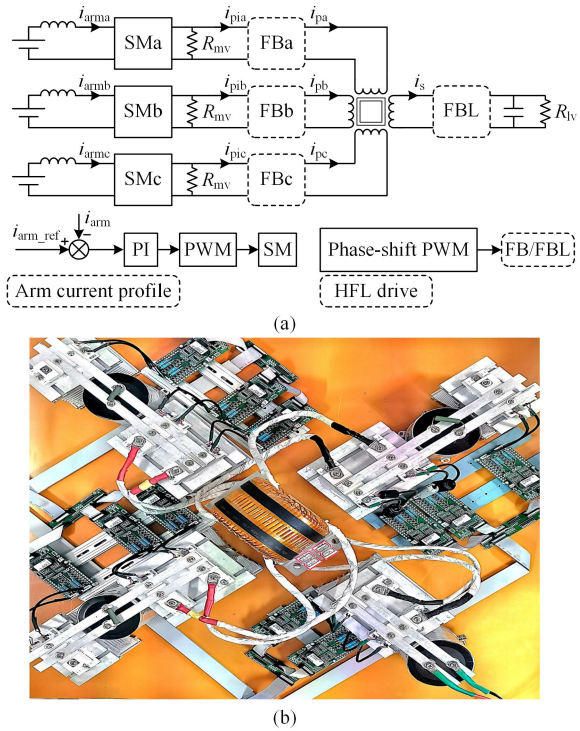


Fig. 18. High-power experimental platform for efficiency test. (a) Structure and drive diagram. (b) Prototype.

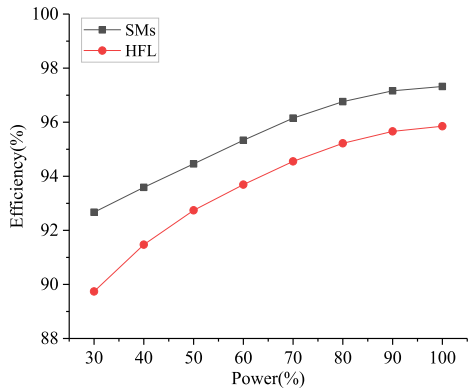


Fig. 19. Efficiency test plots by high-power platform.

can be obtained from the datasheet, $D$ is the duty ratio, $f_{\rm sw}$ is the switching frequency, $u_{\rm ref}$ is the reference blocking voltage, $T_j$ is the temperature coefficient, $K_v$ is the voltage coefficient, and $E_{\rm on\_}T$, $E_{\rm off\_}T$, and $E_{\rm rec}$ are the switching energy losses, all of which can be obtained from the datasheets.

The power losses of HFT are mainly distributed on cores and windings, which can be calculated by means of the existing research [42], [44]

$$\begin{cases} P_{\rm core} = K\left(\frac{2}{\Delta B^2\pi^2}\int_0^{f_1}\left(\frac{dB(t)}{dt}\right)^2 dt\right)^{\alpha-1} B_m^{\beta} \\ P_w = \sum_{h=1}^{n} R_{\rm dc} F_h I_h^2 \end{cases} \tag{25}$$

where $f_1$ is the operating frequency of TAB, $B$ is the flux density, $K$, $\alpha$, and $\beta$ are determined by the magnetic core characteristics, $\Delta B$ is the peak-to-peak magnetic induction, $R_{\rm dc}$ is the dc resistance of the winding, and $F_h$ and $I_h$ are the ac resistance factor and the current rms value at the $h$th harmonic, respectively.

This article calculates and compares the efficiency of CM-SST with the isolation-stage transmitting ripple power and DDM$^2$C-SST [23]–[29] in which the DAB does not transmit ripple power. What needs to be specially noted is that the CM-SST can realize the natural elimination of arms second-order circulating current, the power loss caused by which can be ignored. The DDM$^2$C-SST should be divided into two categories according to whether an additional circulation suppression strategy is designed, one contains circulation and one does not.

From the formulae (2), (23), and Fig. 16, it can be known that different power configurations of MVdc and LVdc will cause

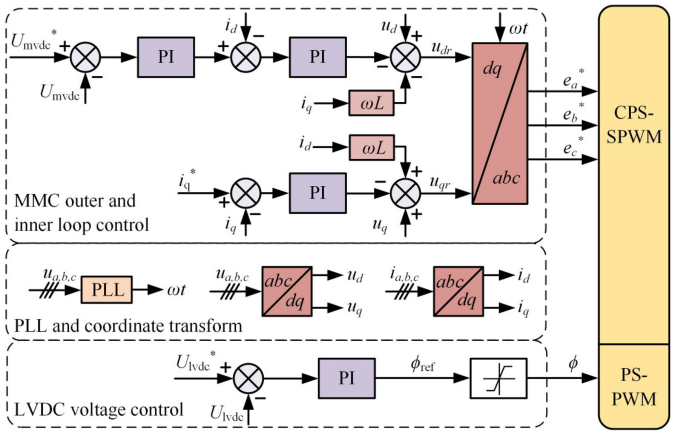


Fig. 20. Overall control block diagram of CM-SST.

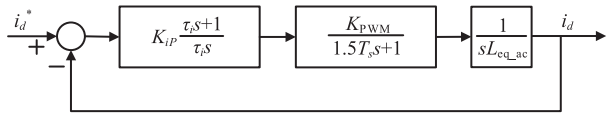

Fig. 21. Control diagram of the inner current controller.

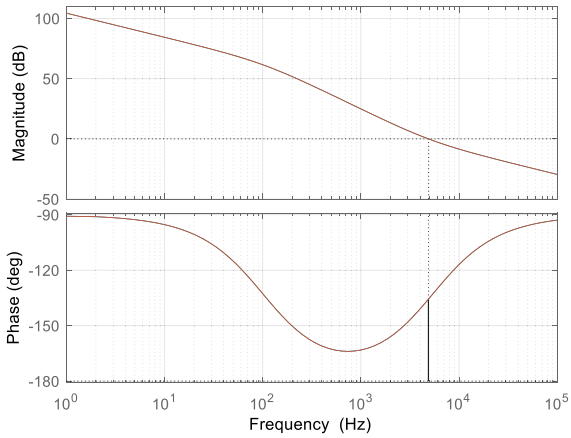


Fig. 22. Bode diagram of the inner current controller.

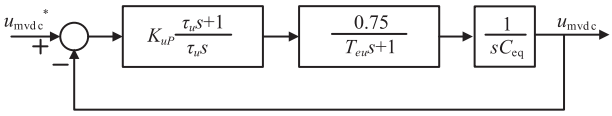

Fig. 23. Simplified configuration diagram of the external voltage controller.

different loss proportions on SM and HFL. Therefore, in order to fully illustrate the efficiency performance of CM-SST under different ports' loads, the discussion is divided into three cases on the basis of the differences, as shown in Fig. 16. The three cases are as follows.

*Case 1:* Only MVdc bus has load and the LVdc bus at zero load.
*Case 2:* Only LVdc bus has load and the MVdc bus at zero load.
*Case 3:* Both MVdc bus and LVdc bus have load.

It can be known from the analysis in Section III-C that the CM-SST can achieve natural elimination of arms circulating current. Therefore, the DDM$^2$C-SST with and without arms circulating current is compared with CM-SST in efficiency. The efficiency calculation plots from 30% load to full load in the three cases are shown in Fig. 17. It can be seen from the calculation results that the efficiency of CM-SST in the three cases is slightly lower than the DDM$^2$C-SST without arms circulating current but slightly higher than the DDM$^2$C-SST with arms circulating current, as shown in Fig. 17(a)–(c).

In addition, it can be seen from Fig. 16 and formula (24) that when the LVdc bus has a load and the MVdc bus has zero load, the proportion of additional loss caused by the ripple current is the lowest, whereas when the MVdc bus has a load and the LVdc bus has zero load, the proportion of additional loss caused by the ripple current is the highest. Fig. 17(d) can show this point clearly.

In order to test the efficiency performance of the proposed CM-SST, this article built a high-power experimental platform, as shown in Fig. 18, the effectiveness of which has been validated in [47] and [48]. The arms' currents $i_{\mathrm{arm}\,a}$, $i_{\mathrm{arm}\,b}$, and $i_{\mathrm{arm}\,c}$ are controlled by SMs, showing symmetry among the three phases of *abc*; $R_{\mathrm{MV}}$ simulates the load of the MVdc bus so that the current flowing through SM includes the current of MVdc and LVdc at the same time, and the phase-shift modulation is adopted between FB and FBL.

The efficiency test results are shown in Fig. 19. Under the different power configurations of MVdc and LVdc, the proportions of losses formed on SM and HFL are different, so this article gives the test data on SM and HFL separately. According to formulae (2), (23), and Fig. 16, the current flowing through SM and HFL can be obtained at any MVdc and LVdc power configuration, and the overall loss can be obtained after calculating the losses, respectively. Due to the constraints of the HFT manufacturing process and winding methods in the laboratory, the test efficiency is slightly lower than the theoretical calculation values, especially in the HFL stage.

### C. Control

*1) Overall Control of CM-SST:* From the above analysis, it can be known that the CM-SST can simultaneously realize the automatic balancing of SMs voltage and the natural elimination of SMs ripple voltage and arms circulating current without any additional control. The overall control block diagram is shown in Fig. 20.

The MMC stage adopts the traditional dc voltage external loop and ac current inner loop control method. Since it is no longer necessary to design additional SMs voltage balance strategy and arms circulating current suppression strategy, the system control is significantly simplified, which saves the sensors and computing resource of the control center. All FBs in CHFB-based HFL adopt fixed-frequency fixed-duty signals, and FBLs adopt phase-shift modulation based on the timing of CHFB to control the active power interaction between LVdc and CHFB.

*2) Controllers Design of MMC:* The controllers' designs of MMC are divided into the inner current controller and external

TABLE IV
CONTROLLERS DESIGN SUMMARY

| | Inner current controller | External voltage controller | FBL voltage controller |
|---|---|---|---|
| Crossing frequency | 1e^3 | 226 | 3.06e^4 |
| Phase margin | 53.3 | 41.5 | 44.3 |
| Proportional gain | 5.3 | 0.176 | 0.02 |
| Integral gain | 113.3 | 35.2 | 655 |

TABLE V
SIMULATION AND EXPERIMENTAL PARAMETERS

| Parameters | Simulation | Experiment |
|---|---|---|
| MVDC voltage/ $U_{\text{mvdc}}$ | 6kV | 250V |
| Line to line voltage/ $U_{\text{ac}}$ | 3kV | 125V |
| LVDC voltage/ $U_{\text{lvdc}}$ | 750V | 125V |
| Rated active power/ $P$ | 1MW | 2kW |
| Fundamental AC frequency/ $f$ | 50Hz | 50Hz |
| CPS PWM frequency/ $f_{\text{sm}}$ | 2kHz | 2kHz |
| Arm inductance/ $L_{\text{g}}$ | 10mH | 2.5mH |
| Capacitance of SM/ $C$ | 110μF | 23.5μF |
| Number of SMs per arm/ $n$ | 2 | 2 |
| Number of FBLs | 4 | 4 |
| Transformer turns ratio/ $n_{\text{t}}$ | 4:1 | 1:1 |
| HFL switching frequency/ $f_{\text{l}}$ | 10kHz | 10kHz |

voltage controller. For the PI regulator parameters calculation of the inner current loop, take the *d*-axis control diagram as an example. The *d*-axis control diagram of the inner current loop can be obtained, as shown in Fig. 21, while neglecting the resistance on the ac side [49].

$T_s$ is the sampling period, $K_{iP}$ and $K_{iI} = K_{iP}/\tau_i$ are the proportional and integral gains of the current loop, respectively, and $K_{\text{PWM}}$ is the pulsewidth modulation (PWM) equivalent gain. The open-loop transfer function is

$$W_{oi}(s) = \frac{K_{iP}K_{\text{PWM}}(\tau_i s + 1)}{\tau_i L_{\text{eq\_ac}} s^2(1.5T_s s + 1)}. \tag{26}$$

For the quick tracking of the reference signal, the current controller can be designed to be a typical first-order system and then can be obtained as

$$K_{iP} = \frac{L_{\text{eq\_ac}}}{3T_s K_{\text{PWM}}}, \quad K_{iI} = \frac{R_{\text{eq\_ac}}}{3T_s K_{\text{PWM}}} \tag{27}$$

where $L_{\text{eq\_ac}}$ and $R_{\text{eq\_ac}}$ are the equivalent inductance and resistance of ac side, respectively. Based on the system parameters, as given in Table V, the bode diagram of the inner current controller is shown in Fig. 22.

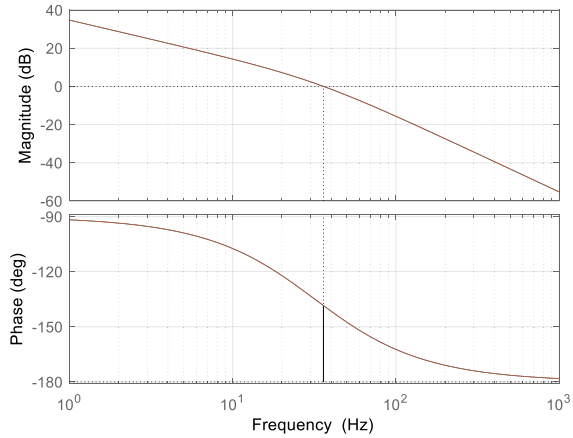


Fig. 24. Bode diagram of the external voltage controller.

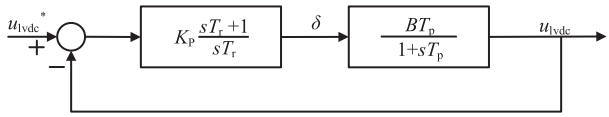


Fig. 25. Simplified configuration diagram of the FBLs voltage controller.

The simplified configuration diagram of the external voltage loop, as shown in Fig. 23, can be obtained from the article presented in [47].

In the external voltage controller, $T_{eu} = \tau_u + 3T_s$ is the sampling period of the voltage loop, $K_{uP}$ and $K_{uI} = K_{uP}/\tau_u$ are the proportional and integral gains, respectively, and the open-loop transfer function of the external loop can be obtained as

$$W_{ou}(s) = \frac{0.75K_{iP} \times (\tau_u s + 1)}{C\tau_u s^2(T_{eu}s + 1)}. \tag{28}$$

The controller of the external voltage loop can be designed to be a second-order system

$$K_{uP} = \frac{4C_{\text{eq}}}{5T_{eu}}, \quad K_{uI} = \frac{4C_{\text{eq}}}{25T_{eu}^2} \tag{29}$$

where $C_{\text{eq}}$ represents the equivalent capacitance of MMC SMs. Based on the parameters, as given in Table V, the bode diagram of the external voltage controller is shown in Fig. 24.

*3) Controller Design of FBL:* FBLs adopt single voltage loop control, and the design of its controller can refer to DAB [50]. Then, the simplified configuration diagram of the FBL voltage loop can be obtained, as shown in Fig. 25.

$$\begin{cases} P_{\text{con\_}T} = f_0 \int_0^{1/f_0} u_{\text{con\_}T}(i_T(t), T_j) i_T(t) D_T(t) dt \\ P_{\text{con\_}D} = f_0 \int_0^{1/f_0} u_{\text{con\_}D}(i_D(t), T_j) i_D(t) D_D(t) dt \\ P_{\text{sw\_}T} = f_0 \int_0^{1/f_0} f_{sw}(E_{\text{on\_}T} + E_{\text{off\_}T})(i_T(t), T_j)(u_c/u_{\text{ref}})^{K_v} dt \\ P_{\text{sw\_}D} = f_0 \int_0^{1/f_0} f_{sw} E_{\text{rec}}(i_D(t), T_j)(u_c/u_{\text{ref}})^{K_v} dt \end{cases} \tag{24}$$

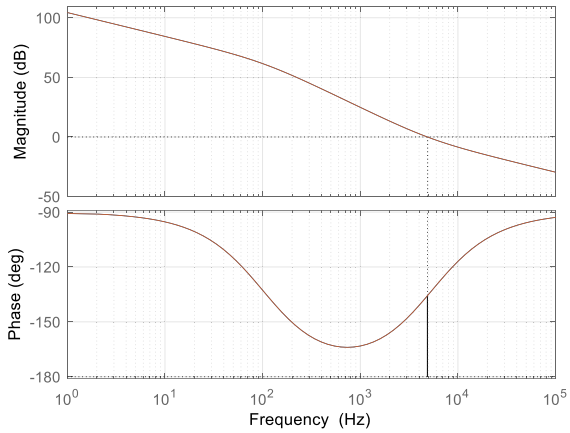


Fig. 26. Bode diagram of the FBLs voltage controller.

The open-loop transfer function of the external loop can be obtained as

$$W_{oFBL}(s) = \frac{K_p B}{s}\frac{T_p}{T_r}\left(\frac{1+sT_r}{1+sT_p}\right) \tag{30}$$

where $T_p = -1/A$, $K_p$ is valued at 0.038, $T_r$ is 655, and

$$\begin{cases} A = -\frac{1}{R_{\text{lvdc}}C_{\text{lvdc}}} - \frac{8}{C_{\text{lvdc}}\pi^2}\sum_{n=0}^{\infty}\left[\frac{\cos(\varphi_z(n))}{(2n+1)^2|Z(n)|}\right] \\ B = \frac{16U_{\text{chfb}}}{C_{\text{lvdc}}\pi^2}\sum_{n=0}^{\infty}\left[\frac{\sin(\varphi_z(n)-(2n+1)\phi)}{(2n+1)|Z(n)|}\right] \end{cases} \tag{31}$$

where

$$\begin{cases} |Z(n)| = \sqrt{R_L^2+[(2n+1)2\pi f_s L_s]^2} \\ \varphi_z(n) = \tan^{-1}\left(\frac{(2n+1)2\pi f_s L_s}{R_{Ls}}\right). \end{cases} \tag{32}$$

Based on the system parameters, as given in Table V, the bode diagram of the FBLs voltage controller is shown in Fig. 26. In addition, the crossing frequency, phase margin, proportional gain, and integral gain are summarized in Table IV.

## V. Simulation and Experimental Verification

CM-SST adopts the control methods as shown in Fig. 18. The MVac side is connected to MVac power grid, while the MVdc and LVdc sides are connected to resistive loads. The simulation and experimental parameters are given in Table V.

### A. Simulation Results

In order to fully verify the natural elimination of SMs ripple voltage and arms second-order frequency current, in the simulation design of this article, the system is divided into four working modes.

*Mode 1:* MVdc bus is at 30% load, HFL is not driven, and LVdc bus is at zero load.

*Mode 2:* MVdc bus is at 30% load, HFL is driven, and LVdc bus is at zero load.

*Mode 3:* MVdc bus is at 100% load, HFL is driven, and LVdc bus is at zero load.

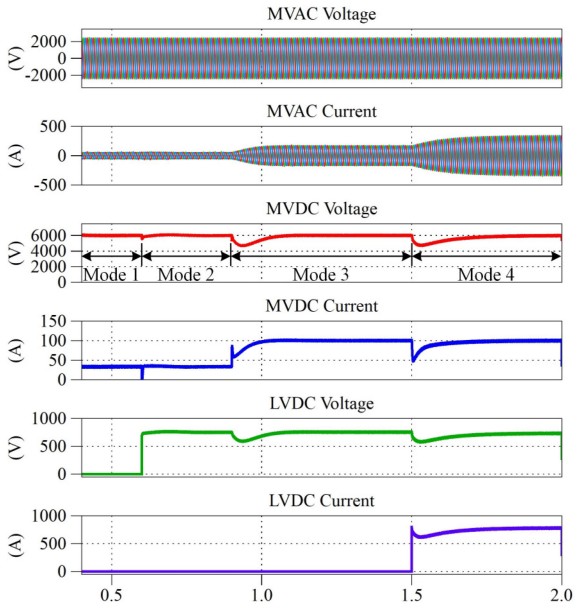


Fig. 27. Simulation waveforms of three ports.

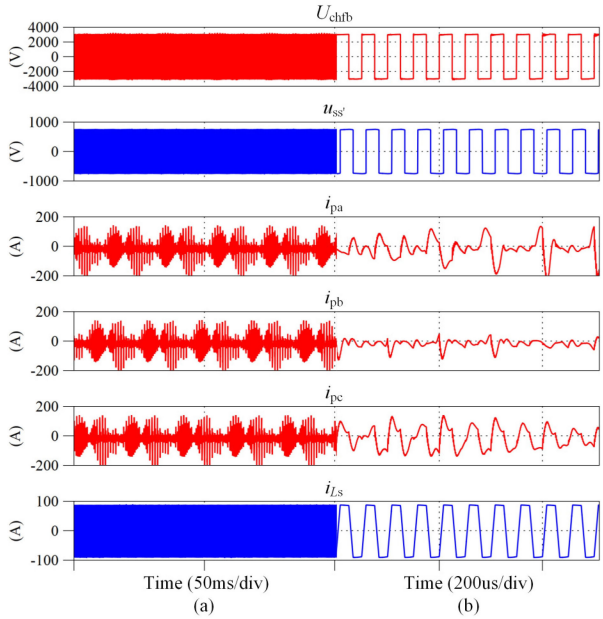


Fig. 28. Internal working mode of FB and FBL in HFL with (a) five fundamental frequency cycles and (b) ten switching frequency cycles.

*Mode 4:* MVdc bus is at 100% load, HFL is driven, and LVdc bus is at 100% load.

Fig. 27 shows the dynamic simulation waveforms of three ports. It can be seen that CM-SST can achieve good operation in different modes. Fig. 28 shows the internal working mode of FB and FBL in HFL; all FBs adopt synchronous modulation signals, and the voltage $U_{\text{chfb}}$ of CHFB can be obtained. As shown in Fig. 28(a), the currents $i_{pa}$, $i_{pb}$, and $i_{pc}$ in the power channel formed by TAB exhibit three-phase symmetry, which is the basis of the ripple-power decoupling analyzed in Section III-A. Phase-shift modulation is adopted between FBs and FBL.

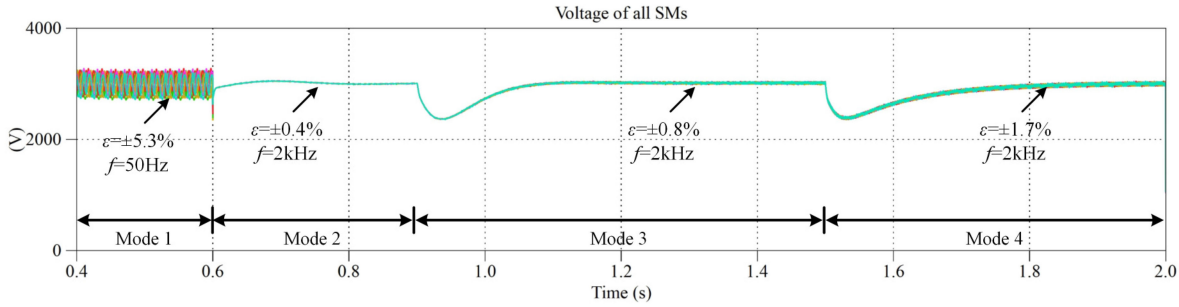


Fig. 29. Verification of SMs ripple-voltage elimination.

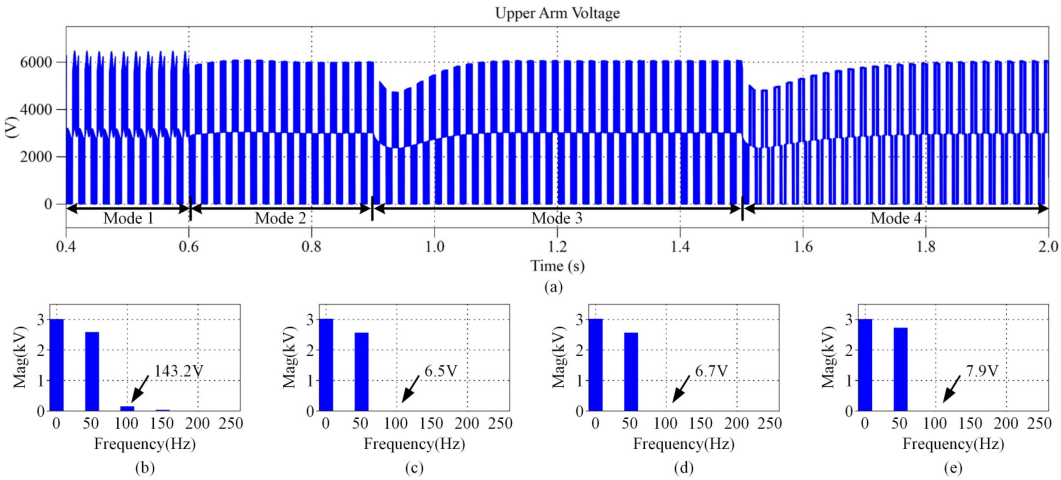


Fig. 30. Simulation waveforms of arm voltage. (a) Upper arm voltage and the FFT analysis results in (b) Mode 1, (c) Mode 2, (d) Mode 3, and (e) Mode 4.

When the ripple currents are offset in the power decoupling channel, the current on the FBL side no longer contains low-frequency ripples.

Fig. 29 shows the waveforms of all SMs capacitor voltages in four modes. Figs. 30 and 31 show the simulated waveforms of arm current and arm voltage and the fast Fourier transform (FFT) analysis results of the four modes. Before the HFL is driven in Mode 1, the SM voltage fluctuation is mainly low-frequency components. According to the analysis in Section II-C, it can be known that second-order voltage and second-order circulation will be further formed in the arms, as shown in Figs. 29(b) and 30(b). When entering Mode 2, HFL is driven and the power decoupling channel is formed. The SM capacitors show switched-capacitor characteristics under synchronous modulation of TAB, and the SM input ripple currents can cancel each other out. Only switching harmonics exist on the capacitors, and the second-order voltage and circulating current will be automatically eliminated accordingly, as shown in Figs. 30(c) and 31(c). Since SM capacitors no longer need to absorb low-frequency ripple current, this greatly reduces the size of the capacitors. As can be seen from Mode 3 in the three groups of simulation waveforms, the elimination effect of ripple voltage, arms second-order voltage, and circulating current is not affected. According to the simulation waveform of Mode 4, when the LVdc bus has power output, this characteristic is still not affected, and the switching harmonics on the SM capacitor slightly increase, as shown in Fig. 29. What should be specially noted is that the impedance, including inductances and resistances of TAB, has been set to about 10% of the inconsistency, and the simulation results show that this does not affect the effectiveness of the CM-SST.

Fig. 32 shows the verification waveforms of the automatic balancing of SMs voltage. After artificially setting the inconsistency of SMs' parameters, such as the capacitance and drive delay time, the SMs voltage appears unbalanced in Mode 1. After the HFL is driven in Mode 2, all SMs voltage can achieve the automatic balance without any additional control.

### *B. Experimental Results*

In order to further verify the effectiveness of the proposed CM-SST, a down-scaled three-level platform, as shown in Fig. 33, was built, and the parameters are listed in Table V.

The experimental waveforms, as shown in Fig. 34, are the verification of natural elimination of SMs ripple voltage and arms second-order circulating current. After the HFL is driven and the power decoupling channel is formed, the three-phase symmetrical ripple power in horizontal SMs will cancel each other, and the ripple voltage will be naturally eliminated, as shown in Fig. 34(a), then the arms circulating current will be

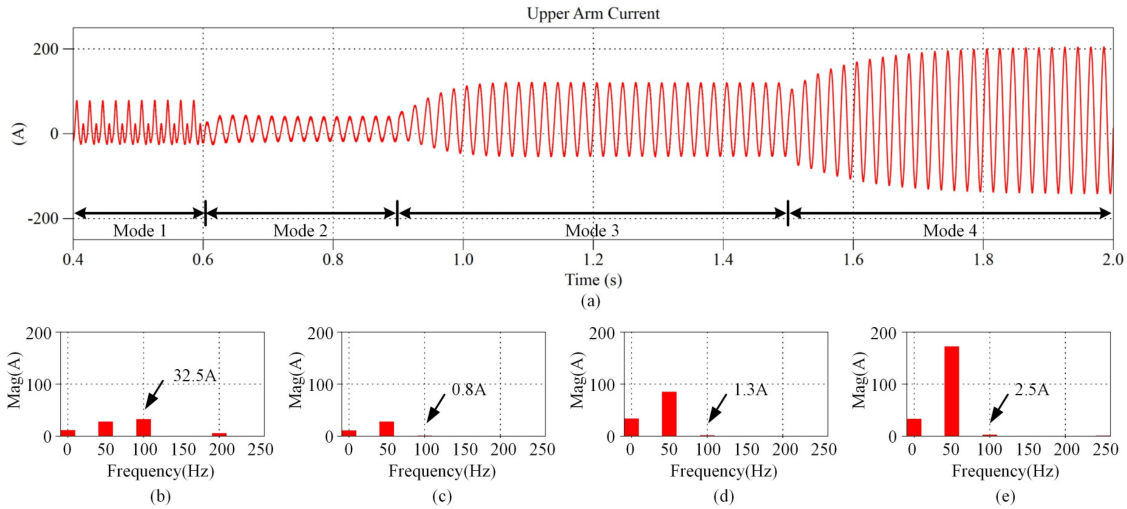


Fig. 31. Verification of arm second-order circulating current elimination. (a) Upper arm current and the FFT analysis results in (b) Mode 1, (c) Mode 2, (d) Mode 3, and (e) Mode 4.

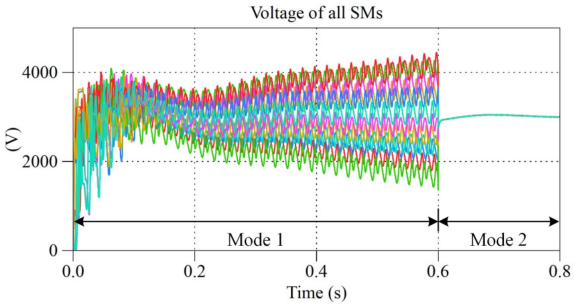


Fig. 32. Verification of SMs voltage automatic balance.

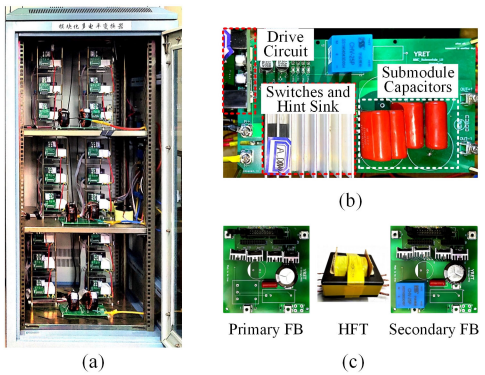


Fig. 33. Prototype of the down-scaled experimental platform. (a) Overall platform. (b) SM. (c) FB and HFT.

eliminated from the root cause, as shown in Fig. 34(b). After artificially setting the inconsistency of SMs' parameters, the automatic balancing verification of SMs voltage is shown in Fig. 35, including both the horizontal SMs balancing and vertical SMs balancing.

The internal working mode of FB and FBL in HFL is shown in Fig. 36. As shown in Fig. 36(a), the current transmitted by

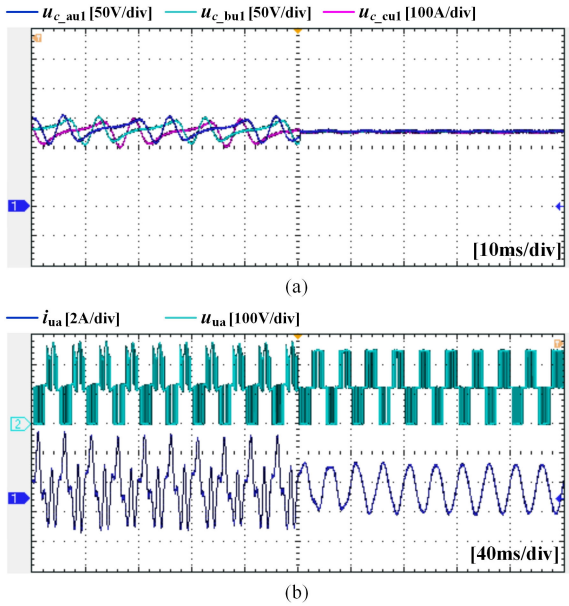


Fig. 34. Verification of natural elimination of (a) SMs ripple voltage and (b) arms second-order circulating current.

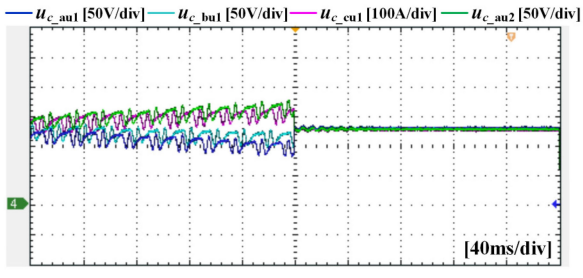


Fig. 35. Verification of automatic balancing of SMs voltage.

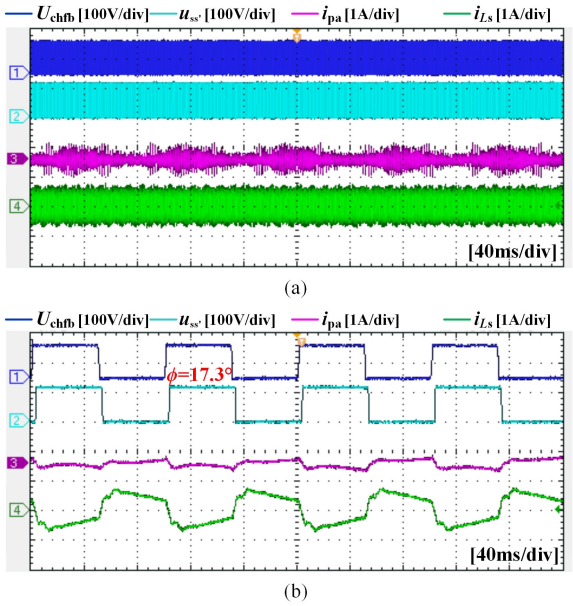


Fig. 36. Internal working mode of FB and FBL in HFL with (a) five fundamental frequency cycles and (b) four switching frequency cycles.

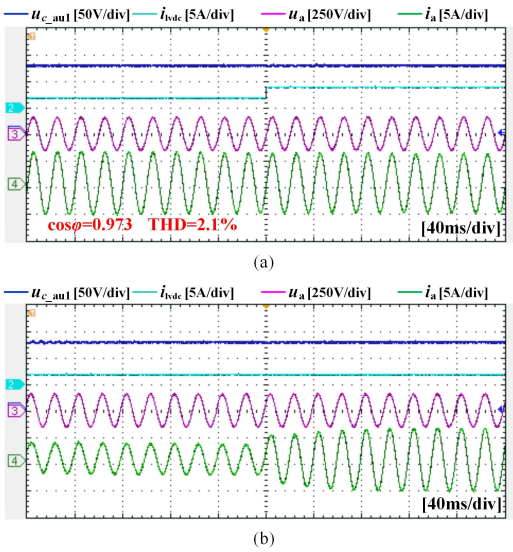


Fig. 37. Dynamic experimental waveforms. (a) LVdc load from 50% to 100%. (b) MVac load from 50% to 100%.

FB contains the active component and ripple component. After the ripples are decoupled in the power channel formed by TAB, FBL adopts phase-shift modulation to transfer the active current to realize the power exchange between CHFB and LVdc bus.

Fig. 37 shows the dynamic experimental waveforms of CM-SST. As shown in Fig. 37(a), when the output power of the LVdc bus is stepped from 50% to 100%, the SMs voltage oscillates slightly, and the grid-connected power on the MVac side is also not affected. As shown in Fig. 37(b), when the grid-connected power is stepped from 50% to 100%, the stability of SMs voltage and LVdc output power is good. The above experimental results verify that CM-SST has good dynamic performance.

## VI. Conclusion

Aiming at the application of hybrid medium- and low-voltage multibus multiport distribution network, this article proposes a CM-SST, which is composed of MMC stage and HFL stage based on a CHFB. The CHFB in HFL helps to reduce the numbers of switching modules in the form of multiplexing, and the decoupling channel achieves the automatic balancing of capacitors voltage and natural elimination of SM ripple power, and then the arms second-order circulating current can be eliminated. Therefore, the CM-SST can simultaneously realize size reducing and control simplification. The evaluation results show that the sizing of CM-SST can be decreased by 46.6% compared with the existing MMC-based SST topology.

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