Letters

Capacitive Power Transfer System With Integrated Wide Bandwidth Communication

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***Abstract*—This letter proposed a novel method for compensation network design used in capacitive power transfer (CPT) systems to achieve simultaneous power and data delivery. The proposed method combines both ladder filter and resonant circuit designs, allowing the existing double-sided CL compensation topology to exhibit different characteristics under the power channel and the communication channel. The proposed system significantly reduces the design complexity and increases the bandwidth for data transfer while maintaining the circuit resonance at the wireless power transfer frequency. The system is compatible with both amplitude shift keying (ASK) and frequency shift keying (FSK) modulation methods, passing the high-frequency data carrier with an approximately unity gain. Detailed circuit parameter design and system performance analysis are presented, and a new metric power to signal is introduced to analyze the effect of the data communication on the power transfer. A prototype CPT system rated at 10 W is built, which demonstrates a 81.2% dc–ac efficiency and a data transfer rate of 10 kbps by using either ASK or FSK modulation techniques.**

***Index Terms*—Capacitive power transfer (CPT), communication, wireless power transfer (WPT).**

I. Introduction

CAPACITIVE power transfer (CPT) technology emerges as a cheaper and lighter alternative solution to wireless power transfer technology in recent years. It uses two pairs of metal plates to form the capacitors, allowing power transferred through alternating electric fields. Compared to inductive power transfer technology, the CPT technology also has a better performance in electromagnetic interference containment and misalignment, etc. [1], [2].

Most CPT researchers focus on improving power transfer capability and power density [3], [4]; however, little attention is paid to data transfer for CPT systems, especially in-band communication using the same electric field couplers. The main challenges to integrate wireless communication into a CPT system are from its high system sensitivity and the components restrictions under the high operating frequency. The disturbance caused by the data signal modulation leads to drops in power transfer efficiency and power transfer capability. Works in [5]–[7] are designed for low-power applications like sensors and bio-implants and have poor power transfer efficiency. In [8], it achieved a full-duplex communication CPT system rated at 100 W, but the data channel must be carefully designed to maintain a desired signal-to-noise ratio (SNR). To summarize, the existing in-band communication solutions are complex, and their communication bandwidth is limited at a specific frequency.

Motivated by the aforementioned drawbacks, this letter proposes a novel compensation parameter design method to achieve simultaneous power and data transfer based on the existing double-sided CL topology. Besides meeting resonance requirements for power transfer as presented in [9], the CL components also need to satisfy the high-pass conditions for communication signal. In such a way, the CPT system behaves as an amplifier under the power channel frequency. Meanwhile, it presents the properties of a high-pass filter under the communication channel frequency. Instead of transmitting data at a specific frequency, the proposed method provides an extended frequency region for communication, compatible with amplitude shift keying (ASK) or frequency shift keying (FSK) modulations. Multiple strings of data can be transferred under different frequencies at the same time, which maximizes the data transfer capacity.

II. System Structure and Data Channel Design

A. System Operating Principle

The system diagram is presented in Fig. 1. A dc source is connected with a high-frequency dc/ac inverter to power the entire CPT system. A double-sided CL topology is used to form resonant compensation networks at both sides of the capacitive couplers C_{s1} and C_{s2}. The data stream is modulated with a carrier signal at a frequency f_d and injected into the main power loop through the series modulator on the primary side. The data are then retrieved by the demodulation circuit on the secondary

Manuscript received January 12, 2022; revised February 12, 2022 and March 8, 2022; accepted March 9, 2022. Date of publication March 15, 2022; date of current version April 28, 2022. *(Corresponding author: Qi Zhu.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3158994.

Digital Object Identifier 10.1109/TPEL.2022.3158994

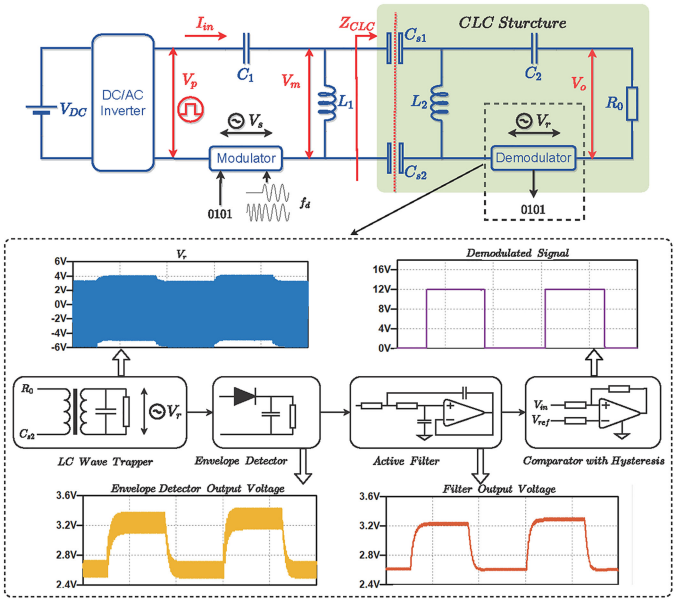

Fig. 1. Proposed system structure with wireless communication.

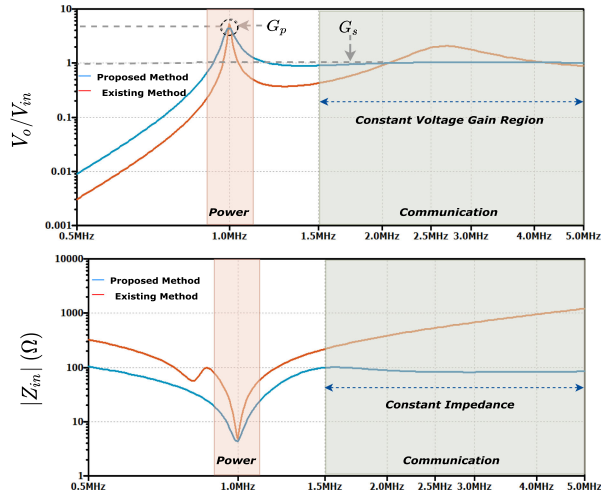

Fig. 2. Frequency response of the output voltage gain and system input impedance.

side, in which multi-stage filtering circuits inside recover the original data signals.

Assume a half-bridge inverter is used, V_p can be yielded as

$$V_p = \sum_{k=1}^{\infty} \frac{2}{k\pi} sin(k\omega t) V_{\rm DC} = \frac{2V_{\rm DC}}{\pi} \sum \left(V_{p1} + \frac{1}{3}V_{p1} + \frac{1}{5}V_{p1} + \cdots + \frac{1}{k}V_{p1} \right) \quad (1)$$

where ω is the CPT system operating frequency, and V_{p1} is the fundamental voltage component. The dc bias from the half-bridge is ignored due to dc blocking capacitor C_1. The system input voltage $V_{\rm in}$ is defined as the sum of the two sources: $V_{\rm in} = V_p + V_s$. As V_p and V_s are independent sources, and of two frequencies, superposition theorem can be applied to analyze the systems.

Existing compensation network designs focus on improving the CPT system power transfer efficiency by tuning the CPT system at a specific operating frequency [10]. Nonetheless, above the frequency of interest, the output voltage gain value is fluctuating, as shown in Fig. 2. This brings design difficulties to integrate inband communication feature and limits the bandwidth of the communication channel. In contrast, the CLC structure of the proposed system (shown in Fig. 1) are designed to obtain an approximately constant voltage gain curve in a high-frequency region for communication purpose; and the primary CL network is then designed to boost the voltage gain at a lower frequency to maintain resonance for the power transfer. Fig. 2 shows the overall frequency response of the system voltage gain, as well as the system input impedance using the proposed tuning method.

Once the data carrier frequency is allocated to that region, ideally, the carrier signal amplitude will not change. Instead of transmitting data under a specific frequency, the data can be transferred in a wide range, which significantly extends the bandwidth for the communication channel in the CPT system. In addition, more frequencies can be used to transfer multiple threads of data at the same time to improve data transfer capacity. Data can be transferred alongside the power delivery without affecting its power transfer capability. The proposed method can work with ASK and FSK modulations with different modulator designs.

B. Data Channel Parameter Design

In the conventional design method, the secondary CL section is designed to step down the voltage and to amplify the current [11]. In this letter, the proposed design method preserves the functionality of the CL section and meanwhile absorbs the coupling capacitor C_s, serving as a CLC high-pass filter, where $C_s = C_{s1}C_{s2}/(C_{s1} + C_{s2})$.

The proposed design method begins from choosing the cutoff frequency ω_c of the CLC structure and the equivalent load resistance R_0. As guided in [12], a third-order CLC high-pass filter could be designed as follows. The parameters g_1, g_2, and g_3 are the normalized filter coefficients

$$C_s = 1/(g_1\omega_c R_0), L_2 = R_0/(g_2\omega_c), C_2 = 1/(g_3\omega_c R_0). \quad (2)$$

Note that in most of the CPT applications, the coupling capacitance C_s is a given value. Therefore, the component values for L_2 and C_2 can be easily fixed providing the filter coefficients. In this study, Butterworth filter design is chosen as an example to ensure maximum flatness of the output voltage gain, and the filter coefficients are given as

$$g_1 = 1.5, g_2 = 4/3, g_3 = 0.5. \quad (3)$$

Given the coefficients from the above equation, the transfer function of voltage gain in the CLC section then can be expressed as

$$G_2(s)|_{\omega>\omega_c} = \frac{V_o(s)}{V_m(s)} = \frac{s^3}{s^3 + (2\,\omega_c)\,s^2 + (2\,\omega_c{}^2)\,s + \omega_c{}^3} \approx 1. \quad (4)$$

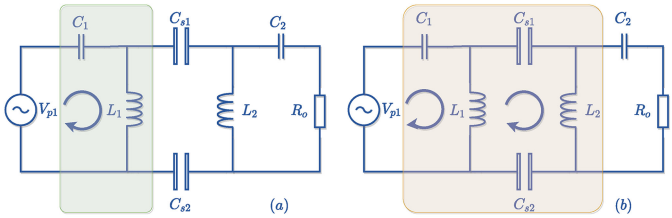

Fig. 3. Double-sided CL compensation design. (a) Method 1: CL resonance without couplers. (b) Method 2: CL resonance with couplers.

As the frequency ω increases beyond the corner frequency ω_c, the voltage gain ratio G_2 converges to 1. The input impedance of the CLC structure Z_{CLC} becomes purely resistive, a constant of R_0.

$$\begin{cases} \underset{\omega>\omega_c}{\Re(Z_{\text{CLC}})} = \dfrac{9\,R_0\,\omega^4}{9\,\omega^4+4\,\omega^2\,{\omega_c}^2+4\,{\omega_c}^4} \approx R_0 \\ \underset{\omega>\omega_c}{\Im(Z_{\text{CLC}})} = \dfrac{(-6\,R\,\omega_c)\,\omega^4+\left(-3\,R\,{\omega_c}^3\right)\omega^2-6\,R\,{\omega_c}^5}{9\,\omega^5+(4\,{\omega_c}^2)\,\omega^3+(4\,{\omega_c}^4)\,\omega} \approx 0 \end{cases}. \tag{5}$$

Based on (5), define the voltage gain of the primary CL section as G_1, and the overall system voltage gain under communication channel frequency G_s, which yields

$$G_1(s)|_{\omega>\omega_c} = \frac{V_m(s)}{V_s(s)} = \frac{L_1C_1R_0\,s^2}{L_1C_1R_0\,s^2+L_1s+R_0} \tag{6}$$

$$G_s(s)|_{\omega>\omega_c} = |V_o(s)/V_s(s)| = G_1(s)G_2(s) \approx G_1(s). \tag{7}$$

From the above equations, it could be seen that when $\omega > \omega_c$, the system voltage gain is mainly governed by the primary CL section. It needs to obtain the high-pass characteristics as the cascaded CLC structure does. Detailed conditions and relationships among L_1, C_1, and G_1 will be discussed together with the power channel design in the next section.

III. Power Channel Design and Comparison

The double-sided CL compensation network also needs to resonant at a lower system operating frequency ω_p to accommodate the power needs. As analyzed in [13], it has two different compensation design techniques, as depicted in Fig. 3. One is to resonate with the local CL loops, which is less sensitive to coupling variations. The other resonates with the coupling plates, requiring less input current to achieve the desired output power. To differentiate the design, the angular frequency under those two design methods is notated as ω_{p1} and ω_{p2}, respectively.

A. Method 1: CL Resonance Without Couplers

Method 1 suggests that the following requirements need to be met:

$$\omega_{p1}^2L_1C_1 = \omega_{p1}^2L_2C_2 = 1. \tag{8}$$

The output voltage gain and the input impedance phase angle under the power channel then can be obtained as

$$G_p = |V_{\text{out}}/V_{\text{in}}| = C_1/C_2 \tag{9}$$

$$\theta_1 = \text{atan}\left(\frac{{C_2}^2\,R_0\,\omega_{p1}}{C_s} - \frac{C_2\,R_0\,\omega_{p1}\,(C_1+C_2)}{C_1}\right). \tag{10}$$

Equations (2), (3), and (8) yield the relationship between cutoff frequency and system operating frequency

$$\omega_{p1}/\omega_c = \sqrt{g_2g_3} \approx 0.816. \tag{11}$$

When the symmetrical design is applied as shown in [9], the unity gain can be obtained, yet the zero phase angle (ZPA) cannot be achieved

$$\theta_1 = \text{atan}(3C_sR_0\omega_{p1}) = 58.518^\circ. \tag{12}$$

To obtain ZPA condition, as shown in (10), $C_1 = 1.5C_s$. With an asymmetrical design of $C_1 = 0.5C_2$, the output voltage is half of the input voltage.

$$\theta_{1,ZPA} = \text{atan}\left(\frac{3\,C_s\,R_0\,w_c\,(2\,C_1-3\,C_s)}{C_1}\right). \tag{13}$$

Recall (6) and (7), with the conditions listed in (8) and (11), G_1 can be rewritten as

$$\begin{cases} G_1(s) = \dfrac{6\,s^2}{6\,s^2+3\,\omega_c s+4\,{\omega_c}^2}, & \text{Symmetrical} \\ G_1(s) = \dfrac{3\,s^2}{3\,s^2+3\,\omega_c s\,+4\,{\omega_c}^2}, & \text{Asymmetrical} \end{cases}. \tag{14}$$

In either designs, if the frequency is above the corner frequency of the CLC structure ω_c, then the s^2 term will be more dominant, so the voltage gain G_1 will approach 1.

B. Method 2: CL Resonance With Couplers

Method 2 suggests that the following requirements need to be met:

$$\begin{cases} \omega_{p2}^2L_{eq1}C_1 = 1, & L_{eq1} = \dfrac{L_1\left(C_s\,L_2\,\omega_{p2}^2-1\right)}{C_s\,L_1\,\omega_{p2}^2+C_s\,L_2\,\omega_{p2}^2-1} \\ \omega_{p2}^2L_{eq2}C_2 = 1, & L_{eq2} = \dfrac{L_2\left(C_s\,L_1\,\omega_{p2}^2-1\right)}{C_s\,L_1\,\omega_{p2}^2+C_s\,L_2\,\omega_{p2}^2-1} \end{cases}. \tag{15}$$

By solving (2), (3), and (15), we can get the input impedance as

$$Z_{\text{in}} = \frac{V_{\text{in}}}{I_{\text{in}}} = \frac{{\text{C}_\text{s}}^2\,{L_1}^2\,{L_2}^2\,\omega_{p2}^6}{R_0\left(\text{C}_\text{s}\,L_1\,\omega_{p2}^2+\text{C}_\text{s}\,L_2\,\omega_{p2}^2-1\right)^2}. \tag{16}$$

The above equation states that the system input impedance does not have any imaginary part, which implies that the ZPA condition will always hold. If the symmetrical design is applied, the inductor value could be designed as

$$L_2 = \frac{g_1+2\,g_3-\sqrt{{g_1}^2+4\,{g_3}^2}}{2\,C_s\,g_1\,\omega_{p2}^2} \approx 0.232/(C_s\omega_{p2}^2). \tag{17}$$

The relationship between the CLC structure cutoff frequency and system operating frequency can also be yielded as

$$\frac{\omega_{p2}}{\omega_c} = \frac{\sqrt{2g_2}\sqrt{g_1+2\,g_3+\sqrt{{g_1}^2+4\,{g_3}^2}}}{2} \approx 0.682 \tag{18}$$

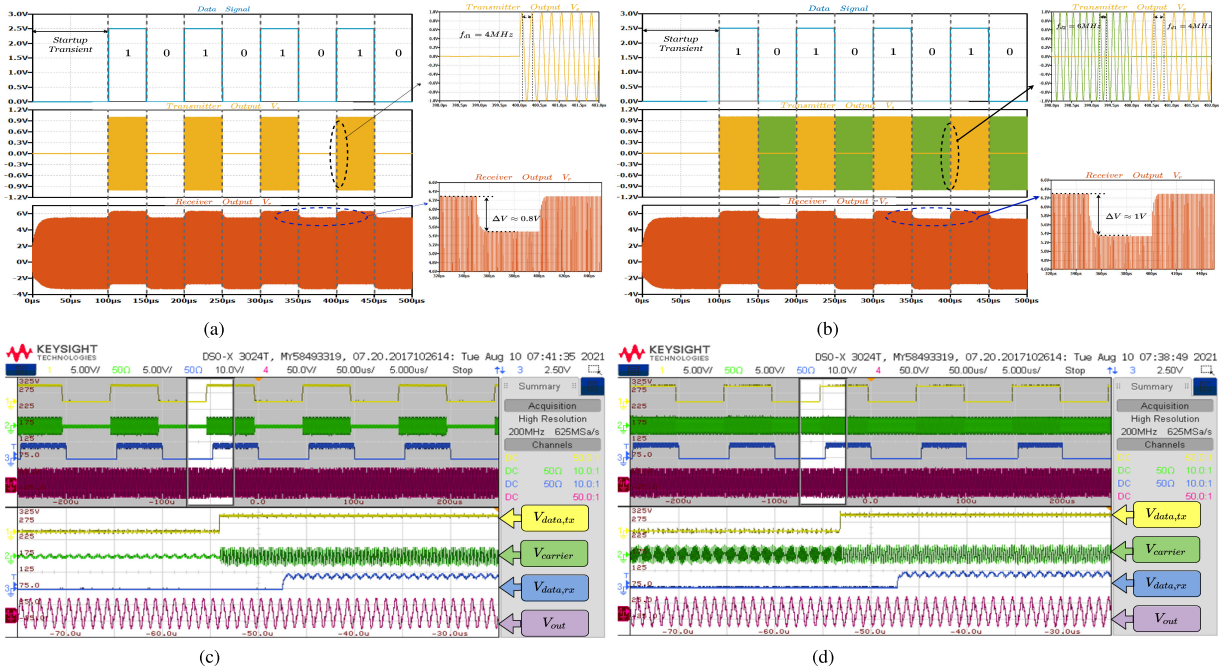

Fig. 4. Simulation and experimental waveforms. (a) System simulation results with ASK modulation. (b) System simulation results with FSK modulation. (c) System experimental results with ASK modulation. (d) System experimental results with FSK modulation.

TABLE I
COMPARISON OF DIFFERENT DESIGN METHODS

Attributes \ Mode	Method 1 (no ZPA)	Method 1 (ZPA)	Method 2 (ZPA)
ω_p/ω_c	0.816	0.816	0.682
θ	58.518°	0°	0°
G_p	1	0.5	4.505
$PSR(k=3)$	2.308	1.154	10.396
$PSR(k=4)$	10	5	45.05
$PSR(k=5)$	3.333	1.667	15.017
$PSR(k=6)$	10	5	45.05

and the voltage gain under the power channel is calculated as a constant, $G_p = 4.505$.

Similar to the symmetrical design analysis in (14), the voltage gain of primary CL section G_1 will reach 1 as the frequency rises above ω_c.

C. Design Comparison

The attribute power to signal ratio (PSR) is introduced to describe how much impact the communication signal on the original power signal. A higher PSR value indicates that the data signal has a very low effect on the original power transfer system, which helps to avoid the cross-talk between the two channels. The PSR is defined as

$$\text{PSR} = \frac{V_{p1}G_p}{(k\%2)(1/k)V_{p1}G_p + V_sG_s}, \text{ and } k \in \mathbb{Z} \qquad (19)$$

k is the ratio of the data carrier frequency over the system operating frequency. Assume the same sources are applied to the aforementioned three designs, we normalize $|\hat{V_s}|$, and set $|\hat{V_{p1}}| = 10|\hat{V_s}|$. In Table I, it compares three different designs.

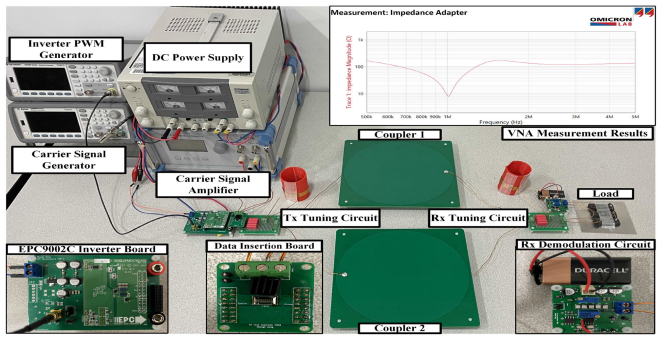

Fig. 5. Experimental setup and measured system input impedance.

It could be seen that with the Method 2 tuning method, coupled with a data frequency of an even number k ratio, the system has a higher PSR value. The power signal should have a much higher amplitude than the data signal. In addition, setting k as an even number can help avoid the clash between the high-order harmonic components of the power frequency and the data carrier frequency. The simulation model has been built and verified with Method 2, as shown in Fig. 4(a) and (b). A voltage variation of 1 V can be observed using either modulation technique. This voltage variation can be further filtered and recovered to the original data signal.

IV. EXPERIMENTAL RESULTS

Fig. 5 shows the experiment setup of the CPT system with the proposed compensation design method. The system is rated at 10 W, using $EPC9002\,C$ as the inverter to generate square-wave ac voltage excitation from the dc supply on the primary side. A

TABLE II
PARAMETERS OF EXPERIMENTAL SETUPS

Parameter	Value	Parameter	Value
Operating Frequency	$1MHz$	L_1,L_2	$11.4\mu H$, $11.5\mu H$
Carrier 1 Frequency	$4MHz$	C_1,C_2	$1.51nF$,$1.48nF$
Carrier 2 Frequency	$6MHz$	CT	Coilcraft PFD3215
Corner Frequency	$1.47MHz$	R_0	150Ω
Data Rate	$10kbps$	V_{DC}	$20V$
Coupler (C_{s1},C_{s2})	$1.02nF$	PSR	57.3

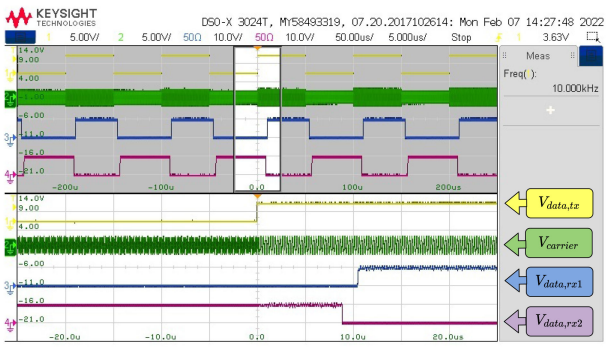

Fig. 6. Experimental results with the dual-frequency demodulator.

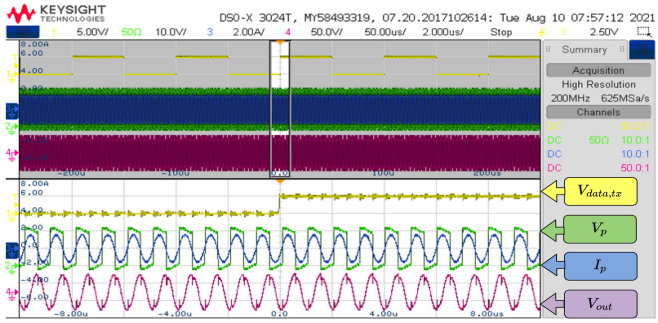

Fig. 7. Waveforms of data, inverter, and load voltage.

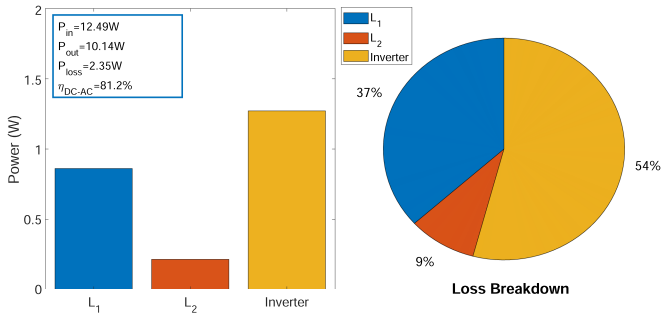

Fig. 8. Loss breakdown of the proposed system.

data insertion board is connected in series with the inverter and the primary CL tuning circuit. A 9-V battery is used to power the Op-Amps for filtering and retrieving the data signals. From the VNA measurement results, it can be seen that the system input impedance curve is flat, which is consistent with the simulation results in Fig. 2. Detailed system parameters are listed in Table II.

Fig. 4(c) and (d) demonstrates the system performance by both ASK and FSK modulations. To avoid ground wire connections, all oscilloscope channels use high-frequency differential probes to conduct measurements. The yellow trace is the input data signal, while the blue is the recovered signal on the secondary side. In either case, the data can be demodulated and retrieved without any missing bits or errors. It should be noted that there is a delay in the data signal between input and output, which is caused by multistage filtering processes on the demodulation board. The initial prototype is estimated to have an SNR of 15 dB, mainly caused by the 1-MHz high-frequency switching.

The dual-frequency demodulator is designed to decode multiple strings of data at the same time to maximize the data transfer capacity. As shown in Fig. 6, it can successfully retrieve the data signals embedded in the 4- and 6-MHz carriers, respectively.

Fig. 7 shows the voltage and current profiles from the inverter and the voltage across the load. It could be measured that the phase between the voltage and the current is of a degree of $-3.8\,\mathrm{deg}$, which indicates that the ZPA condition is almost achieved considering practical turning error. In addition, the output voltage stays the same regardless of the data state changes, proving that the data signal has a minimal impact on the power transfer. The system has a peak dc–ac efficiency of 81.2% with 10-W output power on the load. A detailed loss breakdown is shown in Fig. 8. The inverter loss is of 1.28 W, which contributes over 50% of the total loss due to the high-frequency switching.

V. CONCLUSION

This letter introduces a novel compensation/filtering design technique of a CPT system for achieving in-band data communication while maintaining wireless power transfer. The proposed design significantly extends the communication bandwidth with minimal effect on the characteristics of the conventional CPT system. The operating principles and design procedures are elaborated to provide insights into choosing appropriate operating modes and data carrier frequencies. The system is fully implemented and verified by both simulations and experiments results. A prototype rated at 10 W has been built and a dc–ac efficiency of about 81.2% is achieved. On the communication side, both ASK and FSK modulation techniques have been used to achieve wireless data transfer at a rate of 10 kbps.

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