Asymmetric Phase-Shift Modulation Strategy of DAB Converters for Improved Light-Load Efficiency

Gen Chen, Zhangyong Chen, Yong Chen, *Senior Member, IEEE*, Chenchen Feng, and Xintong Zhu

***Abstract*—Dual active converter (DAB) can achieve high efficiency when the voltage ratio (the ratio of the input voltage to the output voltage equivalent to the primary side) is one, but when the voltage ratio is not one, the light-load efficiency drops sharply. Based on the realization logic of DAB light-load, this article proposes a modulation method with asymmetric compression duty cycle, which only increases one degree of freedom and does not need additional components to significantly improve the light-load efficiency. First, this article introduces the existing problems and solutions of the traditional scheme and puts forward a new modulation strategy. Then, the operating modes and power characteristics are analyzed. Then, the influence of duty cycle compression on reflux power and current stress is analyzed. Finally, a prototype with an input voltage of 100–200V, an output voltage of 50 V, and a full load power of 300–600 W is built to verify the analysis.**

***Index Terms*—Backflow power, current stress, dual active converter (DAB) converter, light-load efficiency, soft switching.**

I. Introduction

Dual active bridge (DAB) converter was first proposed in [1] to pursue higher power density for high power applications. In [2], a medium-voltage power conversion system with DAB as the core topology was constructed, and the efficiency reached 99% under the power background of 10 kW. Since then, DAB converter has been found to have the advantages of high efficiency, high power density, bidirectional power flow, simple structure and easy integration, easy to realize soft switching, etc., so it has been studied a lot [3]–[8].

However, in recent years, due to the development of electric vehicles, dc microgrid, distributed generation and other technologies, more efficient battery energy storage system (ESS) have become one of the key issues [3]–[6]. Converters in ESSs are required to easily switch between charging and discharging modes, to achieve high voltage gain, and to achieve electrical isolation between the high voltage and low voltage sides for safety. Therefore, DAB converter stands out and is widely used in medium and high power applications.

In [1], the simplest modulation method of DAB, namely single-phase-shifting modulation, was proposed at the same time with the topology structure of DAB. In single phase shift (SPS) strategy, the primary voltage duty ratio and the secondary voltage duty ratio are both 50%, but there is a phase-shift between the primary side and secondary side. The power flow can be controlled by adjusting the size of the phase-shift. When the voltage ratio (defined as the ratio of the output voltage to the input voltage) is equal to 1, soft switching over the full power range can be achieved with the SPS strategy. However, when the voltage ratio deviates from 1, the soft switching range shrinks rapidly, the soft switching can no longer be realized under light-load. At the same time, the loss caused by large backflow power is also highlighted. Therefore, the light-load efficiency decreases rapidly [9].

A number of strategies have been proposed to solve this problem. Extended-phase-shift (EPS) adds an internal phase-shift in the primary side so that the primary side voltage has a 0 level as a buffer when the positive and negative alternates, thus reducing the backflow power and current stress [10], [11]. Dual phase-shift (DPS) adds inner phase-shift on both the primary side and the secondary side, which can also reduce the backflow power and current stress [12], [13]. On the basis of DPS, triple-phase-shift (TPS) adds a degree of freedom, which allows the inner shift phase on both sides to be unequal. TPS can achieve better performance, but too many degrees of freedom make it very complicated to calculate [14]. In addition, [15] points out that these schemes can only improve efficiency when the output voltage variation range (defined as the ratio of the maximum output voltage to the minimum output voltage) is less than 1.5. In ESS, it is very common for the output voltage variation range to be greater than 2. Therefore, a novel midpoint clamped DAB converter is proposed to widen the output voltage range. Because SPS modulation is still used, the problem of low light-load efficiency has not been well solved. In order to solve the problem of low light-load efficiency of SPS, [16] proposed to use dc blocking capacitor to introduce voltage bias to reduce the backflow power and expand the ZVS range, but this scheme only applies to the case when the output voltage is twice the input voltage. In [17], a variable switching frequency modulation strategy is proposed to improve the performance of SPS, but a high frequency is needed to ensure the realization

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Gen Chen, Yong Chen, Chenchen Feng, and Xintong Zhu are with the School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China (e-mail: 544056107@qq.com; ychencd@uestc.edu.cn; 269365620@qq.com; 413691157@qq.com).

Zhangyong Chen is with the School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China, and also with the Yangtze Delta Region Institute, University of Electronic Science and Technology of China, Huzhou 313001, China (e-mail: zhang_yong_ch@126.com).

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of soft switching under light-load. A resonant DAB converter is proposed in [18] which can switch between full bridge and half bridge structures. It reduces backflow power and circulating current at the expense of additional components, which makes controller design more difficult and brings additional losses. A hybrid modulation strategy based on GaN devices is proposed in [19] to optimize the light-load efficiency of DAB, but GaN devices will increase the cost greatly. In addition to the modulation strategy, some optimization and control methods are also proposed to improve the efficiency of DAB [20]–[24]. These methods are generally optimized for a certain goal, such as minimum stress, minimum backflow power, and minimum RMS current. These solutions require complex calculations and rely on accurate modeling.

In order to solve the problem of low light-load efficiency of DAB converter, a modulation strategy with asymmetric compression duty cycle is proposed in this article. The proposed strategy only increases one degree of freedom on the basis of the traditional single phase-shift, and the light-load efficiency can be improved obviously without additional devices. The idea of the proposed scheme is that the advantages of SPS modulation in the case of heavy load and the disadvantages of light-load are well known. At present, most of the modulation strategies use SPS modulation in the case of full load or close to full load. Therefore, according to the logic of light-load realization, this article proposes a modulation scheme that compresses the duty cycle, which shortens the power transmission time and reduces the return power and forward power.

In Section II, the problems existing in the traditional scheme and the ideas to solve the problems are described, and the strategies of this article are put forward. In Section III, the operating modes and power characteristics of the proposed strategy are analyzed in detail. The effect of compression duty cycle on return power and current stress is analyzed in Section IV, and the experimental results are included in Section V. Finally, Section VI concludes this article.

II. Ideas for the Generation of the Proposed Strategies

A. Problems of Traditional Phase Shifting Strategy

As mentioned above, the efficiency of traditional single phase-shift strategy will be reduced when the voltage ratio deviates from 1. Moreover, it is especially serious under light-load conditions. One of the reasons is that when the voltage ratio deviates from 1, some switches in the single-phase-shift strategy cannot realize soft switching under light-load, so the loss increases and the efficiency decreases.

Another important factor has to do with the implementation logic for light-loads. In the isolated DAB converter, the transmitted power P is equal to forward power P_F minus back-flow power P_B. So, as P_B gets bigger, P_F needs to get bigger to make sure P stays constant. The increase of P_F and P_B must mean the increase of root-mean-square value and effective value of current, so the loss of the resistive part of each device will increase, resulting in lower efficiency. At heavy load, as shown in Fig. 2(a), both P and P_F are large, and P_B is relatively small

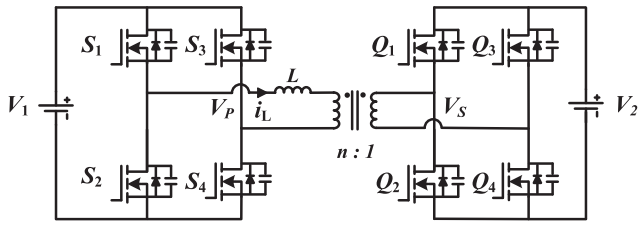

Fig. 1. DAB converter topology.

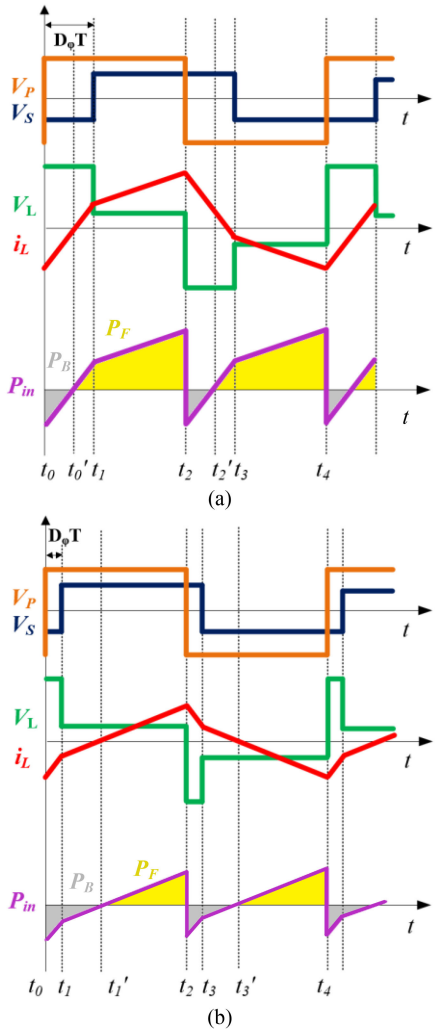

Fig. 2. Waveforms of DAB in traditional modulation strategy. (a) Heavy load. (b) Light-load.

compared to them. And since the ratio of P_B to total power is small, the reduction of efficiency caused by it will not be large. However, under light-load, as shown in Fig. 2(b), the P_F is still large due to the 50% duty cycle, so P_B also needs to be a large value to get a small P. Then, the loss caused by this large P_B is highlighted, and the efficiency is significantly reduced.

In order to improve the light-load efficiency, this article proposes an asymmetric compressed duty cycle scheme in terms of the logic of light-load implementation, which changes the logic of light-load implementation to: small PF minus small PB, thus reducing the impact of return power on light-load efficiency and current stress can also be reduced at the same

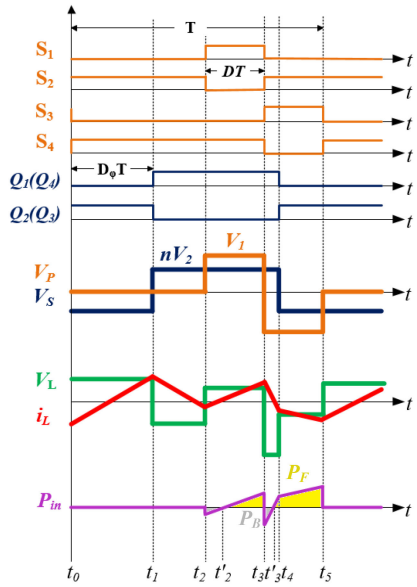

Fig. 3. Waveforms of DAB in the proposed modulation strategy.

time. Due to the increased degree of freedom, the adjustable range of light-load is enlarged, and the soft switching can be implemented simultaneously.

B. Proposed Modulation Strategy

Fig. 3 shows the waveforms of DAB in the proposed modulation strategy. We define the rising edge of S_4 as $t = 0$. S_1, S_3, Q_1, and Q_3 are complementary to S_2, S_4, Q_2, and Q_4, respectively. The duty cycle of the secondary side is fixed at 0.5. It can be seen from this definition that φ can represent the degree of phase-shift of the original and secondary edges, D represents the duty cycle D of the primary side voltage. For convenience of expression, define $D_\varphi = \frac{\varphi}{2\pi}$. Of course, there are some constraints (1) between these two variables to ensure that the timing of the switch is as shown in the figure above

$$\left(\frac{1}{2} - D \le D_\varphi \le 1 - 2D\right) \cap \left(D_\varphi \le \frac{1}{2}\right). \tag{1}$$

III. Modal Analysis and Power Calculation

A. Operation Modes

From Fig. 3, there are five operation modes in a switching cycle which can be described as follows.

1) Mode 1 (t_0-t_1): As shown in Fig. 4(a), on the primary side, S_2 and S_4 are conducting, the output voltage of primary H-bridge V_P is zero. So, the inductor voltage is opposite to the primary voltage of transformer. On the secondary side, Q_2 and Q_3 are conducting, V_S is opposite to output voltage V_2. Thus, the inductor current is negative at the beginning, and increases linearly according to the follows:

$$i_L(t) = i_L(t_0) + \frac{nV_2}{L}(t - t_0). \tag{2}$$

When $t = t_1$, the current is changed to positive, which can assure the implement of ZVS at this time.

2) Mode 2 (t_1-t_2): Fig. 4(b) shows the equivalent circuit for mode 2. The state of the primary side is the same as that of mode 1. On the secondary side, Q_2 and Q_3 are turned OFF at t_1. Meanwhile, Q_1 and Q_4 are turned ON with ZVS. Then, the inductor voltage is clamped at $-nV_2$, and the inductor current decrease linearly according to the follows:

$$i_L(t) = i_L(t_1) - \frac{nV_2}{L}(t - t_1). \tag{3}$$

When $t = t_2$, the current is changed to negative, which can assure the implement of ZVS at this time.

3) Mode 3 (t_2-t_3): As shown in Fig. 4(c), on the primary side, S_2 is turned OFF at t_2, and S_1 is turned ON with ZVS. The state of the secondary side is the same as that of mode 2. So, the inductor voltage is clamped at V_1–nV_2, the inductor increases linearly according to the follows:

$$i_L(t) = i_L(t_2) + \frac{V_1 - nV_2}{L}(t - t_2). \tag{4}$$

At $t = t_3$, the current is positive to implement ZVS.

4) Mode 4 (t_3-t_4): As shown in Fig. 4(d), on the primary side, S_1 and S_4 are turned OFF at t_3, and S_2 and S_3 is turned ON with ZVS. The state of the secondary side is the same as that of modes 2 and 3. So, the inductor voltage is clamped at -V_1–nV_2, the inductor decreases linearly according to the follows:

$$i_L(t) = i_L(t_3) + \frac{-V_1 - nV_2}{L}(t - t_3). \tag{5}$$

At $t = t_4$, the current is negative to implement ZVS.

5) Mode 5 (t_4-t_5): Fig. 4(e) shows the equivalent circuit for mode 5. The state of the primary side is the same as that of mode 4. On the secondary side, Q_1 and Q_4 are turned OFF at t_4. Meanwhile, Q_2 and Q_3 are turned ON with ZVS. Then, the inductor voltage is clamped at $-V_1+nV_2$, and the inductor current decrease linearly according to the follows:

$$i_L(t) = i_L(t_4) + \frac{-V_1 + nV_2}{L}(t - t_4). \tag{6}$$

At $t = t_5$, the current is negative to implement ZVS.

According to the above analysis, this scheme can realize ZVS at every switching moment. However, it is worth noting that this cannot be achieved in all cases, and the specific conditions for implementation will be analyzed in detail in the following text.

B. Power Transfer

According to the above analysis, the current expressions at each turning point can be listed. It is worth noting that since the proposed strategy no longer has a semi-periodic symmetry, it is necessary to calculate all the points within a period. To simplify the process of the analysis, we assume $n = 1$ and all devices are ideal

$$i_L(t_1) = i_L(t_0) + \frac{V_2}{L} D_\varphi T_S \tag{7}$$

$$i_L(t_2) = i_L(t_1) - \frac{V_2}{L}(1 - 2D - D_\varphi) T_S \tag{8}$$

$$i_L(t_3) = i_L(t_2) + \frac{V_1 - V_2}{L} D T_S \tag{9}$$

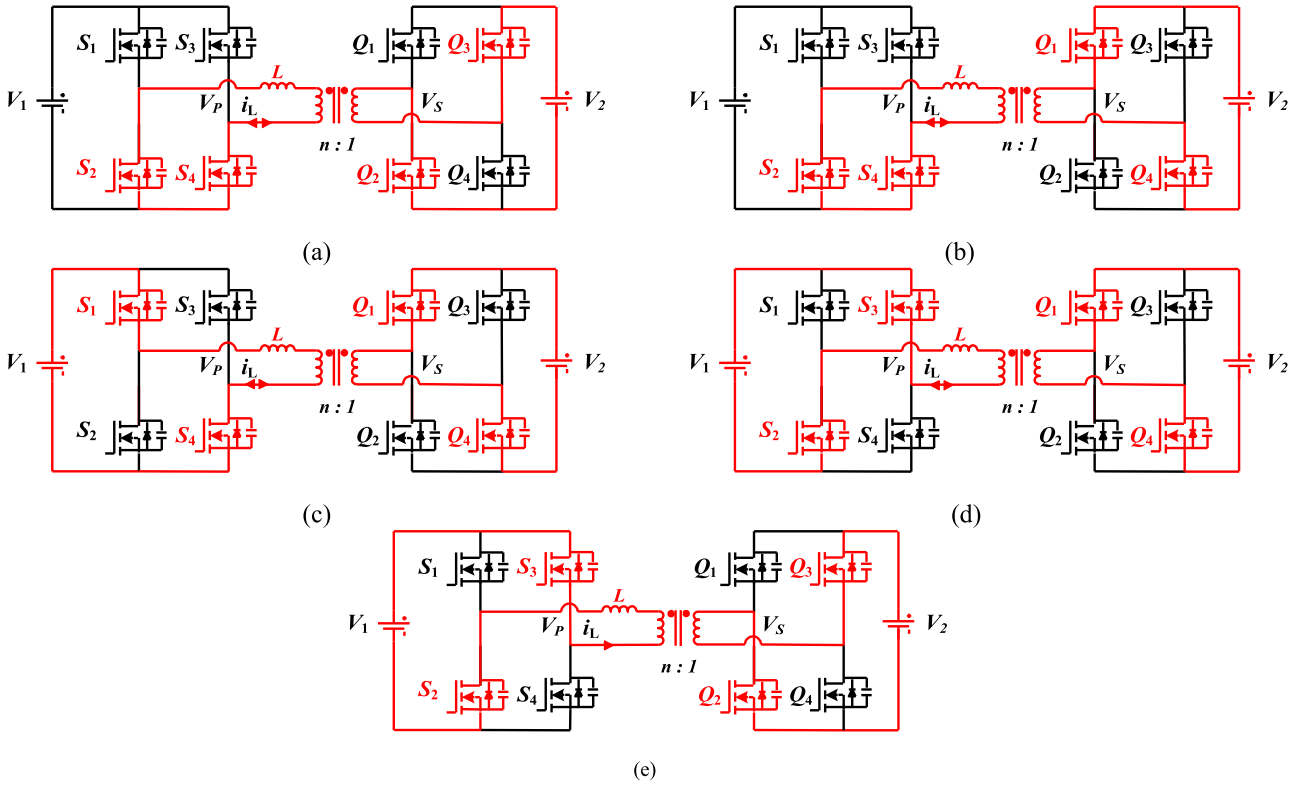

Fig. 4. Operation modes of the proposed strategy. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5.

$$i_L(t_4) = i_L(t_3) + \frac{-V_1 - V_2}{L}\left(D_\varphi + D - \frac{1}{2}\right)T_S \tag{10}$$

$$i_L(t_5) = i_L(t_0). \tag{11}$$

In addition, there is always a certain resistance *R* in the circuit, and forms an *RL* loop with the inductor *L*, which makes the bias of the inductor current always decaying exponentially under the action of periodic signals. In the final steady state of the circuit, if the inductor current is continuous, the average value of the inductor current within a period always tends to 0. Then, there is the following formula:

$$\int_0^{T_S} i_L(t)dt = 0. \tag{12}$$

By substituting the above formulas (7)–(11) and combining with Fig. 3, it is easy to get

$$i_L(t_0) = \frac{V_2}{4Lf_S}\left(-4D^2K - 4D_\varphi + 1\right) \tag{13}$$

where $K = \frac{V_1}{nV_2} = \frac{V_1}{V_2}$.

Then, $i_L(t_0)$ is substituted into formula (7)–(10) to obtain the current expression of other turning points

$$i_{\mathrm{L}}(t_1) = \frac{V_2}{4Lf_S}\left(-4D^2K + 1\right) \tag{14}$$

$$i_{\mathrm{L}}(t_2) = \frac{V_2}{4Lf_S}\left(-4D^2K + 4D_\varphi + 8D - 3\right) \tag{15}$$

$$i_{\mathrm{L}}(t_3) = \frac{V_2}{4Lf_S}\left[\left(4D - 4D^2\right)K + 4D_\varphi + 4D - 3\right] \tag{16}$$

$$i_{\mathrm{L}}(t_4) = \frac{V_2}{4Lf_S}\left[\left(-4D_\varphi - 4D^2 + 2\right)K - 1\right]. \tag{17}$$

Average power is

$$P = \frac{1}{T_S}\int_0^{T_S} V_1 i_L(t)dt = \frac{V_1V_2}{4Lf_s}\left(4D_\varphi - 4{D_\varphi}^2 + 4D^2 - 1\right). \tag{18}$$

For the convenience of expression, we define the unified transmission power P' as follows:

$$P' = \frac{P}{P_{\text{base}}} = 8D_\varphi - 8{D_\varphi}^2 + 8D^2 - 2 \tag{19}$$

where $P_{\text{base}} = \frac{V_1V_2}{8Lf_s}$.

Similarly, the average power of the traditional single-phase-shift strategy is

$$P'_{\text{SPS}} = 8D_\varphi\left(1 - 2D_\varphi\right). \tag{20}$$

Fig. 5 shows the power curve between the traditional scheme and the proposed scheme. The maximum power of this scheme can only reach 2/3 of that of the traditional scheme, but the light-load adjustment range is expanded, so this article focuses on the light-load performance.

IV. Analysis of the Effect of Duty Ratio Compression on Light-Load

The proposed strategy compresses the duty ratio of the primary side and makes the primary voltage presents three states of "0," "+," and "-," in sequence within a cycle. While the duty ratio of the secondary side stays constant at 50%, and the voltage only alternates between two states of "+" and "-." This strategy

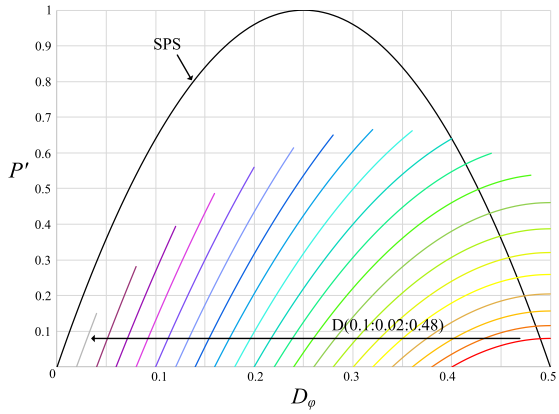

Fig. 5. 2-D curves of unified power P' with D_φ.

makes the voltage and current of the inductor no longer have the property of semiperiodic symmetry. The power variation is more concentrated, and the forward power and backflow power required for light-loads are reduced, as are the RMS current and current stress. These features will be analyzed in detail in this section.

A. *Effect of Duty Ratio Compression on Backflow Power*

Backflow power refers to the reverse power flow when the polarity of voltage and current on one side of the transformer is opposite. As shown in Fig. 2(a), for the interval of t_0-t_0' and t_2-t_2', the power is negative and the energy is transmitted from the output side to the input side. Due to the existence of backflow power, in order to achieve the target power, a larger forward power is required to offset this backflow power, which results in great RMS current and loss and low efficiency. So, in fact, backflow power can represent the RMS current to some extent.

It is not difficult to find that there is a certain contradiction between backflow power and soft-switching. As shown in Fig. 3, at the time $t = t_2$, if the backflow power is required to be 0, the inductor current needs to be positive, but in order to achieve soft-switching, the inductor current needs to be negative. In addition, at $t = t_3$, since the voltage changes directly from positive to negative, the backflow power must exist, unless the current is zero at this time. These contradictions are unavoidable, but compared to Fig. 2, it is obvious that the backflow power is much reduced. Because the traditional phase-shift modulation method under light-load conditions: a large forward power minus a large backflow power, a small transmission power can be achieved. However, in this article, due to the duty ratio is compressed, the time of effective power transmission is also shortened and the forward power is reduced, so the backflow power only needs to be a smaller value to achieve the same transmission power.

According to the positive and negative conditions of the current at each turning point, the calculation of backflow power can be divided into four situations. The following is an example for calculation of one of them.

The condition 1 is $i'_{\mathrm{L}}(t_2) < 0, i'_{\mathrm{L}}(t_3) > 0, i'_{\mathrm{L}}(t_4) < 0$. As can be seen from Fig. 3, backflow power appears in t_2-t_2 and t_3-t_3. In this case, the expression of backflow power is given in (21) and (22). Although the switches also operate at $t = t_0$ and $t = t_5$, the current does not affect the power because the primary voltage is 0 at this time

$$P_{\mathrm{BF1}} = \frac{1}{T}\int_{t_2}^{t_2'} V_1 \left|i_L(t)\right| dt + \frac{1}{T}\int_{t_3}^{t_3'} V_1 \left|i_L(t)\right| dt = \frac{L f_s V_1 i_L(t_2)^2}{2(V_1 - V_2)} + \frac{L f_s V_1 i_L(t_3)^2}{2(V_1 + V_2)}. \tag{21}$$

The unified backflow power is defined as

$$P'_{\mathrm{BF1}} = \frac{P_{\mathrm{BF1}}}{P_{\mathrm{base}}}. \tag{22}$$

In addition, the other three situations are as follows.
Condition 2: $i'_{\mathrm{L}}(t_2) > 0, i'_{\mathrm{L}}(t_3) > 0, i'_{\mathrm{L}}(t_4) < 0$

$$P'_{\mathrm{BF2}} = \frac{i_L(t_3)^2}{4(K+1)}. \tag{23}$$

Condition 3: $i'_{\mathrm{L}}(t_2) < 0, i'_{\mathrm{L}}(t_3) < 0, i'_{\mathrm{L}}(t_4) < 0$

$$P'_{\mathrm{BF3}} = -\left[i_L(t_2) + i_L(t_3)\right] D. \tag{24}$$

Condition 4: $i'_{\mathrm{L}}(t_2) < 0, i'_{\mathrm{L}}(t_3) > 0, i'_{\mathrm{L}}(t_4) > 0$

$$P'_{\mathrm{BF4}} = \frac{i_L(t_2)^2}{4(K-1)} + \frac{i_L(t_4)^2}{4(K-1)} + \left[i_L(t_3) + i_L(t_4)\right]\left(D + D_\varphi - \frac{1}{2}\right). \tag{25}$$

Then, by combining equations (15)–(17), (21)–(25), the expression of backflow power can be obtained as

$$P'_{\mathrm{BF}} = \begin{cases} P'_{\mathrm{BF2}} D_\varphi \geq D^2 K - 2D + \frac{3}{4} \\ P'_{\mathrm{BF3}} D_\varphi \leq D^2 K - DK - D + \frac{3}{4} \\ P'_{\mathrm{BF4}} D_\varphi \leq -D^2 - \frac{1}{4K} + \frac{1}{2} \\ P'_{\mathrm{BF1}} \mathrm{other}. \end{cases} \tag{26}$$

According to Fig. 2, the backflow power of the traditional single-phase-shift strategy is also divided into two cases

$$P'_{\mathrm{BF}} = \begin{cases} \frac{i_L(t_0)^2}{2(K+1)} i_L(t_1) > 0 \\ \left[i_L(t_0) + i_L(t_1)\right] D_\varphi + \frac{i_L(t_1)^2}{2(K-1)} i_L(t_1) \leq 0. \end{cases} \tag{27}$$

It is worth noting that in (27), the current values are not (13) and (14) but match those in Fig. 2.

Fig. 6 shows the curves of backflow power with the variation unified power. It can be seen that the backflow power of the

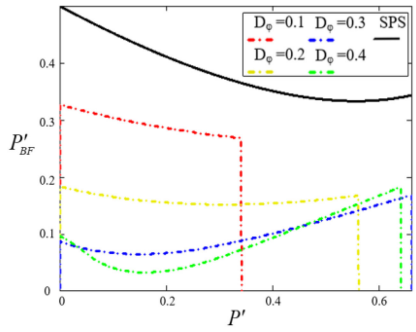

Fig. 6. Curves of the backflow power with the variation unified power ($K = 2$).

proposed strategy is smaller than that of the traditional strategy under light-load.

B. Effect of Duty Ratio Compression on Current Stress and RMS Current

Current stress is one of the important reasons affecting the light-load efficiency. The larger it is, the greater the ON and OFF losses of the switching tubes will increase, and the greater the power consumed by parameters, such as the parasitic resistance of the circuit, which cannot be ignored in light-load situations. It is easy to know that the current stress must be the current value at some turning point, and it can be seen from (13)–(17) that the current value at the turning point is related to D_φ, D, and K.

When $K \geq 1$, according to the analysis in Section IV-A, the inductance current will rise in mode 1 (t_0-t_1)and fall in Mode 2(t_1-t_2), and the slope of rise and fall is the same. And because the time of mode 2 is shorter than that of mode 1, the following relationship must exist:

$$i_L(t_0) < i_L(t_2) < i_L(t_1). \tag{28}$$

In both modes 4 and 5, the inductance current decreases continuously, so there is clearly a relationship

$$i_L(t_0) < i_L(t_4) < i_L(t_3). \tag{29}$$

So, $t = t_2$ and $t = t_4$ must not be the time when the maximum current value occurs. The maximum current can only occur at $t = t_0$, $t = t_1$, and $t = t_3$.

From (28) and (29), it is clearly that $i_L(t_0)$ is the smallest value in the three points so that it must satisfied equation (30), if $|i_L(t_0)|$ is the maximum current value

$$\begin{cases} |i_L(t_0)| > |i_L(t_1)| \\ |i_L(t_0)| > |i_L(t_3)| \end{cases} \Rightarrow \begin{cases} i_L(t_0) < -i_L(t_1) \\ i_L(t_0) < -i_L(t_3). \end{cases} \tag{30}$$

Substitute (13), (14) and (16) into (30), the relationship between the current stress I_{MAX} and φ, D, and K can be obtained. The other cases which $|i_L(t_1)|$ or $|i_L(t_3)|$is the maximum current value can be calculate as the same way.

Finally, the maximum current value I_{MAX} can be expressed as

$$I_{\mathrm{MAX}} = \begin{cases} i_L(t_1), 1 \leq K < \frac{1-2D_\varphi}{4D^2} \\ |i_L(t_0)|, \frac{1-2D_\varphi}{4D^2} \leq K < \frac{1}{2D} \\ i_L(t_3), K \geq \frac{1}{2D}. \end{cases} \tag{31}$$

For traditional single-phase-shift modulation, due to its symmetric nature, the maximum current can only be in one situation. As shown in Fig. 2, the maximum current $\mathrm{I_{MAX}}$ appears at both $t = t_0$ and $t = t_2$, and can be expressed as

$$I_{\mathrm{MAX}} = \frac{V_2}{4Lf_S}(4D_\varphi + K - 1). \tag{32}$$

Fig. 7(a) shows the variation curves of the maximum current with the unified power. The black curve represents the traditional single-phase-shift strategy, and the colored curve represents the situation of different D_φ values, respectively. The vertical axis I'_{MAX} in Fig. 7(a) has been normalized, and $I_{\mathrm{MAX}} = \frac{V_2}{4Lf_S} I'_{\mathrm{MAX}}$. In addition, it is worth noting that the strategy in this article only focuses on light-load where the normalized power is less than

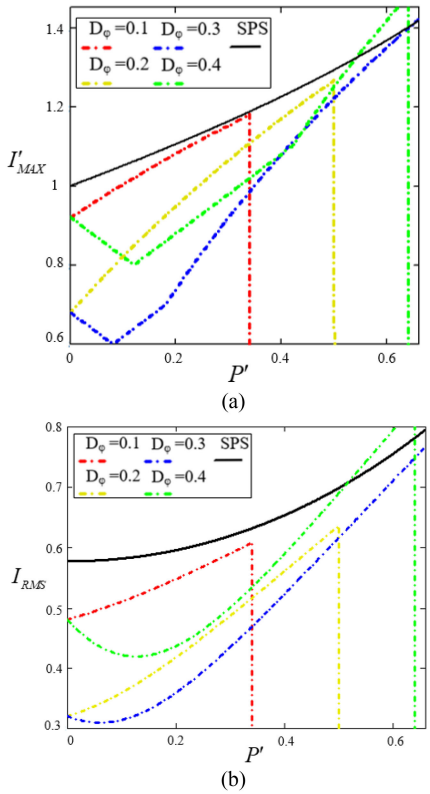

Fig. 7. Curves of the current with the variation unified power ($K = 2$) (a) Maximum currents. (b) RMS currents.

50%. It can be clearly seen from the figure that, in the condition of same power, the scheme in this article can reduce the current peak value at various D_φ values.

Considering that RMS current is also an important index, RMS current is also calculated in this article

$$I_{\mathrm{RMS}} = \sqrt{\frac{1}{T}\int_0^T i(t)^2 dt}. \tag{33}$$

Fig. 7(b) shows the RMS current curve, which is very similar to the stress trend.

The above analysis is only for the case of $K \geq 1$, and the case of K less than 1 can be analyzed in the same way but not considered in this article.

C. Soft Switching Conditions and Loss Analysis

As mentioned earlier, ZVS can not be implemented in all situations. Since the auxiliary inductance is large and the parasitic capacitance of the switching tube is small, the direction of the current can be approximated as the basis for judgment when calculating the soft switching condition. According to this condition, and then simply organized, the boundary equation when all switching tubes can achieve soft switching can be listed as follows:

$$D_\varphi > -D^2 - \frac{1}{4K} + \frac{1}{2} \tag{34}$$

$$D < \frac{1}{\sqrt{4K}} \tag{35}$$

$$D_\varphi < D^2K - 2D + \frac{3}{4} \tag{36}$$

$$D_\varphi > D^2K - D - DK + \frac{3}{4}. \tag{37}$$

This is only an approximate condition and more precise conditions can be calculated with energy. But, what is certain is that this condition is all close to 0 and we can achieve a more stable ZVS effect by fine-tuning the parameters.

Under the condition of ZVS, the heavy load losses are mainly conduction losses, while the light-load losses are mainly turn-OFF losses and conduction losses [25].

Turn-OFF loss is

$$p_{\text{off}} = U_{\text{DS}} \cdot I_{\text{off}} \cdot \frac{t_r + t_f}{2} \cdot f_S \tag{38}$$

where U_{DS} is the turn-OFF voltage, I_{off} is the turn-OFF current, t_r is the rise time, and t_f is the fall time[26].

Conduction losses include losses of magnetic elements and switching devices. The conduction loss of the magnetic element is

$$p_{\text{cond1}} = \left(\frac{R_L + R_{Tp}}{n^2} + R_{Ts}\right) \cdot I_{\text{rms}}^2 \tag{39}$$

where *RL* is the resistance of the auxiliary inductor, RTP is the resistance of the primary winding of the transformer, and RTS is the resistance of the secondary winding of the transformer.

The conduction loss of the switching device is

$$p_{\text{cond2}} = \sum_{i=1}^{8} R_{\text{DSon}} \cdot I_{i,\text{rms}}^2 \tag{40}$$

where R_{DSon} is the equivalent ON-resistance, Ii, RMS is the RMS current of the switching tube.

In addition to these, there are some minor losses and unknown losses that cannot be calculated. Among them, the minor losses include capacitance losses and core losses. Capacitance losses can be calculated using equivalent series resistance. The calculation of core loss is more complicated and is generally approximated as a fundamental wave and then calculated using the Steinmetz equation

$$p_{\text{core}} = k \cdot f_s^\alpha \cdot B^\beta \cdot V \tag{41}$$

where k,α, and β are constants and V is volume. However, for EPS, DPS, and the proposed strategy, etc., the harmonic content is high and such a method is not accurate. A more accurate method of calculating core losses can be found in [27] but is more complex and requires extremely detailed device data and some statistical methods. Here, only the formula of eddy current loss is given, A is the area of the cross-section of the core, α is a numerical constant, and n0 characterizes the statistical distribution of the local coercive fields. The hysteresis loss can be equivalent to sine wave. A more detailed description can be found in the original text

$$p_{\text{CE}} = \frac{A}{8\pi\rho}\frac{1}{T}\sum_{i=1}^{n}\left[\int_{t_{i-1}}^{t_i}\left(\frac{dB_i(t)}{dt}\right)^2 dt\right] \tag{42}$$

$$p_{\text{EE}} = \sqrt{\frac{A\alpha n_0}{\rho}}\frac{1}{T}\sum_{i=1}^{n}\int_{t_{i-1}}^{t_i} dt\left(\left|\frac{dB_i(t)}{dt}\right|\right)^{\frac{3}{2}}. \tag{43}$$

The results of the two methods are different, but they both account for a very small percentage of the total losses. In addition to the methods mentioned above, improved Steinmetz methods are provided in the literature [28] and [29], which can also be used to estimate core losses.

Unknown losses include losses in the absorption circuit and losses due to temperature-induced parameter changes, as well as other losses that cannot be estimated. These losses often cannot be calculated. The loss distribution is shown at the end of Section V.

Moreover, from [25], the losses in DAB come from two main components: switching losses and conduction losses. When the ZVS condition is satisfied, the losses mainly come from turn-OFF losses and conduction losses. Turn-OFF loss is related to current stress, and conduction loss is related to RMS current. Therefore, in the experiment of this article, the selection of parameters follows three principles.

1) The soft switching condition is satisfied.
2) Keep current stress and RMS current as small as possible.
3) Variation of parameters is continuous.

Taking the case of $K = 2$ in this article as an example, it can be seen from Fig. 7 that the strategy proposed in this article has less current stress and RMS current when D_φ is between (0.2, 0.4), so the selected parameters should be in this range as much as possible. In addition, considering that the conduction loss accounts for the largest proportion, discrete fitting is made for the value of the minimum RMS. The result is very close to two segments of the boundary condition of ZVS, namely equations (34) and (35). Substituting $K = 2$, (44) and (45) can be obtained. This result satisfies the above three conditions. So, in the final experiment, (44) and (45) are used as the basis of selection

$$D_\varphi = -D^2 + \frac{3}{8}, P' \in \left[0, \frac{1}{2}\right] \tag{44}$$

$$D = \frac{1}{\sqrt{8}}, P' \in \left(\frac{1}{2}, \frac{2}{3}\right]. \tag{45}$$

It is worth noting that these two formulas are only used to provide a selection basis for the experimental parameters and are not unique or optimal. In addition, since boundary conditions are used for calculation, parameter values should be fine-tuned according to (34) and (35) in actual experiments. For different values of *K*, the results can be recalculated using the above method.

D. Performance Advantages of the Proposed Method

The advantages of the proposed method in terms of current stress and back-flow power have been analyzed in detail in the previous two sections. It can be seen that the proposed method has obvious advantages under light-load conditions. Furthermore, in this section, the working conditions of the two methods under 20% load are selected. It is worth noting that, for the traditional method, each power condition corresponds to two D_φ values actually. Only the smaller D_φ value is used in the preceding and subsequent analyses, because the larger D_φ value corresponds to several times the current stress and backflow power of the smaller one. For the proposed method, each power

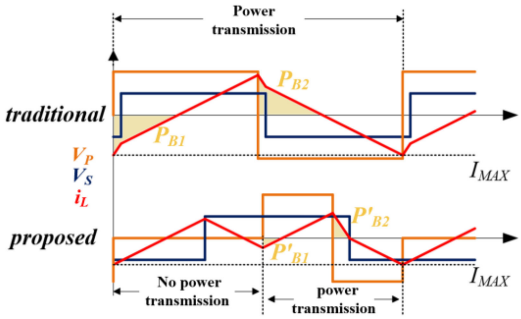

Fig. 8. Waveforms of the two schemes at 20% load ($K = 2$).

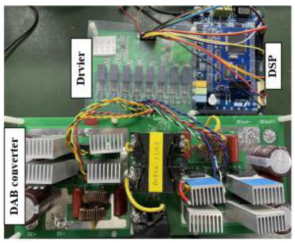

Fig. 9. Schematic diagram of the experimental prototype.

condition corresponds to an infinite number of choices due to the addition of one degree of freedom.

Fig. 8 shows the waveforms of the two schemes under 20% load, where $K = 2$. In the proposed scheme, the duty cycle of the primary voltage is compressed, so a complete cycle is divided into power transmission phase and no power transmission phase. During the power transmission, the waveforms of the two schemes are similar, but the traditional scheme transmits power throughout the whole cycle, with large values of forward and backflow power. However, the power transmission time of the proposed scheme is compressed to less than half cycle, and both the forward power and the backflow power are greatly reduced. The value of power becomes smaller, while the value of voltage does not change, so the value of current also becomes smaller. On the other hand, the trend of current changes from a large triangle like "up, up, down, down" to a saw-tooth shape with alternating up and down, which decreases the maximum value of current. As shown in the graph, the I_{MAX} is reduced by nearly half.

V. Experimental Results

To verify the above analysis, a prototype with a maximum power of 300 W was built and shown in Fig. 9. The specific parameters are given in Table I. The switches is selected as mosfet (INFINEON:6R099C6). In this article, experiments were carried out for all cases under 60% load, and the corresponding experimental results are shown in Fig. 10. The cases of $K = 3$ (150–50 V) and $K = 4$ (200–50 V) are given in Figs. 11 and 12. The parameter selection method is the same as that when $K = 2$. It can be seen that in all these cases, the proposed scheme implements soft switching and maintains both backflow power and current stress at small values. Regarding the selection of control variables during the experiments, the combinations with better performance are roughly selected based on the previous analysis, which are not optimal solutions.

TABLE I
Parameters of Prototype

Auxiliary inductor	L	39.5μH
Leakage inductance	L_m	1.7μH
Input capacitor	C_{in}	540μF
Output capacitor	C_{out}	540μF
Transformer turns ratio	n	1
Switching frequency	f	50kHz
Dead time	t_d	0.1μs
Input voltage	V_1	100V-200V
Output voltage	V_2	50V
Power	P	0~600W

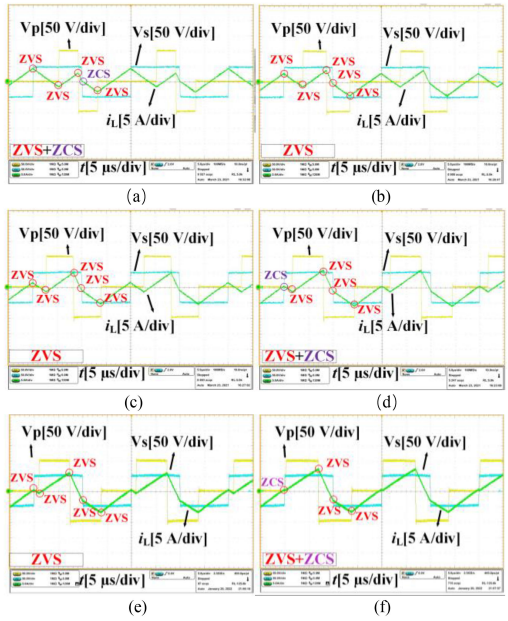

Fig. 10. Experimental waveform of the proposed scheme ($K = 2$). (a) $P' = 0.1$. (b) $P' = 0.2$. (c) $P' = 0.3$. (d) $P' = 0.4$. (e) $P' = 0.5$. (f) $P' = 0.6$.

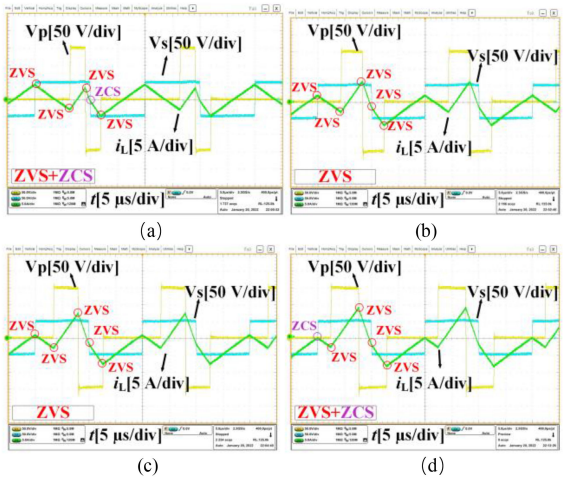

Fig. 11. Experimental waveform of the proposed scheme ($K = 3$). (a) $P' = 0.1$. (b) $P' = 0.2$. (c) $P' = 0.3$. (d) $P' = 0.4$.

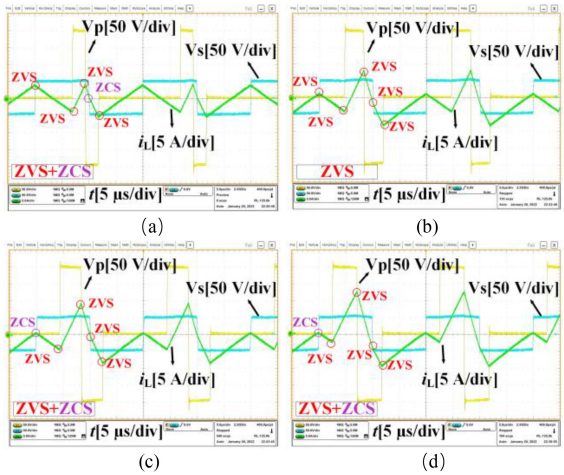

Fig. 12. Experimental waveform of the proposed scheme ($K = 4$). (a) $P' = 0.1$. (b) $P' = 0.2$. (c) $P' = 0.3$. (d) $P' = 0.4$.

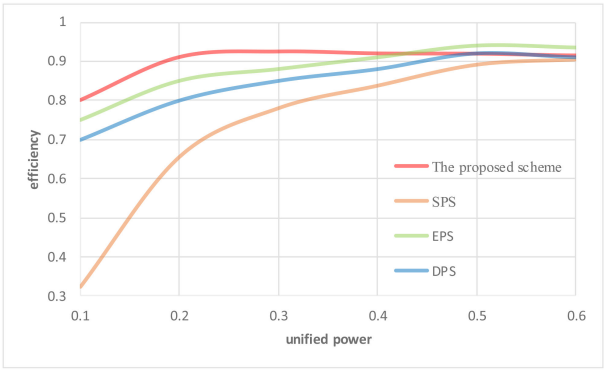

Fig. 13. Curves of the efficiency varied with unified power.

Fig. 13 shows the efficiency curve of the proposed strategy, traditional SPS, EPS, and DPS. It is obvious that the efficiency of the proposed strategy is greatly improved compared with the traditional strategy. For example, at 10% load, the efficiency of SPS is only about 30%, while the efficiency of the proposed strategy is 80%, which is 2.6 times that of the former. DPS can achieve very small current stress and almost zero backflow power under light-load, but it cannot guarantee all switches to achieve soft switching, which brings additional loss. The efficiency of other strategies is below 80% at 20% load, while the efficiency of this article strategy has exceeded 90%, and the efficiency of the subsequent load cases has been maintained at a high level of around 90%.

In Section IV-C, the losses have been calculated. Fig. 14 shows the distribution of losses combined with experimental loss ($V_1 = 100$ V, $V_2 = 50$ V, $P = 60$ W, and $P' = 0.2$). P_{SW} refers to the on and off losses of the switch, or only to the off losses when soft switching is implemented. P_{cond1} refers to the copper losses of inductors and transformers, and P_{cond2} refers to the copper losses of switching devices. P_{minor} includes core losses and capacitor losses. P_U is unknown losses.

VI. Conclusion

A modulation strategy with asymmetric duty cycle compression for DAB converters is proposed in this article. This strategy is considered from the perspective of the implementation logic

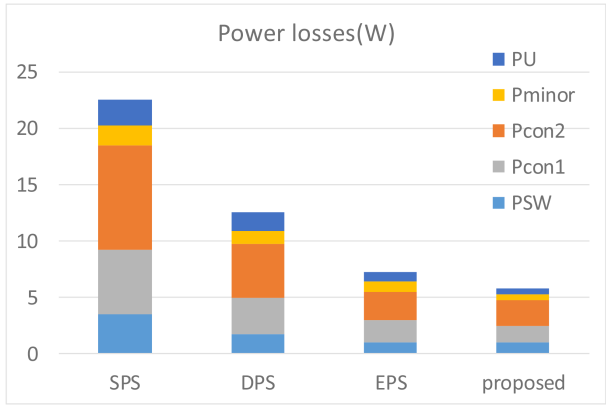

Fig. 14. Total experimental losses and the distribution of each losses ($V_1 = 100$ V, $V_2 = 50$ V, $P = 60$ W, and $P' = 0.2$).

of light-load. By compressing the duty ratio of the primary side voltage of the DAB converter, the power transmission time is shortened, the forward power and backflow power are reduced and changing the original logic of large forward power minus large backflow power to small forward power minus small backflow power. A prototype with an input voltage of 100–200 V, an output voltage of 50 V and a full load power of 300–600 W is built and tested. Experimental results show that the advantages of the proposed strategy are obvious under light-load, which implements soft switching and maintains both return power and current stress at low levels, with a huge improvement in efficiency compared to the conventional strategy.

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Gen Chen was born in Sichuan, China, in 1998. He received the B.S. degree in automation, and the M.S. degree in control engineering from the School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu, China, in 2019 and 2022, respectively.

His current research interests include bidirectional converters, soft switching techniques, power factor correction converters, and resonant converters.

Zhangyong Chen was born in Sichuan, China, in 1988. He received the B.S. degree in electrical engineering and its automation and the Ph.D. degree in electrical engineering from Southwest Jiaotong University, Chengdu, China, in 2010 and 2015, respectively.

From September 2014 to September 2015, he was a Visiting Student with Future Energy Electronics Center, Virginia Tech, Blacksburg, VA, USA. Since January 2016, he was been a Lecturer with the School of Energy Science and Engineering. Since July 2018, he has been an Associate Professor with the School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu, China. His current research interests include switching-mode power supplies, soft switching techniques, power factor correction converters, and renewable energy sources.

Yong Chen (Senior Member, IEEE) was born in Sichuan, China, in 1977. He received the B.S. degree in industrial automation from Taiyuan University of Science and Technology, Taiyuan, China, in 2001, the M.S. degree in control theory and control engineering from Guangxi University, Nanning, China, in 2004, and the Ph.D degree in control theory and control engineering from Chongqing University, Chongqing, China, in 2007.

He was a Visiting Scholar with School of Mechanical Engineering, The University of Adelaide, Adelaide, SA, Australia. He was a Professor with the School of Automation Engineering, UESTC, where he has been a Professor and a Ph.D. Supervisor with the School of Automation Engineering. His current research interests include power electronics, motor control, energy control, and network control.

Chenchen Feng was born in Sichuan, China, in 1997. He received the B.S. degree in automation and the M.S. degree in control engineering from the School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu, China, in 2019 and 2022, respectively.

His current research interests include soft switching techniques, switching-mode power supplies, and resonant converters.

Xintong Zhu was born in Shanxi, China, in 1997. He received the B.S. degree in electrical engineering and its automation and the M.S. degree in control engineering from the University of Electronic Science and Technology of China, Chengdu, China, in 2019 and 2022, respectively.

His current research interests include resonant converters and soft switching techniques.