Analysis and Design of a Two-Phase Series Capacitor Dual-Path Hybrid DC-DC Converter

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***Abstract*—In this article, a two-phase series capacitor dual-path hybrid dc–dc converter with the step-down ratio of less than 1/6 is proposed for the first time. In this converter, the output current is divided into capacitance- and inductance-path, so the average value and ripple of inductance current are reduced. On the same time, the conduction loss caused by inductance equivalent series resistance (ESR) is also reduced. The addition of series capacitor leads to desirable characteristics, including lower switching stress, switching loss, parasitic output capacitance loss on MOSFET, automatic phase current balancing, duty ratio extension, etc. A 120 W prototype has been designed to demonstrate theoretical analysis. Obtained efficiency was up to 93.18% at full load. Experimental results show good agreement with theoretical analysis and high feasibility of proposed converters.**

***Index Terms*—Dual-path, hybrid converter, series capacitor converter, step-down converter.**

I. Introduction

With the rapid development of data center and telecommunications applications, dc–dc converters with large step-down ratio are needed in more and more occasions. Google proposed a 48V bus architecture, which usually requires one or two-stage conversion, and the voltage drops to about 1 V. Among them, many scholars have done relevant work. Lee proposed sigma converter, which is a hybrid topology composed of *LLC* converter and buck converter. Minjie proposed linear extendable group operated (LEGO) switched capacitor combined with buck converter.

The above hybrid topology has the advantages of two topologies and significantly improves the performance of the converter. Hybrid step-down dc–dc combines buck converter and switched capacitor dc–dc converter, which can have the advantages of switched capacitor topology and buck topology at the same time. Compared with the traditional buck converter, the hybrid topology proposed by [1] reduces the voltage of the inductor, and the capacitor bears part of the output current, which reduces the loss of the inductor, which is very favorable for the application when the inductor loss is dominant. Considering the size of the converter, when the output *LC* parameters and switching frequency are the same, the peak current ripple is only 1/4 of that of the three-level buck converter, which can significantly reduce the inductance value, which means smaller converter size and higher power density. At the same time, it has the characteristics of large step-down ratio compared with traditional buck converter.

Interleaved multiphase buck converters [5] have been mostly adopted for point-of-load regulation below 3.3 V and above 10 A from input voltage exceeding 12 V. The voltage stress and switching loss of the switch can be reduced by connecting the capacitor in series in the two-phase buck converter. At the same time, it has the functions of automatic phase-to-phase current balance and duty cycle expansion.

Texas Instruments proposed a monolithic integrated series capacitor buck (SC-buck) converter in [3], with a switching frequency of 5 MHz and high power density. However, capacitors and inductors are not integrated inside the chip and its switching loss and inductance loss are large.

SC converters with soft switching function are proposed in [4-13], but the voltage and current peak generated during resonance is large, which requires a high stress MOSFET. To solve above problem, many advanced hybrid topologies are proposed [14-27]. Such as in [14], a virtual intermediate bus structure is proposed which greatly improves the converter performance.

In [2], the SC-buck converter is quantitatively compared with the traditional buck converter, the detailed loss analysis of SC-buck under high frequency is given, and the advantages of SC-buck under high frequency are proved.

In order to have the advantages of hybrid buck topology and SC-buck topology at the same time, a two-phase series capacitor dual-path hybrid dc–dc converter with at least 1/6 step-down ratio is proposed. Whether compared with hybrid buck topology or SC-buck topology, the new topology has some kind of superiority.

The characteristics of this topology are as follows.

1) *Large Step-Down Ratio, Equivalent Duty Cycle Expansion:* Under the same step-down ratio, the duty cycle of hybrid dc–dc buck converter is larger than that of traditional buck converter, and the new topology also has the double step-down ratio characteristics of SC-buck converter, which further expands the duty cycle.

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2) *Smaller Inductance Current Ripple and Current* RMS: Due to the dual-path hybrid structure and the addition of series capacitor of the new topology, part of the output current is provided by the fly-capacitor, which reduces the voltage and current of the inductor, reduces the size of the inductor and improves the power density.
3) *Reduced Voltage Rating for Switches:* The series capacitor bears half of the input voltage, which reduces the voltage stress of most switches, and the ON resistance of MOSFET increases with the withstand voltage, which means that the on loss of the new topology can be significantly reduced, because MOSFET with low withstand voltage and low on resistance can be used. At the same time, due to the reduced voltage before the MOSFET is turned ON, the switching loss is also reduced, so the new topology can achieve relatively higher efficiency at high frequencies.
4) *Automatic Phase Current Balancing:* In the steady state, the voltage on the series capacitor satisfies the ampere-second balance, which provides a balanced loop between the two phases. This current sharing mechanism is inherent to the topology and acts like a damped harmonic oscillator. Especially in the case of high frequency, the additional high frequency current sampling circuit and control circuit are eliminated, making the control simpler.

In this article, a two-phase series capacitor dual-path hybrid converter is proposed and analyzed. Section II introduced the principle of operation, including control methods and modal analysis. Section III analyzed the performance of the converter, compared with other converters, and clarified the superiority of its performance. Section IV and Section V are the experimental results and the conclusion.

II. Principle of Operation

A single dual-path hybrid converter is used as the basic unit, two basic units are interleaved in parallel, and a series capacitor and two switches are added to form a two-phase series capacitor dual-path hybrid converter.

In this topology, the voltage of C_t remains unchanged at steady state and can be regarded as a constant voltage source. Switches S_{a2} and S_{c2} are connected to C_t, respectively. The direction of S_{a2} cannot be changed, otherwise when S_{c1} is turned ON, the output voltage will be clamped to ground, causing the converter to produce an abnormal working mode.

The capacitance value of the capacitor C_t is much larger than the capacitance value of the capacitor C_{fly1}, which can ensure that in the series mode, the capacitor C_t is equivalent to a voltage source, and its voltage fluctuation is small and approximately unchanged.

The control method adopted by the proposed topology is duty cycle control, and its duty cycle cannot exceed 50%, otherwise the working mode of the converter will change, which makes the step-down ratio of the topology at least 1/6.

In order to simplify the analysis and derivation of the theory, the following assumptions can be made:

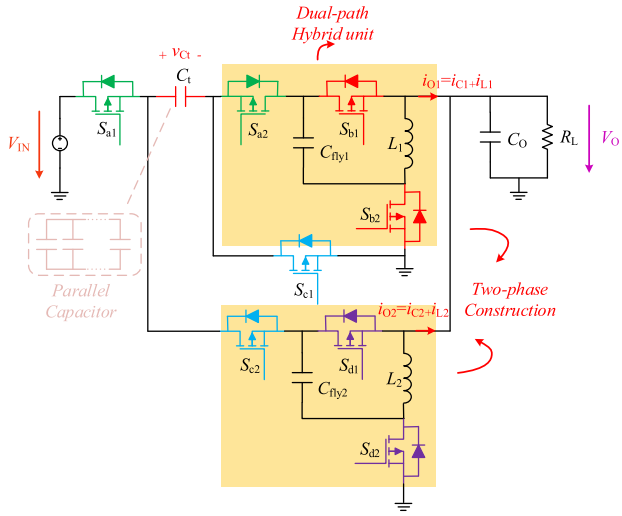


Fig. 1. Proposed two-phase SC dual-path hybrid converter.

1) The power switches S_{a1}-S_{d2} are ideal with no voltage drop. When the driving signal is not applied, the reverse conduction resistance is infinite.
2) The value of the capacitor C_t is very large, and its voltage is considered constant in the steady state.
3) The value of the C_{fly} capacitor is very small relative to C_t, so when the C_{fly} capacitor is charged in series with the C_t capacitor, it is assumed that the voltage of C_t will not drop.
4) The inductance is large enough to ensure that it works in the continuous conduction mode (CCM) mode.

There are four working modes of the proposed converter as shown in Fig. 2, and the main voltage and current waveforms are shown in Fig. 3.

1) Mode 1 (t_0-t_1)*:* S_a and S_d are turned on, and S_b and S_c are turned OFF, so phase A works in charging mode and phase B works in freewheeling mode. For the working mode of phase A at this time, the input voltage charges C_t, C_{fly1} and L_1, and the voltage of the inductor L_1 is:

$$V_{L1-\text{on}} = V_{\text{in}} - V_{C\text{fly1}} - V_{Ct} - V_O. \tag{1}$$

The voltage of the inductor L_2 is

$$V_{L2-\text{off}} = -V_O. \tag{2}$$

2) Mode 2 (t_1-t_2): Both S_a and S_c are turned OFF, and both S_b and S_d are turned ON. At this time, both phases A and B are working in the freewheeling state, and the voltages of the inductors L_1 and L_2 are both $-V_o$.
3) Mode 3 (t_2-t_3): S_a and S_d are turned OFF, and S_b and S_c are turned ON. At this time, phase A is in the freewheeling state, and the capacitor C_t charges C_{fly2} and L_2 of phase B. The voltage of L_2 in this mode is

$$V_{L2-\text{on}} = V_{Ct} - V_{C\text{fly2}} - V_O. \tag{3}$$

4) Mode 4 (t_3-t_4): The state of the switch of this mode is the same as that of mode 2, and the voltage of the inductor L_2

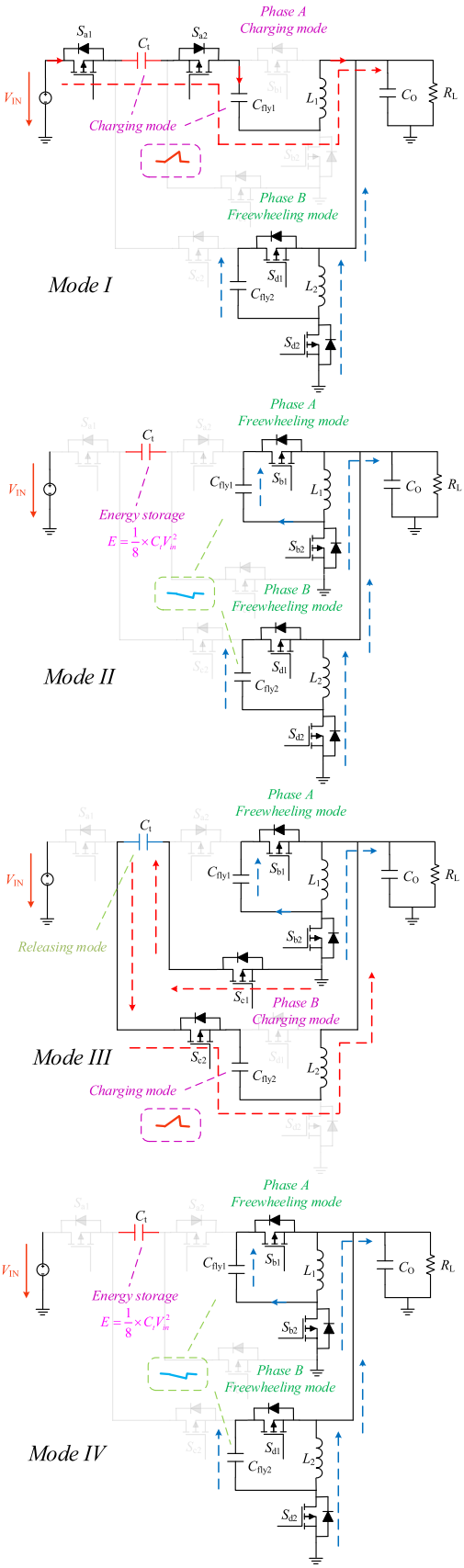


Fig. 2. Working modes of the proposed circuit.

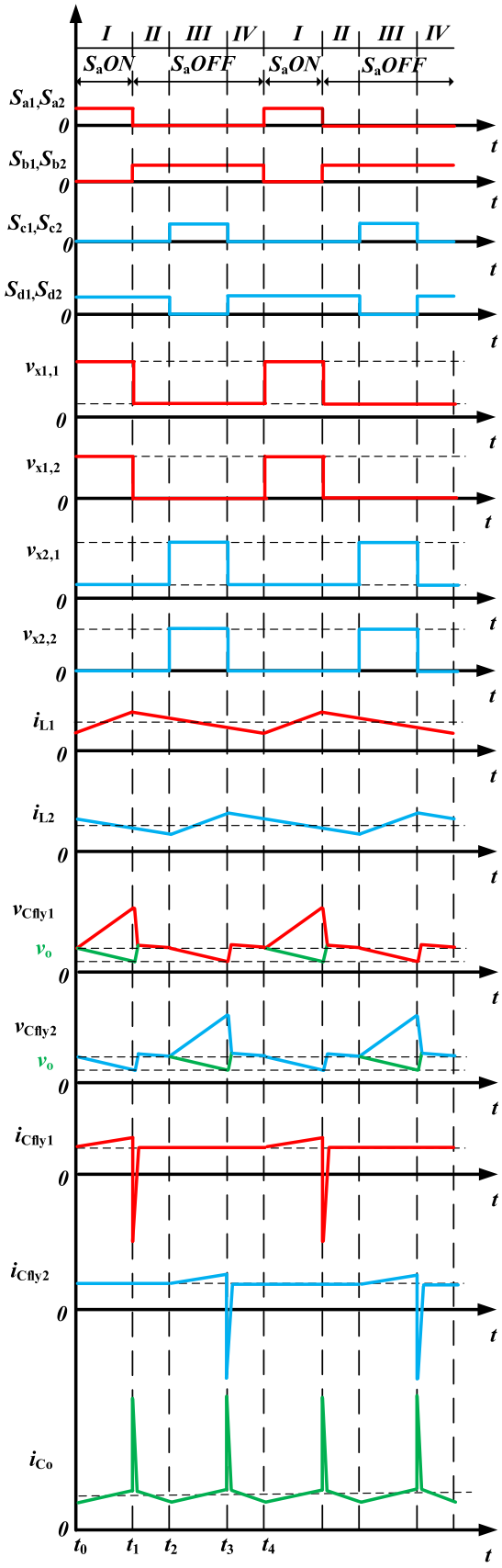


Fig. 3. Main voltage and current waveforms.

is -V_o. The voltage of the inductor L_1 is

$$V_{L1-\text{off}} = -V_O. \tag{4}$$

The voltage of the two fly-capacitors in this article is actually a spiked waveform, as shown in Fig. 3, but its peak value decreases with the increase of the capacitor value. At the same time, the voltage of this part is relatively small compared to the average voltage. The calculation is concise, thinking that the fly-capacitor voltage is equal to the output voltage V_o. In fact, the expression for delta $V_{C\text{fly}}$ can be derived

$$\Delta V_{C\text{fly}} = (I_L/C_{\text{fly}})\, DT_S. \tag{5}$$

III. Performance Analysis

A. Voltage Conversion Ratio

Inductor L_1 is charged in mode I and discharged in other modes. Using the volt-second balance, and then according to (1) and (4), we can get the following equation:

$$(V_{\text{in}} - V_{C\text{fly}1} - V_{Ct} - V_O)(t_1 - t_0) = V_O(t_4 - t_1). \tag{6}$$

Here, $V_{\text{fly}1}$ is the voltage of the capacitor $C_{\text{fly}1}$, V_{in} is the input voltage, and V_{Ct} is the voltage of the series capacitor.

In the same way, apply the volt-second balance to L_2, and then according to (2) and (3), the following equations are obtained

$$(V_{Ct} - V_{C\text{fly}2} - V_O)(t_3 - t_2) = V_O(t_2 - t_0 + t_4 - t_3). \tag{7}$$

The duty cycle control method is adopted, and the duty cycle D is defined as

$$D = \frac{t_1 - t_0}{t_4 - t_0} = \frac{t_3 - t_2}{t_4 - t_0} = \frac{t_d}{T_S} \tag{8}$$

where t_d is the ON-time and T_s is the switching period. Combining (6)–(8), and the relationship between the fly-capacitor voltage and the output voltage mentioned above, the series capacitor voltage can be obtained as

$$V_{Ct} = \frac{1}{2} V_{\text{in}}. \tag{9}$$

Then according to either of (6) and (7), the voltage conversion ratio M can be calculated

$$M = \frac{V_O}{V_{\text{in}}} = \frac{D}{2(1+D)}. \tag{10}$$

The comparison of the voltage conversion ratio of different topologies is shown in Fig. 4. Due to the limitation of the control method, D<0.5, according to Fig. 6 It can be seen that the conversion ratio M<1/6.

B. Inductor DC Current Analysis

According to the parameters defined in Fig. 3, the currents of inductor L_1 and inductor L_2 can be expressed as:

$$I_{L1} = I_{C,11} D + (I_{C,12} + I_{O1})(1 - D) \tag{11}$$

$$I_{L2} = I_{C,21} D + (I_{C,22} + I_{O2})(1 - D). \tag{12}$$

The definition of I_{O1} is shown in Fig. 1, it represents the output current of the A-phase converter, the definition of I_{O2} is similar, and it represents the output current of the B-phase converter. $I_{C,11}$ is the current when $C_{\text{fly}1}$ is charging, and $I_{C,12}$ is the current when $C_{\text{fly}1}$ is discharging. The same is true for $I_{C,21}$ and $I_{C,22}$, that is, the current when $C_{\text{fly}2}$ is charging and discharging, respectively.

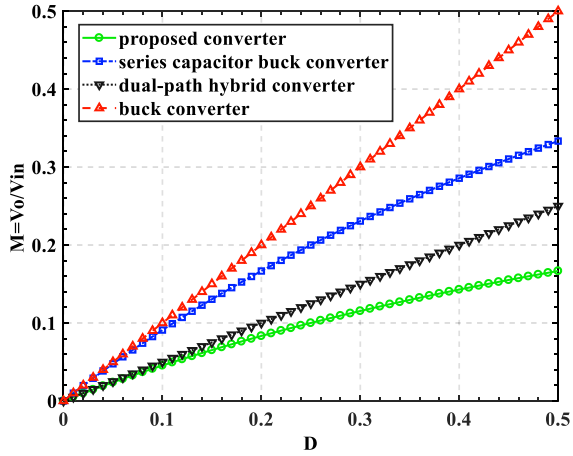


Fig. 4. Comparison of voltage conversion ratio of different topologies.

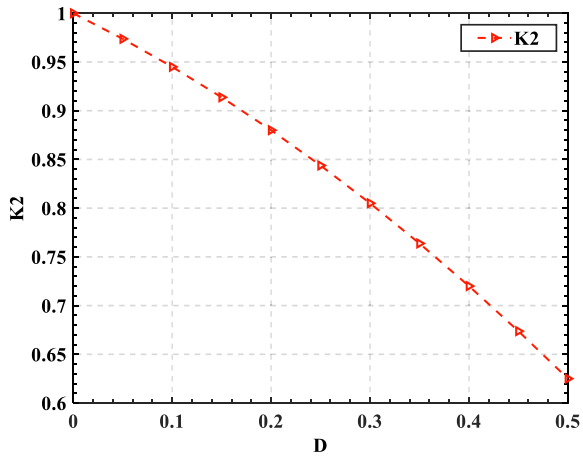


Fig. 5. Current ratio K_2 changes with duty cycle D.

The flying capacitors $C_{\text{fly}1}$ and $C_{\text{fly}2}$ meet the ampere-second balance in the steady state, that is, in the periodic steady state, the average current of the capacitor is 0, and we get

$$I_{C,11} D + I_{C,12}(1 - D) = I_{C,21} D + I_{C,22}(1 - D) = 0. \tag{13}$$

The obtained (13) is then substituted into (11) and (12). The average currents of the inductors L_1 and L_2 are, respectively,

$$I_{L1} = I_{O1}(1 - D) \tag{14}$$

$$I_{L2} = I_{O2}(1 - D). \tag{15}$$

Define the average value of the total inductor current as

$$I_L = I_{L1} + I_{L2}. \tag{16}$$

Then finally get the relationship between output current and inductor current

$$I_L = I_O(1 - D). \tag{17}$$

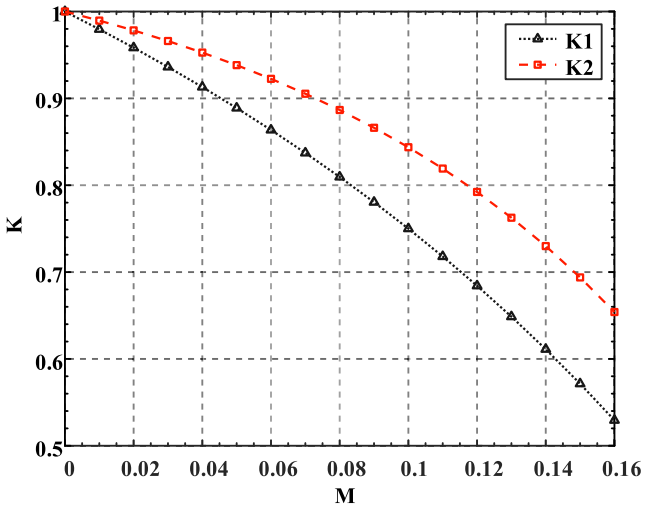


Fig. 6. Current ratio K_1 and K_2 changes with conversion ratio M.

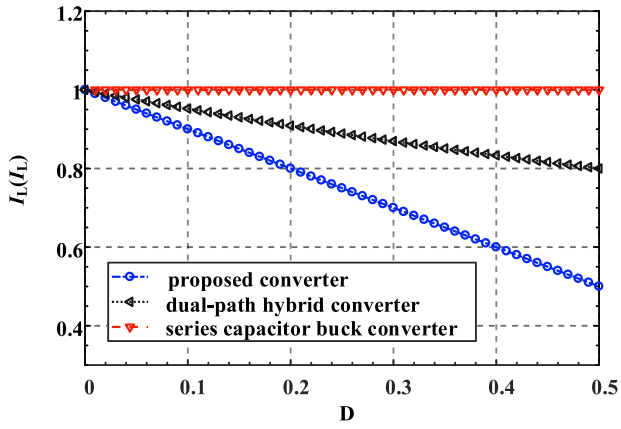


Fig. 7. Comparison of inductor current of different topologies.

Ensure that the conversion ratio and load are the same. Compared with the traditional two-phase SC-buck converter, the conversion ratio and the inductor current are

$$M = M_{\text{SC}} = \frac{D_{\text{SC}}}{2} \tag{18}$$

$$I_L^{\text{SC}} = I_{L1}^{\text{SC}} + I_{L2}^{\text{SC}} = I_O. \tag{19}$$

Calculate the ratio K_1 and express it with the conversion ratio M

$$K_1 = \frac{I_L}{I_L^{\text{SC}}} = 1 - D = \frac{1 - 4M}{1 - 2M} < 1. \tag{20}$$

Second, comparing the two-phase dual-path hybrid converter [1], the conversion ratio and the average value ratio of the inductor current are

$$M = M_D = \frac{D_D}{1 + D_D} \tag{21}$$

$$K_2 = \frac{I_L}{I_L^D} = \frac{1 - D}{1 - D_D}. \tag{22}$$

According to the condition that the conversion ratio and the load are equal, the relationship of the duty cycle is further derived

$$D_D = \frac{D}{2 + D}. \tag{23}$$

Then the inductor current ratio K_2 can be expressed as a function of D

$$K_2 = \frac{(1 - D)(2 + D)}{2}. \tag{24}$$

Due to the limitation of D, it can only take a value between 0 and 0.5, and the value range of K_2 can be simply analyzed.

As shown in Fig. 5, the change trend and range of the current ratio K_2 are shown, which is always less than 1, indicating that the inductor current of the proposed converter is always less than the two-phase dual-path hybrid converter.

Substituting again, denoting D with M, we can get

$$K_2 = \frac{(1 - 4M)(1 - M)}{(1 - 2M)^2}. \tag{25}$$

Under the same load condition, Fig. 6 shows the changes of the two current ratios K_1 and K_2 with the voltage conversion ratio M.

The comparison of the inductor current in different topologies is shown in Fig. 7.

This shows that in the case of equal load, the average value of the inductor current of the proposed topology is smaller than the average value of the output current. This is because the output current is no longer completely provided by the inductor, but part of it is provided by the fly-capacitor.

This is of great significance for reducing the inductance loss, especially the conduction loss, which makes this topology more advantageous in high output current applications.

C. Inductor Ripple Current Analysis

Since the series capacitor shares half of the input voltage, and the flying capacitor further shares part of the inductor voltage, the inductor current ripple is much lower than the inductor current ripple in the traditional converter.

For a single inductor L_1 to analyze, in the mode I, the inductor L_1 is charged, you can get

$$\Delta I_{L1} = \frac{(0.5V_{\text{in}} - 2V_O)}{L_1} D T_S = \frac{V_O}{L_1}(1 - D)T_S. \tag{26}$$

This equation can be expressed in the form of conversion ratio M and V_{in}

$$\Delta I_{L1} = \frac{M(1 - 2M)}{2(1 - M)} V_{\text{in}} \frac{T_S}{L_1}. \tag{27}$$

Ensure that the conversion ratio and load are the same. Compared with the traditional two-phase SC-buck converter, the inductor current ripple is

$$\Delta I_{L1}^{\text{SC}} = \frac{V_O(1 - D_{\text{SC}})}{L_1} T_S = M(1 - 2M) \frac{V_{\text{in}} T_S}{L_1}. \tag{28}$$

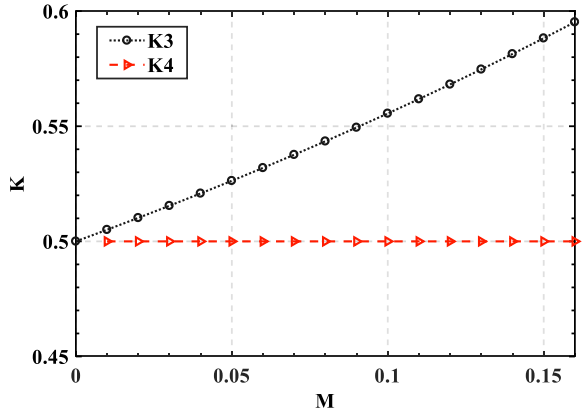


Fig. 8. Current ratio K_3 and K_4 changes with conversion ratio M.

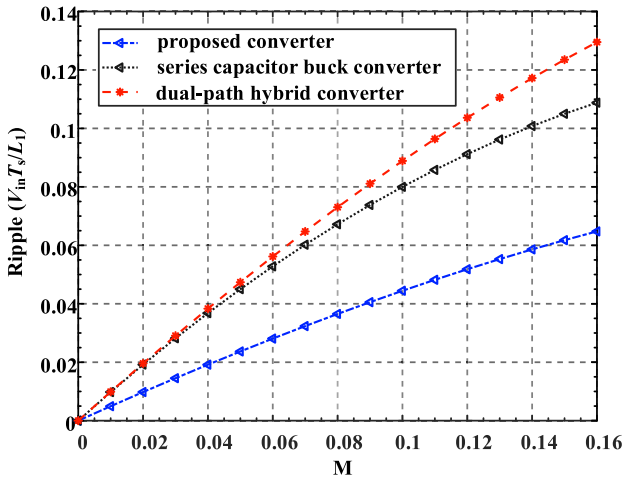


Fig. 9. Comparison of inductor ripple current of different topologies.

Calculate the current ripple ratio K_3 as

$$K_3 = \frac{\Delta I_{L1}}{\Delta I_{L1}^{SC}} = \frac{1}{2(1-M)}. \tag{29}$$

Secondly, comparing the two-phase dual-path hybrid converter, the inductor current ripple is

$$\Delta I_{L1}^{D} = \frac{V_O(1-D_D)}{L_1}T_S = \frac{D_D}{1+D_D}(1-D_D)\frac{V_{in}}{L_1}T_S. \tag{30}$$

Substituting the result of (21) into the above equation, the equation for M is obtained

$$\Delta I_{L1}^{D} = \frac{M(1-2M)}{1-M}\frac{V_{in}}{L_1}T_S. \tag{31}$$

Calculate another current ripple ratio K_4 as

$$K_4 = \frac{\Delta I_{L1}}{\Delta I_{L1}^{D}} = \frac{1}{2}. \tag{32}$$

Fig. 8 shows the relationship between the two current ripple ratios and the voltage conversion rate M, and Fig. 9 shows the relationship between the current ripple of the inductor L_1 and the voltage conversion rate M.

Fig. 10 shows the changes of the four current ratios with the voltage conversion ratio M. Among them K_1, K_3 are the parameters of SC-buck converter, K_2, K_4 are the parameters of two-phase dual-path hybrid converter. Assuming that the output current, switching period, inductance, and input voltage are the same, then the relative magnitude of K can represent the relative magnitude of the current. It can be seen that considering the ripple current and the dc current comprehensively, the equivalent ripple current coefficient and the dc current coefficient relative to SC-buck can be obtained at about 0.146.

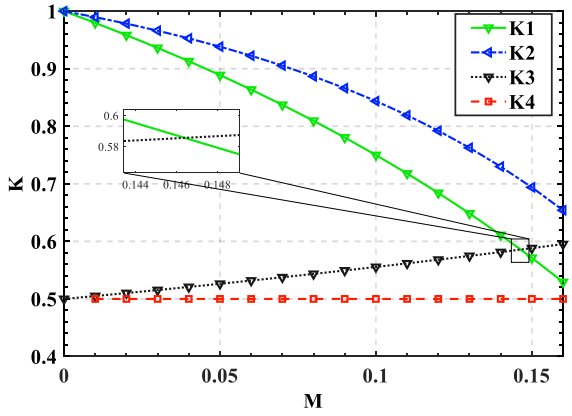


Fig. 10. Current ratio K_1, K_2, K_3, K_4 changes with conversion ratio M.

TABLE I
SWITCH STRESS OF PROPOSED CONVERTER

Switch	Voltage Stress	Current Stress
S_1	$V_{in}/2$	MI_o
S_2	MV_{in}	MI_o
S_3	$(1/2\text{-}M)V_{in}$	$\{M/(1\text{-}2M)\}I_o$
S_4	$(1/2\text{-}M)V_{in}$	$\{(1\text{-}2M\text{-}4M^*M)/(2\text{-}4M)\}I_o$
S_5	$V_{in}/2$	MI_o
S_6	$(1\text{-}M)V_{in}$	MI_o
S_7	$(1/2\text{-}M)V_{in}$	$\{M/(1\text{-}2M)\}I_o$
S_8	$(1/2\text{-}M)V_{in}$	$\{(1\text{-}2M\text{-}4M^*M)/(2\text{-}4M)\}I_o$

D. Switch Stress and Ratings

Switch stress is one metric for comparing switch size (which is tied to cost), and total switch stress for a converter is defined as

$$S = \sum_{i=1}^{n} V_i I_{\mathrm{RMS},i} \tag{33}$$

where V_i is the steady-state voltage blocking requirement of switch i, $I_{\mathrm{RMS},i}$ is the steady-state RMS current through switch i, and n represents the number of switches in a converter. This is also referred to as the voltage ampere (VA) product.

Table I gives the switch stress in the proposed converter. By comparing the results in the article [2], it can be seen that only the switch S_6 has a larger stress. Even so, the stress of each switch can still be smaller than that of the SC-buck converter.

Normalize the switching stress, the normalization basis is the product of input voltage and output current(each switch stress is divided by $V_{in}I_o$). The normalized maximum voltage stress comparison is given in Table II. The maximum switch stress for each converter occurs at the highest conversion ratio explored.

TABLE II
NOMINAL MAXIMUM SWITCH STRESS COMPARISON

Converter	Maximum Normalized Switch Stress
Buck (steady state)	1.33(M=0.167)
Series capacitor buck (steady state)	0.95(M=0.167)
Series capacitor buck (hot-plug compliant)	1.11(M=0.167)
Proposed converter (steady state)	0.78(M=0.167)
Proposed converter (hot-plug compliant)	0.86(M=0.167)

Without any additional circuitry, the phase A switches need to be rated for the full input voltage to withstand a hot-plug event [2].

E. Automatic Current Balancing

A unique benefit of the proposed converter is automatic inductor current balancing. Since sampling of high-frequency currents is very challenging, this feature makes the converter particularly advantageous in high-frequency applications. Furthermore, there is no longer a circulating current problem between the two phases, and a current-sharing control loop does not need to be added to the converter, which improves the power density of the converter and simplifies the control strategy.

The following briefly introduces the principle of automatic balance of two-phase currents [28]. The key point is the addition of capacitor C_t. In different modes, the capacitor C_t is charged and discharged separately. For phase B, the capacitor C_t is equivalent to the intermediate power supply and supplies power to the load. Assuming that in a certain situation, the A-phase current is greater than the B-phase current, it will cause the capacitor C_t voltage to increase, which will reduce the average voltage of the A-phase switch node and increase the average voltage of the B-phase switch node, thereby reducing the A-phase current and increasing the B-phase current. The opposite is the same. It should be noted that as long as the converter works, this feedback relationship will always exist, so that the two-phase currents always change in the same trend direction. The specific feedback process can be clearly shown in Fig. 11.

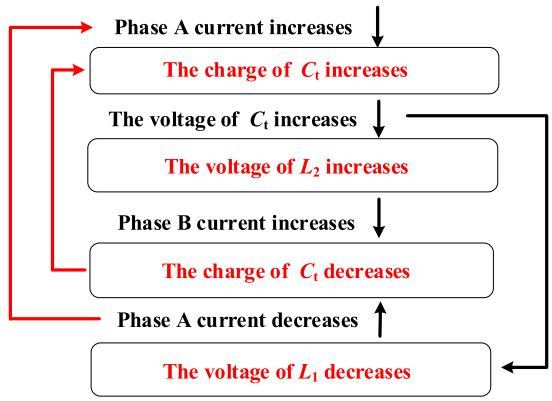
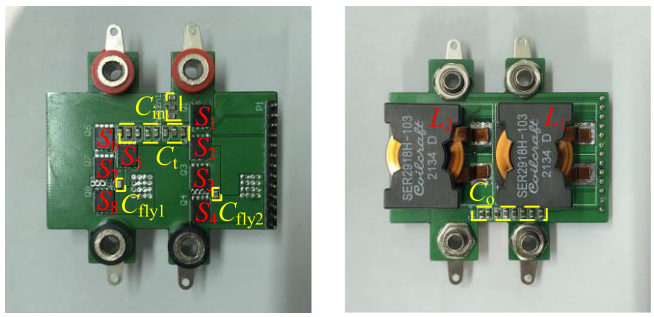


Fig. 11. Automatic current balancing feedback block diagram.

TABLE III
EXPERIMENTAL PARAMETERS OF THE PROTOTYPE

Label	Value	Item
C_t	80μF	50V,(10μF*8), GRM21BR61H106KE43L (Murata)
C_{in}	30μF	50V,(10μF*3), GRM21BR61H106KE43L (Murata)
C_{fly1}, C_{fly2}	10μF	25V,10μF, GRJ21BR61E106KE01L (Murata)
C_o	176μF	10V,(22μF*8), C2012X5R1A226KT000N(TDK)
L_1, L_2	10μH	10μH, DCR:2.6mΩ, SER2918H-103KL,Coilcraft
S_1-S_8	/	80V,100A,$R_{ds(on)max}$=5.7mΩ, BSC057N08NS3G(Infineon)



(a) (b)

Fig. 12. Photographs of the designed prototype. (a) Top side. (b) Bottom side.

IV. EXPERIMENTAL RESULTS

A 100 kHz, 6 V/120 W with 48 V input voltage prototype is built based on the proposed design method, which helps to verify the performance of the above proposed converter. The specific circuit parameters are given in Table III. The picture of the prototype is shown in Fig. 12.

The model of the oscilloscope used in the experiment is MSO 5204B, the voltage probe is P5205, and the current probe is TCP0030A. The main power supply is 62150H-600, the auxiliary power supply is RIGOL DP832, and the load is a dc electronic load IT8514B+.

In the experiment, the connection loss was not measured, that is, the loss on the wires connected from the main power supply to the converter and the wires connected to the load from the converter, so the efficiency obtained will be lower than the actual efficiency.

Fig. 13 shows the key voltage waveforms. The theoretical value of node voltage $V_{x1,1}$ is V_{in} to V_o, and the theoretical value of node voltage $V_{x1,2}$ is V_{in}-V_o to 0. Their amplitudes are the same, which is equivalent to that the node voltage $V_{x1,1}$ has an amplitude of V_o offset relative to the node voltage $V_{x1,1}$.

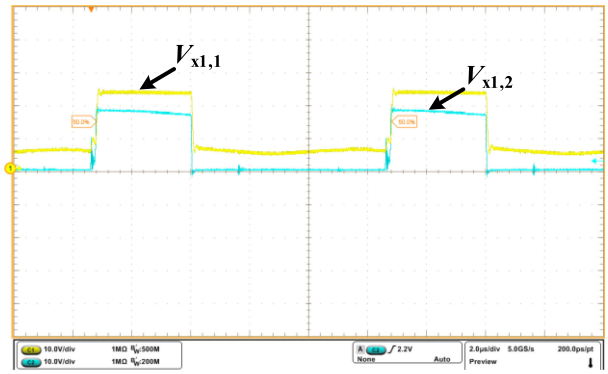


Fig. 13. Voltage waveform of key nodes.

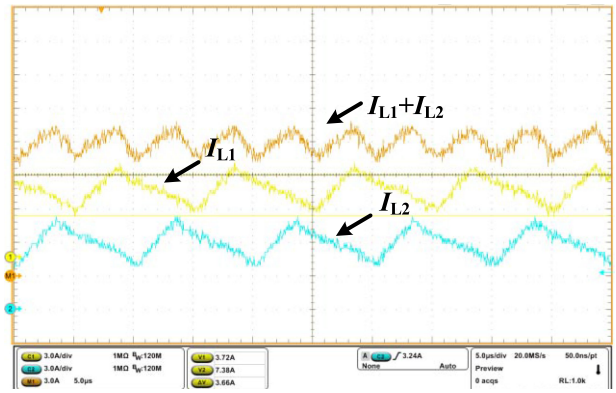


Fig. 14. Inductor current and synthetic current waveform.

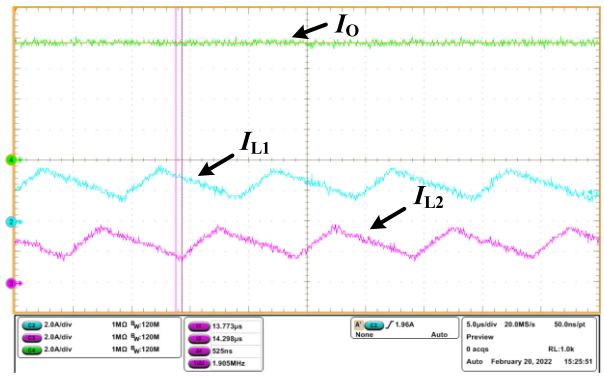


Fig. 15. DC Current Verification.

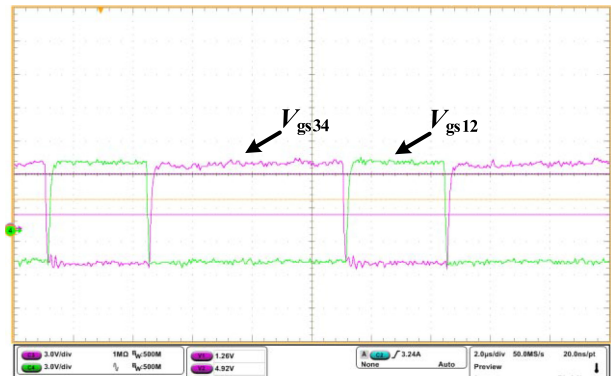


Fig. 16. V_{gs} waveform (represents drive signal).

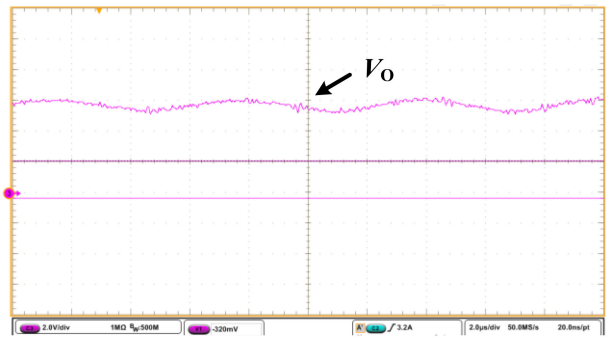


Fig. 17. V_o waveform.

Fig. 14 shows the waveforms of the two-phase inductor currents. In order to clearly show the phase relationship of the two-phase inductor currents, they are measured at the same time. It can be seen that the two-phase inductor current has a staggered characteristic, which reduces the current ripple. Since the current flowing into the *RC* terminal of this converter has a large current spike, which exceeds the test range of the probe, the current flowing into the *RC* terminal is not measured directly, but is approximated by the addition of two-phase currents. It should be noted that this part of the peak current has a very low impact on the output voltage, which is related to the shunt ratio of the capacitor and the inductance, as well as the duty cycle. Simply put, the larger the duty cycle, the more the capacitor shunt, the smaller the inductor current, the larger the *RC* terminal drop current spike, and the larger the output voltage ripple.

The verification of the dc current is shown in Fig. 15. Among them, the contract of two-phase current is 5 A, and the output current is 7.69 A, and the duty cycle is 33%. It is consistent with the formula (17) in the theoretical analysis. This verifies the correctness of the previous theoretical derivation.

Fig. 16 shows the drive signal, with a 1% dead time reserved, during which the inductor current flows through the MOSFET body diode. If the dead time is too long, the loss of the MOSFET body diode is too large and the converter efficiency is too low. If the dead time is too short, a pass- through problem may occur. The conduction strategy of phase shifting 180° makes the two phases work alternately. When the conversion ratio is 8/1, the duty cycle is 33%.

Fig. 17 shows the waveform of the output voltage. When a driving signal with a 33% duty cycle is used, the theoretical step-down ratio is 8:1. Under the condition of 48 V input, the output is 6 V, which verifies the correctness of the previous theoretical analysis. Properly increasing the output capacitor can reduce the output ripple.

Figs. 18 and 19 show the response of the output voltage and current to a step load in the open loop state. The experiment is obtained by increasing the load from 25% to 50% and then dropping it to 25%. It can be seen that the time of the transient process is about 5.5 ms, whether it is a sudden load increase

TABLE IV
PROPERTIES COMPARISON BETWEEN DIFFERENT STEP-DOWN TOPOLOGIES

Symbol	Voltage conversion with 0.5 duty cycle	Power level	Power density	Switching frequency	Power transistors	Efficiency
Proposed	1/6	120W	169W/in^3	100kHz	Si	93.18%
48V-5V direct conversion 1MHz DC-DC Converter in [10]	1/2	30W	/	1MHz	GaN	85.23%
48V-12V 1/16 Brick DC-DC Converter in [11]	1/2	300W	730W/in^3	/	GaN	95%
48V-2V Flying Capacitor Multilevel Converter in [12]	Fixed-ratio	20W	/	83.3kHz	GaN	85%
48-to-6 V Multi-Resonant-Doubler Switched-Capacitor Converter in [13]	Fixed-ratio	240W	1675W/in^3	70kHz	Si	95.9%

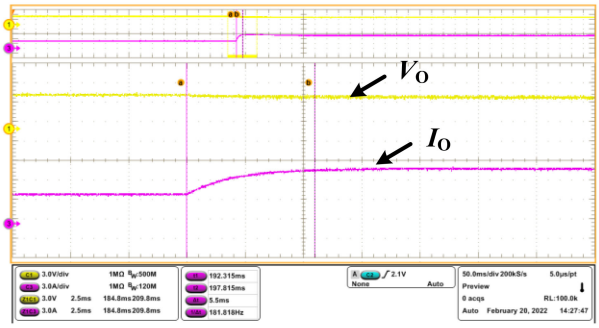


Fig. 18. Dynamic response under sudden increase in load.

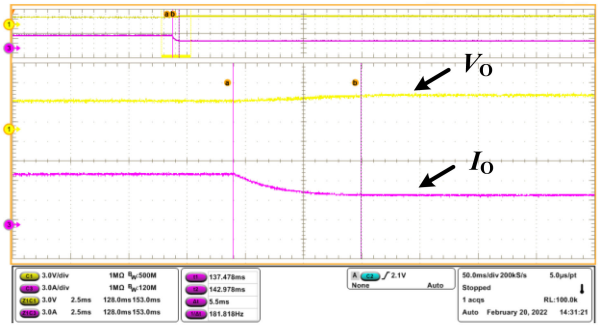


Fig. 19. Dynamic response under sudden decrease in load.

or a sudden load decrease. Demonstrating the extreme dynamic performance of the converter is beyond the scope of this article.

Table IV gives the comparison of the characteristics of different step-down converters. It can be seen from the table that in the conversion of adjustable output voltage, the step-down ratio is the largest when the duty cycle is the same. In a single-stage converter with an adjustable duty cycle and a large step-down ratio, the proposed converter has a higher power density and a good efficiency.

The following is a theoretical loss analysis of the converter. The loss analysis is based on the rated working state of the converter, that is, the input voltage is 48 V, the output voltage is 6 V, the output current is 20 A, and the switching frequency is 100 kHz.The dead time is very short, and the freewheeling loss of the MOSFET body diode is negligible. It is considered that when the switch is turned OFF, the leakage current is zero, that is, the turn-OFF loss is ignored, too.

First, the switching loss of the switch. The theoretical calculation formula is

$$P_{L\_S} = \frac{1}{6} I \times V_s \left(\frac{Q_g}{I_g} \right) f \tag{34}$$

where V_s is the switch voltage, I_g is the drive current, and I is the average current when the switch is turned ON and OFF. The drive current is calculated according to the drive circuit

$$I_g = \frac{V - V_{\text{plat}}}{R} \tag{35}$$

where V is the drive or turn-OFF voltage, V_{plat} is the Miller platform voltage, and R is the turn-ON or turn-OFF resistance.

The conduction loss of the switch is

$$P_{L\_SC} = I_{\text{rms}}^2 \times R_{\text{DS(on)}}. \tag{36}$$

Drive loss of the switch

$$P_{L\_D} = U_{gs} Q_g f. \tag{37}$$

In the formula, Q_g is the gate charge of the power switch, U_{gs} is the gate-source voltage drop when the power switch is fully turned ON, and f is operating frequency. Because the switching frequency is not high, the driving loss is very low, accounting for less than 1%.

The dc conduction loss of the inductor

$$P_{L\_DC} = I_{\text{dc}}^2 \times \text{DCR}. \tag{38}$$

Magnetic loss of inductance

$$P_{L\_AC} = (\Delta I)^2 \times \text{ACR} \tag{39}$$

Capacitance loss and line loss are relatively small compared to the above types of loss and are negligible. Calculate the theoretical value of each part loss and the percentage of total loss under the rated working condition. The resulting loss analysis graph is shown in Fig. 20. It can be seen that the conduction

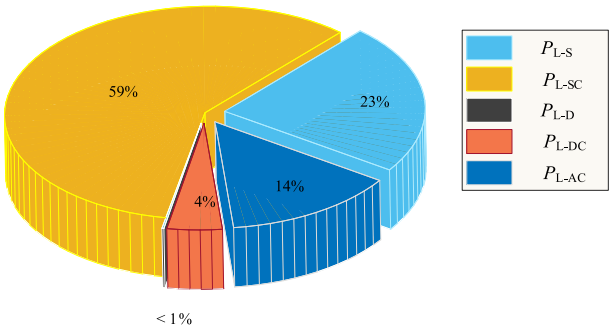


Fig. 20 Pie chart of loss distribution of the proposed converter.

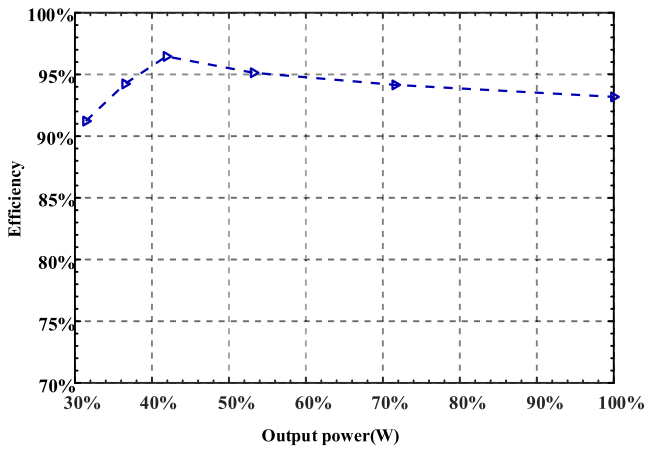


Fig. 21 System efficiency with changing loads.

loss of the switch accounts for the largest proportion, followed by the switching loss, and then the ac loss of the inductor. Driving loss is relatively low. Si material transistors are more suitable for low-voltage and high-current applications due to their low ON-resistance characteristics. However, its limited switching frequency limits the power density of the system. Considering the system efficiency and system power density comprehensively, a balance is achieved between the two, and the power density should be increased as much as possible while ensuring the efficiency.

Fig. 21 shows the efficiency curve of the system under different load conditions, which is measured in experiment. It can be seen that the efficiency first increases and then decreases with the increase of the load, reaching the peak efficiency at about 40% of the rated load, and then the efficiency is 93.18% at full load.

V. Conclusion

A new type of two-phase series capacitor dual-path hybrid converter is proposed in this article. The converter has lower inductor dc current and ripples current, and has the advantages of two-phase current self-balancing, duty cycle expansion, low voltage stress, and low switching loss. The topology is analyzed in detail, and the comparison results with the SC-buck converter and two-phase dual-path hybrid converter are given. The experimental results are consistent with the theoretical analysis, and the efficiency of the system reaches 93.18% under full load.

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