Analysis and Design of a Nonisolated DC Transformer With Fault Current Limiting Capability

Yanan Ye, *Student Member, IEEE*, Xiaotian Zhang, *Senior Member, IEEE*, Jiuyang Jin, Yue Wang, *Member, IEEE*, and Xu Yang, *Senior Member, IEEE*

***Abstract*—The dc–dc converter, also termed as dc transformer, plays an important role in the future dc grids. It is used to interconnect network segments or lines with different voltage levels. A nonisolated modular multilevel dc–dc converter is presented in this article, which can realize bidirectional power regulation and dc fault current limiting. The control strategy is simplified and the current stresses are decreased due to the employment of autotransformers. The nonisolated structure can reduce the requirements of autotransformers, because only part of the transmitted power flowing though the autotransformers. The operation principle and control strategy of this converter are illustrated in detail. The analyzes of power transmission, submodule (SM) capacitor voltage ripple, the optimal configuration, and the efficiency of this converter are also provided. The optimal design methods of the dc transformer are proposed to reduce the costs and power losses according to the analysis results. Simulations performed in power systems computer aided design/electromagnetic transients including DC (PSCAD/EMTDC) and experiments based on a down-scaled prototype verify the operation principle, control strategy, and theoretical analysis. The simulation results and experiment results show the performances of the converter under steady state, power regulation, and fault conditions.**

***Index Terms*—DC–DC converter, dc grids, down-scaled prototype, fault current limiting capability, PSCAD/EMTDC, power transmission.**

I. Introduction

THE dc transmission system is gaining more attraction for large-scale renewable energy integration due to the advantages of larger capacity, longer transmission distance, and higher efficiency comparing to the ac transmission system [1], [2]. However, even though lots of HVdc point-to-point systems have been put into practical application all around the world [3], so far no dc grid with different voltage levels has been seen. Therefore, the dc–dc converters are essential in the future dc grids. They are required to interconnect the network segments or lines with different voltage levels [4]–[6]. Besides, other abilities for dc transformers, such as bidirectional power flow regulation and fault current limiting are also indispensable. In particular, when fault happens, the fault current may cause severe damages to the dc transformer and other equipment in the dc grid. Therefore, realizing fault current limiting for the dc transformers is essential.

In the past decades, the dc transformers have gained significant research attentions [7]–[11]. The developments of modular dc transformers for the medium-voltage (MV) or high-voltage (HV) dc applications have been revealed in this article. Normally, the dc–dc converters are classified into the isolated dc transformers and nonisolated dc transformers according to whether there is galvanic isolation between input and output dc sides [12]. The isolated structures offer inherent dc fault blocking capability and convenient dc interconnection. However, the isolated dc transformers have the disadvantages of higher costs, lower efficiency comparing to the nonisolated dc transformers.

The dual-active bridge (DAB) converter and the front-to-front (FTF) converter are two typical isolated dc transformers topologies. The input-series output-parallel dual-active bridge (ISOP-DAB) converter composed of numerous single DAB units is a popular option for the HVdc and MVdc applications [13]. The ISOP-DAB converter has the advantages of high efficiency and an excellent dynamic performance due to the zero-voltage switching and high operation frequency. However, such topology requires a huge number of isolated transformers, which significantly increases the costs and volume [14], [15]. To reduce the number of isolated transformers, series connected switches are used in each DAB units. However, this may lead to the issue of unequal voltage stresses across semiconductor devices.

Modular multilevel converters (MMCs) have the flexible and scalable architecture, which are popular solutions to achieve dc–ac conversion in the HVdc and MVdc system [16], [17]. The basic unit of MMC is usually half-bridge submodule (SM) (HBSM) or full-bridge SM (FBSM). Hence, the FTF dc–dc converter, which consists of two MMCs is another feasible option for realizing voltage conversion in dc grids [7], [18], [19]. The isolated configuration can achieve large voltage conversion ratio, galvanic isolation, and fault current limiting. Nevertheless, due to the large number of semiconductor devices, the FTF dc–dc converter has the disadvantages of high investment costs, high losses, and low power density.

There are also some topologies, which combine the MMC and the DAB to realize high voltage (HV) conversion ratio [20]–[23]. Parida and Das [24] proposed a new topology, which comprises a

Manuscript received October 21, 2021; revised January 26, 2022; accepted March 3, 2022. Date of publication March 15, 2022; date of current version April 28, 2022. This work was supported by the National Key R&D Program of China under Grant 2018YFB0904600. Recommended for publication by Associate Editor M. S. ElMoursi. *(Corresponding author: Xiaotian Zhang.)*

The authors are with the Department of Electrical Engineering, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: yeyanan@stu.xjtu.edu.cn; arch.j8@gmail.com; jin666@stu.xjtu.edu.cn; davidwangyue@mail.xjtu.edu.cn; yangxu@xjtu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3158819.

Digital Object Identifier 10.1109/TPEL.2022.3158819

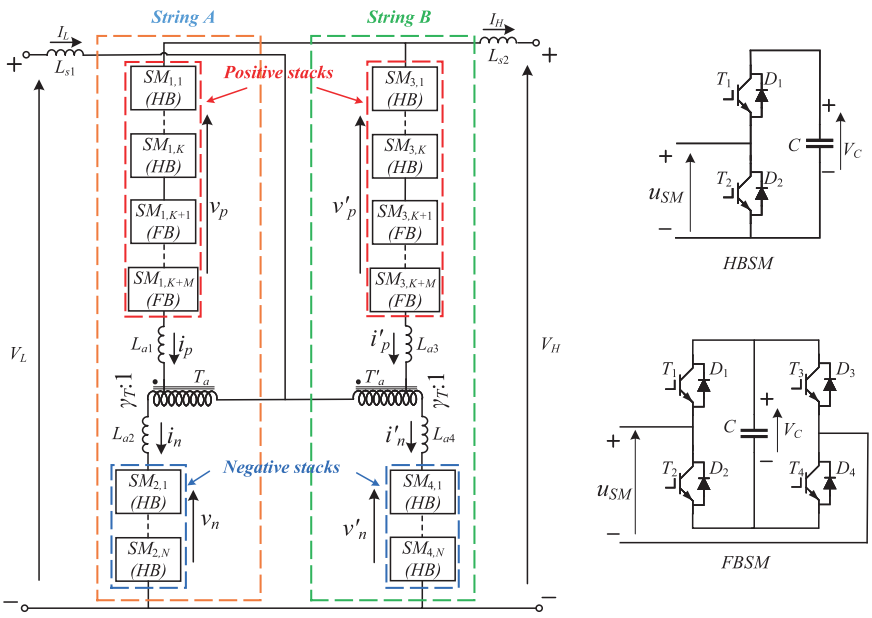


Fig. 1. Topology of the dc–dc converter.

voltage source MMC and a current source MMC to interconnect two different types of HVdc networks.

The HVdc autotransformer (HVdc-AT) is one of the typical nonisolated dc transformer topologies [25], [26]. It can considerably reduce the costs and losses due to the nonisolated structure. However, the HVdc-AT still requires an isolated transformer, which is difficult to design and takes a large volume. Some topologies employ series connected SMs instead of transformers to realize the energy balance of the stacks [27], [28]. However, it will increase the costs and power losses because the number of SMs increases. To solve this problem, the topologies utilizing capacitive filters are proposed [29], [30].

The modular multilevel DC converter (M2DC) is another typical nonisolated dc transformer topology, which does not require isolated transformers [31]–[35]. However, the current stresses will be increased without transformers, especially when the voltage conversion ratio increases. Besides, it utilizes the ac component to maintain the power balance of stacks. Therefore, the M2DC requires output filters to prevent ac currents from entering to the dc network. Some other topologies replace the filters with series-cascaded SMs [36]–[40]. However, the costs and the power losses of these topologies will be huge if the number of SMs increases.

In order to reduce costs and losses as much as possible, the hybrid-cascaded dc–dc converter and some other similar topologies, which do not require isolated transformer or output filters have been proposed in [41]–[46]. These topologies utilize the SM capacitors to store and transfer the energy and can significantly reduce the number of SMs. However, a large number of insulated gate bipolar transistors (IGBTs) or other switching devices are required to be connected to the dc terminals, especially when the voltage conversion ratio is high. Moreover, too many series-connected switches may lead to the issue of unequal voltage stresses.

In future dc grids, multiport dc–dc converters are necessary. Hence, based on the topologies of the dc transformers with two terminals, some topologies of multiport dc transformers are proposed [47]–[49].

This article presents a nonisolated modular multilevel dc–dc converter for MVdc or HVdc applications. It has the advantages of low costs, low losses, and small size due to the nonisolated architecture. It can realize bidirectional power regulation and fault current limiting. The analyzes of the power transmission, the SM capacitor voltage ripple, the optimal configuration, and the efficiency of the converter are performed. The design of the converter is optimized according to the theoretical analysis. The operation principle, control strategy, and theoretical analysis are validated via the simulation and experiment.

The rest of this article is organized as follows. The topology, operation principle, and control strategy of the dc transformer are described in Section II. The analysis and design methods are illustrated in Section III. The simulation results and experiment results are presented in Sections IV and V, respectively. Finally, Section VI concludes this article.

II. Topology, Operation Principle, and Control Strategy

A. Topology

The circuit diagram of the dc–dc converter with two-string architecture is shown in Fig. 1. This converter consists of two strings, which are basically symmetrical to prevent the ac currents from entering the dc sides. Each string consists of an autotransformer T_a (T'_a) with the turns ratio of γ_T, two arm inductors L_{a1} and L_{a2} (L_{a3} and L_{a4}), and two stacks consisting of series-cascaded SMs. The voltages of the low voltage (LV) side and HV side are represented by V_L and V_H ($V_L < V_H$), respectively. The voltage conversion ratio of the converter is

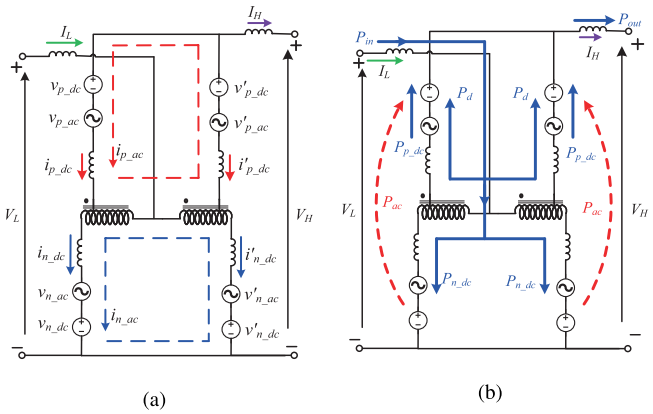


Fig. 2. Current flowing paths and power flowing paths of the converter. (a) Current flowing paths. (b) Power flowing paths.

defined as $\gamma = V_H/V_L$. The terminal currents are represented by I_L and I_H. The line inductors are represented by L_{s1} and L_{s2}, respectively. Furthermore, it can also be extended to the three-string architecture and bipolar system for the specific conditions. The autotransformers are mainly employed to simplify the control strategy by keeping the modulation indexes of all stacks the same. They can also reduce the current stresses comparing to the topology without autotransformers when the transmitted power is the same. The two autotransformers are coupled in reverse coupling mode to avoid the influence of the dc bias, because there are dc current components flowing through the autotransformers. The turns ratio γ_T of the autotransformer is determined by the voltage conversion ratio γ of the dc–dc converter, $\gamma_T = 1/(\gamma - 1)$. The values of arm inductance and leakage inductance of autotransformer determine the maximum power of the dc transformer. The stacks consist of series-cascaded SMs for realizing the voltage conversion and fault current limiting. The positive stack contains M FBSMs and N HBSMs, while the negative stack is composed of N HBSMs. The positive stack can also provide fault limiting capability, because it can insert reverse voltage to inhibit fault currents when a dc fault happens on either the input or output dc side.

B. Operation Principle

There are two general assumptions enforced in this section and following analysis: 1) all the semiconductor switches and passive elements are ideal and 2) the ac voltage components generated by stacks are ideal sinusoidal.

To explain the operation principle, the current flowing paths and power flowing paths of the dc–dc converter are presented in Fig. 2. The paths of dc current components are indicated by solid arrows, while the paths of circulating ac current components are indicated by dotted arrows. The ac current components of the stacks are used to maintain the stability and balance of SM capacitor voltages and they are represented by the i_{p_ac} and i_{n_ac}. Each stack is equivalent to a dc voltage source and an ac voltage source.

The input power (P_{in}) of the dc–dc converter is divided into two parts under normal operation. One part of the power flows from the LV side to the HV side directly, which is represented by P_d. The dc power P_d is determined by the input power and voltage conversion ratio ($P_d = P_{\text{in}}/\gamma$). Another part of the power flows from the LV side to the negative stack, which is represented by P_{n_dc}. This power is converted to ac power P_{ac} via the negative stack and transferred to the positive stack. Finally, the ac power is converted into dc power P_{p_dc} and transferred to the HV side. The transmission of ac power P_{ac} is achieved via the ac current components. The values of the ac power and the ac current components are determined by the phase shift between the ac voltage components of the positive and negative stacks.

When the phase shift between ac voltage components of the positive and negative stacks is greater than $180°$, the ac active power is transferred from the negative stacks to the positive stacks via the generated ac currents. To balance the energy of stacks, the negative stacks absorb the dc power and release the ac power. The positive stacks absorb the ac power and release the dc power. The values of dc current components of positive stacks are greater than 0. Therefore, the output current is greater than 0, which means that the power is transferred from the LV side to the HV side. Similarly, when the phase shift between ac voltage components of the positive and negative stacks is less than $180°$, the ac active power is transferred from the positive stacks to the negative stacks via the generated ac currents. The positive stacks absorb the dc power and release the ac power. The negative stacks absorb the ac power and release the dc power. The values of dc current components of positive stacks are less than 0. Therefore, the output current is less than 0, which means that the power is transferred from the HV side to the LV side.

An important characteristic of the topology is the inherent symmetry, which is essential to prevent the ac currents from entering the dc sides. Since the ac current components only circulate inside the converter, the fundamental frequency of the ac voltage components of the stacks does not have to be 50/60 Hz, which is applied in MMC widely. As the ac frequency increases, the size of passive components, such as capacitors, inductors, and autotransformers, can be reduced. However, the higher ac operating frequency also means the higher switching frequency of the semiconductor devices, which increases the power losses. In the specific applications, the selection of ac operating frequency depends on the tradeoff between power losses and device requirements including SM capacitor voltage fluctuation and size of dc transformer.

C. Control Strategy

The control diagram of the dc–dc converter is presented in Fig. 3. Define the output current I_H as the current flowing into the HV side and the power P as the power transferred from LV side to HV side. Then, the output current and power are obtained as

$$I_H = -2I_{p\_\text{dc}} \tag{1}$$

$$P = V_H I_H = -2V_H I_{p\_\text{dc}}. \tag{2}$$

Fig. 3(a) shows the control method of power regulation. The power is regulated by adjusting the phase shift between the ac voltage components of the positive stack and negative

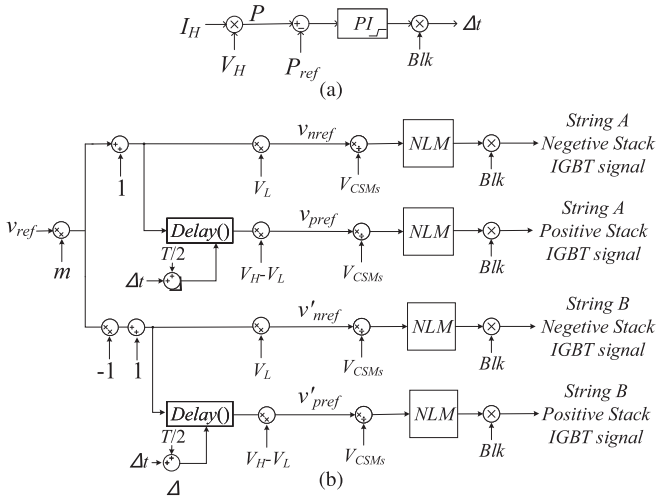


Fig. 3. Control diagram of the dc–dc converter. (a) Power regulation control strategy. (b) IGBT driving signal modulation.

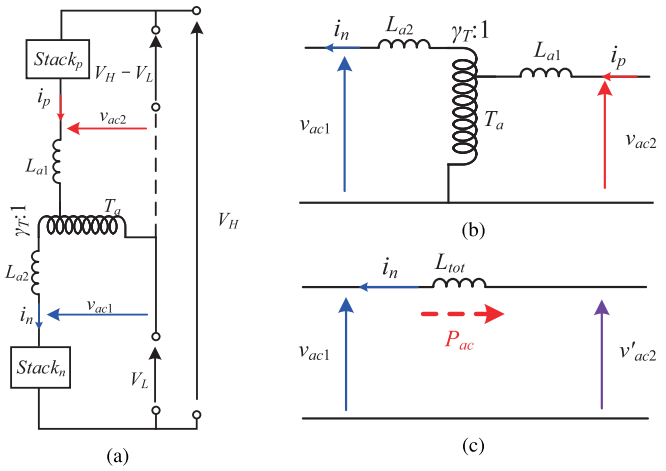


Fig. 4. Derivation of equivalent circuit. (a) Circuit of String A. (b) Simplified circuit of String A. (c) Equivalent circuit of String A.

stack, which is determined by Δt. When $\Delta t > 0$, the power is transferred from the LV side to HV side, and the opposite is also true. Besides, as the absolute value of Δt increases, the value of transmitted power also increases. When a dc fault happens on the dc side, the block signal Blk is used to realize fault current limiting by setting Δt to zero and blocking all the switches.

The modulation strategy is shown in Fig. 3(b). The reference voltage v_{ref} determines the waveform of ac voltage component of stacks, and it can be set to sine-waveform, square-waveform, or quasi-square-waveform, etc. The period and amplitude of the fundamental ac voltage components are T and 1, respectively. The modulation index of all the stacks is the same and represented by m. The Δt is used to adjust the phase shift of the ac voltage components of stacks. The nearest level modulation method is applied to ensure voltage balance of SM capacitors. It is popular when the stack consists of a large number of SMs because it has better reliability than other modulation methods [50].

III. Theoretical Analysis

A. Power Transmission

The simplified circuit of the dc–dc converter with one string is shown as Fig. 4(a). The stack voltages and arm currents can be decomposed into dc components and ac components, which are expressed as

$$v_{p,n}(t) = V_{p\_\text{dc},n\_\text{dc}} + \sqrt{2}V_{p\_\text{ac},n\_\text{ac}}\sin(\omega t + \varphi_{p,n}) \quad (3)$$

$$i_{p,n}(t) = I_{p\_\text{dc},n\_\text{dc}} + \sqrt{2}I_{p\_\text{ac},n\_\text{ac}}\sin(\omega t + \theta). \quad (4)$$

In this section, the theoretical analysis results are obtained based on that v_{ref} is a sine wave. Ignoring the small high-order harmonics components, the stack voltages are composed of dc components and fundamental components. The dc voltages components of stacks are used to withstand the voltages of dc sources. Hence, the V_{n_dc} and V_{p_dc} are equal to the V_L and $V_H - V_L$, respectively. Therefore, the voltages of the negative stack and positive stack in String A are obtained as

$$v_n(t) = V_L + mV_L\sin(\omega t). \quad (5)$$

$$v_p(t) = (V_H - V_L) + m(V_H - V_L)\sin\left[\omega\left(t - \Delta t - \frac{T}{2}\right)\right]. \quad (6)$$

Equation (6) can be simplified as

$$v_p(t) = (\gamma - 1)V_L - m(\gamma - 1)V_L\sin(\omega t - \varphi) \quad (7)$$

where $\omega = \frac{2\pi}{T} = 2\pi f$, $\varphi = \omega\Delta t$.

Thus, the circuit can be simplified to Fig. 4(b). The ac voltages (v_{ac1} and v_{ac2}) can be obtained as

$$v_{\text{ac1}}(t) = v_{n\_\text{ac}}(t) = mV_L\sin\omega t \quad (8)$$

$$v_{\text{ac2}}(t) = -v_{p\_\text{ac}}(t) = m(\gamma - 1)V_L\sin(\omega t - \varphi). \quad (9)$$

Utilizing the equivalent circuit of transformer, the circuit is equivalent to the circuit as Fig. 4(c), and the total equivalent inductance is L_{tot}, which contains the equivalent leakage inductance $L_{\text{Ta\_eq}}$ of the autotransformer. Due to $v'_{\text{ac2}}(t) = \gamma_T \cdot v_{\text{ac2}}(t)$, the ac current component of negative stack can be calculated as

$$i_{n\_\text{ac}}(t) = -\frac{1}{L_{\text{tot}}}\int_0^t [v_{\text{ac1}}(t) - v'_{\text{ac2}}(t)]\text{d}t \quad (10)$$

$$i_{n\_\text{ac}}(t) = -\frac{m \cdot V_L \cdot \sin(\frac{\varphi}{2}) \cdot \sin\left(\omega t - \frac{\varphi}{2}\right)}{\pi f L_{\text{tot}}} \quad (11)$$

where $L_{\text{tot}} = L_a + \gamma_T^2 L_a + L_{\text{Ta\_eq}}$.

Therefore, $\varphi_n = 0$, $\varphi_p = -(\pi + \varphi)$, and $\theta = -(\pi + \frac{\varphi}{2})$.

Due to the exist of autotransformers, the relationship between the voltages and currents of the positive stack and negative stack is presented as

$$\frac{I_{p\_\text{ac}}}{I_{n\_\text{ac}}} = \frac{V_{n\_\text{ac}}}{V_{p\_\text{ac}}} = \gamma_T. \quad (12)$$

Hence, the ac current component of positive stack is easily obtained as

$$i_{p\_ac}(t) = -\frac{\gamma_T \cdot m \cdot V_L \cdot \sin(\frac{\varphi}{2}) \cdot \sin\left(\omega t - \frac{\varphi}{2}\right)}{\pi f L_{\text{tot}}}. \tag{13}$$

Due to the energy balance of the stacks, the average power absorbed by the stack is zero. Therefore, it can be obtained as

$$P_n = \frac{1}{T}\int_0^T v_n(t) \cdot i_n(t)\mathrm{d}t = 0 \tag{14}$$

$$P_p = \frac{1}{T}\int_0^T v_p(t) \cdot i_p(t)\mathrm{d}t = 0. \tag{15}$$

Submitting (3) and (4) to (14) and (15), the relationships between dc current components and ac current components can be derived as

$$V_{n\_dc} I_{n\_dc} = -\frac{\sqrt{2}}{2} m V_{n\_dc} I_{n\_ac} \cos\frac{\varphi}{2} \tag{16}$$

$$V_{p\_dc} I_{p\_dc} = \frac{\sqrt{2}}{2} m V_{p\_dc} I_{p\_ac} \cos\frac{\varphi}{2}. \tag{17}$$

Hence, the dc current components of negative arm and positive arm are obtained as

$$I_{n\_dc} = -\frac{\sqrt{2}}{2} m I_{n\_ac} \cos\frac{\varphi}{2} \tag{18}$$

$$I_{p\_dc} = \frac{\sqrt{2}}{2} m I_{p\_ac} \cos\frac{\varphi}{2}. \tag{19}$$

Submitting (11) and (13) to (18) and (19), respectively, the dc current components of negative stack and positive stack are calculated as

$$I_{n\_dc} = \frac{m^2 \cdot V_L \cdot \sin\varphi}{4\pi f L_{\text{tot}}} \tag{20}$$

$$I_{p\_dc} = -\frac{\gamma_T m^2 \cdot V_L \cdot \sin\varphi}{4\pi f L_{\text{tot}}}. \tag{21}$$

Submitting (21) into (1) and (2), the output current and power can be obtained as

$$I_H = -2I_{p\_dc} = \frac{\gamma_T m^2 \cdot V_L \cdot \sin\varphi}{2\pi f L_{\text{tot}}} \tag{22}$$

$$P = V_H I_H = \frac{(\gamma_T + 1) m^2 \cdot V_L^2 \cdot \sin\varphi}{2\pi f L_{\text{tot}}}. \tag{23}$$

When $\varphi = \frac{\pi}{2}$, the transmitted power is maximum and the value is

$$P_{\max} = V_H I_{H\_\max} = \frac{(\gamma_T + 1) m^2 \cdot V_L^2}{2\pi f L_{\text{tot}}}. \tag{24}$$

The current stresses of stacks can be calculated according to (18) and (19). When the power is maximum, the current stresses of the positive stacks and negative stacks are maximum, which can be calculated as

$$\frac{\sqrt{2} I_{p\_ac}}{I_{p\_dc}} = \frac{\sqrt{2} I_{n\_ac}}{I_{n\_dc}} = \frac{2}{m\cos\frac{\varphi}{2}}. \tag{25}$$

It can be seen that the current stresses of the positive stacks and negative stacks are the same due to the same modulation indexes. Besides, increasing the modulation index can reduce the current stresses. The current stresses will also be increased as the phase shift increases. Hence, the phase shift should be small when the dc transformer operates at rated power to reduce the current stresses. In this article, phase shift is designed to be 0.3 at rated power condition and 0.5 at maximum power condition.

Furthermore, if the topology employs inductors instead of the autotransformers, one of the modulation indexes of the positive stacks and negative stacks will decrease. The current stresses will increase when the power is same. Therefore, the employment of the autotransformers can reduce the device current stresses at the same power.

B. SM Capacitor Voltage Ripple

It is significant for the converter to ensure the SM capacitor voltages balance and stable. Therefore, the selection of the SM capacitance is important to satisfy the requirement of SM capacitor voltage ripple. The fluctuation of capacitor voltage is usually limited within 10%, which is widely accepted for MMC [51]. The SM capacitor voltages in the stacks should be balanced well in normal operation. The ripple of single capacitor voltage is represented by $v_{C\_\text{rip}}(t)$. The capacitance is C and the dc component of single SM capacitor voltage is V_C. The equivalent amount of capacitors used to balance voltage in this stack is N_C, which is related to the control strategy. Therefore, the stack energy stored in the SM capacitors is presented as

$$\begin{aligned} e_{\text{ST}}(t) &= \frac{1}{2} C N_C [V_C + v_{C\_\text{rip}}(t)]^2 = \frac{1}{2} C N_C V_C^2 \\ &\quad + C N_C V_C v_{C\_\text{rip}}(t) + \frac{1}{2} C N_C v_{C\_\text{rip}}^2(t). \end{aligned} \tag{26}$$

Ignoring the quadratic term of the fluctuation value, which is too small comparing to others, the capacitor voltage ripple can be obtained as

$$v_{C\_\text{rip}}(t) = \frac{e_{\text{ST\_ac}}(t)}{C N_C V_C}. \tag{27}$$

At the same time, the ac energy components of stacks can be calculated by the stack power exchange

$$e_{\text{ST}p\_\text{ac}}(t) = \int_0^t v_p(t) \cdot i_p(t)\mathrm{d}t \tag{28}$$

$$e_{\text{ST}n\_\text{ac}}(t) = \int_0^t v_n(t) \cdot i_n(t)\mathrm{d}t. \tag{29}$$

The voltages and currents of stacks have been obtained in the previous section. Therefore, the ac components of the total energy stored in the stacks are obtained as

$$e_{\text{ST}p\_\text{ac}}(t) = \frac{m^2 V_L^2}{16\pi^2 f^2 L_{\text{tot}}} \cdot A(t) \tag{30}$$

$$e_{\text{ST}n\_\text{ac}}(t) = \frac{m^2 V_L^2}{16\pi^2 f^2 L_{\text{tot}}} \cdot B(t) \tag{31}$$

where

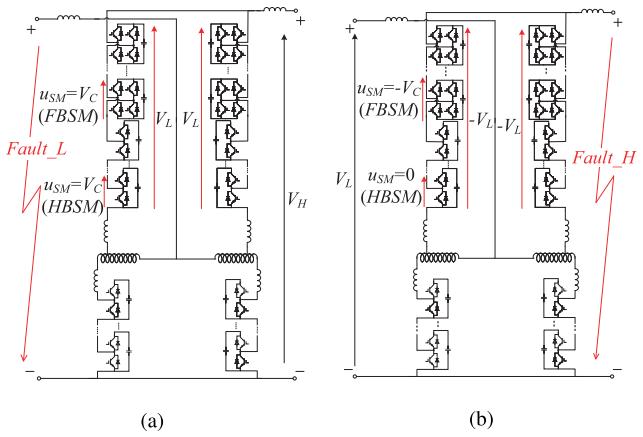


Fig. 5. Voltages that positive stacks withstand under fault conditions. (a) DC fault happens on LV side. (b) DC fault happens on HV side.

$$A(t) = \frac{4 - m^2 - 4\cos\varphi + m^2\cos 2\varphi}{m}\sin\omega t + \frac{m^2\sin 2\varphi - 4\sin\varphi}{m}\cos\omega t + (\sin 2\varphi - \sin\varphi)\sin 2\omega t + (\cos\varphi - \cos 2\varphi)\cdot\cos 2\omega t,$$

$$B(t) = \frac{4 - 4\cos\varphi}{m}\cdot\sin\omega t + \frac{2m^2 - 4}{m}\sin\varphi\cdot\cos\omega t - \sin\varphi\cdot\sin 2\omega t - (1 - \cos\varphi)\cdot\cos 2\omega t.$$

Substituting (30) and (31) into (27), respectively, then the ac components of SM capacitor voltages can be calculated as

$$v_{Cp\_\text{rip}}(t) = \frac{m^2V_L^2}{16CN_{Cp}V_C\pi^2f^2L_{\text{tot}}}\cdot A(t) \tag{32}$$

$$v_{Cn\_\text{rip}}(t) = \frac{m^2V_L^2}{16CN_{Cn}V_C\pi^2f^2L_{\text{tot}}}\cdot B(t) \tag{33}$$

where $N_{Cp} = K + M$ and $N_{Cn} = N$.

The fluctuation of SM capacitor voltage is calculated as

$$\xi_{p,n} = \frac{v_{Cp,n\_\max} - v_{Cp,n\_\min}}{V_C}. \tag{34}$$

C. Fault Limiting Capability

Due to the low impedance in the dc system, the current will increase quickly when a dc fault occurs, which may cause great damages to the cables and equipment in the dc system. Hence, fault current limiting capability is an important characteristic for the dc–dc converters applied in dc grids. This topology can realize fault current limiting when a dc fault happens on the either dc side. As shown in Fig. 5, there are two fault conditions considered in this article, which may cause the great damages. The pole-to-pole fault happens on the HV side ($V_H = 0$ V) and the pole-to-pole fault happens on the LV side ($V_L = 0$ V). No matter which dc side the fault occurs, the positive stacks need to provide reverse voltage to withstand the voltage of the other dc side. Therefore, series-cascaded FBSMs, which can provide reverse voltage are required to be inserted into the positive stacks. The negative stacks are only composed of HBSMs because the negative stacks have slight effect on the fault current limiting when the fault happens on either dc side.

The quantities of the two types of SMs in different stacks are required to realize both voltage conversion and fault current limiting. First of all, the stacks should be able to generate the required ac voltages with the dc offsets for voltage conversion. Hence, the first requirements for number of the SMs are obtained as

$$N\cdot V_C \geq (1+m)\cdot V_L \tag{35}$$

$$(M+K)\cdot V_C \geq (1+m)\cdot(V_H - V_L) \tag{36}$$

where N, M, and K are the number of HBSMs in the negative stacks, the numbers of FBSMs, and HBSMs in the positive stacks, respectively.

Second, the amounts of the FBSMs and HBSMs in the positive stacks are required to ensure that the converter realizes fault current limiting. When a dc fault occurs in the LV side, as shown in Fig. 5(a), the voltage of each positive stack should be larger than V_H to suppress the fault current. Therefore, the output voltages of HBSMs and FBSMs in the positive stacks are all V_C and the total voltage is larger than V_H. As shown in Fig. 5(b), when a dc fault occurs in the HV side, the voltage of each the positive stack should be less than $-V_L$ to suppress the fault current. However, the HBSMs cannot withstand reverse voltage and the output voltages of HBSMs are either V_C or 0 V. Therefore, the output voltages of FBSMs in the positive stacks are all V_C and the output voltages of HBSMs in the stacks are all 0 V. According to the abovementioned constraints, the requirements of the SMs number can be obtained as

$$(M+K)\cdot V_c \geq V_H \tag{37}$$

$$-M\cdot V_c \leq -V_L. \tag{38}$$

In order to reduce the costs and improve efficiency, the number of semiconductor devices should be as fewer as possible, which means that the number of FBSMs (M) should be minimum. Hence, the optimal configuration principles of the strings are obtained as

$$N = \frac{2V_L}{V_c} \tag{39}$$

$$M = \frac{V_L}{V_c} \tag{40}$$

$$K = \max\left\{\frac{(\gamma + m\gamma - m - 2)V_L}{V_c}, \frac{(\gamma-1)V_L}{V_c}\right\}. \tag{41}$$

The rated capacitor voltage V_C is selected according to the normal withstand voltage of semiconductor devices, which is constant. Once V_C is determined, M and N are selected depending on V_L only, while K is also affected by the voltage conversion ratio of the converter γ. If the terminal voltages are fixed, the optimal configuration of the dc transformer is determined. Besides, with the increase of voltage conversion ratio γ, the percentage of the required FBSMs decreases.

D. Converter Efficiency

The power losses are mainly composed of the losses of semiconductors and the losses of autotransformers. The losses of semiconductors including conduction losses and switching losses, which can be calculated according to the approach proposed in [8] and [52]. The amplitudes of dc voltage component and ac voltage component of the stack are represented by $V_{\rm dc}$ and $V_{\rm ac}$, respectively. The instantaneous value of arm current is represented by the $i_{\rm Arm}$. The total number of the SMs in the arm is represented by n. The average conduction losses of each HBSM in the arm are calculated as

$$P_{C,T1} = \frac{1}{2\pi}\int_0^{2\pi} \delta \cdot V_{CE}(i_{{\rm Arm},n}) \cdot i_{{\rm Arm},n} {\rm d}\omega t \tag{42}$$

$$P_{C,D1} = \frac{1}{2\pi}\int_0^{2\pi} \delta \cdot V_{F}(i_{{\rm Arm},p}) \cdot i_{{\rm Arm},p} {\rm d}\omega t \tag{43}$$

$$P_{C,T2} = \frac{1}{2\pi}\int_0^{2\pi} (1-\delta) \cdot V_{CE}(i_{{\rm Arm},p}) \cdot i_{{\rm Arm},p} {\rm d}\omega t \tag{44}$$

$$P_{C,D2} = \frac{1}{2\pi}\int_0^{2\pi} (1-\delta) \cdot V_{F}(i_{{\rm Arm},n}) \cdot i_{{\rm Arm},n} {\rm d}\omega t \tag{45}$$

$$P_C = P_{C,T1} + P_{C,D1} + P_{C,T2} + P_{C,D2} \tag{46}$$

where

$$\delta = \frac{\rm V_{dc}}{2nV_C}(1 + m\sin(\omega t)), m \quad = \frac{2V_{\rm ac}}{V_{\rm dc}} \tag{47}$$

$$i_{{\rm Arm},p} = \begin{cases} i_{\rm Arm}\ , & i_{\rm Arm} > 0 \\ 0\ , & i_{\rm Arm} \le 0 \end{cases} \tag{48}$$

$$i_{{\rm Arm},n} = \begin{cases} 0\ , & i_{\rm Arm} \ge 0 \\ i_{\rm Arm}\ , & i_{\rm Arm} < 0. \end{cases} \tag{49}$$

The rated capacitor voltages are represented by V_C and the frequency of ac voltage component is represented by $f_{\rm ac}$. The scalar quantity $K_{\rm sw}$ is set as 1.5 to realize the capacitor voltages balance. The average switching losses of each HBSM in the arm can be calculated as

$$P_{{\rm SW},T1} = f_{\rm sw}(E_{T\rm on} + E_{T\rm off})\frac{I_{{\rm arm}n\_{\rm dc}} \cdot V_C}{I_{\rm ref} \cdot V_{\rm ref}} \tag{50}$$

$$P_{{\rm SW},D1} = f_{\rm sw}E_{\rm Drr}\frac{I_{{\rm arm}p\_{\rm dc}} \cdot V_C}{I_{\rm ref} \cdot V_{\rm ref}} \tag{51}$$

$$P_{{\rm SW},T2} = f_{\rm sw}(E_{T\rm on} + E_{T\rm off})\frac{I_{{\rm arm}p\_{\rm dc}} \cdot V_C}{I_{\rm ref} \cdot V_{\rm ref}} \tag{52}$$

$$P_{{\rm SW},D2} = f_{\rm sw}E_{\rm Drr}\frac{I_{{\rm arm}n\_{\rm dc}} \cdot V_C}{I_{\rm ref} \cdot V_{\rm ref}} \tag{53}$$

$$P_{\rm SW} = P_{{\rm SW},T1} + P_{{\rm SW},D1} + P_{{\rm SW},T2} + P_{{\rm SW},D2} \tag{54}$$

where

$$f_{\rm sw} = K_{\rm sw}f_{\rm ac}\frac{2V_{\rm ac}}{nV_C}. \tag{55}$$

Therefore, the total losses of one HBSM in the arm can be calculated as

$$P_{l\_{\rm HB}} = P_C + P_{\rm SW}. \tag{56}$$

Although the output voltage of FBSM could be 0 V, V_C or $-V_C$, the output voltage of the FBSM is either 0 V or V_C in normal operation, which is the same as the HBSM. It means that the switch states of S_1 and S_2 in FBSMs are the same as those in HBSMs. The switch S_4 is on and switch S_3 is off all the time. Therefore, comparing to the losses of each HBSM in the arm, the increased losses of each FBSM are the conduction losses of the S_4 and D_4

$$P_{C,T4} = \frac{1}{2\pi}\int_0^{2\pi} V_{CE}(i_{{\rm Arm},n}) \cdot i_{{\rm Arm},n} {\rm d}\omega t \tag{57}$$

$$P_{C,D4} = \frac{1}{2\pi}\int_0^{2\pi} V_{F}(i_{{\rm Arm},n}) \cdot i_{{\rm Arm},p} {\rm d}\omega t \tag{58}$$

$$P_{l\_{\rm FB}} = P_{CT4} + P_{CD4} + P_{l\_{\rm HB}}. \tag{59}$$

The total losses of semiconductor in the presented converter can be calculated as

$$P_{l\_{\rm SM}} = 2(K \cdot P_{l\_{\rm HB}\_p} + M \cdot P_{l\_{\rm FB}\_p} + N \cdot P_{l\_{\rm HB}\_n}) \tag{60}$$

where $P_{l\_{\rm HB}\_p}$, $P_{l\_{\rm FB}\_p}$, and $P_{l\_{\rm HB}\_n}$ represent the total semiconductor losses of the HBSMs in one positive stack, the total semiconductor losses of the FBSMs in the positive stack and the total semiconductor losses of the HBSMs in one negative stack.

The power losses from the autotransformer are mainly composed of the core losses and copper losses. The total power losses from one autotransformer increase with the transferred power and can be estimated to be 0.5% of the rated apparent power [8]. Hence, the total losses from each autotransformer is approximated as

$$P_T = 0.5\% \cdot S_{\rm at} \tag{61}$$

where $S_{\rm at}$ is the rated apparent power of each autotransformer.

The voltage of the LV side is 500 kV and the rated SM capacitor voltage is 2 kV in the calculation. The ac operating frequency is 200 Hz and the IGBT (CM1200HC-90R) is selected as the semiconductor for the calculation in this article. The amounts of SMs are selected according to the analysis results in Section III-C. Then, the efficiencies of the dc transformer under different power and different voltage conversion ratios are calculated and shown in Fig. 6.

E. Comparison

The comparison of the FTF, HVdc-AT, M2DC, and the dc transformer in this article based on costs, efficiency, and current stresses is completed [7], [25], [36]. The parameters and functions of converters for comparison are all the same. The voltage of the LV side is 500 kV, the voltage of the HV side is 750 kV, and the rated power is 1000 MW. All the topologies insert some FBSMs to achieve fault current limiting except FTF, which can achieve that inherently. The comparison results are shown in Table I.

First, it can be seen that the FTF requires more semiconductor devices than the other topologies due to the isolated structure, even though it does not require any FBSM to realize fault current limiting. Hence, the investment costs of the FTF is higher than that of the other dc transformers and the costs of other

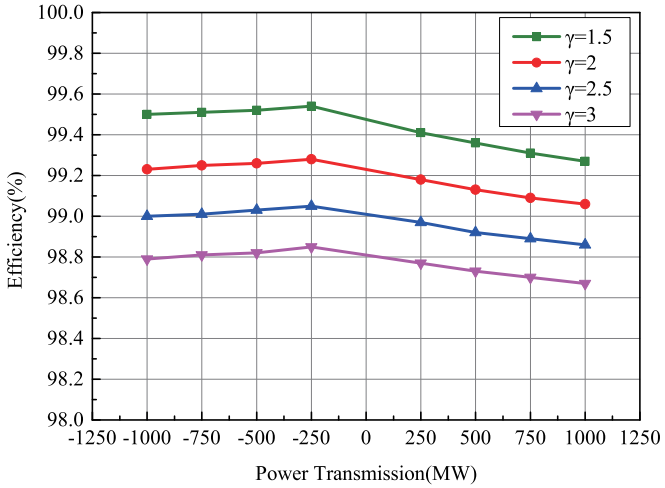


Fig. 6. Efficiencies of the dc transformer under different power and different voltage conversion ratios.

TABLE I
COMPARISON OF THE DIFFERENT DC TRANSFORMERS

Items	FTF in [7]	HVdc-AT in [25]	M2DC in [36]	Topology in Fig. 1
Number of IGBTs	4500	4000	4000	4000
Efficiency	98.03%	99.27%	99.32%	99.27%
Current stresses of positive stacks	2.02	2.02	2.02	2.02
Current stresses of negative stacks	2.02	2.02	4.04	2.02
I_{dc} in positive stacks (kA)	$-2/3$	$-2/3$	$-2/3$	$-2/3$
I_{dc} in negative stacks (kA)	1	$1/3$	$1/3$	$1/3$
Magnetics devices	Isolated transformer	Isolated transformer	Large inductors	Autotransformers

three topologies are basically the same. Second, the efficiency of FTF is much lower than the other topologies because it requires the larger number of semiconductor devices and the apparent power of the transformer is greater than that of the other three topologies. The efficiencies of other three topologies are basically the same. Third, with the modulation index $m = 1$, the current stresses are all about 2, except the current stresses of negative stack in M2DC is much larger than that in the other three topologies because it does not employ the transformer. However, the dc current of the primary stack in the FTF is much larger than in other topologies due to the isolated structure. Finally, the power transferred by transformer in the FTF is equal to the power of the converter. Whereas only part of the power of the converter is transmitted through the transformers in HVdc-AT and the topology in this article.

In summary, the FTF has high investment costs and low efficiency due to the isolated structure. The M2DC has high current stresses due to no transformer. The HVdc-AT has the similar performance to the topology in this article. However, the topology in this article employs the autotransformers instead of the isolated transformer, which means that this topology has smaller size than HVdc-AT. Besides, the HVdc-AT employs eight arms while the topology in this article employs four arms. This causes that the control strategy of HVdc-AT is more complex than that of the topology in this article.

TABLE II
SIMULATION PARAMETERS

Symbol	Description	Value
V_L	Low voltage	500 kV
V_H	High voltage	800 kV
P_{rate}	Rated power	1000 MW
K	Number of HBSMs in positive stack	150
M	Number of FBSMs in positive stack	250
N	Number of HBSMs in negative stack	500
m	Modulation index of Stack	1
f	AC frequency	200 Hz
$L_{a1}, L_{a2}, L_{a3}, L_{a4}$	Arm inductor	50 mH
C	SM capacitance	8 mF
L_{s1}, L_{s2}	Line inductance	50 mH
$\gamma_T : 1$	turns ratio of Autotransformer	5 : 3
L_T	Autotransformer leakage reactance	4 mH

IV. SIMULATION RESULTS

A model of the dc–dc converter, as shown in Fig. 1, is built in power systems computer aided design/electromagnetic transients including DC (PSCAD/EMTDC) to verify the analysis results and explain the design methods. The detail parameters of the converter in simulation are shown in Table II. The dc–dc converter is employed to interconnect two dc networks in the simulation. The simulation results including steady state, dynamic, and fault conditions are presented in Figs. 7 and 8.

The parameters of this converter are designed as an example to explain the design methods according to the analysis results. First, the voltage conversion ratio γ of converter and the turns ratio γ_T of autotransformers can be obtained as $\gamma = \frac{8}{5}$ and $\gamma_T = \frac{5}{3}$. The rated voltage of SM capacitor is set as $V_C = 2$ kV and the modulation index is set as $m = 1$. Then, the number of FBSMs and HBSMs in the positive stack and the amounts of HBSMs in the negative stack can be calculated according to (39)–(41). The value of φ is set to 0.3 when the dc–dc converter operates at rated power ($P_{\varphi=0.3} = 1000$ MW). Then, the $f \cdot L_{\text{tot}}$ can be calculated as 31.35 according to (23). The capacitance value of SMs is related to the capacitor voltage ripple. The minimum value of $f \cdot C$ can be calculated as 0.84 to guarantee $\xi \leq 10\%$ when $\varphi = \pm 0.5$ according to (30) and (31). Then, the values of f, L_{tot} and C can be selected according to the requirements of rated power and capacitor voltage ripples. Various allocations exist, an example of $f = 200$ Hz, $C = 8$ mF, and $L_{a1,2,3,4} = 50$ mH is accepted here.

Fig. 7 shows the simulation results when the dc transformer operates at rated power of 1000 MW. In the dynamic simulation, the power is regulated ranging from -1000 to 1500 MW. Fig. 7(a) shows the voltages and currents of the stacks in String A. The phase shift between the ac current component of positive stack and negative stack is greater than 180°. The dc current component of positive stack is less than 0. The phase of ac current component and ac voltage component is opposite, meaning that the positive stack absorb ac power and release dc power. Similarly, the voltage and current of negative stack indicate that the negative stack absorb dc power and release ac

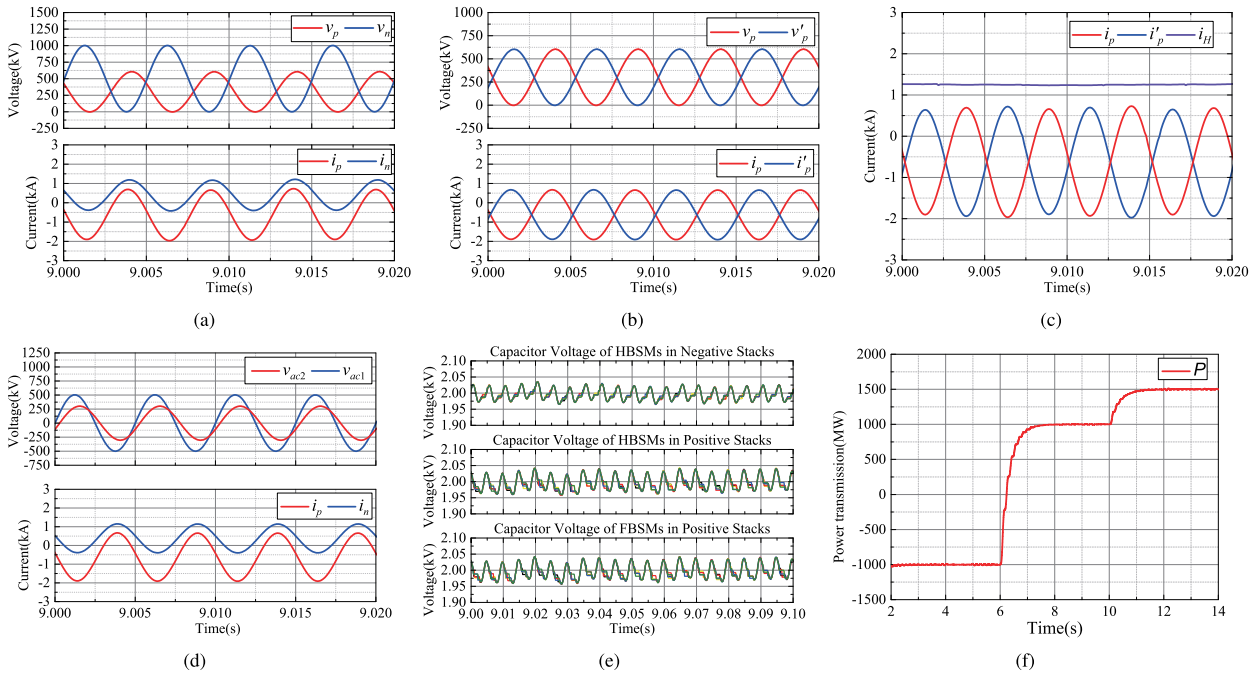


Fig. 7. Simulation results under steady state and power regulation condition. (a) Voltages and currents of the positive and negative stacks of String A. (b) Voltages and currents of the positive stacks of two string. (c) Currents of positive stacks in each strings and output current. (d) Arm currents and the ac voltages generated by stacks and dc sides. (e) SM capacitor voltage ripples in positive stack and negative stack of String A. (f) Power during regulation.

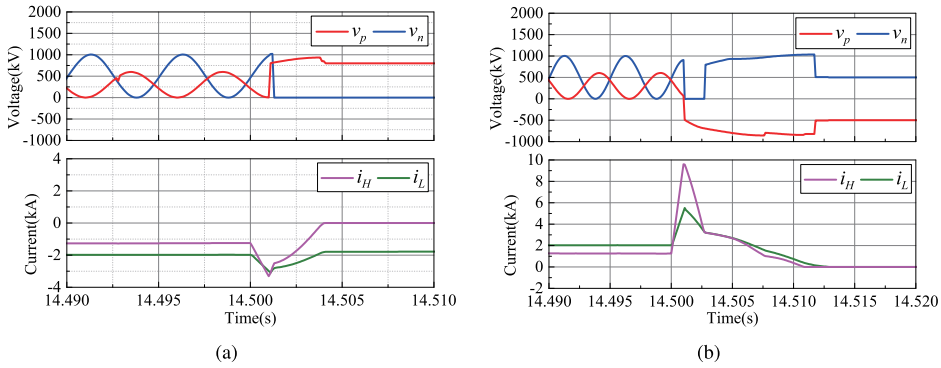


Fig. 8. Waveforms of stack voltages and terminal currents under fault conditions. (a) Fault happens on LV side. (b) Fault happens on HV side.

power. Fig. 7(b) and (c) displays the waveforms of the voltages of the positive stacks, arm currents of positive stacks, and the output current. The voltages and currents of two positive stacks are symmetrical. The output current contains nearly zero harmonics, which means that the ac current components only flow within the dc–dc converter due to the symmetry. Fig. 7(d) shows the ac voltages (v_{ac1} and v_{ac2}) generated by the stacks and dc sides and the arm currents. The amplitudes of v_{ac1} and v_{ac2} are 300 kV and 500 kV, respectively, which are the same as the stack ac voltage components. The phase of ac current is opposite to the voltage, meaning that the ac power is transferred from the negative stack to the positive stack.

Fig. 7(e) shows the waveforms of SM capacitor voltages. It indicates that the SM capacitor voltages are balanced to the rated value of 2 kV and the capacitor voltage ripples are less than 5%, which is within the range of expectations. Fig. 7(f) presents the waveform of the output current under the condition of power regulation. The power is adjusted from -1000 to 1000 MW at

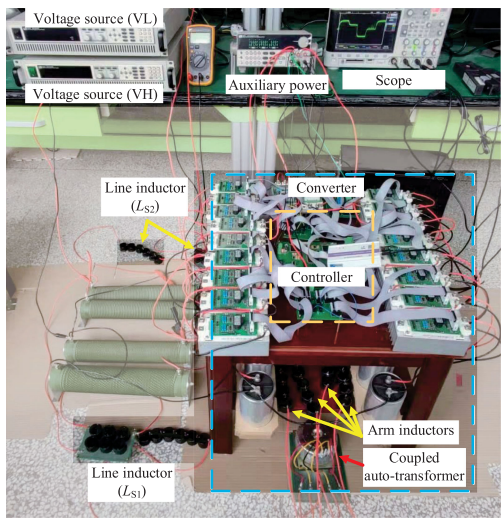


Fig. 9. Experimental platform of the dc–dc converter.

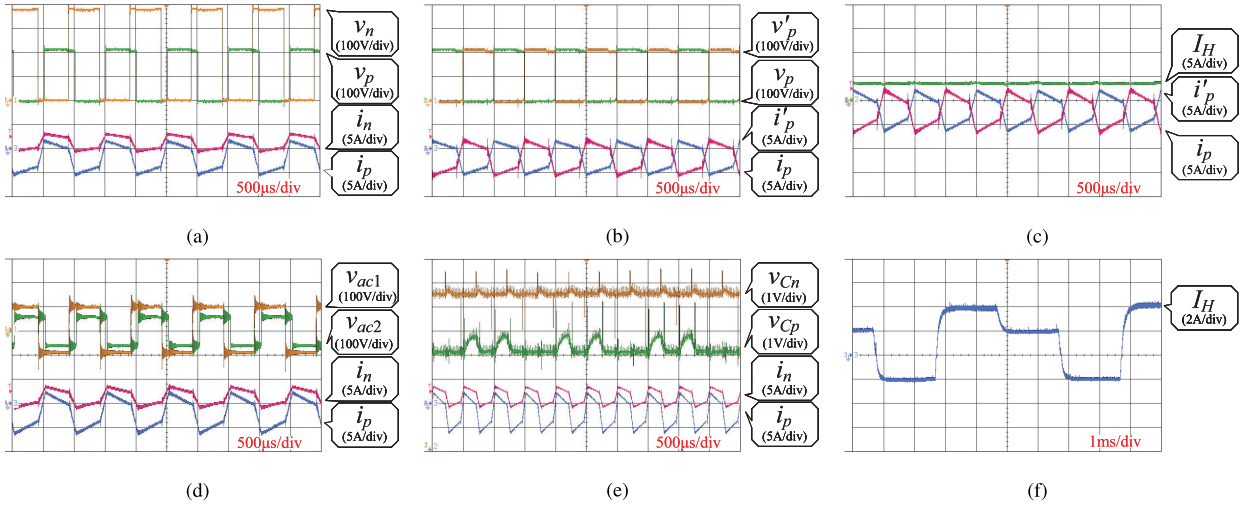


Fig. 10. Experiment results under steady state and power regulation condition. (a) Voltages and currents of the positive stack and negative stack. (b) Voltages and currents of positive stacks of two strings. (c) Currents of positive stacks of two strings and the output current. (d) Arm currents and ac voltages generated by stacks and dc sides. (e) Capacitor voltages of the submodules and the arm currents. (f) Output current during power regulation.

TABLE III
EXPERIMENTAL PARAMETERS

Symbol	Description	Value
V_L	Low voltage	200 V
V_H	High voltage	300 V
P	Rated power	1200 W
K	Number of HBSMs in positive stack	1
M	Number of FBSMs in positive stack	2
N	Number of HBSMs in negative stack	4
m	Modulation index	1
$\gamma_T : 1$	turns ratio of Autotransformer	2:1
f	AC frequency	1000 Hz
$L_{a1}, L_{a2}, L_{a3}, L_{a4}$	Arm inductance	2.64 mH
C	SM capacitance	550 μF
L_{s1}, L_{s2}	Line inductance	3.64 mH

$t = 6$ s and from 1000 to 1500 MW at $t = 10$ s. The simulation results verify the operation principle and control strategy of the dc transformer. The dc–dc converter has excellent dynamic response and accuracy of the steady state.

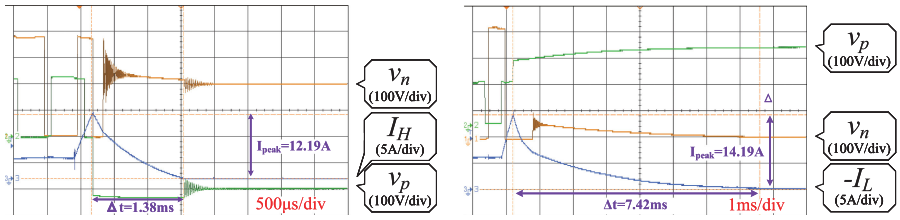
Fig. 8 shows the performance of converter under dc fault conditions. Usually, it will take about some time to block all the IGBTs after the occurrence of fault due to the fault detection and signal communication, and the delay time is set as 1 ms in this simulation. The power is -1000 MW before the a dc fault happens on the LV side and the power is 1000 MW before the a dc fault happens on the HV side. Fig. 8(a) presents the simulation results when a dc fault happens on the LV side at $t = 14.5$ s. All the HBSMs and FBSMs in positive stack withstand the voltage of HV side. The fault current decreases rapidly, but it reduces to 0 slowly due to currents, which flow through the freewheeling diodes of the HBSMs in the negative stack. Similarly, Fig. 8(b) presents the simulation results when a dc happens on the HV side at $t = 14.5$ s. The fault current decreases rapidly after the fault occurrence. These simulation results validate that the proposed optimal configuration is reasonable to achieve fault current limiting.

V. EXPERIMENT RESULTS

In this section, to verify the theoretical analysis and simulation results, a 1.2 kW, 200 V/300 V laboratory prototype based on this topology is built and the experimental platform is shown in Fig. 9. The positive stack employs one HBSM and two FBSMs and the negative stack employs four HBSMs. The rated capacitor voltage is 100 V. The detailed parameters of this prototype are shown in the Table III. Due to the dc voltage is low, the number of submodules in the prototype is small. Therefore, the conventional two-level phase-shift control method illustrated in [53] is adopted to simplify the control.

The waveforms of stack voltages and arm currents at rated power are shown in Fig. 10(a). There are parasitic resistances of SMs and fluctuation of capacitor voltage. Therefore, the ac voltage components of the positive and negative stacks do not conform to the turns ratio of autotransformer exactly. As a result, the arm current waveforms are not totally trapezoidal. Fig. 10(b) shows the currents and voltages of positive stacks, and Fig. 10(c) displays the output current and currents of positive stacks. The currents and voltages of positive stacks are symmetrical, and the output current contains nearly no harmonic component. Fig. 10(d) shows the ac voltages generated by the stacks and dc side. The amplitudes of $v_{\rm ac1}$ and $v_{\rm ac2}$ are 200 V and 100 V, respectively. The amplitudes of the ac current components are determined by the phase shift and amplitudes of the ac voltages. Fig. 10(e) displays the waveforms of SM capacitor voltages and the arm currents. The capacitor voltages are all about 100 V and the voltage ripples are less than 1 V. The experimental result of power regulation is shown in Fig. 10(f). Because the dc side voltage is constant, the power is represented by the output current. The output current I_H is adjusted from 4 to 2 A, then to -2 A, and finally back to 4 A. The time interval is 2 s. The prototype experimental results validate that the operation principle and control strategy of the dc transformer.

The experiment results of laboratory prototype under dc fault conditions are shown in the Fig. 11. When the current detected by the controller exceeds the set value, the controller blocks all



(a) (b)

Fig. 11. Experimental results under fault conditions. (a) Fault happens on the LV side. (b) Fault happens on the HV side.

the semiconductor switches of the converter. The fault happens on LV side when $P = -1.2$ kW and the fault happens on HV side when $P = 1.2$ kW. The experimental waveforms of fault on the HV side are shown in Fig. 11(a) and $I_H \geq 10$ A is set for fault detection. Since it takes some time to detect fault and block all the semiconductor devices after the occurrence of dc fault, the peak value of fault current is a little larger than the set value. Both the HBSMs and FBSMs in the positive stack provide reverse voltage in fault current circuit when the fault occurs in the LV side. Fig. 11(b) shows the experimental waveforms when a dc fault happens on the HV side. The fault determination condition is $-I_L \geq 8$ A. Similarly, the peak value of fault current is a little larger than the set value. The reverse voltage of the positive stack is generated via the FBSMs, which makes the fault current rapidly drop and gradually reduce to zero. According to the experimental results shown in Fig. 11, it can be seen that this converter can realize the bidirectional fault current limiting.

VI. Conclusion

A nonisolated modular multilevel dc transformer is presented in this article for the interconnection of network segments or lines with different voltage levels in HV or MV dc grids. It can realize bidirectional power regulation and bidirectional fault current limiting. Due to the nonisolated structure, only part of the power flowing though the autotransformer, which can reduce the requirements of autotransformers. The control strategy is simplified and the current stresses are decreased due to the employment of autotransformers. The optimal design methods of the dc transformer are proposed to reduce the costs and power losses according to the analysis results. Comparing to the classical dc transformers, such as FTF, HVdc-AT, and M2DC, this dc transformer has the advantages of lower costs, higher efficiency, lower current stresses, and smaller volume. Finally, the operation principle, control strategy, and theoretical analysis are verified by simulation results and experiment results. This article provides an alternative scheme for the selection of dc transformer in future dc grids, and the theoretical basis of the design methodology is provided.

References

[1] D. Elliott *et al.*, A comparison of AC and HVdc options for the connection of offshore wind generation in great britain," *IEEE Trans. Power Del.*, vol. 31, no. 2, pp. 798–809, Apr. 2016.

[2] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-Based HVdc power transmission systems: An overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.

[3] D. Jovcic, D. van Hertem, K. Linden, J. Taisne, and W. Grieshaber, "Feasibility of DC transmission networks," in *Proc. 2nd IEEE PES Int. Conf. Exhib. Innov. Smart Grid Technol.*, 2011, pp. 1–8.

[4] N. G. Hingorani, "Power electronics in electric utilities: Role of power electronics in future power systems," *Proc. IEEE*, vol. 76, no. 4, pp. 481–482, Apr. 1988.

[5] R. W. De Doncker, C. Meyer, R. U. Lenke, and F. Mura, "Power electronics for future utility applications," in *Proc. 7th Int. Conf. Power Electron. Drive Syst.*, 2007, pp. K-1–K-8.

[6] D. Jovcic and B. T. Ooi, "Developing DC transmission networks using DC transformers," *IEEE Trans. Power Del.*, vol. 25, no. 4, pp. 2535–2543, Oct. 2010.

[7] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. de Novaes, "Isolated DC/DC structure based on modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 89–98, Jan. 2015.

[8] S. H. Kung and G. J. Kish, "A modular multilevel HVdc buck-boost converter derived from its switched-mode counterpart," *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 82–92, Feb. 2018.

[9] X. Zhang, M. Tian, X. Xiang, J. Pereda, T. C. Green, and X. Yang, "Large step ratio input-series-output-parallel chain-link DC-DC converter," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4125–4136, May 2019.

[10] D. Jovcic and L. Zhang, "LCL DC/DC converter for DC grids," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2071–2079, Oct. 2013.

[11] C. Sun, X. Zhang, and X. Cai, "A step-up nonisolated modular multilevel DC-DC converter with self-voltage balancing and soft switching," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13017–13030, Dec. 2020.

[12] J. D. Páez, D. Frey, J. Maneiro, S. Bacha, and P. Dworakowski, "Overview of DC-DC converters dedicated to HVdc grids," *IEEE Trans. Power Del.*, vol. 34, no. 1, pp. 119–128, Feb. 2019.

[13] B. Zhao, Q. Song, J. Li, Q. Sun, and W. Liu, "Full-process operation, control, and experiments of modular high-frequency-link DC transformer based on dual active bridge for flexible MVDC distribution: A practical tutorial," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6751–6766, Sep. 2017.

[14] W. Chen, X. Ruan, H. Yan, and C. K. Tse, "DC/DC conversion systems consisting of multiple converter modules: Stability, control, and experimental verifications," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1463–1474, Jun. 2009.

[15] R. Giri, R. Ayyanar, and E. Ledezma, "Input-series and output-series connected modular DC-DC converters with active input voltage and output voltage sharing," in *Proc. 19th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2004, pp. 1751–1756.

[16] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[17] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, control, and applications of the modular multilevel converter: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 37–53, Jan. 2015.

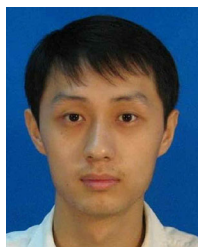
[18] I. A. Gowaid, G. P. Adam, B. W. Williams, A. M. Massoud, and S. Ahmed, "The transition arm multilevel converter—A concept for medium and high voltage DC-DC transformers," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2015, pp. 3099–3104,

[19] M. M. C. Merlin *et al.*, "The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability," *IEEE Trans. Power Del.*, vol. 29, no. 1, pp. 310–317, Feb. 2014.

[20] X. Xiang, X. Zhang, T. Luth, M. C. M. Merlin , and T. C. Green, "A compact modular multilevel DC-DC converter for high step-ratio MV and HV use," *IEEE Trans. Ind. Electron.*, vol. 65, no. 9, pp 7060–7071, Sep. 2018.
[21] S. Cui, J. Hu, and R. W. De Doncker, "Control and experiment of a TLC-MMC hybrid DC-DC converter for the interconnection of MVdc and HVdc grids," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2353–2362, Mar. 2020.
[22] S. Cui, N. Soltau, and Rik W. De Doncker, "A high step-up ratio soft-switching DC-DC converter for interconnection of MVDC and HVdc grids," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2986–3001, Apr. 2018.
[23] M. Ashraf, Y. Nazih, F. Alsokhiry, K. H. Ahmed, A. S. Abdel-Khalik, and Y. Al-Turki, "A new hybrid dual active bridge modular multilevel based DC-DC converter for HVdc networks," *IEEE Access*, vol. 9, pp. 62055–62073, 2021.
[24] N. Parida and A. Das, "Modular multilevel DC-DC power converter topology with intermediate medium frequency AC stage for HVdc tapping," *IEEE Trans. Power Electron.*, vol. 36, no. 3, pp. 2783–2792, Mar. 2021.
[25] A. Schn and M. M. Bakran, "A new HVdc-dc converter for the efficient connection of HVdc networks," in *Proc. PCIM Eur. Conf. Proc.*, May 2013, pp. 525–532.
[26] W. Lin, "DC-DC autotransformer with bidirectional DC fault isolating capability," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5400–5410, Aug. 2016.
[27] H. You and X. Cai, "A three-level modular DC/DC converter applied in high voltage DC grid," *IEEE Access*, vol. 6, pp. 25448–25462, 2018.
[28] S. Du, B. Wu, and N. R. Zargari, "A transformerless high-voltage DC-DC converter for DC grid interconnection, *IEEE Trans. Power Del.*, vol. 33, no. 1, pp. 282–290, Feb. 2018.
[29] S. Du, B. Wu, K. Tian, D. Xu, and N. R. Zargari, "A novel medium-voltage modular multilevel DC-DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, pp. 7939–7949, Dec. 2016.
[30] S. Du, B. Wu, D. Xu, and N. R. Zargari, "A transformerless bipolar multistring DC-DC converter based on series-connected modules," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1006–1017, Feb. 2017.
[31] S. Norrga, L. Ängquist, and A. Antonopoulos, "The polyphase cascaded-cell DC/DC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2013, pp. 4082–4088.
[32] G. J. Kish, M. Ranjram, and P. W. Lehn, "A modular multilevel DC/DC converter with fault blocking capability for HVdc interconnects," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 148–162, Jan. 2015.
[33] S. Dey and T. Bhattacharya, "A hybrid modular DC-DC converter topology for hybrid interlink in HVdc," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2021, pp. 1681–1687.
[34] B. Xia *et al.*, "A modular multilevel DC/DC converter interconnecting HVdc systems," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, 2017, pp. 4477–4481.
[35] J. A. Ferreira, "The multilevel modular DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 10, pp. 4460–4465, Oct. 2013.
[36] S. Dey and T. Bhattacharya, "A transformerless DC-DC modular multilevel converter for hybrid interconnections in HVdc," *IEEE Trans. Ind. Electron.*, vol. 68, no. 7, pp. 5527–5536, Jul. 2021.
[37] R. Vidal-Albalate *et al.*, "A modular multi-level DC-DC converter for HVdc grids," in *Proc. 42nd Annu. Conf. IEEE Ind. Electron. Soc.*, 2016, pp. 3141–3146.
[38] S. Du and B. Wu, "A transformerless bipolar modular multilevel DC-DC converter with wide voltage ratios, *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8312–8321, Nov. 2017.
[39] F. Zhang, W. Li, and G. Joós, "A transformerless hybrid modular multilevel DC-DC converter with DC fault ride-through capability," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2217–2226, Mar. 2019.
[40] F. Zhang, G. Joós, and W. Li, "A transformer-less modular multilevel DC-DC converter with DC fault blocking capability," in *Proc. IEEE Southern Power Electron. Conf.*, 2017, pp. 1–6.
[41] J. Yang, Z. He, H. Pang, and G. Tang, "The hybrid-cascaded DC-DC converters suitable for HVdc applications," *IEEE Trans. Power Electron.*, vol. 30, no. 10, pp. 5358–5363, Oct. 2015.
[42] S. Zhang *et al.*, "A monopolar symmetrical hybrid cascaded DC/DC converter for HVdc interconnections," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 248–262, Jan. 2021.
[43] B. Li, X. Zhao, S. Zhang, Q. Fu, S. Wang, and D. Xu, "A hybrid modular DC/DC converter for HVdc applications," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3377–3389, Apr. 2020.
[44] B. Li, X. Zhao, D. Cheng, S. Zhang, and D. Xu, "Novel hybrid DC/DC converter topology for HVdc interconnections," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5131–5146, Jun. 2019.
[45] S. Zhang, B. Li, X. Zhao, Y. Zhang, W. Wang, and D. Xu, "A transformerless hybrid modular step-up DC/DC converter for bipolar and symmetrical monopolar HVdc interconnection," in *Proc. 4th IEEE Workshop Electron. Grid*, 2019, pp. 1–6,
[46] Y. Quan, B. Li, X. Zhao, T. Wei, W. Li, and D. Xu, "A capacitive energy transfer DC/DC converter for HVdc applications," in *Proc. IEEE 4th Int. Elect. Energy Conf.*, 2021, pp. 1–6,
[47] X. Wang, J. Ke, X. Li, H. Xu, C. Ma, and J. Bai, "A modular multi-port DC/DC converter for DC grid," in *Proc. 4th Int. Conf. HVdc*, 2020, pp. 939–944,
[48] W. Lin, J. Wen, and S. Cheng, "Multiport DC-DC autotransformer for interconnecting multiple high-voltage DC systems at low cost," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6648–6660, Dec. 2015.
[49] F. Qin, T. Hao, F. Gao, T. Xu, D. Niu, and Z. Ma, "A multiport DC-DC modular multilevel converter for HVdc interconnection," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2020, pp. 520–524,
[50] Q. Tu and Z. Xu, "Impact of sampling frequency on harmonic distortion for modular multilevel converter," *IEEE Trans. Power Del.*, vol. 26, no. 1, pp. 298–306, Jan. 2011.
[51] H. Lee, J. Jung, and S. Sul, "A switching frequency reduction and a mitigation of voltage fluctuation of modular multilevel converter for HVdc," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 483–490,
[52] A. Schoen, A. Birkel, and M.-M. Bakran, "Modulation and losses of modular multilevel converters for HVdc applications," in *Proc. Int. Exhib. Conf. Power Electron.*, 2014, pp. 1–8.
[53] Y. Qiao, X. Zhang, X. Xiang, X. Yang, and T. C. Green, "Trapezoidal current modulation for bidirectional high-step-ratio modular DC-DC converters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3402–3415, Apr. 2020.

Yanan Ye (Student Member, IEEE) received the B.S. degree in electrical engineering from the Beijing Institute of Technology, Beijing, China, in 2018. He is currently working toward the Ph.D. degree in electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His research interests include the design and control of dc–dc converters for HVdc transmission.



Xiaotian Zhang (Senior Member, IEEE) was born in Xi'an, China, in 1983. He received the B.S. (Hons.) and M.S. degrees in electrical engineering from Jiaotong University, Xi'an, China, in 2006 and 2009, respectively, and the Ph.D. (Hons.) degree in electrical engineering and electronics from the University of Liverpool, Liverpool, U.K., in 2012.

Until 2015, he was with the Department of Electrical Engineering, Imperial College London, London, U.K. He is currently an Associate Professor with the Department of Electrical Engineering, Xi'an Jiaotong University, Xi'an. His research interests include control and design of HVdc converters.

Jiuyang Jin received the B.S. degree in electrical engineering in 2019 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the M.S. degree in electrical engineering.

His research interests include dc–dc converter in HVdc and dc power flow controller.

Yue Wang (Member, IEEE) was born in Liaoning, China, in 1972. He received the B.S. degree from Xi'an Jiaotong University, Xi'an, China, in 1994, the M.S. degree from Beijing Jiaotong University, Beijing, China, in 2000, and the Ph.D. degree from Xi'an Jiaotong University, in 2003, all in electrical engineering.

He is currently a Full Professor with the School of Electrical Engineering, Xi'an Jiaotong University. His research interests include wireless power transfer, active power filters, multilevel converters, and HVdc.

Xu Yang (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1994 and 1999, respectively.

Since 1999, he has been a member with the Faculty of School of Electrical Engineering, Xi'an Jiaotong University, where he is currently a Professor. From November 2004 to November 2005, he was with the Center of Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, Blacksburg, VA, USA, as a Visiting Scholar. He then came back to Xi'an Jiaotong University, and engaged in the teaching and research works in power electronics and industrial automation area. His research interests include soft switching topologies, pulsewidth modulation control techniques and power electronic integration, and packaging technologies.