An Integrated GaN Overcurrent Protection Circuit for Power HEMTs Using SenseHEMT

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***Abstract*—GaN power high-electron-mobility transistors (HEMTs), with their fast switching transients and poor overcurrent tolerance, require overcurrent protection (OCP) circuits that can respond in under 0.5 μs. Monolithically integrating digital and analog circuits with GaN power devices is enabled by recent advancements in high-voltage GaN integration platforms. Thus, integrated OCP designs can be used to reduce the protection response time, the area penalty, and the assembly complexity. This work presents the first fully integrated, senseHEMT-based GaN OCP integrated circuit (IC) with an adjustable current limit and programmable blanking time, suitable for a wide range of power applications. The IC, implemented on a 200-V GaN-on-Silicon-on-Insulator (GaN-on-SOI) process, contains a power HEMT with a senseHEMT for current sensing, a totem-pole-based gate driver, an analog comparator, and a set of logic circuits to enable high-speed closed-loop OCP. The fabricated design is tested in both a clamped switching setup and a 12–48 V boost converter. The minimum OCP response time is estimated to be 36 ns with $dI_D/dt \geq 30$ A/μs, one of the fastest amongst state-of-the-art OCP circuits for GaN.**

***Index Terms*—Current sensing, GaN, GaN-on-Silicon-on-Insulator (GaN-on-SOI), high-electron-mobility transistor (HEMT), monolithic integration, overcurrent (OC) protection (OCP), SenseHEMT.**

I. Introduction

THE LOW parasitic capacitances and the absence of reverse recovery in Gallium Nitride (GaN) high-electron-mobility transistors (HEMTs) have enabled MHz switching frequencies for high-voltage (HV) power converters, making power HEMTs the ideal choice for building converters with high efficiency and power density. For example, commercial GaN-based laptop chargers can achieve a 50% volume reduction compared to Si-based solutions [1]. The short-circuit (SC) withstand time (SCWT) of power devices is a critical consideration in HV and high-current applications. In the event of an SC fault, SCWT is the maximum time available to the converter control circuitry for taking corrective action before permanent device damage occurs. The SCWT of GaN power HEMTs is estimated to be around 0.5 μs [2], [3], which is about six times lower than that of SiC power devices [4], [5], and much shorter than the typical 10 μs of commercial Si offerings [5]. Aside from the immediate device destruction due to SC events, repetitive overcurrent (OC) stress above the rated value can cause the performance degradation in HEMTs, such as a rise in gate-leakage current, threshold voltage, and on-resistance [6].

TABLE I
Characteristics of GaN OC Scenarios

Scenario	1	2	3
Condition	Short-circuit	Overcurrent	Overcurrent
dI_D/dt **Limiter**	Parasitic inductance	Power-inductor saturation behaviour	Power inductor
OCP Speed Requirement	Fastest ($\leq 0.5\,\mu$s)	Fast ($\leq 2\,\mu$s)	Slower (variable)

Scenarios that cause OC events can be broadly categorized into the following three types, as summarized in Table I.

1) The power device is turned ON during a pre-existing SC, or an SC is formed during a normal conduction period. In both cases, the drain current of the device (I_D) increases rapidly with a high risk of device destruction [7]. The speed of the OC event is only limited by parasitic elements, requiring sub-μs OCP response.
2) The power inductor current exceeds its saturation current limit, resulting in significantly reduced inductance and causing a rapid increase in I_D. The available time for OCP response depends on the particular inductor, but is typically on the order of μs for MHz operation.
3) The power device is pushed outside its safe operating area by converter operation, such as start-up or load-step transients. The current slew rate in these cases is relatively slow, limited by the power inductor and requiring the slowest OCP.

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Clearly, a fast response time is critical for GaN OCP circuits, particularly during SC faults, which in turn requires fast detection of OC events.

Concurrently, advancements in GaN process technologies are enabling performance improvements in all aspects of GaN-based power conversion. As a result, the adoption of monolithic GaN half-bridge and drivers is making GaN converters more compact and efficient [8]–[10]. With reliability still being a concern in high-density GaN integrated circuits (ICs), the next step in GaN integration should be focused on sensing and power device protection [11].

This work proposes a monolithically integrated OCP design for GaN HEMTs utilizing an embedded senseHEMT, fabricated in a 200-V GaN-on-Silicon-on-Insulator (GaN-on-SOI) process. The design incorporates GaN-based comparison and logic circuits alongside the power HEMT and its driver to enable on-chip decision-making for a rapid OCP response. In addition, the integrated senseHEMT enables fast, highly accurate, bidirectional current sensing with minimal losses. To the best of the authors' knowledge, it is the first demonstration of a high-speed, closed-loop GaN OCP circuit using a senseHEMT, suitable for detecting all three OC scenarios.

The rest of this article is organized as follows. Section II introduces the state of the art of GaN OCP and current-sensing techniques. Section III discusses the capabilities and limitations of the current GaN integration platforms to highlight the key considerations in monolithic OCP designs. Section IV introduces the proposed OCP architecture, and Section V summarizes experimental characterization data from the various sub-blocks of the design. Section VI presents experimental results from prototypes utilizing the fabricated GaN IC. Finally, Section VII concludes this article.

II. Prior Art of GaN OCP and Current Sensing

The three commonly used OCP techniques for GaN power devices are inductive, series resistor, and $R_{\mathrm{DS,on}}$-based sensing. In addition, the correlation between the gate–source voltage (V_{GS}) and I_D of power HEMTs has also been used for detecting OC events. An OCP system using V_{GS}-sensing was demonstrated to respond in 70 ns to an SC fault with $dI_D/dt = 45$ A/μs [12]. Nonetheless, drawbacks of this method include a limited OC range (approximately 30–40 A) and poor detection accuracy due to variations in the V_{GS}-I_D relationship across operating conditions and device samples. Thus, the majority of the literature has focused on the three aforementioned sensing techniques, as described in the following.

Inductive current sensing uses a portion of the power-loop inductance to sense OC events, thereby reducing sensing losses. A series coil can be implemented using PCB traces, which minimizes its volume impact. When the power device experiences sufficient dI_D/dt, the induced voltage on the coil exceeds a preset threshold, triggering the OCP [13]–[15]. During SC events, this method can respond within 38 ns [13]. However, the lack of direct sensing of the current amplitude and the variability of the induced coil voltage limits the practicality of this method in other OC events.

Current sensing using a series resistor is widely used in Si-based converters and is easy to adapt for OCP. However, the added resistor in the current path increases ohmic losses and the power-loop inductance of the converter, limiting the operating frequency. In comparison, the on-resistance of the power device, $R_{\mathrm{DS,on}}$, can be used for current sensing, eliminating the additional resistor and associated losses. A common OCP application of this technique is known as "de-sat," which has become the most widely adopted technique for OCP in commercialized power HEMTs [16]–[19]. In this technique, when the on-state drain–source voltage, $V_{\mathrm{DS,on}}$, exceeds a preset reference ($V_{\mathrm{DS,ref}}$), OCP is activated. This method, also commonly used in IGBTs, is power-efficient and easy to realize, but has two major drawbacks. First, the $V_{\mathrm{DS,on}}$ of the device changes rapidly during the turn-ON and turn-OFF transients, necessitating fast, HV blocking elements for safe operation of the LV sensing circuitry, which can be challenging to implement. Second, the reference must be calibrated to account for the nonlinearity and variation of HEMT $R_{\mathrm{DS,on}}$ over process, temperature, and operating conditions [20]. Furthermore, GaN HEMTs suffer from $R_{\mathrm{DS,on}}$ degradation and V_{th} instability subject to the trapping effects under dynamic operating conditions [21], adding inaccuracy to the measurement. Thus, generating an accurate $V_{\mathrm{DS,ref}}$ reference becomes a critical task in this technique.

While $R_{\mathrm{DS,on}}$-based current sensing does not require monolithic integration, on-chip sensing, and protection circuits can be more effective in tracking power-device conditions while reducing design volume. An integrated de-sat OCP circuit proposed in [22] achieves a fast OC response. However, the blanking time of the design is fixed by an external RC filter, limiting the range of application of the circuit. Furthermore, Scenario 3 detection often requires knowing the current amplitude in the power device with relatively high accuracy, as shown in Table I. The de-sat scheme in [22] uses the logic threshold of inverters in the process as $V_{\mathrm{DS,ref}}$. Thus, the work in [22] is only suitable for protection in Scenarios 1 and 2. A fully integrated current sensing circuit was demonstrated in [23] with an embedded electrode between the source and the gate electrode [24]. Nevertheless, the response time of the design is over 50 μs [23], not suitable for SC protection in HV applications. An integrated partial $R_{\mathrm{DS,on}}$-sensing structure using the outermost fingers as the current sensors is proposed in [25]. The design enables both drain-side and source-side sensing, eliminating the need for an HV blocking circuit. The temperature dependency of $V_{\mathrm{DS,ref}}$ is compensated using an embedded temperature sensor. Using the embedded source-sensing finger in [25], the voltage across the source sensing finger is read using two cascaded two-stage GaN amplifiers, separately packaged and discretely implemented with the power device in [26]. However, the results presented in [25] and [26] are limited to open-loop current sensing.

In Si applications, an on-chip reference transistor, matched to the power device, can be used to generate a $V_{\mathrm{DS,ref}}$ that is compensated for the changing operating conditions using additional LV circuits [27]. The reference transistor should be close to the hotspot in the power transistor to achieve the best matching between the devices. This technique is similar in principle to the current-sharing MOSFET concept in Si, more commonly known as SenseFET current sensing. Using a discrete transistor identical to the GaN power device, current sensing is

accomplished in [28]. However, the current-ratio mismatch due to its temperature dependency necessitates additional transistor characterization and thermal analysis for accurate current sensing. Furthermore, a discrete implementation is more constrained in operating bandwidth with higher area penalty and process mismatch, incentivizing monolithic integration. An integrated senseHEMT in a 650 V GaN process was used for closed-loop current-mode control in [29]. Nevertheless, the GaN IC only contains the senseHEMT and a gate driver, with the remaining circuit built using a PCB.

III. Strengths and Drawbacks of GaN Integration

At present, Si bipolar-CMOS-DMOS (BCD) technologies represent the state-of-the-art in terms of monolithic power-management ICs (PMICs), with the ability to integrate high-performing digital and analog circuits alongside high- and medium-voltage power devices. The advantages of one-chip PMICs include near-zero interconnect parasitics, better area optimization, reduced component counts, fewer interconnection defects, and lower assembly complexity. These create strong incentives for monolithic integration of GaN protection circuits for the high performance.

Nonetheless, current GaN process technologies are roughly three decades behind Si BCD in maturity, posing several limitations in the design of complex GaN PMICs:

1) low-voltage (LV) devices with large feature sizes ($L_{\min} \geq 1\,\mu$s);
2) the lack of critical components, such as HV diodes, HEMTs at intermediate voltage ratings, and complementary p-type HEMTs;
3) poor matching between LV devices relative to their sizes;
4) limited accuracy in simulation models and shortage of process variation data; and
5) the absence of mature design-rule checks in process design kits.

These limitations create strong tradeoffs between the area usage, power consumption, speed, and robustness of GaN circuits. In particular, the performance of analog circuits is significantly impacted by the poor matching performance of current GaN technology. The measured I_D–V_{GS} curves of the two identical e-HEMTs in a resistor–transistor logic (RTL) NAND gate across four different ICs are shown in Fig. 1. The devices had a gate-length (L) of $1.3\,\mu$m and a width (W) of either $12\,\mu$m or $48\,\mu$m. The observed inter and intradie mismatch among the devices is significantly higher than what is commonly found in a $0.18-\mu$m Si BCD process, even at the larger device size. This places additional limits on the maximum performance of analog circuits. Given these constraints, current monolithic GaN technology is best suited for implementing sensing and protection circuits with no more than several hundred LV HEMTs [11], [30].

IV. IC Design

The proposed OCP IC architecture is shown in Fig. 2, which consists of the following:

1) a power e-HEMT, M_{power}, and integrated gate driver;
2) an embedded senseHEMT, M_{sense}, for current sensing;

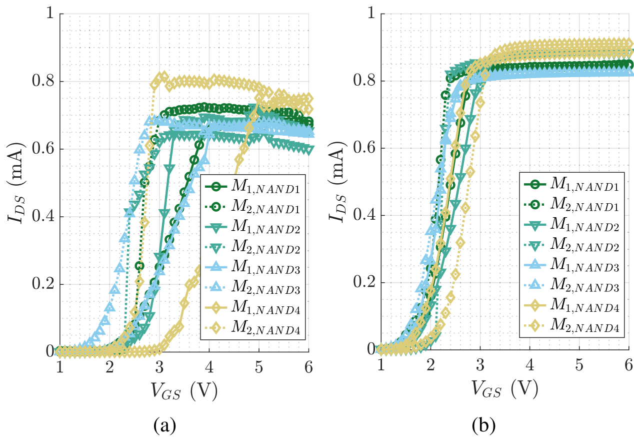


Fig. 1. $I_D - V_{\mathrm{GS}}$ measurements of adjacent HEMT devices, M_1 and M_2, having (a) $W = 12\,\mu$m and (b) $W = 48\,\mu$m, in two-input RTL NAND gates located on four different ICs.

4) a programmable blanking circuit to protect the comparator inputs from power-stage noise; and
5) OCP decision logic, based around an edge-sensitive RTL flip-flop with asynchronous reset.

M_{power} is normally controlled by the external gating signal, G_{dig}, which can be overridden by the OCP logic via the EN_{drv} signal when an OC event is detected. The OCP state can be reset using the external $\overline{\text{clear}}$ signal. Fig. 3 shows a simplified operating diagram of the OCP circuit. When I_{power} exceeds the set current limit I_{lim}, the comparator detects the OC event with some delay t_{comp}. The OCP decision logic reacts to the comparator output, $\mathrm{clk}_{\mathrm{DFF}}$ and disables the gate driver. M_{power} is turned OFF after the signal has propagated through the gate driver over t_{drv}. Thus, the overall OCP response time t_{OCP} is given by

$$\begin{aligned} t_{\mathrm{OCP}} &= t_{\mathrm{comp}} + t_{\mathrm{react}} \\ &= t_{\mathrm{comp}} + t_{\text{clk-to-Q}} + t_{\mathrm{AND}} + t_{\mathrm{drv}} \end{aligned} \tag{1}$$

where

t_{comp} = comparator delay;
t_{react} = reaction delay of the OCP circuit, from $\mathrm{clk}_{\mathrm{DFF}}$ to G;
t_{drv} = propagation delay of the driver;
$t_{\text{clk-to-Q}}$ = clock-to-Q delay of the flip-flop;
t_{AND} = propagation delay of the AND gate.

t_{OCP} is dominated by t_{comp} and t_{drv}, since $t_{\text{clk-to-Q}}$ and t_{AND} are small digital-circuit delays. t_{drv} is independently determined by optimal gate-driving of the power-HEMT, making t_{comp} the critical element in improving the speed of the OCP. For example, for a power HEMT operating at $f_{\mathrm{sw}} = 1$ MHz, with $D = 50\%$, $I_{D,\mathrm{avg}} = 5$A, and a 10% current-ripple, a 40-ns comparator delay contributes approximately $\Delta I_{\mathrm{comp}} = 100$ mA, or 2%, to the current detection error, ΔI_{ocp}. The sub-blocks of the OCP circuit are further described in the following.

A. Power HEMT and Integrated Gate Driver

The power device, M_{power} is a 200-V e-HEMT with a designed $R_{\mathrm{DS,on}}$ of 80 mΩ at $V_{\mathrm{GS}} = 6$ V. The integrated driver, shown in Fig. 4, consists of a dead-time generation block, three pre-driver

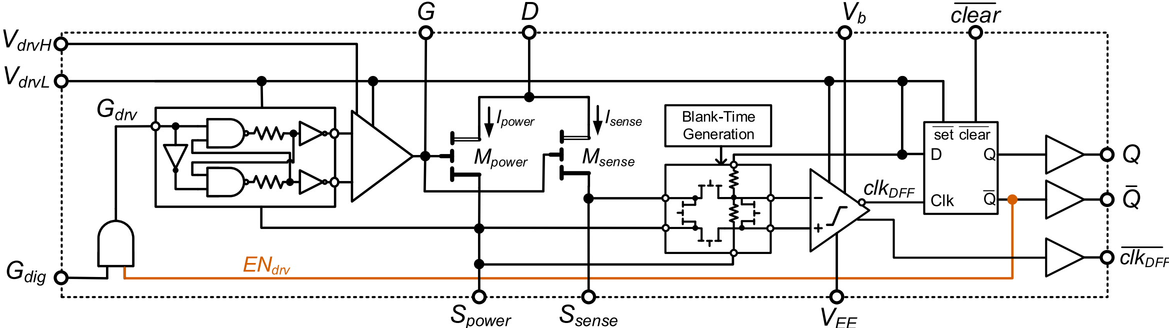


Fig. 2. Proposed GaN OC protection IC.

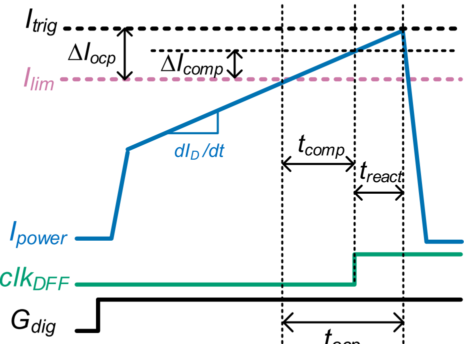


Fig. 3. OCP timing diagram, showing the current-sensing error caused by various delay components.

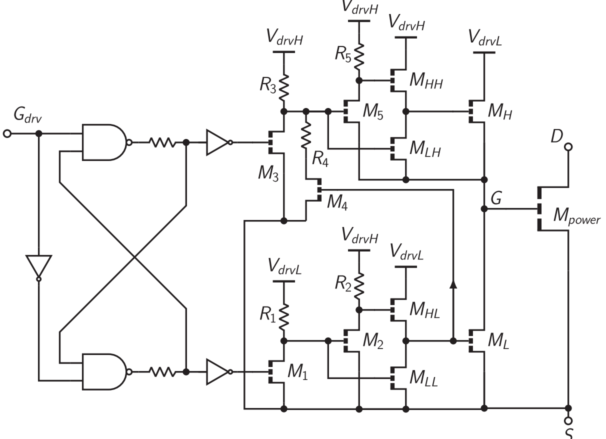


Fig. 4. Integrated gate driver.

complementary device, totem-pole structures are used in the two final stages to limit the static power consumption of the driver. Thus, two supply voltages, $V_{\mathrm{drv}L}$ and $V_{\mathrm{drv}H}$, are required for a full-swing gate drive [31].

B. SenseHEMT for Current Sensing

When M_{power} and the embedded senseHEMT, M_{sense}, have equal V_{GS} and V_{DS}, their current ratio is dependent primarily on their active-region geometries, which provides a stable and accurate way to determine I_{power} based on I_{sense}. With

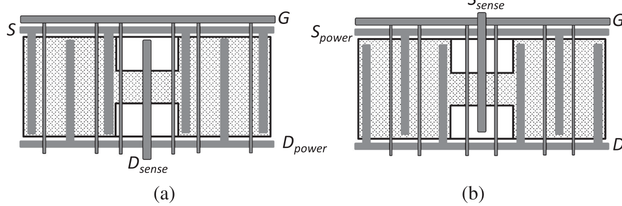


Fig. 5. Layout of the senseHEMT in (a) common-source configuration and (b) common-drain configuration.

$V_{\mathrm{GS,power}} = V_{\mathrm{GS,sense}}$, the ratio is defined by

$$K_{\mathrm{sense}} = \left.\frac{I_{\mathrm{power}}}{I_{\mathrm{sense}}}\right|_{V_{\mathrm{DS,power}}=V_{\mathrm{DS,sense}}} = \left.\frac{W_{\mathrm{power}}}{W_{\mathrm{sense}}}\right|_{L_{\mathrm{power}}=L_{\mathrm{sense}}}. \tag{2}$$

A senseHEMT can be used in one of two configurations: common-source or common-drain, as shown in Fig. 5. A common-source configuration guarantees $V_{\mathrm{GS,power}} = V_{\mathrm{GS,sense}}$, which significantly lessens the accuracy impact of the operating current levels on the current-sensing ratio. However, when used with a low-side power device, the LV sensing circuitry must interface with the HV D_{power} node, necessitating high-speed HV blocking switches at the interface as demonstrated in [29] and increasing design complexity. On the other hand, the common-drain configuration results in

$$V_{\mathrm{GS,sense}} = V_{\mathrm{GS,power}} - I_{\mathrm{power}}R_{\mathrm{DS,on}} + I_{\mathrm{sense}}R_{\mathrm{sense,on}} \tag{3}$$

which can cause minor changes to K_{sense} during operation as I_{power} (and possibly I_{sense}) changes, translating to small current-sensing errors. However, the sensing circuitry in the common-drain configuration only interfaces with LV nodes (with the senseHEMT itself acting as a blocking switch) when used with the low-side device, greatly simplifying the design. As such, this work uses a common-drain senseHEMT, as shown in Fig. 2.

In senseFET applications with lower speed requirements, an amplifier-based current-sensing scheme is commonly used, where the amplifier forces the source (or drain) voltage of M_{sense} to track the corresponding terminal on M_{power} by adjusting the senseFET drain current. This current is then compared to a reference to identify when it has crossed some predefined threshold [32]. This arrangement relaxes the offset and speed

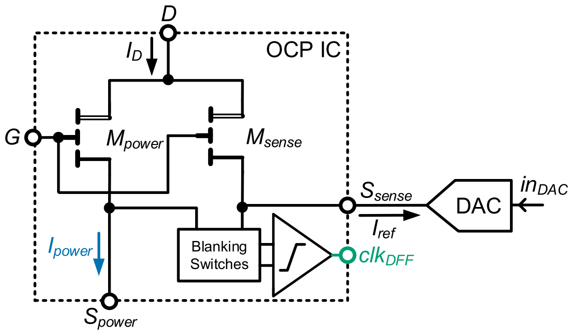


Fig. 6. Comparator-based senseHEMT current sensing.

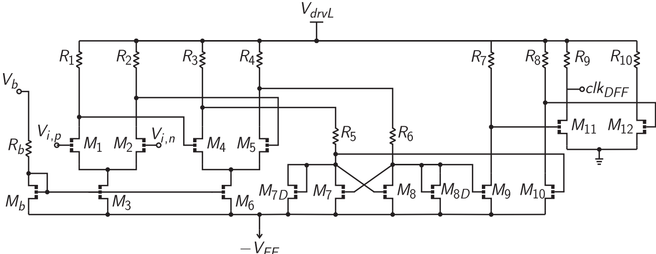


Fig. 7. Comparator used for $V_{S,\text{power}}$ and $V_{S,\text{sense}}$ comparison.

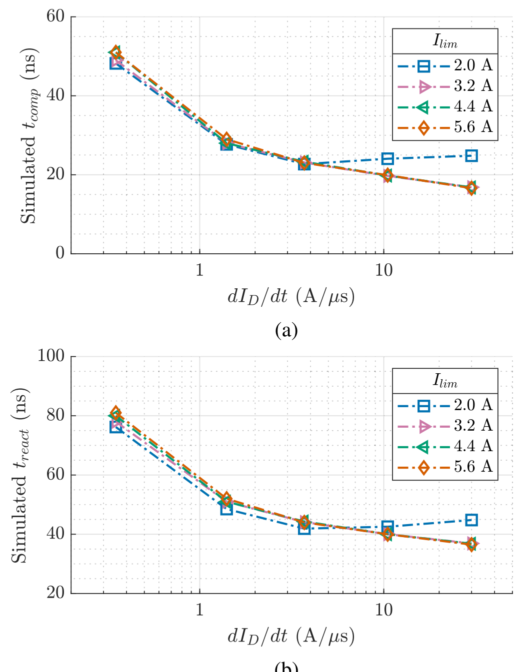


Fig. 8. Simulated (a) t_{comp} and (b) t_{react} at various I_{lim} and dI_D/dt.

requirements on the comparison circuitry. However, the amplifier is required to have high gain and bandwidth for accurate current sensing, which is challenging to implement in HV GaN. Alternatively, the comparison can be made directly at the source (or drain) of the power- and senseHEMTs using a high-speed, low-offset comparator, as shown in Fig. 6, with the external reference current I_{ref} injected directly through the senseHEMT [33]. As it is more practical to implement this comparator in GaN, this work employs the comparator-based sensing scheme. I_{ref} is generated by an external digital-to-analog converter (DAC), providing a versatile way to adjust the reference. The comparator identifies the instant when $V_{S,\text{power}} = V_{S,\text{sense}}$, which indicates $I_{\text{power}} = K_{\text{sense}} I_{\text{ref}}$.

C. Analog Comparator

The GaN-based analog comparator shown in Fig. 7 is used to compare the source voltages of M_{power} and M_{sense}. It consists of two gain stages (M_{1-2} and M_{4-5}) and a latching stage with positive feedback (M_{7-8} and M_{7D-8D}) to boost the comparator's gain. Since the common-mode voltage of the inputs are near the ground level of the circuit, and the GaN process used in this works lacks a complementary p-type device, the comparator uses a negative supply, $-V_{\text{EE}}$, to provide the input pair with sufficient overdrive voltage. The bias currents of the gain stages are controllable via the external voltage V_b for testing flexibility. M_{7-8} and M_{7D-8D} are made the same size, thereby reducing hysteresis effects and maximizing the speed of the comparator. A series of RTL inverters after the latching stage further amplify the comparator output to full scale and level-shift the signal to the digital ground of the IC by taking advantage of the negative-V_{GS} capability of the HEMTs.

Due to the lack of maturity in current GaN processes, it is challenging to reduce the comparator's power consumption while achieving reasonably low t_{comp}. The comparator design used in this work has a simulated current consumption of 2.6 mA at $V_{\text{drv}L} = 6$ V and $-V_{\text{EE}} = -3$ V. The simulated t_{comp} and t_{react} values using various current limits for the power HEMT, $I_{\text{lim}} = K_{\text{sense}} I_{\text{ref}}$, are shown in Fig. 8. The delays are constant for a given current slew rate, dI_D/dt, regardless of the actual current limit. Meanwhile, higher dI_D/dt accelerates the voltage transitions on the comparator inputs, leading to a reduced t_{comp}. Similarly, t_{drv} is reduced when operating with higher dI_D/dt, reducing t_{react}.

D. Programmable Blanking Circuit

While the source nodes (S_{power} and S_{sense}) mostly remain at around ground-level, HV switching noise from the power-stage can cause false OC detection, or gate overvoltage on the comparator input pair (since $V_{\text{GS,max}} = 7$ V). To prevent this, a network of five LV blanking switches, as shown in Fig. 9, is added between the source nodes and the comparator inputs ($V_{i,p}$ and $V_{i,n}$). These switches prevent the power-stage noise from propagating to the comparator immediately after a switching event for a predetermined blanking time t_{blank}. They are controlled by a programmable blanking-time generation block that employs a bank of binary-weighted capacitors for 3-bit control over t_{blank}.

When the power HEMT is OFF ($G_{\text{dig}} = \text{LOW}$), switches M_{B1} and M_{B4} are also OFF, keeping the comparator isolated from the power-stage, while M_{B5} shorts the sources for safety considerations. At the same time, switches M_{B2} and M_{B3} connect the comparator inputs to fixed voltages generated by a resistive

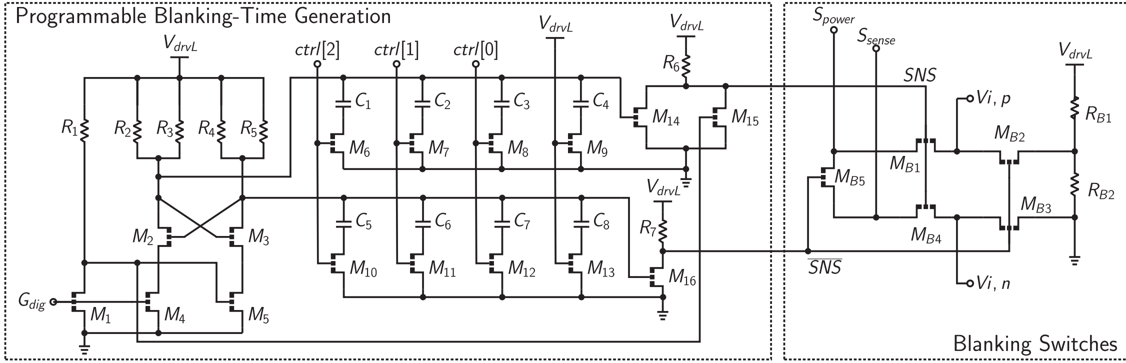


Fig. 9. Programmable comparator-input blanking circuit.

ladder. Once G_{dig} transitions high, $M_{B2,3,5}$ are turned OFF in preparation for normal operation. After the programmed t_{blank} duration has passed, M_{B1} and M_{B4} are turned ON to connect the source nodes to the comparator inputs, allowing OC detection. Since the optimal t_{blank} varies across operating conditions, the blanking-time generation circuit incorporates a 3-bit control signal, ctrl[2:0], for dynamic adjustments of t_{blank}. The designed circuit can produce a t_{blank} value between 2 and 31 ns relative to G_{dig}. Since t_{blank} dictates the minimum comparator response time, selecting the optimal value is critical for balancing the robustness of the OCP response against reaction time, especially in events like Scenario 1, when fault currents have a dI_{DS}/dt that is not constrained by the inductor.

E. OCP Decision Logic

Once the comparator detects an OC event, a set of logic circuits latches the comparator output and keeps the power-HEMT driver disabled until the OCP state is externally reset. The edge-triggered flip-flop shown in Fig. 2, based on the design reported in [11], is activated by the toggling comparator output, clk_{DFF}, which then lowers the EN_{drv} signal, forcing the power HEMT to shut OFF and blocking the external gating signal via an AND gate. The circuit remains in this state until the flip-flop is reset via the $\overline{\text{clear}}$ signal.

F. Simulated Operation

The simulated waveforms of the OCP design are shown in Fig. 10. At the start of the simulation (not shown), the system is reset to the operational state and M_{power} is turned ON with an inductive load, with the OC limit set to $I_{\text{lim}} = 4.4$ A. As the HEMT current ramps up, it exceeds the limit at t_1, as evidenced by $V_{i,p} (\approx V_{S,\text{power}})$ exceeding $V_{i,n} (\approx V_{S,\text{sense}})$. The comparator responds accordingly at t_2 by raising clk_{DFF} and triggering the flip-flop, which leads to the power HEMT turning OFF at t_3.

The circuit operating under an SC (Scenario 1) with $I_{\text{lim}} = 5.6$ A and two different t_{blank} settings (2 ns and 7 ns) is shown in Fig. 11. G_{dig} is set high at $t = 0$ ns with the HEMT drain shorted to 200 V. Due to driver delay, M_{power} turns ON at $t = t_{\text{drv}} = 12$ ns. The comparator (and logic) reacts in approximately 14 ns after the end of the blanking period. This is significantly shorter than the delay in Fig. 10 as a result the higher dI_D/dt in a SC

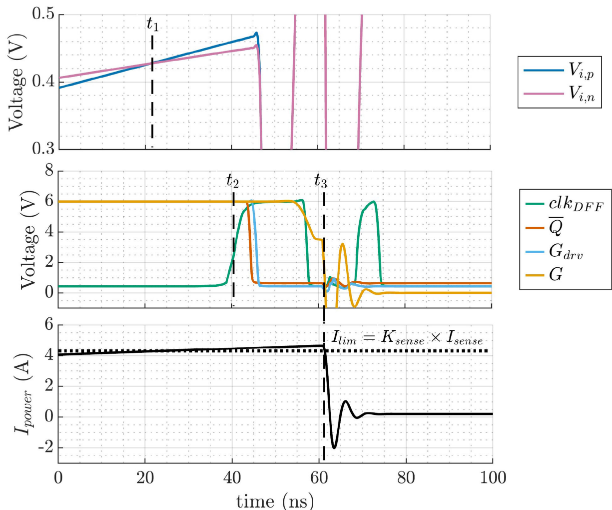


Fig. 10. Simulated waveforms of the OCP circuit in Scenario 3 with $I_{\text{lim}} = 4.4$ A, showing an OC event at t_1 being detected at t_2, causing the power HEMT to shut down at t_3. The short comparator output transition at $t \approx 70$ ns is a result of the source-voltage-ringing from the device turn-OFF.

event. Since the fault occurs immediately upon device activation, t_{blank} is directly added to t_{ocp}. Consequently, the fastest simulated SC protection time, $t_{\text{scp,min}} = 28$ ns, is obtained for the lowest t_{blank} setting (2 ns). Since a nonzero t_{blank} is necessary to avoid false triggering the OCP during turn-ON transients, this clearly shows the tradeoff between robustness and speed of OCP. As the minimum t_{blank} requirement changes with converter operating conditions, this also demonstrates the importance of dynamic t_{blank} programmability for optimizing t_{ocp}.

V. Experimental Circuit Characterization

The proposed GaN OCP design was fabricated in a 200-V GaN-on-SOI process, as shown in Fig. 12. The die, packaged in a 60-pin QFN, measures approximately 4 mm $\times$ 4 mm.

A. Power HEMT and SenseHEMT

The characterization results of $R_{\text{DS,on}}$ and K_{sense} are shown in Fig. 13. The measured $R_{\text{DS,on}}$-variation of the fabricated power HEMT over temperature is approximately 50% lower

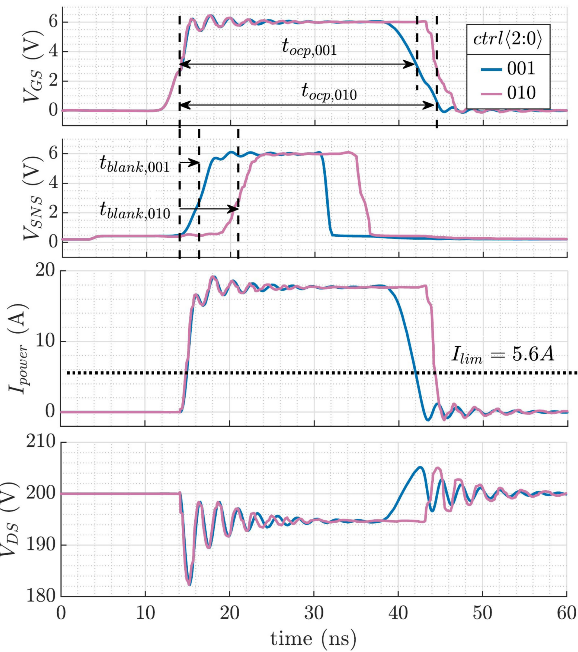


Fig. 11. Simulated waveforms of the OCP circuit in Scenario 1 (SC) with $t_{\text{blank},001} = 2$ ns and $t_{\text{blank},010} = 7$ ns, resulting in $t_{\text{ocp},001} = 28$ ns and $t_{\text{ocp},010} = 31$ ns, respectively. t_{blank} directly impacts t_{OCP} in this scenario.

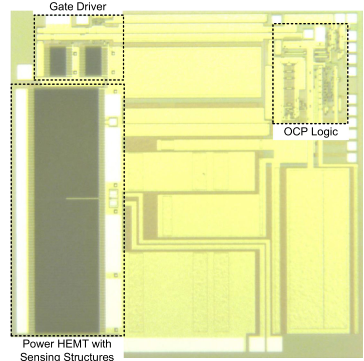


Fig. 12. OC protection IC.

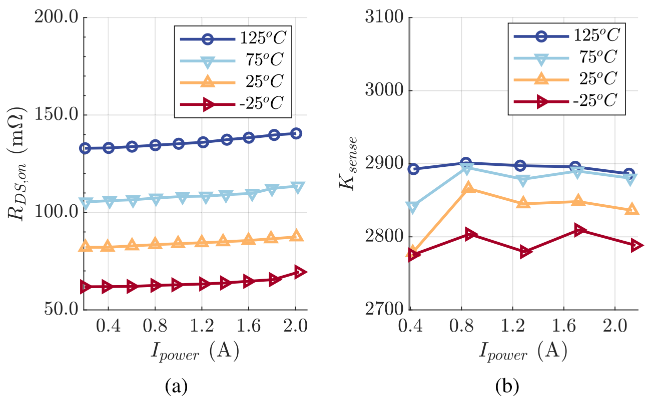


Fig. 13. (a) Measured on-resistance, $R_{\text{DS,on}}$, of the power HEMT in the OCP design, and (b) current-sensing ratio, K_{sense}, across various currents and ambient temperatures [11].

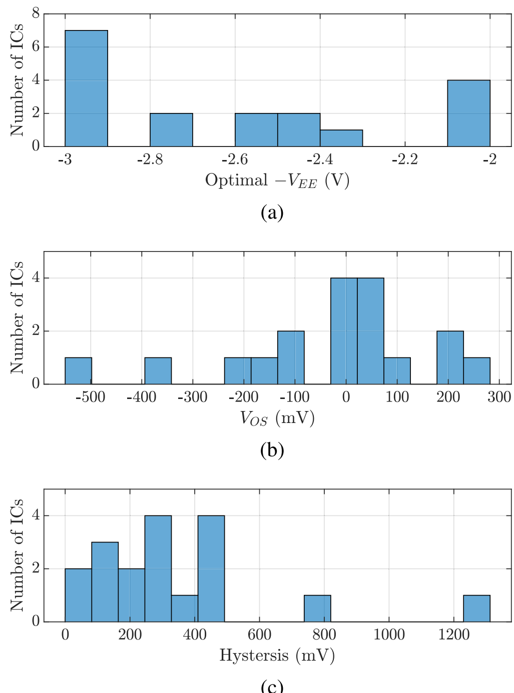


Fig. 14. Measured distributions of (a) optimal $-V_{\text{EE}}$, (b) offset voltage, and (c) hysteresis of comparator samples on 18 different dies.

than commercially available Si power MOSFETS, demonstrating the GaN's superior thermal performance. The senseHEMT was implemented as a partial finger embedded at the centre of the power HEMT to achieve stable matching across operating conditions. To minimize sensing losses while maintaining good matching, the senseHEMT was designed to have $K_{\text{sense}} \approx 2800$. K_{sense} was measured according to (2) over a range of operating currents and temperatures, as shown in Fig. 13(b). The measured values vary by less than 1% across I_{DS} and below 2% over temperature, demonstrating the effectiveness of the senseHEMT structure for accurate current sensing.

B. Comparator

The offset voltage (V_{OS}) and hysteresis of the comparator, which impact the accuracy of the OC detection, was characterized to calibrate the external current reference to the senseHEMT. As shown in Fig. 1, the small- to medium-sized LV HEMTs in the chosen GaN process exhibit a great degree of mismatch, impacting successful operation of the comparator. The offset and hysteresis of the comparator are dependent on $-V_{\text{EE}}$, as observed from the experimental results. For the comparison across samples, the optimal $-V_{\text{EE}}$ was tuned to obtain stable operation with minimal hysteresis for each comparator. The resulting $-V_{\text{EE}}$ distribution, varying between -2 and -3 V, is shown in Fig. 14(a). With the optimal $-V_{\text{EE}}$ applied, $V_{i,n}$ was ramped up and down while $V_{i,p}$, connected to S_{power}, was kept at 0 V to determine the comparator's offset and hysteresis. This sequence was repeated for 18 fabricated ICs, with the results shown in Fig. 14. As predicted in Section III, these GaN-based

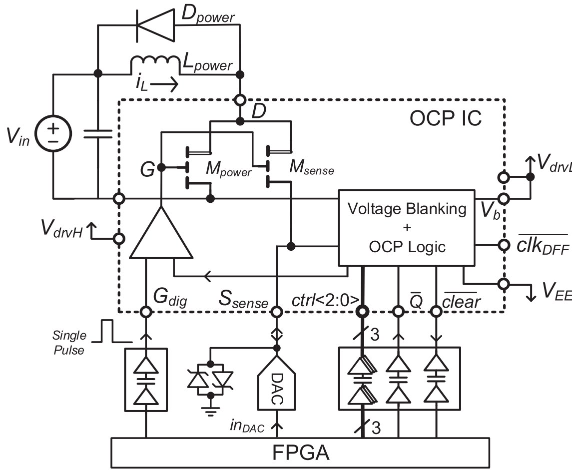


Fig. 15. Single-Pulse CIS circuit using the proposed OCP IC.

comparators are less precise than their Si counterparts. For this work, the current reference in the senseHEMT was digitally programmed to compensate for the comparator hysteresis and offset. A $-V_{\mathrm{EE}}$ of -3 V was used for subsequent experiments.

VI. Experimental Results From OCP Operation

The OCP functionality of the IC was tested in the following two stages:

1) the closed-loop OCP response time versus dI_{DS}/dt was verified using single-pulse clamped inductive switching (CIS) tests;
2) the OCP circuit's dynamic behavior under switching operations was demonstrated using the power HEMT as a protected low-side switch in a boost converter.

For all tests, V_b was connected to $V_{\mathrm{drv}L} = 6$ V, with $-V_{\mathrm{EE}} = -3$ V. Zener diodes were placed on S_{sense} to ensure that LV circuits are protected from overvoltage events.

A. Single-Pulse CIS

In the single-pulse switching test, as shown in Fig. 15, the current in M_{power} ramped up until I_{power} exceeded the current limit set using the DAC, $I_{\lim} = K_{\mathrm{sense}} I_{\mathrm{ref}} = K_{\mathrm{sense}} I_{\mathrm{DAC}}$. The current slew-rate, dI_D/dt, is set by the value of the inductor (L_{power}). D_{power} is realized with a 600-V SiC diode with fast recovery [34]. Measured waveforms for a CIS test with $L_{\mathrm{power}} = 8.2\,\mu$H $(dI_D/dt \approx 3.7\,\mathrm{A}\mu\mathrm{s})$ and $I_{\lim} = 4.4$ A are shown in Fig. 16(a). The IC under test used $-V_{\mathrm{EE}} = -3$ V. The voltage on S_{sense} at the OC trigger point indicates $V_{\mathrm{OS}} = -160$ mV for this sample. Once triggered, M_{power} is turned OFF by the OCP logic, even though G_{dig} from the field programmable gate arrays (FPGA) remains high. The measured reaction delay, t_{react}, in this test was 33 ns, as shown in Fig. 16(b).

The CIS test was repeated with different dI_D/dt and $I_{\lim}$ values to observe the delay performance of the OCP design, as shown in Fig. 17. A correlation between t_{react} and dI_D/dt is observed, as predicted by simulation. Since t_{react} likely dominated by the driver delay (t_{drv}), the observed trend is likely caused by the influence of dI_D/dt on t_{drv}. In addition, the effect of

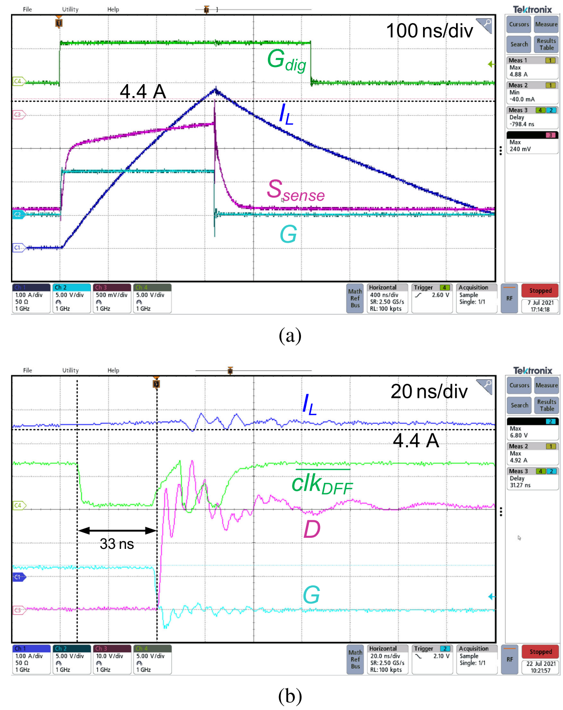


Fig. 16. (a) Measured waveforms from the single-pulse CIS test, with $L_{\mathrm{power}} = 8.2\,\mu$H and $I_{\lim} = 4.4$ A. (b) Zoomed-in waveforms showing the OCP reaction.

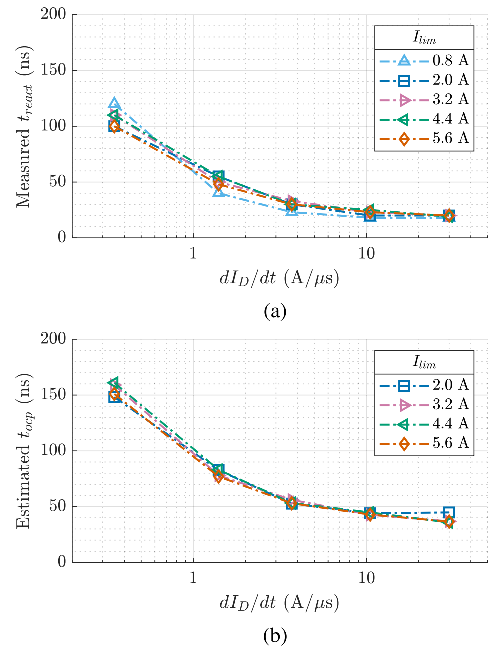
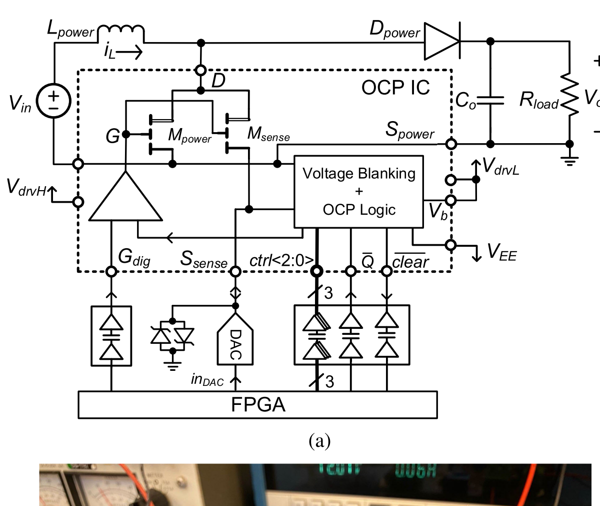


Fig. 17. (a) Experimental measurements of t_{react} and (b) estimates of t_{ocp} using experimental t_{react} and simulated t_{comp} across $I_{\lim}$ and dI_D/dt. Reported $I_{\lim}$ values include the adjustments for V_{OS} compensation.

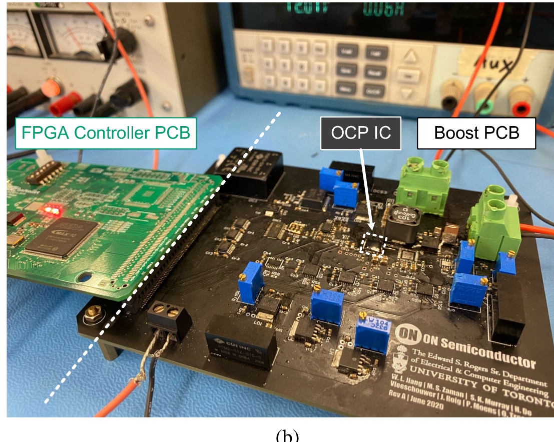
I_{power} on t_{react} is minimal, as expected. The experimental values display the same trend as simulations, with t_{react} measurements matching closely for $dI_D/dt > 3$ A/μs. t_{react} at lower dI_D/dt is measured to be approximately 20–30 ns longer than simulated values. As SC faults are associated with high dI_D/dt and for OC

TABLE II
STATE-OF-THE-ART OCP DESIGNS FOR GAN POWER DEVICES

Parameters	WiPDA 2017 [12]	EPE 2020 [13]	TPEL 2021 [18]	TPEL 2020 [35]	ISPSD 2019 [22]	JESTPE 2020 [23]	**This work**
Device Rating	Not stated	200 V	650 V	650 V	200 V	Not stated	**200 V**
Monolithic Integration	No	No	No	No	Yes	Yes	**Yes**
Detection Method	V_{GS} sensing	Inductive sensing	$R_{DS,on}$-based (De-sat)	$R_{DS,on}$-based (De-sat)	$R_{DS,on}$-based (De-sat)	$R_{DS,on}$-based	**SenseHEMT**
Current Limit	Adjustable (limited)	N/A (SC only)	Adjustable	Bandpass: fixed De-sat: adjustable	Fixed	Adjustable	**Adjustable**
Bi-Directional Sensing	No	Yes	No	No	No	Yes	**Yes**
Temperature Compensated	No	Yes	No	No	No	Yes	**Yes**
Fastest Reported Response Time	70 ns	38 ns	125 ns	Bandpass: 36 ns De-sat: 2 μs	40 ns	55 μs	**36 ns**

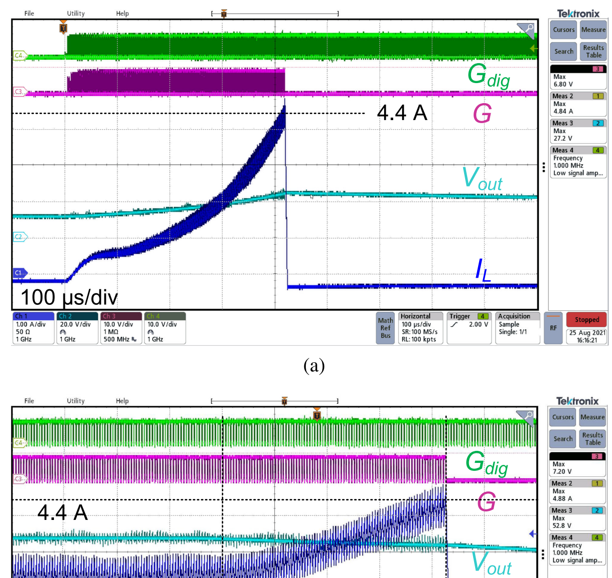


(a)



(b)

Fig. 18. (a) Boost converter test setup, which was (b) implemented on a PCB and controlled using an FPGA.



(a)

(b)

Fig. 19. OCP operation in a 12–48 V boost converter operating in open loop, with a current limit of 4.4 A. Results show OCP being activated during (a) converter start-up and (b) load-step transient from 0.6 to 2 A, with I_L stepping from 2.4 A.

Scenarios 2 and 3, the additional delay translates to a smaller ΔI_{ocp}, the longer t_{react} measured at low dI_D/dt is less critical for the device protection.

The overall OCP response time t_{OCP} is estimated by adding the simulated t_{comp} from Fig. 8(a) to the measured t_{react}. The resulting values are shown in Fig. 17(b), ranging from 36 to 160 ns for dI_D/dt values between 0.35 A/μs and 30 A/μs. Compared to state-of-the-art OCP designs for GaN HEMTs, summarized in Table II, the proposed circuit uniquely enables a high-speed, compact protection solution with adjustable current limit, suitable for bidirectional current limiting.

B. Boost Converter Operation

The power HEMT with the fabricated OCP circuit was used as the low-side switch in an asynchronous, 12–48 V, 1-MHz boost converter, with the digital inputs controlled by an FPGA via isolated drivers. The experimental test setup is shown in Fig. 18.

The converter was operated in open loop, with the OCP captured in Fig. 19. A blanking-time setting of ctrl[2:0] $= 010$, which corresponds to $t_{\text{blank}} \approx 7$ ns, and a current limit of $I_{\text{lim}} = 4.4$ A were used. The start-up transient of the converter is shown in Fig. 19(a). Although the HEMT gating signal was

programmed to gradually increase the duty cycle, the inductor current experienced a sharp increase beyond I_{lim}. Consequently, the power HEMT was automatically disabled by the OCP circuit once I_{power} exceeded the preset limit.

Fig. 19(b) shows OCP being triggered by a load-step transient. The converter was operating in steady-state prior to t_a, when the load current was stepped up from 0.6 to 2 A. As I_L ramped up toward the required 8 A value in response, the HEMT current exceeded the preset 4.4 A limit, resulting in device and converter shut-down at t_b.

VII. Conclusion

This work demonstrates a monolithically integrated OCP circuit in a 200-V GaN-on-SOI process, with adjustable current limit and bidirectional capability. The proposed design uses a senseHEMT for near-lossless current sensing, a comparator with programmable blanking time for robust OC detection, and a set of digital-logic circuits for fast closed-loop protection. The comparator blanking time is programmable to enable flexible and dynamic optimization across operating conditions. The design is experimentally tested using both single-pulse CIS and a 12–48 V boost converter, demonstrating ultrafast protection over a diverse range of conditions. The OCP response time, estimated from the measured results, is below 100 ns for devices operating with $dI_D/dt > 1$ A/μs, and can be as low as 36 ns at 30 A/μs. Despite the limitations of current GaN technology, such as large feature sizes, poor matching, and limited models, this design has demonstrated high-speed current sensing, on-chip closed-loop current protection, and the feasibility of fully integrated current-mode control in HV GaN converters.

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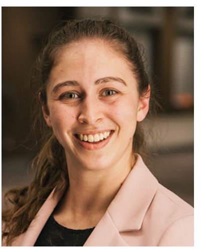

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