An Integrated Driver With Bang-Bang Dead-Time Control and Charge Sharing Bootstrap Circuit for GaN Synchronous Buck Converter

Ching-Jan Chen, *Senior Member, IEEE*, Pin-Ying Wang, Sheng-Teng Li, Yen-Ming Chen, and Yu-Cheng Chang

***Abstract*—This article proposes a high-frequency integrated gate driver for gallium nitride (GaN) synchronous buck converter. The proposed adaptive bang-bang dead-time control minimizes dead-time at any load condition. Thus, it mitigates the excessive power loss caused by GaN device reverse conduction in high-frequency applications. The proposed charge sharing bootstrap circuit ensures sufficient gate overdrive voltage with reduced chip area. Fabricated in a TSMC 0.25-μm BCD process, the driver integrated circuit enabled GaN-based buck converter to operate at 10 MHz switching frequency with minimal dead-time to as low as 0.4 ns under light load and heavy load conditions. Compared with fixed dead-time control, the proposed work improves around 5% efficiency under heavy load condition. The fully integrated bootstrap circuit with 100 and 60 pF (HV) capacitor obtained the lower than 0.6 V driving voltage drop with only 45% capacitance and around half of the voltage drop compared with a conventional bootstrap circuit. Besides, the proposed driver successfully tackled the parasitic ringing and dead-time overcharging issues in the GaN converter.**

***Index Terms*—Bang-bang control, bootstrap circuit, buck converter, dead-time, driver, gallium nitride (GaN).**

I. Introduction

GALLIUM nitride (GaN) synchronous buck converter features high efficiency and high power density than silicon counterpart. GaN is a high electron mobility transistor with low on-resistance, low parasitic capacitances, and high breakdown voltage characteristics [1], [2]. Compared to silicon, a GaN device allows more efficient power conversion at high switching frequency operation [3]–[5]. Thus, GaN is suitable for the space-constrained and fast response required applications such as fifth-generation (5G) telecom power and industrial power supplies. Fig. 1 shows the circuit diagram of the widely used synchronous rectifier buck converter, where high side switch Q_H and low side switch Q_L are discrete GaN devices.

Manuscript received April 26, 2021; revised August 19, 2021 and January 3, 2022; accepted March 2, 2022. Date of publication March 16, 2022; date of current version April 28, 2022. This work was supported in part by the National Chung-Shan Institute of Science and Technology, and in part by the Ministry of Science and Technology, Taiwan. Recommended for publication by Associate Editor J. Wang. *(Corresponding author: Ching-Jan Chen.)*

The authors are with the Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan (e-mail: chenjim@ntu.edu.tw; r07921028@ntu.edu.tw; r06921071@ntu.edu.tw; jerry140147@gmail.com; r09943129@ntu.edu.tw).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3159717.

Digital Object Identifier 10.1109/TPEL.2022.3159717

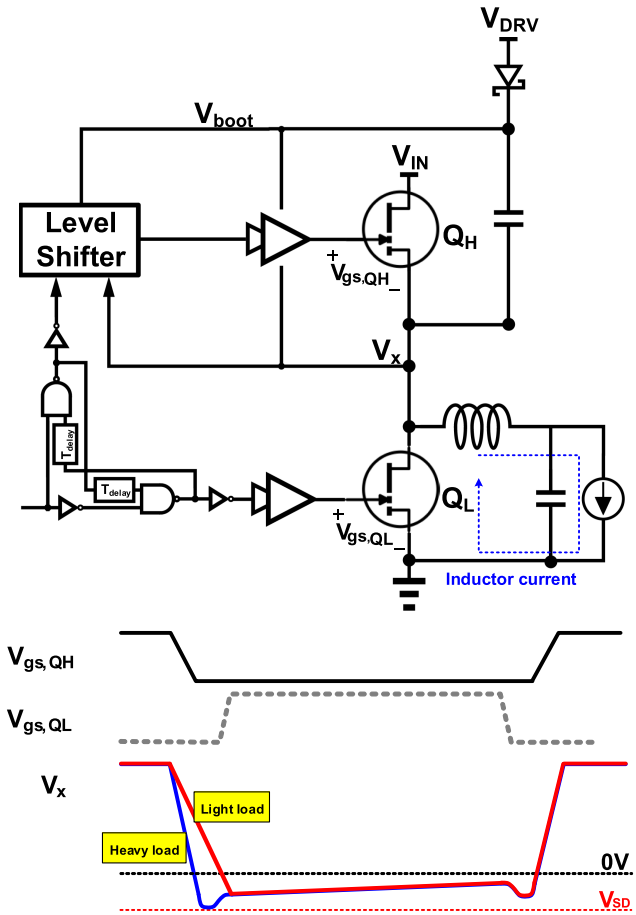


Fig. 1. GaN synchronous buck converter with fixed dead-time control.

Minimizing dead-time can improve the efficiency of a high-frequency GaN synchronous converter. High-to-low dead-time is the period between the falling edge of switching node voltage V_x and the rising edge of low side switch $V_{gs,QL}$. A fixed dead-time control [6]–[10] is often used to avoid high side switch and low side switch shoot-through or hard-switching. However, the high-to-low dead-time would be larger when the load increase, as shown in Fig. 1. It is because inductor current determines V_x slew rate during high-to-low dead-time. The extended dead-time at heavy load would cause additional reverse conduction loss, especially severe for GaN power devices. GaN device does not have a body diode. As shown in Fig. 2, the GaN device has a

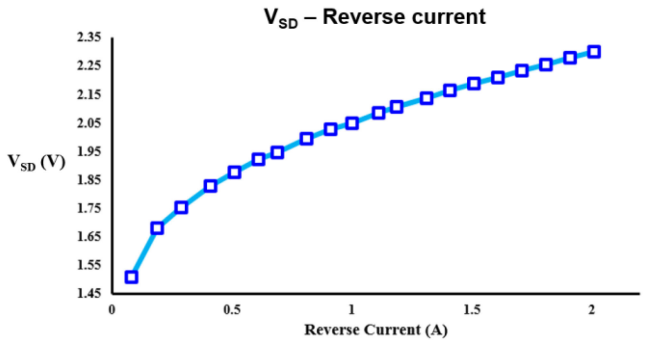


Fig. 2. Reverse current versus source drain voltage of GaN device EPC8009.

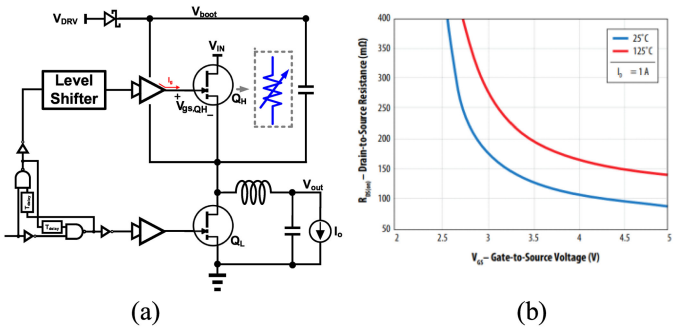


Fig. 3. Conventional buck converter with bootstrap circuit (a) schematic (b) relationship between gate-source voltage and on-resistance [11].

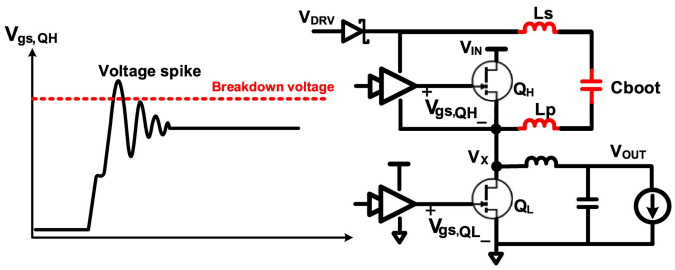


Fig. 4. Gate driving issue with the off-chip capacitor.

larger reversed bias voltage drop than the Silicon device (typical 0.7 V), and the voltage drop increases as the output load increases [11]. Thus, dead-time needs to be minimized especially for high-frequency operation.

Besides, a GaN device with enough gate overdrive voltage is important for achieving high efficiency. Since the GaN device only has the n-type structure, a bootstrap circuit must provide the suitable gate overdrive voltage for the high side switch. The gate-source voltage $V_{gs,QH}$ is related to the on-resistance of the GaN device Q_H, which is shown in Fig. 3. As V_{gs} increases, the on-resistance of the GaN device would be reduced. Therefore, maintaining the suitable V_{gs} value is one of the main issues for GaN driver applications. A large bootstrap capacitor is needed to get the lower voltage drop on the gate-source voltage. A general method is choosing the off-chip capacitor since the cost of the chip area would be decreased. Nevertheless, using the off-chip capacitor would have a problem in high-frequency applications, as shown in Fig. 4. The extra parasitic inductance of bonding wire and printed circuit board (PCB) due to the off-chip capacitor would cause a larger voltage spike on V_{gs}. Therefore, the on-chip capacitor is required to avoid possible gate breakdown of the enhancement-mode (E-mode) GaN device. Therefore, this work focused on the two issues of driving E-mode GaN device, first, reverse conduction loss caused by the high-to-low dead-time; and second, GaN gate voltage drop due to the small on-chip bootstrap capacitor.

Literature for GaN-based converter with adaptive dead-time control or charge sharing bootstrap is limited. The work in [6]–[10] and [12] do not implement adaptive dead-time control. The dead-time controls in [13]–[16] are applied to the monolithic Si-based converter, which does not need to manage the ringing in V_x and V_{gs} waveforms. The adaptive control in [17] is not illustrated clear, and the dead-time varies with loading from 0.9 ns to 3.9 ns for the load range between 0.1 and 1.2 A. Thus, minimized dead-time is not achieved. In [18] and [19], dead-time optimization based on switching model is proposed. In [20], the charge sharing technique drives the on-chip NMOS transistor output stage, which is not for discrete GaN half-bridge switches.

This work proposes an adaptive dead-time control by bang-bang control loop to reduce reverse conduction loss effectively. The proposed control minimized the high-to-low dead-time by locking switching node (V_x) and low side $V_{gs,QL}$ waveform. Specific sensing for dead-time control is also designed to avoid the voltage spike issue in high-frequency GaN converter. Compared to [13], a pair of inverters are replaced by a comparator to sense more accurate voltage because of a lower threshold voltage of the GaN device. This work also proposes the charge sharing bootstrap circuit to drive the discrete GaN device in the synchronous converter and ensure sufficient gate overdrive voltage with reduced chip area. Using the HV capacitor and the input voltage, the GaN device would be turned ON with a smaller Vgs voltage drop using a smaller on-chip capacitor area. The proposed circuit also solved the overcharge issue on the bootstrap capacitor during dead-time in GaN applications. The implemented synchronous buck converter with 12 V input and 10 MHz switching frequency suits 5G telecom power [21]–[23], and industrial power supplies for real-time microcontrollers [24], [25]. Based on Fig. 2, the buck converter suffers more dead-time loss as output current increases. That means the proposed dead-time control can be applied to high output current applications such as server power in the future.

II. System Overview

The system architecture of the GaN-based synchronous buck converter with the proposed gate driver is illustrated in Fig. 5. The gate driver IC has two main blocks: bang-bang dead-time control and the bootstrap circuit with charge sharing. The bang-bang dead-time control gate driver, which includes comparator sensing, delay time modulator, and dead-time generator, can reduce the reverse conduction loss by minimizing the high-to-low dead-time. Two enhancement-mode EPC8009 GaN FETs Q_H and Q_L are employed as power switches. This GaN device is chosen because it is the most suitable one in voltage level

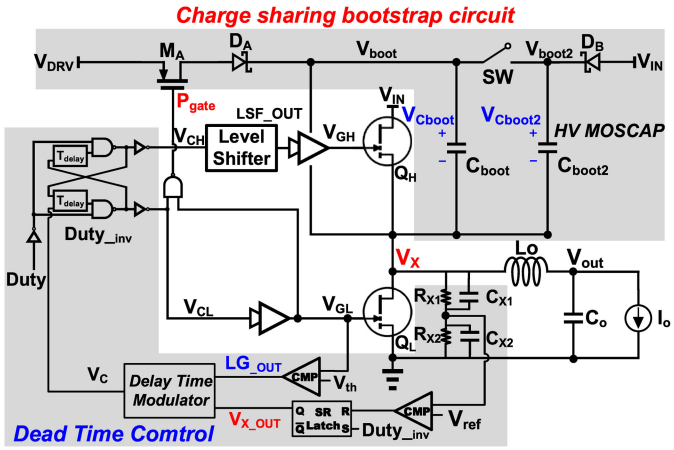


Fig. 5. System architecture of the proposed gate driver IC.

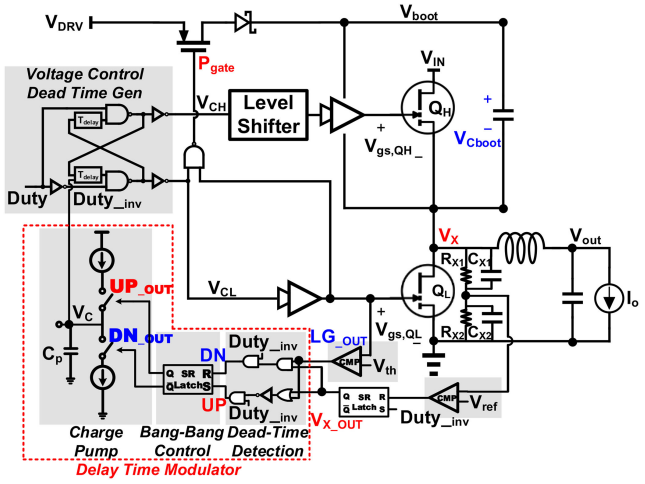


Fig. 6. Block diagram of the proposed driver with bang-bang dead-time control.

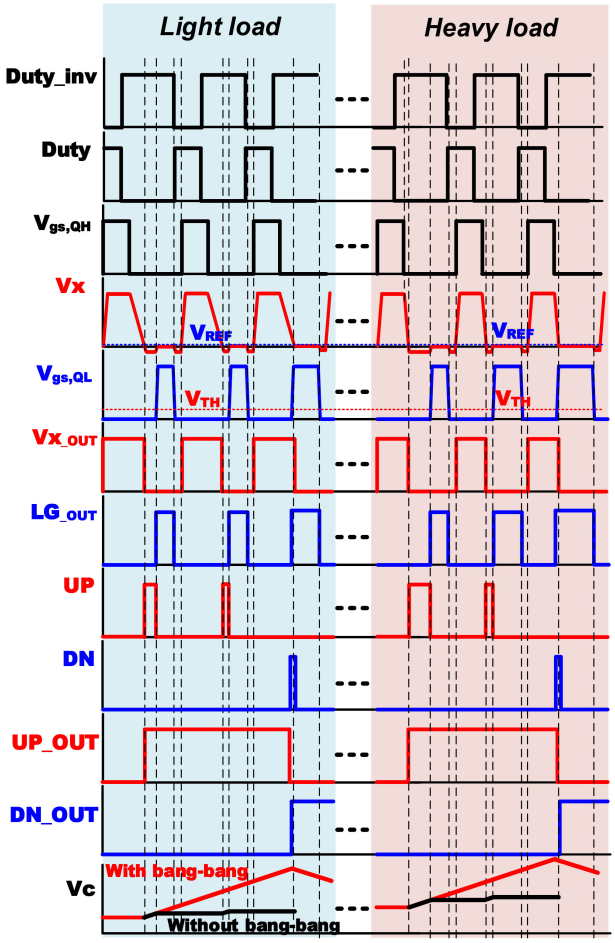


Fig. 7. Operation waveform of dead time control.

with a SPICE model for IC co-simulation. They are driven by high side and low side gate drivers with gate signal V_{GH} and V_{GL}, respectively. The duty signal is provided externally. The dead-time modulator generates high side driver and low side driver control signals V_{CH} and V_{CL}. The level shifter is utilized to transfer duty signals from the low voltage domain to the high voltage bootstrap domain.

The bootstrap circuit with charge sharing capacitor generates sufficiently high V_{boot} with reduced on-chip capacitor area for high side gate driver. One low voltage bootstrap capacitor and one high voltage bootstrap capacitor can share their charges by a switch to avoid large bootstrap voltage drop during driving. The bootstrap capacitor is designed fully on-chip to reduce the gate-loop parasitic inductor, which may cause V_{gs} switching spike.

III. Proposed GaN Driver With Bang-Bang Dead-Time Control

The block diagram of the proposed GaN driver with bang-bang dead-time control is shown in Fig. 6. The dead-time control sub-blocks include comparators, dead-time detection, bang-bang control, charge pump, and dead-time generator. Since the dead-time from low-side power switch turn-OFF to high-side power switch turn-ON does not change with loading [2]. The proposed control only adjusts the high-to-low dead-time (from high-side power switch turn-OFF to low-side power switch turn-ON) to reduce control complexity. The proposed dead-time control can also be applied to minimize low-to-high dead-time by adding another bang-bang control to the low-to-high dead-time generator.

A. Operation Principle of Dead-Time Control

The operation waveform is shown in Fig. 7. The waveform shows the operation when dead-time control is enabled at light load, and then a light-to-heavy load change happens. The ideal high-to-low dead-time control shall let V_X falling edge be synchronous with $V_{gs,QL}$ turn-ON timing, which means almost no high-to-low dead-time. Since the power switch would turn-ON when V_{gs} reaches the threshold voltage (V_{th}), low side GaN FET $V_{gs,QL,}$ and voltage level V_{th} are fed to a comparator to get real turn-ON timing. The switching node (V_X) is also fed to a comparator. Two comparator outputs (V_{x_OUT} and $LG_{\_OUT}$) are fed into the dead-time detection block to generate compensation

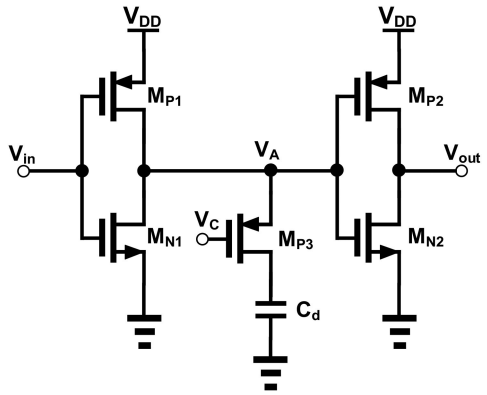


Fig. 8. Circuit implementation of voltage-controlled delay line.

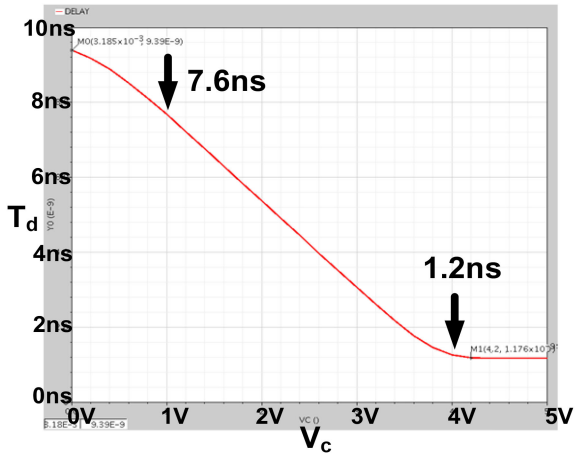


Fig. 9. Controlled voltage versus delay of the voltage-controlled delay line in Fig. 8.

signals (UP and DN). If V_x falling edge is before $V_{gs,QL}$ turn-ON timing, UP signal would be high during the dead-time. On the contrary, if Vx falling edge is after $V_{gs,QL}$ turn-ON timing, DN signal would be high in the overlap region. Equation (1) shows the key logic equation of the dead-time detection block.

$$\begin{aligned} DN &= \overline{LG\_OUT} \cdot V_{X\_OUT} \cdot Duty_{inv} \\ UP &= LG\_OUT \cdot \overline{V_{X\_OUT}} \cdot Duty_{inv} \end{aligned} \quad (1)$$

When Vx_OUT, LG_OUT, and Duty_inv are high, the high-to-low dead-time occurs. In contrast, when Vx_OUT and LG_OUT are low and Duty_inv is high, the high-to-low overlap region occurs. UP and DN signals would be sent to the charge pump to control the voltage of C_p (V_C). Then, the delay generator would vary the dead-time based on V_C to minimize DN and UP pulse widths. However, an issue is that DN and UP signals would compensate the V_C slowly because of the small pulse widths of UP and DN. In order to get a fast loop response, bang-bang control is used to extend UP and DN signals to be UP_out and DN_out. Hence, V_C would adjust faster with bang-bang control, as shown in Fig. 7. The side effect is that V_C will have a ripple at steady-state, which causes a dead-time variation range at steady-state, as will be shown in Figs. 14 and 26.

The voltage-controlled dead-time generator adjusts delay according to V_C. Fig. 8 shows the circuit implementation of voltage-controlled delay line T_{delay} in the dead-time generator. Fig. 9 shows the relationship between controlled voltage V_C and delay time of the voltage-controlled delay line in Fig. 8. When V_C is high, the resistance of M_{P3} is large, which means the RC time constant can be approximated as the product of M_{P1} on-resistance and parasitic capacitor of the V_A node. When V_C is low, the resistance of M_{P3} is small, which means the RC time constant can be approximated as the product of M_{P1} on-resistance, parasitic capacitor of the V_A node, and C_d. Thus, the delay would be increased.

B. Signal Sensing for Dead-Time Control in High-Frequency GaN Converter

Signal sensing for dead-time control in high-frequency GaN converter is critical because of high voltage spikes and ringing.

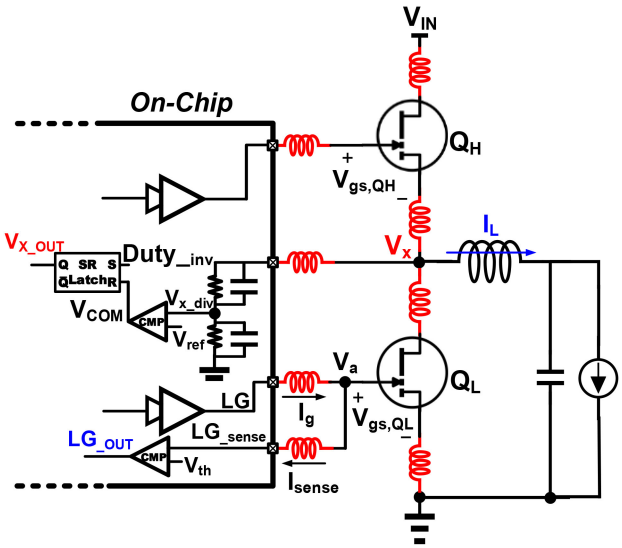


Fig. 10. Block diagram of signal sensing and equivalent circuit of power stage.

Fig. 10 shows the block diagram of signal sensing and the equivalent circuit of the power stage considering the parasitic inductances of PCB and IC wire bonding. As shown in the simulation result in Fig. 11, it would have an obvious voltage ringing on V_x during switching transition, which may cause false identification of dead-time. Therefore, A SR latch is added after the comparator output V_{COM}. It successfully clamped the comparator output after sensing V_x falling edge, as shown in Fig. 11.

Moreover, the Kelvin sensing method is used to get a cleaner $LG_{\_sense}$ waveform. A large voltage spike appears on LG sensing signal since a large and high-slew-rate driving current I_g would pass through the parasitic inductance of IC bonding. Instead, $LG_{\_sense}$ waveform is cleaner because of the very lower di/dt of I_{sense} on the sensing path. As shown in Fig. 12, the voltage spike in LG signal does not appear in $LG_{\_sense}$, and a correct dead-time can be sensed.

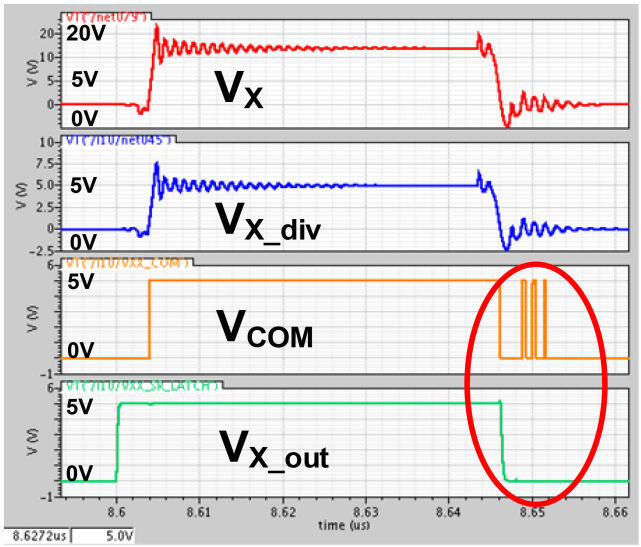


Fig. 11. Simulation result (presim) of V_x sense.

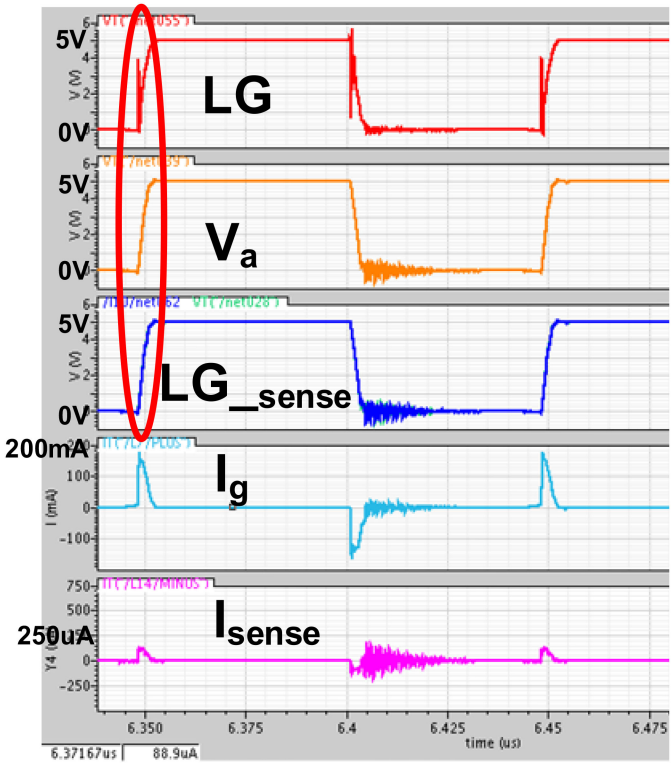


Fig. 12. Simulation result (presim) of $V_{gs,QL}$ sense.

C. Simulation Result

This part shows the Spectre simulation result of the proposed 10 MHz 12 V input to 5 V output synchronous buck converter using EPC8009 GaN device with a loading range from 0.2 to 1 A. In Fig. 13, the voltage of Cp (Vc) would start to track the load from 0 V during start-up. Fig. 14 shows that the minimum high-to-low dead-time is 0.302 ns at light load condition. Fig. 15 shows that the minimum high-to-low dead-time is 0.212 ns

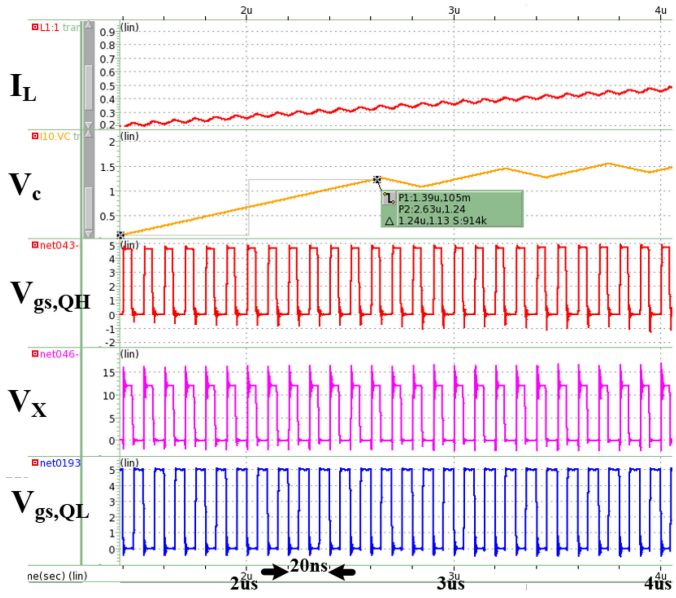


Fig. 13. Simulation result (presim) of dead time control during start-up transient.

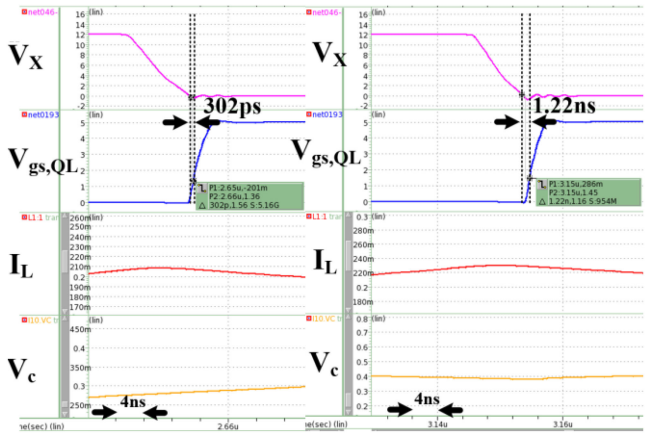


Fig. 14. Simulation result of bang-bang dead-time control at light load.

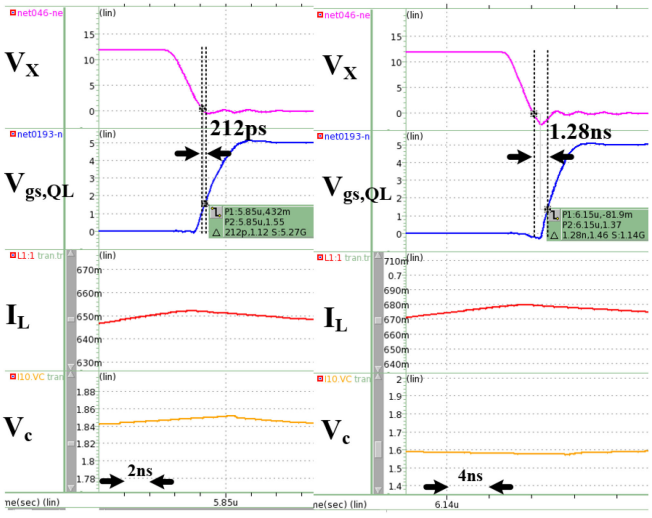


Fig. 15. Simulation result of bang-bang dead-time control at heavy load.

at heavy load condition. Thus, minimum dead-time can be achieved under the entire load range. Besides, it is shown that Vc would be lower at light load condition since it requires a larger delay time between Vx go-low and $V_{gs,QL}$ go-high.

IV. Proposed GaN Driver IC With Charge Sharing Bootstrap Capacitor

A. Concept

The proposed charge sharing bootstrap circuit concept is to use the HV capacitor C_{boot2} in Fig. 5 to store more energy with high voltage (12 V input voltage, V_{IN}). Thus, bootstrap voltage drop during driving is reduced, and lower on-resistance can be achieved. When the duty is OFF (Q_H is OFF, Q_L is ON), V_{DRV}, which provides 5 V gate overdrive voltage for power switch Q_H, and V_{IN} are charging C_{boot} and C_{boot2}, respectively. When the duty is on (Q_H is ON, Q_L is OFF), the charges of C_{boot} and C_{boot2} are shared to supply the driver charging current. In order to deliver the energy from HV capacitor C_{boot2} to bootstrap capacitor C_{boot}, a switch SW is needed to control the timing for charging. In addition, a diode D_B is used to break the current path from V_{boot2} to V_{IN} when V_X voltage level shifts up to V_{IN}.

The relationship between C_{boot}, C_{boot2}, and Q_g, the equivalent gate charge displacement during power switch turn-ON, is expressed in the following:

$$Q_g = C_{boot} \cdot V_{dip} + C_{boot2} \cdot V_{dip2}. \tag{2}$$

where C_{boot} and C_{boot2} are 5 V bootstrap capacitor and 12 V bootstrap capacitor, respectively. V_{dip} represents the voltage drop of C_{boot} from the initial fully charged voltage when duty is OFF to the end value before duty is ON. In the same manner, V_{dip2} represents the voltage drop of C_{boot2}. V_{Cboot} and V_{Cboot2} are the end value of voltage cross C_{boot} and C_{boot2}, respectively, before duty is on. It is necessary to know that the initial voltage V_{Cboot2} is larger than the initial voltage of V_{Cboot} because the input voltage V_{IN} is larger than the driver voltage V_{DRV}. During duty on, C_{boot2} would share the charge with C_{boot}, and the final value of V_{Cboot} and V_{Cboot2} would be the same. Hence, the voltage drop of C_{boot2} (V_{dip2}) can be rewritten as follows:

$$V_{dip2} = V_{Cboot2} - (V_{Cboot} - V_{dip}). \tag{3}$$

By substituting (3) into (2), (2) can be rewritten as follows:

$$Q_g = C_{boot} \cdot V_{dip} + C_{boot2} \cdot [V_{Cboot2} - (V_{Cboot} - V_{dip})]. \tag{4}$$

By (2) and (4), the final voltage drops of C_{boot} (V_{dip}) can be expressed as follows:

$$V_{dip} = \frac{Q_g - C_{boot2} \cdot (V_{Cboot2} - V_{Cboot})}{C_{boot} + C_{boot2}}. \tag{5}$$

From (4), it can be seen that the bootstrap voltage drop of the proposed bootstrap circuit would be lower than the conventional bootstrap circuit when V_{Cboot2} is higher than V_{Cboot}. Besides, the voltage drop can also be predicted and designed based on this equation.

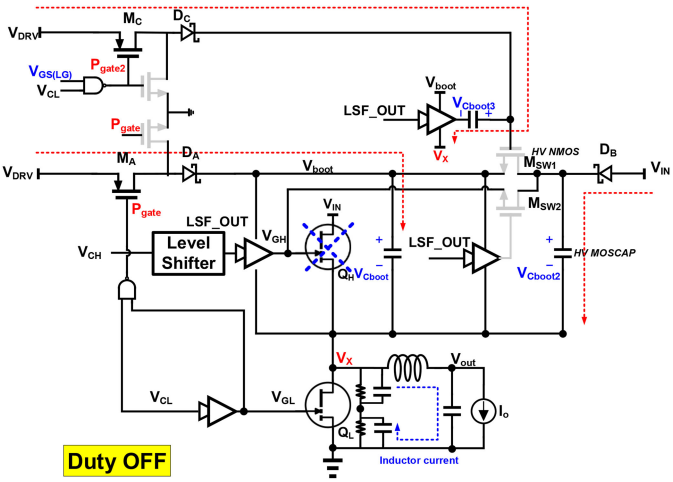


Fig. 16. Operation diagram of the proposed bootstrap circuit during duty OFF.

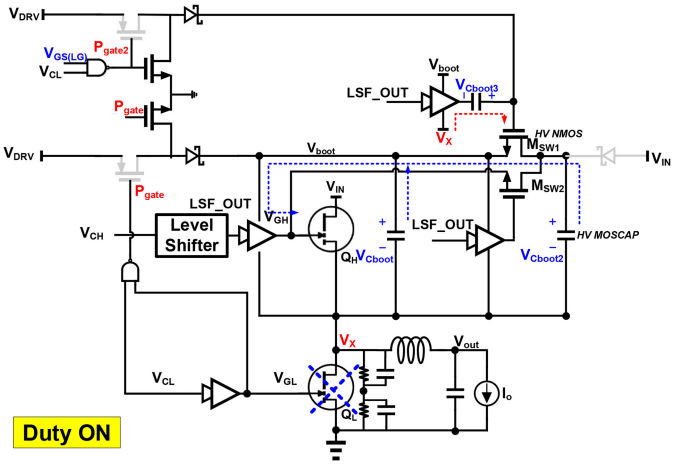


Fig. 17. Operation diagram of the proposed bootstrap circuit during duty ON.

B. Circuit Implementation and Operation

The operation principle of the bootstrap circuit with charge sharing will be introduced in the following. When the duty is low (the low-side switch is turned ON and the high-side switch is turned OFF), the operation diagram is shown in Fig. 16. At this period, the V_X is pulled down to around ground voltage. Hence, C_{boot} would be charged through the charging path (M_A and D_A) by the supply voltage V_{DRV}. C_{boot2} would be charged through the diode (D_B) by the supply voltage V_{IN}. C_{boot3} would be charged through the charge path (M_C and D_C) by the supply voltage V_{DRV}. HV NMOS implements the switch M_{SW1} and M_{SW2} between V_{boot} and the positive terminal of HV MOSCAP since the maximum drain-source voltage would be larger than 5 V.

When duty is high (the low-side switch is turned OFF and the high-side switch is turned ON), the operation diagram is shown in Fig. 17. During this period, V_X is pulled up to the input voltage V_{IN}. C_{boot2} would supply the energy to V_{GH} directly through the fast path (M_{SW2}). If V_{GH} is increased to around V_{boot} minus M_{SW2} threshold, M_{SW2} will turn-OFF and avoid Q_H gate overstress. Besides, the high-level of LSF_OUT (the

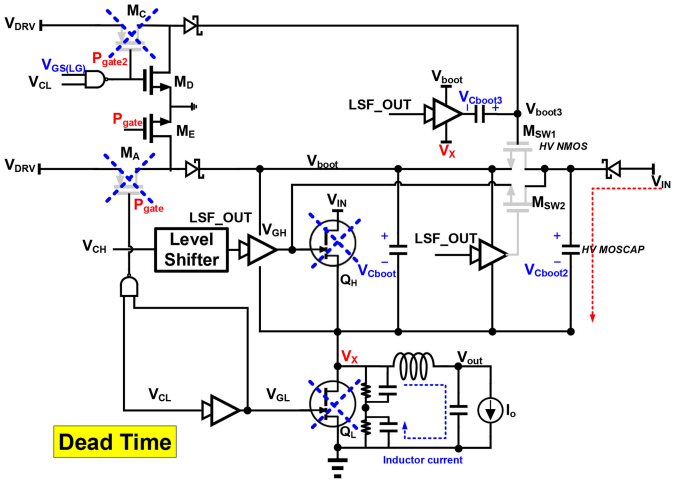


Fig. 18. Operation diagram of the proposed bootstrap circuit during dead-time.

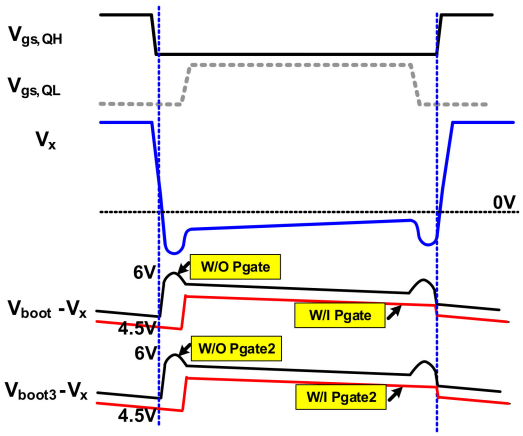


Fig. 19. Operation waveform of bootstrap circuit with charge sharing during dead-time.

output of level shifter) with the help of V_{Cboot3} would turn-ON M_{SW1}. Therefore, C_{boot2} shares the charge with C_{boot}. Finally, the charge from C_{boot} and C_{boot2} would be delivered to V_{GH}.

Figs. 18 and 19 express the operation and waveforms of bootstrap circuit with charge sharing during dead-time, respectively. $V_{gs,QH}$ is the gate-source voltage of high side GaN device Q_H. $V_{gs,QL}$ is the gate-source voltage of low side GaN device Q_L. V_{boot3} represents the gate voltage of M_{SW1}. During dead-time, V_X would go down to around -2 V. This may cause C_{boot} and C_{boot3} to overcharge to 7 V and break down MOSFETS in the driver IC [9], [10]. Therefore, M_A and M_C are designed to be turned OFF by P_{gate} and P_{gate2}, respectively, during dead-time to mitigate C_{boot} and C_{boot3} overcharging issues. However, it would have a floating node in the drain of M_A and M_C. To solve this problem, M_D and M_E are added to provide a low-level voltage to this node. From Fig. 19, it is obvious that V_{Cboot} and V_{Cboot3} would be overcharged if M_A and M_C turn-ON during dead-time. With P_{gate} and P_{gate2} to turn-OFF M_A and M_C, C_{boot} and C_{boot3} would not be charged during dead-time.

TABLE I
CIRCUIT PARAMETERS OF BOOTSTRAP CIRCUIT

Parameters	Values
Max voltage drop of C_{boot2} (V_{Cboot2}-V_{Cboot})	7 V
Min voltage drop of C_{boot2} (V_{Cboot2}-V_{Cboot})	6.5 V
Max gate charge $Q_{g(max)}$	450 pC
Min gate charge $Q_{g(min)}$	370 pC
Bootstrap capacitor (C_{boot})	100 pF

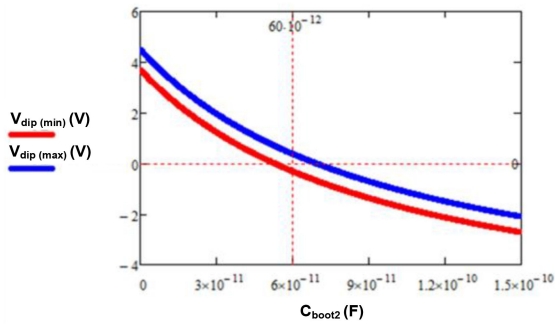


Fig. 20. Minimum and maximum voltage drop of C_{boot} versus C_{boot2}.

C. Design Consideration

The design of C_{boot2} value is related to the voltage drop of the bootstrap capacitor, V_{dip}. V_{dip} affects Q_H gate-source voltage, which is important since it affects the power switch's on-resistance. In a real case, Q_g would have a process variation. Besides, V_{Cboot2} would also vary since there is a charge path during dead-time. Since the switching node voltage (V_x) would vary with the output load, V_{Cboot2} would also vary. Considering the variation from V_{Cboot2} and Q_g to (5), the maximum and minimum voltage drops of C_{boot} can be expressed as (6) and (7), respectively.

$$V_{dip(\max)} = \frac{Q_{g(\max)} - C_{boot2} \cdot \left(V_{Cboot2(\min)} - V_{Cboot}\right)}{C_{boot} + C_{boot2}}. \tag{6}$$

$$V_{dip(\min)} = \frac{Q_{g(\min)} - C_{boot2} \cdot \left(V_{Cboot2(\max)} - V_{Cboot}\right)}{C_{boot} + C_{boot2}}. \tag{7}$$

Based on the circuit parameters shown in Table I and (6), (7), the minimum and maximum voltage drop of C_{boot} versus C_{boot2} can be drawn as Fig. 20. The *y*-axis is the voltage drop of the C_{boot}. The *x*-axis is the capacitance of C_{boot2}. Finally, the C_{boot2} is selected as 60 pF since the average value of the voltage drop from C_{boot} is almost equal to zero.

D. Simulation Result

Fig. 21 shows the simulation result of the bootstrap circuit with charge sharing. When duty is OFF (the low-side switch is ON and the high-side switch is OFF), V_{Cboot} and V_{Cboot2} would be charged to 4.58 V and 10.9 V, respectively. Based on (7), the minimum voltage drop of C_{boot} is calculated as -0.058 V. Thus, the calculated $V_{gs,QH}$ during duty on, which is the difference

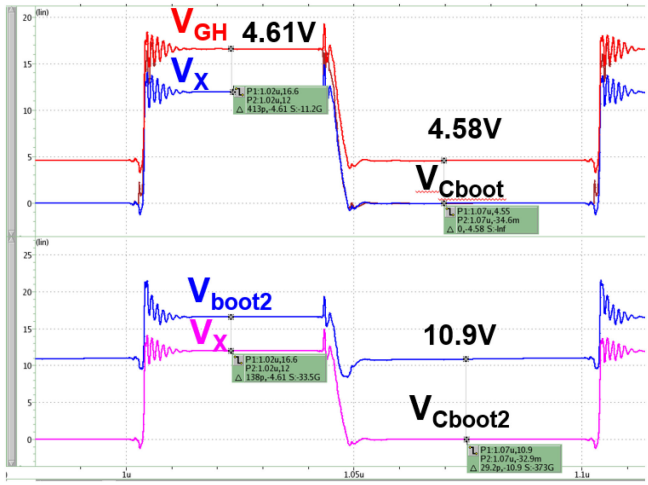


Fig. 21. Simulation result of the bootstrap circuit with charge sharing.

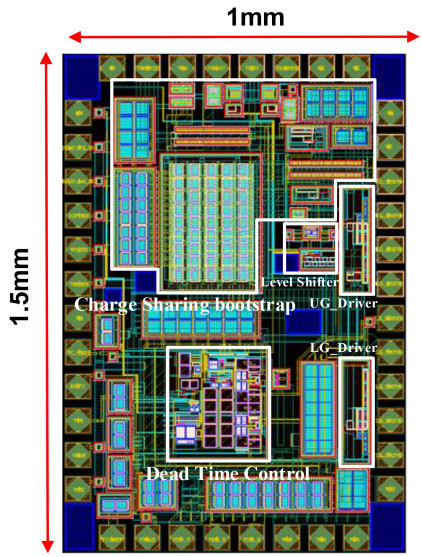


Fig. 22. Chip layout.

voltage of V_{GH} and V_x, is 4.58 + 0.058 = 4.63 V. As shown in Fig. 12, the simulated $V_{gs,QH}$ is 4.61 V, which is close to the theoretical value of 4.63 V.

V. Experimental Verification

The proposed gate driver IC is designed and fabricated using TSMC 0.25 μm HV Bipolar-CMOS-DMOS process. Fig. 22 shows the chip layout. The total chip area is 1.5 mm^2 with 0.2 nF fully integrated bootstrap capacitor to reduce the gate loop parasitic inductance. The 0.2 nF fully integrated bootstrap capacitor is combined by 100 pF C_{boot} (MIM cap and MOS cap), 60 pF C_{boot2} (HV MOS cap), and 40 pF C_{boot3} (MIM cap and MOS cap). Fig. 23 shows the experimental board. Two enhanced mode GaN devices EPC8009 are used as the power switches of buck converter; the inductance is 10 μH; the output capacitance is 10 μF. Table II shows the critical parameters of the experimental converter and driver IC.

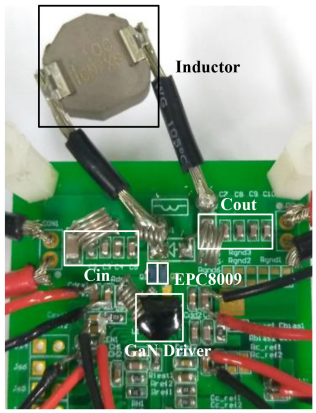
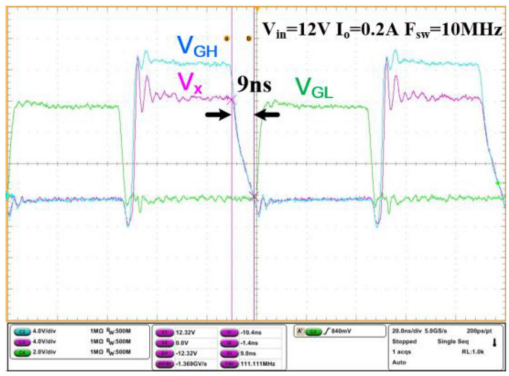


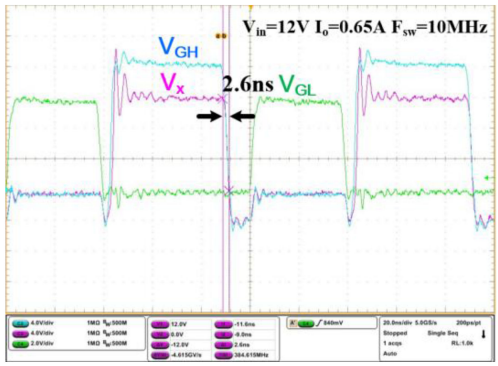
Fig. 23. Photo of the experimental board.

TABLE II
Circuit Parameters of the Experimental Converter and Driver IC

Parameters	Values
On resistance of driver	10 Ω
Maximum EPC8009 Ciss	52 pF
Maximum EPC8009 Coss	28 pF
On resistance of EPC8009	90 mΩ
Input voltage V_{IN}	12 V
Output voltage V_{out}	5 V
Loading current I_o	0.2~0.65 A
Maximum switching frequency	10 MHz
Maximum output power	3.25 W



(a)



(b)

Fig. 24. Measured switching waveforms of buck converter with conventional fixed dead-time control (a) at light load and (b) at heavy load.

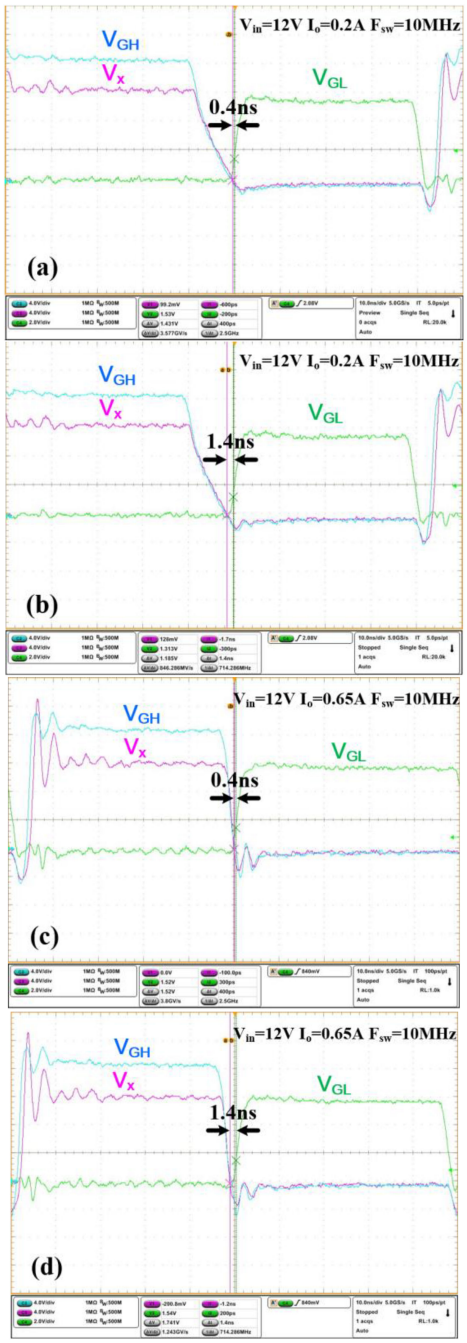


Fig. 25. Measured switching waveforms of the buck converter with the proposed dead-time control at light-load and heavy-load condition (a) minimum dead-time at light-load, (b) maximum dead-time at light-load, (c) minimum dead-time at heavy-load, and (d) maximum dead-time at heavy-load.

Fig. 24 shows the measured switching waveforms of 10 MHz buck converter with conventional fixed dead-time control under light load condition (0.2 A) and heavy load condition (0.65 A), respectively. V_{GH} is the output of the high side gate driver, and V_{GL} is the output of the low side gate driver. V_x is the voltage of the switching node between the high and low side GaN devices. From Fig. 24, the falling time of V_x is 9 ns under light load and 2.6 ns under heavy load. As the load increases, the falling time of V_x would be reduced, as illustrated in Fig. 1. Besides,

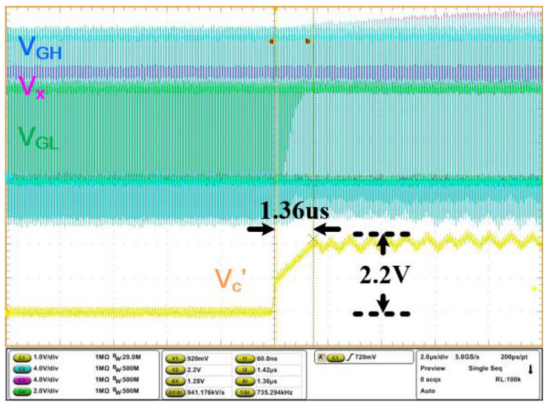


Fig. 26. Measured dead-time control settling behavior.

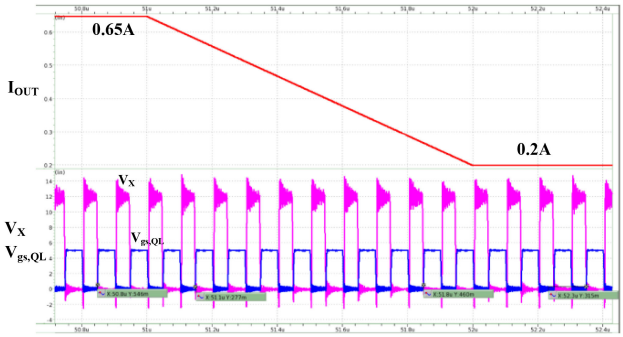


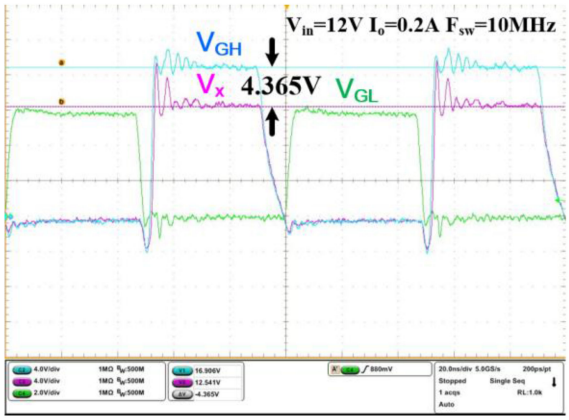
Fig. 27. Simulation result of output load transient from 0.65 to 0.2 A.

the dead-time is 1.8 ns at light load condition and 9.2 ns at heavy load condition. Thus, as the output load increases, the conventional fixed dead-time control exhibits larger dead-time and related loss.

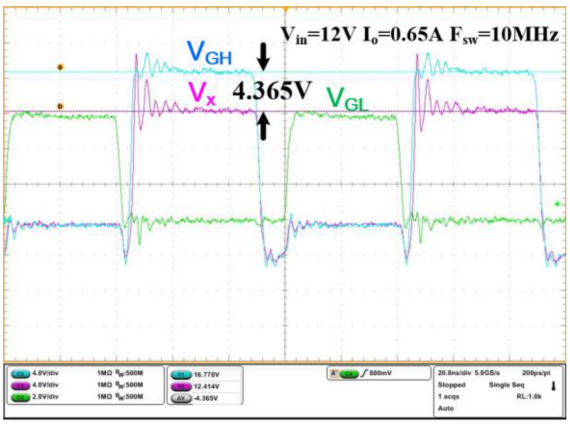
Fig. 25 shows the measurement results of the buck converter with the proposed bang-bang dead-time control at light-load and heavy-load condition. Fig. 25(a) and (b) show that the bang-bang dead-time is 400 ps to 1.4 ns at light load condition. Fig. 25(c) and (d) show that the bang-bang dead-time is 400 ps to 1.4 ns at heavy load condition. The dead-times are measured from the time when the falling edge of V_x passes through zero volt to the time when the rising edge of LG passes through V_{th}. With the proposed control, the dead-time of the buck converter can be locked with a minimum 400 ps dead-time at various load conditions as predicted in the simulations.

Fig. 26 shows the measurement result of dead-time control settling behavior. V_c' is the control voltage of the delay generator (V_C) passing through a unit gain buffer for measurement. When the bang-bang locked loop is turned ON, V_c would rise to compensate the delay. V_c' would follow the rise of V_c after the voltage exceeds the input common-mode range of unit gain buffer. Thus, the settling speed of V_c can be calculated as 0.941 V per microsecond from Fig. 26. Besides, it can be seen that V_C has a ripple at steady-state due to band-band control. This causes a dead-time variation range at steady-state as shown in Fig. 25.

Fig. 27 shows the simulation result of output load transient from 0.65 to 0.2 A within 1 μs. It can be seen that $V_{gs,QL}$ is



(a)



(b)

Fig. 28. Measurement result of charge sharing bootstrap circuit performance (a) at light load (b) at heavy load.

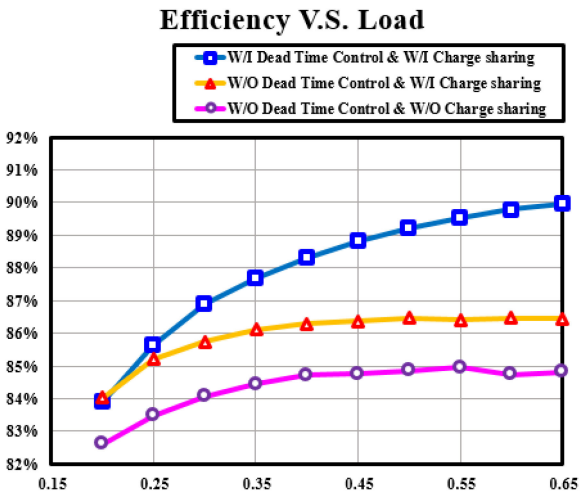
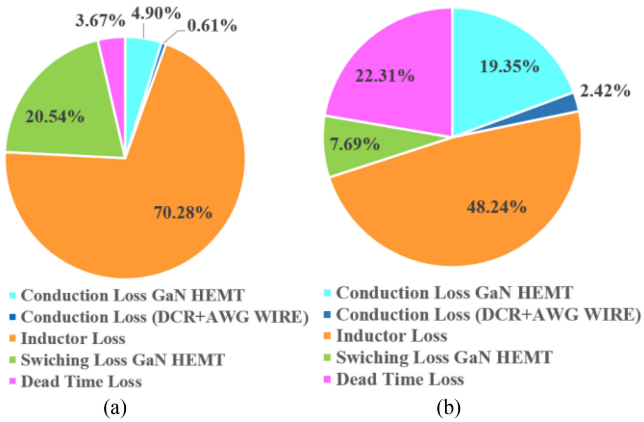


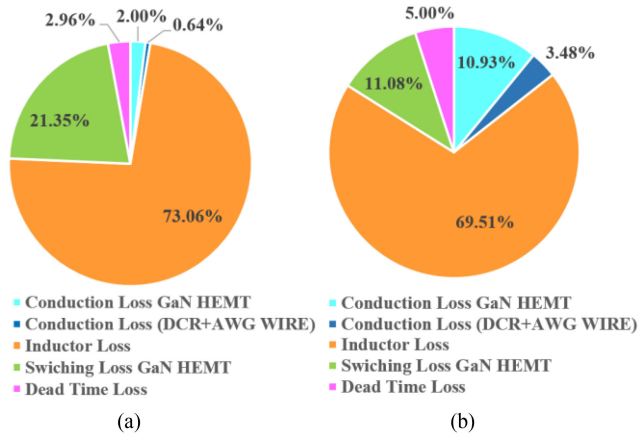
Fig. 29. Measured efficiencies of the buck converter with the proposed and conventional controls.

lower than the threshold voltage when V_x falls to zero during load transient period. Thus, no shoot-through or hard-switching happens during load transient. This is because the slope of V_X falling edge is related to the inductor current value, which does not change as severe as input voltage or load current change.



(a) (b)

Fig. 30. Loss breakdown without dead-time control and charge sharing technique (a) at light load (b) at heavy load.



(a) (b)

Fig. 31. Loss breakdown with dead-time control and charge sharing technique (a) at light load (b) at heavy load.

Thus, the dead-time adjustment does not need to be as fast as load transient speed to avoid shoot-through.

Fig. 28 shows the measured charge sharing bootstrap circuit performance of the 10 MHz buck converter. The experimental result shows that the high side gate-source voltage is 4.365 V both under light and heavy load conditions. The measured gate-source voltage has a 0.245 V deviation from simulation, which may be due to the inaccurate model of diode voltage drop in the bootstrap circuit.

Fig. 29 shows the measured efficiencies of the buck converter with the proposed and conventional controls. For the conventional control without charge sharing bootstrap circuit, 450 pF C_{boot} is designed. With 450 pC Q_g and 450 pF C_{boot}, it would have 1 V voltage drop on the C_{boot}. By adding charge sharing bootstrap circuit, the gate-source voltage of the high side power switch can be increased to 4.365 V with 100 pF C_{boot} (MIM cap and MOS cap), 60 pF C_{boot2} (HV MOS cap), and 40 pF C_{boot3} (MIM cap and MOS cap). In addition, the efficiency of conventional control with the charge sharing bootstrap circuit can improve 1.5% because of the higher gate-source voltage of GaN device Q_H. Compared with fixed dead-time control, the

TABLE III
COMPARISON TABLE

Design	EPC AN015 [26]	ISSCC2015 [6]	ISSCC2016 [17]	This work
Power switch	GaN	GaN	GaN	GaN
Input voltage	42 V	5 – 20 V	3 – 40 V	12 V
Switching frequency	10 MHz	20 MHz	10 – 30 MHz	10 MHz
Bootstrap capacitor	External	On-chip	On-chip	On-chip
Bootstrap protection	Zener Diode	Zener Diode	Active bootstrap	Active bootstrap
Dead-time	8 ns	3.2 ns	0.9 – 3.7 ns	0.4 – 1.4 ns
Max dead-time settling time	--	--	--	1.36 μs
Adaptive dead-time	Without	Without	With	With
Bootstrap capacitor reduction	Without	Without	Without	With

proposed work with dead-time control and charge sharing circuit improves 5% efficiency under 0.65 A condition.

Fig. 30 expresses the loss breakdowns of GaN-based buck converter without dead-time control and charge sharing under light load and heavy load, respectively. Compared between light load and heavy load conditions, it is obvious that conduction loss and dead-time loss would increase as the output load increases. After including the dead-time control and charge sharing bootstrap technique, the loss breakdowns of GaN-based buck converter under light load and heavy load are shown in Fig. 31. Compared with Fig. 30, the conduction loss distribution of GaN HEMT at heavy load would be decreased from 19% to 10% due to the charge sharing bootstrap technique. Besides, the dead-time loss distribution at heavy load would be reduced from 22.31% to 5% because of dead-time control.

VI. CONCLUSION

This work proposes a gate driver IC for GaN-based synchronous buck converter with bang-bang dead-time control and charge sharing bootstrap circuit. The 12 V input to 5 V output buck converter operates at 10 MHz switching frequency with a loading range from 0.2 A to 0.65 A. The fully integrated bootstrap circuit with 100 and 60 pF (HV) capacitor obtained the expected lower than 0.6 V driving voltage drop with only 45% capacitance and around half of the voltage drop compared with a conventional bootstrap circuit. In Table III, compared with other's work, the smallest minimal dead-time of 0.4 ns and adaptive minimized dead-time control under various loadings can be achieved. The maximum settling time is 1.36 μs. Finally, the peak efficiency can achieve 89.9% under 0.65 A condition, which is 5% higher than conventional fixed dead-time control without a charge sharing circuit.

ACKNOWLEDGMENT

The authors would like to thank SIMPLIS Technologies Corporation, USA, for providing SIMPLIS simulation tool, and Taiwan Semiconductor Research Institute, Taiwan for chip fabrication support.

REFERENCES

[1] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the performance of 650-V p-GaN gate HEMTs: Dynamic RON characterization and circuit design considerations," *IEEE Trans. Power Electron.*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017.

[2] A. Lidow, M. de Rooij, J. Strydom, D. Reusch, and J. Glaser, *GaN Transistors for Efficient Power Conversion*. Hoboken, NJ, USA: Wiley, 2019.

[3] X. Ke, J. Sankman, Y. Chen, L. He, and D. B. Ma, "A tri-slope gate driving GaN DC–DC converter with spurious noise compression and ringing suppression for automotive applications," *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 247–260, Jan. 2018.

[4] P. Y. Wang, P. K. Chiu, S. T. Li, C. J. Chen, and C. Hsu, "A 10 MHz GaN driver IC with bang-bang dead-time control for synchronous rectifier buck converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 3776–3781.

[5] P. K. Chiu, P. Y. Wang, S. T. Li, C. J. Chen, and Y. T. Chen, "A GaN driver IC with novel highly digitally adaptive dead-time control for synchronous rectifier buck converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2020, pp. 3788–3792.

[6] M. K. Song, L. Chen, J. Sankman, S. Terry, and D. Ma, "A 20 V 8.4 W 20 MHz four-phase GaN DC–DC converter with fully on-chip dual-SR bootstrapped GaN FET driver achieving 4 ns constant propagation delay and 1 ns switching rise time," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2015, pp. 1–3.

[7] J. Delaine *et al.*, "High frequency DC–DC converter using GaN device," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 1754–1761.

[8] D. Liu, H. C. P. Dymond, J. Wang, B. H. Stark, and S. J. Hollis, "Building blocks for future dual-channel GaN gate drivers: Arbitrary waveform driver, bootstrap voltage supply, and level shifter," in *Proc. Int. Symp. Power Semicond. Devices ICs*, 2019, pp. 79–82.

[9] S. T. Li, P. Y. Wang, C. J. Chen, and C. Hsu, "A 10 MHz GaN driver with gate ringing suppression and active bootstrap control," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, 2019, pp. 1–4.

[10] S. T. Li, P. Y. Wang, C. J. Chen, and C. Hsu, "A 10 MHz GaN based buck converter with dynamic pull-up resistor gate driver," in *Proc. IEEE Int. Future Energy Electron. Conf.*, 2019, pp. 1–4.

[11] Efficient Power Conversion Corp., "EPC8009 datasheet – Enhancement mode power transistor," Datasheet, Apr. 2021. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC8009_datasheet.pdf

[12] Texas Instruments, "LM1210: 200-V, 1.5-A, 3-A half-bridge MOSFET and GaN FET driver with adjustable dead time for applications up to 50 MHz," Datasheet, Rev. B, Jan. 2019. [Online]. Available: https://www.ti.com//lit/ds/symlink/lmg1210.pdf?ts=1649028715069

[13] M. Zhou, Q. Low, and L. Siek, "A high efficiency synchronous buck converter with adaptive dead-time control," in *Proc. Int. Symp. Integr. Circuits*, 2016, pp. 1–4.

[14] F. Lima, M. Santos, J. Barata, and J. Aguiar, "Dead-time control system for a synchronous buck DC–DC converter," in *Proc. Int. Conf. Power Eng., Energy Elect. Drives*, 2007, pp. 423–428.

[15] J. Wittmann, A. Barner, T. Rosahl, and B. Wicht, "A 12V 10MHz buck converter with dead time control based on a 125 ps differential delay chain," in *Proc. Eur. Solid-State Circuits Conf.*, 2015, pp. 184–187.

[16] Z. Chen, Y. Wong, T. Yim, and W. Ki, "A 12A 50V half-bridge gate driver for enhancement-mode GaN HEMTs with digital dead-time correction," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2015, pp. 1750–1753.

[17] X. Ke, J. Sankman, M. K. Song, P. Forghani, and D. B. Ma, "A 3-to-40 V 10-to-30 MHz automotive-use GaN driver with active BST balancing and VSW dual-edge dead-time modulation achieving 8.3% efficiency improvement and 3.4 ns constant propagation delay," in *Proc. IEEE Int. Solid-State Circuits Conf.*, 2016, pp. 302–304.

[18] M. Asad, A. K. Singha, and R. M. S. Rao, "Dead time optimization in a GaN-based buck converter," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2830–2844, Mar. 2022.

[19] Y. Zhang, C. Chen, Y. Xie, T. Liu, Y. Kang, and H. Peng, "A high-efficiency dynamic inverter dead-time adjustment method based on an improved GaN HEMTs switching model," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 2667–2683, Mar. 2022.
[20] A. Seidel, M. S. Costa, J. Joos, and B. Wicht, "Area efficient integrated gate drivers based on high-voltage charge storing," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1550–1559, Jul. 2015.
[21] Texas Instruments, "TPS560200 4.5-V to 17-V input, 500-mA synchronous step-down converter," Datasheet, Rev. C, Feb. 2016. [Online]. Available: https://www.ti.com/lit/ds/symlink/tps560200.pdf?ts=1626141494771&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FISO6741%253FHQS%253Dasc-int-iso-iso_iso67xx-rebs-pf-NextRollNet-tw%2526DCM%253Dyes%2526dclid%253DCPWc3oD43vECFZPrvAod1rIF2g
[22] Texas Instruments, "TPS629210-Q1 3-V to 17-V, 1-A low IQ buck converter," Datasheet, May 2021. [Online]. Available: https://www.ti.com/lit/ds/symlink/tps629210-q1.pdf?ts=1626190398224&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTPS629210-Q1
[23] Texas Instruments, "Multi-MHz GaN power stage reference design for high-speed DC/DC converters," TI Designs: TIDA-01634, Feb. 2018. [Online]. Available: https://www.ti.com/lit/ug/tidue47/tidue47.pdf?ts=1626189420034&ref_url=https%253A%252F%252Fwww.ti.com%252Ftool%252FTIDA-01634%253FHQS%253Dapp-hvp-gan-lmg1020_lmg1210-twit-rd-01634wwe%2526hootPostID%253D509fbdebb9f344e269ede9090d8d6c66
[24] Texas Instruments, "TMS320F2803x real-time microcontrollers," datasheet, Jun. 2021. [Online]. Available: https://www.ti.com/lit/ds/symlink/tms320f28035.pdf?ts=1640692777015&ref_url=https%253A%252F%252Fwww.ti.com%252Fproduct%252FTMS320F28035
[25] Texas Instruments, "TMS320F2806x real-time microcontrollers," Datasheet, Jun. 2021. [Online]. Available: https://www.ti.com/lit/ds/symlink/tms320f28069.pdf?ts=1640619146439
[26] EPC: AN015, "Introducing a family of eGaN FETs for multi-megahertz hard switching applications," 2020, [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/product-training/AN015%20eGaN%20FETs%20for%20Multi-Megahertz%20Applications.pdf

Ching-Jan Chen (Senior Member, IEEE) received the B.S. and Ph.D. degrees in electrical engineering from National Taiwan University (NTU), Taipei, Taiwan, in 2006 and 2011, respectively.

From 2010 to 2011, he was a Visiting Scholar with the Center of Power Electronic Systems (CPES), Virginia Tech, Blacksburg. From 2011 to 2015, he was a Senior Engineer with IC Research and Development Department, Richtek Technology Corporation, Hsinchu, Taiwan. His work was focus on new control scheme development and IC design of the voltage regulator controller for CPU power. In February 2015, he became an Assistant Professor with the Department of Electrical Engineering, NTU, where he is currently an Associate Professor. His current research interests include modeling and control of dc–dc and ac–dc power converters, power conversion for CPU and mobile devices, and power IC design.

Dr. Chen was the recipient of the Young Researcher Award from the Ministry of Science and Technology (MOST), Taiwan, in 2016, the Outstanding Teaching Awards from NTU in 2020, the Research Contribution Award from NTU EECS in 2020, and Ta-You Wu Memorial Award from MOST, Taiwan, in 2021. He served as Session Chair, Topic Chair, and Financial Chair in several IEEE conferences and competitions such as ECCE, ECCE-Asia, International Future Energy Challenge (IFEC), IFEEC, WiPDA Asia, ITEC-Asia Pacific, and VLSI-DAT. He was the Secretary and then Vice-Chair of IEEE PELS Taipei Chapter from 2018 to 2020 and received the IEEE PELS Best Chapter Award in 2018.

Pin-Ying Wang received the B.S. degree in electronic and computer engineering from National Taiwan University of Science and Technology, Taipei, Taiwan, in 2018, and the M.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, in 2020.

Since 2022, he has been with Mediatek Technology Corporation, Hsinchu, Taiwan, and serves as the Engineer with the ADCT Business Unit. His work focused on GaN-based dc–dc converter and IC design of GaN driver. His research interests include power electronics, dc–dc power converter and control, and power IC design.

Sheng-Teng Li received the B.S. degree in communication engineering from National Central University, Taoyuan, Taiwan, in 2017, and the M.S. degree from the Institute of Electrical Engineering, National Taiwan University, Taipei, Taiwan, in 2020.

His research interests include the power management IC design and mixed-signal IC design.

Yen-Ming Chen was born in Taipei, Taiwan. He received the B.S. degree in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2018. He is currently working toward the Ph.D. degree with the Institute of Electrical Engineering, National Taiwan University, Taipei, Taiwan.

He is a Member of the Power Electronics Laboratory, National Taiwan University. His research interests include the power management IC design and mixed-signal IC design.

Yu-Cheng Chang received the B.S. degree in electrical engineering from National Taipei University of Technology, Taipei, Taiwan, in 2019. He is currently working toward the M.S. degree with Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan.

His research interests focus on high-voltage GaN-based power converters, GaN driver ICs. His current research interests include HV power management integrated circuits for automotive and data center applications, silicon and wide-bandgap power devices, analog and mixed-signal ICs.