A Power Adaptive Impedance Reshaping Strategy for Cascaded DC System With Buck-Type Constant Power Load

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***Abstract*—It is well-known that the low-frequency negative input impedance of the constant power load (CPL) is the major cause of the cascaded system instability, and the heavier the power, the worse the stability. In this article, a power adaptive load-side parallel virtual impedance (PALPVI) control strategy is proposed to improve the stability of the cascaded dc system with buck-type CPL. First, a parallel impedance with power adaptability is derived followed up with the derivation of the corresponding compensation controller transfer function to realize it virtually. Considering that the compensation controller is highly dependent on the circuit parameters and needs extra current sensors to acquire the power information, a simplification of the compensation controller is made based on the open-loop characteristics of the buck-type CPL. The final PALPVI control strategy does not require the circuit parameters or any current sensor and has almost no side effect on the dynamic performance. Finally, a 48–24–12 V cascaded dc system is fabricated to verify the feasibility and effectiveness of the proposed PALPVI control strategy.**

***Index Terms*—Buck-type constant power load (CPL), cascaded dc system, impedance reshaping, parallel virtual impedance control, power adaptability.**

I. Introduction

In RECENT years, with the increasing of the dc loads, such as electric vehicles, data centers and communication equipment, and the high-penetration large-scale access of the renewable energy and energy storage systems, the superiority of the dc distribution power system (DPS) is significantly prominent [1]–[8]. In dc DPS, to satisfy the demand of power supply and loads for power quality and voltage amplitude, numerous power converters are mainly connected in cascade [9]–[11]. However, the complex impedance interaction between cascaded converters may lead to the system instability [12], [13].

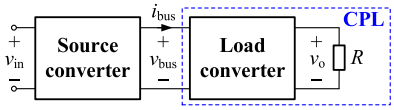

Fig. 1. Typical structure of the cascaded dc system with CPL.

A dc source is cascaded with a constant power load (CPL) can be regarded as the simplest dc DPS, as shown in Fig. 1, where the frontend and downstream converters are called the source and load converters, respectively. The small-signal stability research on such system can be traced back to the Middlebrook criterion proposed in 1976 [14]. Subsequently, an enormous amount of research further extended this stability criterion to more complex dc DPS [2], [4], [6], [8], [15]–[18], showing that the essential reason of the system instability is that the system damping is reduced by the low-frequency negative input impedance of the CPL and causing the oscillation of the dc bus voltage [19]–[22].

Based on the stability criteria, solutions for the instability of the cascaded dc system with CPL have also been widely investigated [23], which can be divided into the passive and active methods [24]. The idea of the passive solutions is to increase the system damping by inserting resistor, *RL* or *RC* dampers [25]. The passive solutions increase the system cost [9], lower the power density [26], [27], and lack adaptability and flexibility. In terms of the active solutions, there are two options [28]–[30], one is to add an active auxiliary circuit between the source and load converters, and the other is to reshape the load input impedance or source output impedance simply by modifying the control loop (also known as the active virtual impedance control). The active auxiliary circuit solution is more applicable to the cascaded systems that have been modularized and cannot be modified, but it also requires high hardware cost and leads to more complex system control [9]. By comparison, the virtual impedance control can improve the system stability at a very low cost, which is more promising.

The existing active virtual impedance control schemes are shown in Fig. 2. Categorized by the location and connection

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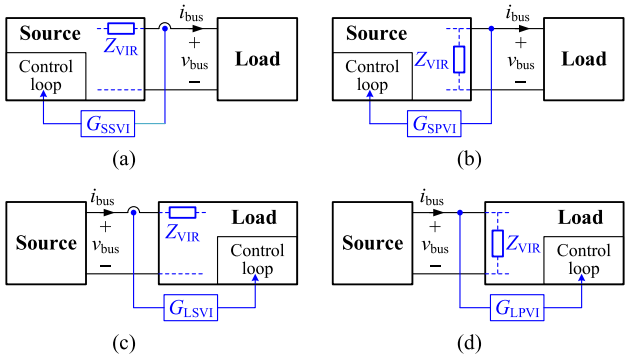


Fig. 2. Existing active virtual impedance control schemes. (a) SSVI. (b) SPVI. (c) LSVI. (d) LPVI.

of the virtual impedance $Z_{\rm VIR}$, there are four ways to realize $Z_{\rm VIR}$, namely source-side series virtual impedance (SSVI) [29], [31]–[33], source-side parallel virtual impedance (SPVI) [34], load-side series virtual impedance (LSVI) [35]–[38], and load-side parallel virtual impedance (LPVI) [35], [37]–[39]. Note that these impedance shaping schemes are mainly used to improve the small-signal stability of system.

When the source of a cascaded system is an *LC* filter or uncontrolled converter that has no closed-loop, the SSVI and SPVI control strategies cannot be used to improve the system stability [9], [29]. Conversely, if the active virtual impedance control is added into the load converter, it is necessary to consider how to ensure the system stability and the dynamic characteristics at the same time [36]. By analyzing the closed-loop transfer functions of the CPL before and after introducing the LSVI control, Zhang *et al.* [29] demonstrated that the LSVI control significantly deteriorates the dynamic performance of the CPL, such as the response time.

As for the LPVI control, Zhang *et al.* [35] also proposed two LPVI control strategies from the perspectives of amplitude and phase, but it cannot adaptively adjust with the change of the system parameters. Furthermore, the transfer functions of the compensation controllers are complex and related to the load power, which means an additional power detection circuit is required [40]. Wu *et al.* [39] presented the direct and optimal LPVI control strategies for the CPL based on the buck converter, and their compensation controllers are easier to implement, but they involve complex calculation and cannot possess the load power adaptability. Recently, Cyriac *et al.* [41] extended the research in [39] to the dual active bridge (DAB) converter, but the above problems are still remained. On the basis of [35] and [39], four parallel virtual impedance configurations (that is, series *RC*, series *RL*, parallel *RC*, and series *RLC*) were examined in [42], and the results show that the series *RL* exhibits the superior dynamic response to external disturbances. Besides, Feng *et al.* [37] proposed an LPVI control strategy to reshape the input impedance of the DAB converter; however, the low-frequency characteristics of the DAB converter are changed and complex calculation is required. To sum up, it is necessary to propose an improved LPVI control strategy with simple implementation and high parameters adaptability.

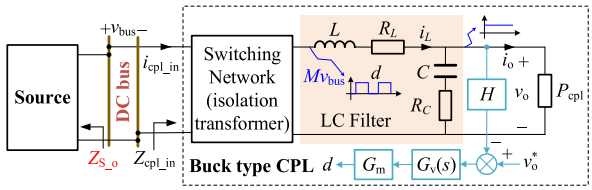


Fig. 3. Structure of the cascaded dc system with buck-type CPL.

In the cascaded system, the bus voltage is commonly higher than the load rated voltage to reduce transmission loss; as a result, a step-down converter is usually needed between the dc bus and load. In this article, based on the widely used buck-type CPL, a specific power adaptive load-side parallel virtual impedance (PALPVI) control strategy is proposed to improve the stability of the cascaded dc system. Its compensation controller is just a band-pass filter and independent of the load power, *LC*, and control parameters, which is easier to design and implement, and has high reliability. Meanwhile, the proposed PALPVI control strategy can realize the power adaptability without any current sensors or power detection circuits. Furthermore, it is proved to have little effect on the dynamic performance of the CPL.

The rest of this article is organized as follows. In Section II, the input impedance of the buck-type CPL and stability analysis of the cascaded dc system are given. In Section III, the adaptive parallel virtual impedance and its control loop are designed and simplified, and the impact of the proposed PALPVI control on the dynamic characteristics of the CPL is analyzed. In Section IV, the case study, simulation analysis, and experiments are carried out, and the proposed PALPVI control strategy is compared with some existing schemes. In Section V, some discussions are given. Finally, Section VI concludes this article.

II. Stability Analysis of Cascaded DC System With Buck-Type CPL

The typology of the cascaded dc system with a buck-type CPL is illustrated in Fig. 3. Here, the switching network converts the dc bus voltage $v_{\rm bus}$ into a square wave with the amplitude being $Mv_{\rm bus}$, and d represents the duty cycle. Here, for the nonisolated buck-type converters, there is $M = 1$; for the isolated buck-type converters, there is $M = N$, and N represents the secondary-to-primary turns-ratio of the transformer. $v_{\rm o}$ is the output voltage of the CPL, $Z_{\rm S\_o}(s)$ is the output impedance of the source converter, and $Z_{\rm cpl\_in}(s)$ is the input impedance of the CPL. On the feedback path, H is the feedback coefficient of the output voltage, $G_{\rm v}(s)$ is the transfer function of the voltage-loop controller, and $G_{\rm m}$ is the gain of the PWM modulator.

A. Input Impedance of the Buck-Type CPL

The prerequisite of the system stability analysis and the input impedance reshaping is to obtain the expression of $Z_{\rm cpl\_in}(s)$. Fig. 4 shows the complete small-signal control block diagram of the buck-type CPL, where the symbols with a cap, namely $\hat{v}_{\rm bus}$, $\hat{i}_{\rm bus}$, $\hat{v}_{\rm o}$, $\hat{d}$, and $\hat{i}_{\rm o}$, are the small-signal perturbations of the bus voltage, bus current, output voltage, duty cycle, and load current, respectively. $y_{\rm in\_op}(s)$, $g_{\rm ii\_op}(s)$, $g_{\rm di}(s)$, $g_{\rm vv\_op}(s)$,

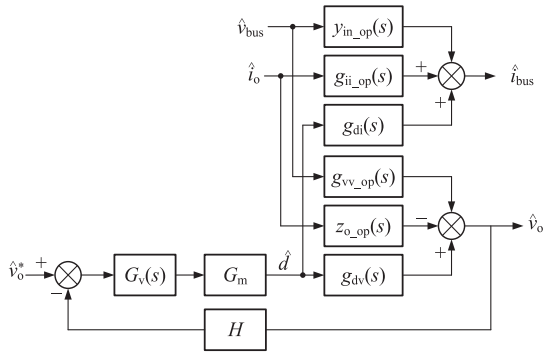


Fig. 4. Small-signal control block diagram of the buck-type CPL.

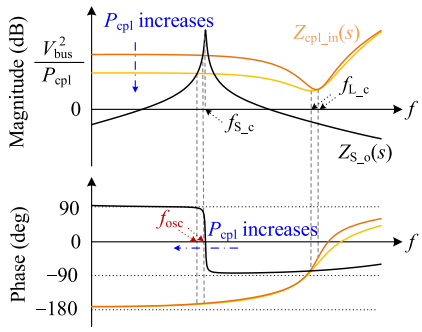


Fig. 5. Typical impedance characteristics of the cascaded dc system.

TABLE I
EXPRESSIONS OF THE OPEN-LOOP TRANSFER FUNCTIONS OF BUCK-TYPE CPL

Transfer functions	Physical meaning	Expressions
$y_{in\_op}(s)$	Input admittance	M^2D^2Cs/G_1
$g_{ii\_op}(s)$	Reverse current-ratio	$MD(R_CCs+1)/G_1$
$g_{di}(s)$	Transfer function from $\hat{d}$ to $\hat{i}_{cpl\_in}$	$MP_{cpl}/V_o+MV_oCs/G_1$
$g_{vv\_op}(s)$	Audio-susceptibility	$MD(R_CCs+1)/G_1$
$z_{o\_op}(s)$	Output impedance	$-(sL+R_L)(R_CCs+1)/G_1$
$g_{dv}(s)$	Transfer function from $\hat{d}$ to $\hat{v}_o$	$MV_{bus}(R_CCs+1)/G_1$

$z_{o\_op}(s)$, and $g_{dv}(s)$ are the open-loop transfer functions of the buck-type CPL, and their expressions are shown in Table I. Here, D, V_{bus}, and V_o represent the steady-state values of d, v_{bus}, and v_o, respectively, the transfer function $G_1(s)$ can be expressed as

$$G_1(s) = LCs^2 + (R_LC + R_CC)s + 1. \tag{1}$$

According to Fig. 4, the open-loop gain $T_{op}(s)$ of the buck-type CPL can be expressed as

$$T_{op}(s) = HG_v(s)G_m g_{dv}(s). \tag{2}$$

Using Mason formula, the closed-loop input impedance $Z_{cpl\_in}(s)$ can be expressed as

$$Z_{cpl\_in}(s) = \left[\frac{y_{in\_op}(s)}{1+T_{op}(s)} - \frac{P_{cpl}}{V_{bus}^2}\cdot\frac{T_{op}(s)}{1+T_{op}(s)}\right]^{-1}. \tag{3}$$

When the frequency is much lower than the cut-off frequency of $T_{op}(s)$, there is $|T_{op}(s)|>>1$, thus $y_{in\_op}(s)/[1+T_{op}(s)]$ in (3) is too small to be considered. With this consideration, $Z_{cpl\_in}(s)$ is approximated to be

$$Z_{cpl\_in}(s) \approx -V_{bus}^2/P_{cpl}. \tag{4}$$

From (4), it can be found that, within the low-frequency range, the closed-loop input impedance of the buck-type CPL is a negative impedance that is proportional to the square of bus voltage V_{bus} and inversely proportional to load power P_{cpl}.

B. Stability Analysis of the Cascaded DC System

Based on [2], if both the source and CPL operate stably independently, the necessary and sufficient condition for the system small-signal stability is that the impedance ratio, that is, $T_m = Z_{S\_o}(s)/Z_{cpl\_in}(s)$, meets the Nyquist stability criterion. Referring to the Bode plots of $Z_{S\_o}(s)$ and $Z_{cpl\_in}(s)$, it can be inferred that if the amplitude curve of $Z_{S\_o}(s)$ intersects with $Z_{cpl\_in}(s)$ and the phase angle difference at the intersection frequency is greater than 180°, the system is unstable, as shown in Fig. 5, where the typical amplitude frequency characteristic curves of $Z_{S\_o}(s)$ and $Z_{cpl\_in}(s)$ are presented. For such cascaded dc system, the research on the impedance characteristics and instability mechanism is very mature [35], and some general conclusions can be drawn as follows:

1) The source output impedance $Z_{S\_o}(s)$ is resistive–inductive below its cut-off frequency f_{S_c} and resistive–capacitive above f_{S_c}. The CPL input impedance $Z_{cpl\_in}(s)$ is approximately negative impedance below f_{S_c}, resistive–inductive above f_{L_c}, and negative resistive–capacitive within (f_{S_c}, f_{L_c}), which can be seen from Fig. 5.
2) The low-frequency negative impedance characteristic of the CPL (i.e., the phase angle is close to –180°) is the main cause of the dc bus voltage oscillation, and the heavier the power P_{cpl}, the worse the system stability.
3) The system oscillation frequency f_{osc} satisfies $f_{osc} < f_{S\_c} << f_{L\_c}$, and f_{osc} is not only related to LC and control parameters but also negatively correlated with P_{cpl}.

III. PROPOSED PALPVI CONTROL STRATEGY AND ITS IMPLEMENTATION

As mentioned previously, the LPVI scheme shown in Fig. 1(d) is very useful for improving the stability of the cascaded dc system. However, its existing implementation methods are very complex and lack power adaptability. In this section, a simple and power-adaptive implementation of the LPVI scheme named as PALPVI is proposed. Note that all symbols with the superscript "P" represent the closed-loop transfer functions of the buck-type CPL with the PALPVI control strategy, such as, $Z_{cpl\_in}^{P}(s) = Z_{cpl\_in}(s)//Z_{VIR}(s)$.

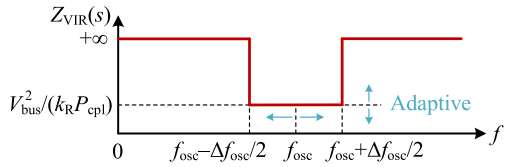


Fig. 6. Adaptively regulated virtual impedance Z_{VIR}.

A. Adaptive Parallel Virtual Impedance $Z_{VIR}(s)$

It is well-known that, to realize a good dynamic performance, the input impedance of the CPL is preferred to be regulated to a negative impedance [43]. However, the additional $Z_{VIR}(s)$ may change this characteristic and degrade dynamic performance. In order to minimize this side effect, $Z_{VIR}(s)$ should only adjust the CPL input impedance around the system oscillation frequency f_{osc}, while becomes invalid in other frequency ranges. For this purpose, as shown in Fig. 6, $Z_{VIR}(s)$ can be designed according to the following rules.

1) Within a frequency range ($f_{osc}-\Delta f_{osc}/2, f_{osc}+\Delta f_{osc}/2$), the $Z_{VIR}(s)$ should be a positive resistance. Here, $\Delta f_{osc} = f_{osc}/Q_R$ is the bandwidth to cover all adjacent frequencies with f_{osc} as the center; Q_R is the quality factor, and the larger its value is, the smaller the effective frequency range of $Z_{VIR}(s)$. Based on the aforementioned analysis, $Z_{cpl\_in}(s)$ is inversely proportional to P_{cpl}. Therefore, $Z_{VIR}(s)$ should also be inversely proportional to P_{cpl}, such that the parallel impedance of $Z_{VIR}(s)$ and $Z_{cpl\_in}(s)$ could adaptively vary with the power. For the convenience of subsequent design, $Z_{VIR}(s)$ is defined as $V_{bus}^2/(k_R P_{cpl})$. Here, k_R is a positive constant to be solved.
2) Outside the frequency range ($f_{osc}-\Delta f_{osc}/2, f_{osc}+\Delta f_{osc}/2$), $Z_{VIR}(s)$ should be $+\infty$, and thus there is $Z_{cpl\_in}^{P}(s) = Z_{cpl\_in}(s)$, which means $Z_{VIR}(s)$ is invalid.

Based on the above analysis, $Z_{VIR}(s)$ can be expressed as

$$Z_{VIR}(s) = \left[\frac{k_R P_{cpl}}{V_{bus}^2} \cdot \frac{(2\pi f_{osc}/Q_R)s}{s^2 + (2\pi f_{osc}/Q_R)s + (2\pi f_{osc})^2}\right]^{-1}. \quad (5)$$

B. Design and Simplification of the Control Loop

The small-signal control block diagram of the buck-type CPL with the PALPVI control strategy is given in Fig. 7. In order to realize the proposed PALPVI control, the dash line section shows an intuitive method of introducing $1/Z_{VIR}(s)$ between the input bus voltage and current. To achieve the same goal through control block transformation, the output of $1/Z_{VIR}(s)$ can be moved to the input side of voltage controller $G_v(s)$, as shown in the red solid line section. This equivalent transformation requires an additional compensation controller $G_{PALPVI}(s)$, which can be expressed as

$$G_{PALPVI}(s) = \frac{1 + T_{op}(s)}{g_{di}(s)G_v(s)G_m}. \quad (6)$$

After the transformation, it can be found that the PALPVI control introduces a bus voltage related term $\hat{v}_{vir}$ into the output

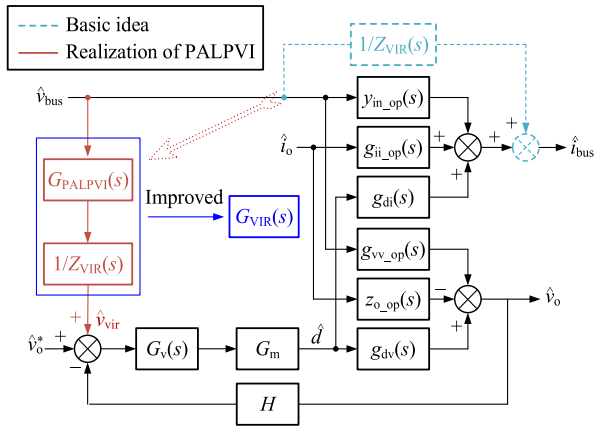


Fig. 7. Control block diagram of the buck-type CPL with the PALPVI control.

voltage reference signal, which is essentially equivalent to the input voltage feed-forward control.

The detailed expression of $G_{PALPVI}(s)$ is given in the Appendix. It can be seen that this expression is complex and difficult to implement. Furthermore, $G_{PALPVI}(s)$ is related to the circuit and control parameters of the CPL. Considering the parameter tolerances and drifts of the circuit elements, it is hard to implement $G_{PALPVI}(s)$ accurately. In addition, $G_{PALPVI}(s)$ is also related to P_{cpl}, indicating that power detection circuit is still required, which further increases the control difficulty and reduces the reliability. With these considerations, based on the open-loop characteristics of the buck-type CPL, the virtual impedance control loop is simplified as follows.

As mentioned in Section II, within the control bandwidth of $T_{op}(s)$, there is $|T_{op}(s)|>>1$, hence, based on (2) and (6), there is

$$G_{PALPVI}(s) \approx \frac{T_{op}(s)}{g_{di}(s)G_v(s)G_m} = H\frac{g_{dv}(s)}{g_{di}(s)}. \quad (7)$$

Then, according to (1) and Table I, there is

$$\frac{g_{dv}(s)}{g_{di}(s)} = \frac{V_{bus}^2}{P_{cpl}} \frac{MD(R_C Cs + 1)}{LCs^2 + (R_L C + R_C C)s + 1 + \frac{V_o^2 Cs}{P_{cpl}}}. \quad (8)$$

Furthermore, the equivalent series resistances of the filter inductance and capacitance should satisfy $R_L << V_o^2/P_{cpl}$ and $R_C << V_o^2/P_{cpl}$, therefore, based on (7) and (8), $G_{PALPVI}(s)$ can be simplified as

$$G_{PALPVI}(s) \approx \frac{HMDV_{bus}^2}{P_{cpl}LC}\left(s^2 + \frac{V_o^2}{P_{cpl}L}s + \frac{1}{LC}\right)^{-1}. \quad (9)$$

From (9), it can be found that $G_{PALPVI}(s)$ is approximated as a second-order low-pass filter, and its cut-off frequency f_G and low-frequency gain A_G can be expressed as

$$f_G = \left(2\pi\sqrt{LC}\right)^{-1} \approx f_{L\_c} \quad (10)$$

$$A_G = HMDV_{bus}^2/P_{cpl} \quad (11)$$

According to Fig. 5, since $f_{L\_c} >> f_{osc}$, there exists $f_G >> f_{osc}$, that is, the center frequency of $1/Z_{VIR}(s)$ is smaller than the cut-off frequency of $G_{PALPVI}(s)$. As a result, the product

TABLE II
ELECTRICAL AND CONTROL PARAMETERS OF EACH CONVERTER

Parameters	Values	
	Source	Buck-type CPL
Filter inductance	560 μH	220 μH
ESR of the filter inductance	0.05 Ω	0.02 Ω
Filter capacitance	170 μF	39 μF
ESR of the filter capacitance	0.05 Ω	0.05 Ω
Feedback coefficient	1/24	1/12
Proportional coefficient of the PI controller	0.2	0.8
Integral coefficient of the PI controller	100	100
Gain of the PWM modulator	1	1
Output voltage	24 V	12 V
Load power	–	81.6 W

term, $1/Z_{\mathrm{VIR}}(s)\cdot G_{\mathrm{PALPVI}}(s)$, still has the band-pass characteristic with f_{osc} as the center frequency. Therefore, within (f_{osc}–$\Delta f_{\mathrm{osc}}/2$, $f_{\mathrm{osc}}+\Delta f_{\mathrm{osc}}/2$), we have

$$\frac{G_{\mathrm{PALPVI}}(s)}{Z_{\mathrm{VIR}}(s)} \approx \frac{A_G}{Z_{\mathrm{VIR}}(s)}. \tag{12}$$

From (11), it can be seen that A_G is inversely proportional to P_{cpl}, therefore, the product of A_G and $1/Z_{\mathrm{VIR}}(s)$ can just eliminate the variable P_{cpl} according to (5) and (11). As shown in Fig. 7, the original $G_{\mathrm{PALPVI}}(s)/Z_{\mathrm{VIR}}(s)$ can be improved to a simplified compensation controller $G_{\mathrm{VIR}}(s)$, and there is

$$G_{\mathrm{VIR}}(s) = \frac{A_{\mathrm{G}}}{Z_{\mathrm{VIR}}(s)} = \frac{HMDk_{\mathrm{R}}(2\pi f_{\mathrm{osc}}/Q_{\mathrm{R}})s}{s^2+(2\pi f_{\mathrm{osc}}/Q_{\mathrm{R}})s+(2\pi f_{\mathrm{osc}})^2}. \tag{13}$$

From (13), it can be seen that $G_{\mathrm{VIR}}(s)$ is only related to the system oscillation frequency f_{osc}, the constants k_{R}, M, the duty cycle D and the feedback coefficient H of the CPL. Compared with $G_{\mathrm{PALPVI}}(s)$ and $1/Z_{\mathrm{VIR}}(s)$, the expression of $G_{\mathrm{VIR}}(s)$ is simpler and easier to implement. Meanwhile, $G_{\mathrm{VIR}}(s)$ is independent of P_{cpl}. Therefore, when the system occurs instability, the proposed PALPVI control strategy is always effective regardless of the load power P_{cpl}. Moreover, no current sensor or power detection circuit is required.

In order to verify the correctness of the above simplification, a cascaded system composed of two buck converters is taken as an example, the electrical and control parameters are shown in Table II, and there is $M = 1$. The Bode plots of the five transfer functions $G_{\mathrm{PALPVI}}(s)$, $1/Z_{\mathrm{VIR}}(s)$, $Hg_{\mathrm{dv}}(s)/g_{\mathrm{di}}(s)$, $G_{\mathrm{PALPVI}}(s)/Z_{\mathrm{VIR}}(s)$, and $G_{\mathrm{VIR}}(s)$ are illustrated in Fig. 8. It can be seen that there are $G_{\mathrm{PALPVI}}(s)\approx Hg_{\mathrm{dv}}(s)/g_{\mathrm{di}}(s)$ and $G_{\mathrm{PALPVI}}(s)/Z_{\mathrm{VIR}}(s)\approx G_{\mathrm{VIR}}(s)$ within the low-frequency range. Therefore, the above simplified method is feasible.

C. Impact of the PALPVI Control Strategy on the CPL

According to the aforementioned analysis, the proposed PALPVI control strategy introduces a new feedback branch into the voltage control loop, which may affect other dynamic characteristics of the CPL. The following will have an investigation of this issue.

It is known that the dynamic performance of a dc–dc converter can be evaluated by its four input-to-output transfer functions,

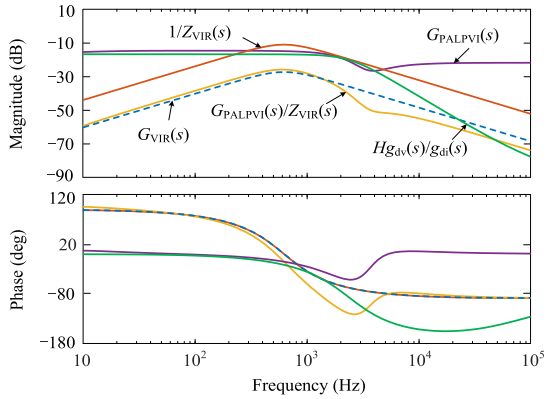


Fig. 8. Bode plots of five transfer functions.

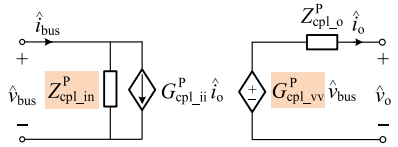


Fig. 9. Two-port small-signal model of the buck-type CPL with the PALPVI control strategy.

namely the closed-loop input impedance $Z_{\mathrm{cpl\_in}}(s)$, the closed-loop reverse current-ratio transfer function $G_{\mathrm{cpl\_ii}}(s)$, the closed-loop audio-susceptibility $G_{\mathrm{cpl\_vv}}(s)$, and the closed-loop output impedance $Z_{\mathrm{cpl\_o}}(s)$ [44]. The two-port small-signal network model of the buck-type CPL with the PALPVI control strategy is illustrated in Fig. 9, where the four closed-loop transfer functions can be derived from Fig. 7, and there are

$$\frac{1}{Z^{\mathrm{P}}_{\mathrm{cpl\_in}}(s)} = \left.\frac{\hat{i}_{\mathrm{bus}}}{\hat{v}_{\mathrm{bus}}}\right|_{\hat{i}_{\mathrm{o}}=0} = \frac{1}{Z_{\mathrm{cpl\_in}}(s)} + \frac{G_{\mathrm{VIR}}(s)}{G_{\mathrm{PALPVI}}(s)} \approx \frac{1}{Z_{\mathrm{cpl\_in}}(s)} + \frac{1}{Z_{\mathrm{VIR}}(s)} \tag{14}$$

$$G^{\mathrm{P}}_{\mathrm{cpl\_ii}}(s) = \left.\frac{\hat{i}_{\mathrm{bus}}}{\hat{i}_{\mathrm{o}}}\right|_{\hat{v}_{\mathrm{bus}}=0} = G_{\mathrm{cpl\_ii}}(s) \tag{15}$$

$$G^{\mathrm{P}}_{\mathrm{cpl\_vv}}(s) = \left.\frac{\hat{v}_{\mathrm{o}}}{\hat{v}_{\mathrm{bus}}}\right|_{\hat{i}_{\mathrm{o}}=0} = G_{\mathrm{cpl\_vv}}(s) + G_{\mathrm{vv\_P}}(s) = G_{\mathrm{cpl\_vv}}(s) + G_{\mathrm{VIR}}(s)\frac{G_{\mathrm{v}}(s)G_{\mathrm{m}}g_{\mathrm{dv}}(s)}{1+T_{\mathrm{op}}(s)} \tag{16}$$

$$Z^{\mathrm{P}}_{\mathrm{cpl\_o}}(s) = \left.\frac{\hat{v}_{\mathrm{o}}}{\hat{i}_{\mathrm{o}}}\right|_{\hat{v}_{\mathrm{bus}}=0} = Z_{\mathrm{cpl\_o}}(s). \tag{17}$$

From (14), the PALPVI control strategy indeed inserts $Z_{\mathrm{VIR}}(s)$ in parallel with $Z_{\mathrm{cpl\_in}}(s)$ to form the expected input impedance $Z^{\mathrm{P}}_{\mathrm{cpl\_in}}(\mathrm{s})$. From (16), the PALPVI control strategy changes the audio-susceptibility $G_{\mathrm{cpl\_vv}}(s)$, that is because $G^{\mathrm{P}}_{\mathrm{cpl\_vv}}(\mathrm{s})$ has one more $G_{\mathrm{vv\_P}}(s)$ than $G_{\mathrm{cpl\_vv}}(s)$. However, as $G_{\mathrm{VIR}}(s)$ is only valid within (f_{osc}–$\Delta f_{\mathrm{osc}}/2$, $f_{\mathrm{osc}}+\Delta f_{\mathrm{osc}}/2$), the PALPVI control strategy has a quite limited effect on the audio-susceptibility. From (15) and (17), the PALPVI control strategy does not change $G_{\mathrm{cpl\_ii}}(s)$ and $Z_{\mathrm{cpl\_o}}(s)$, which means

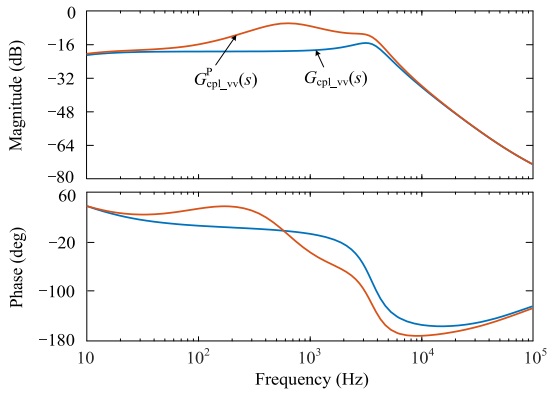


Fig. 10. Bode plots of $G_{\mathrm{cpl\_vv}}(s)$ and $G^{\mathrm{P}}_{\mathrm{cpl\_vv}}(s)$.

the dynamic performance of the CPL to the output current disturbance $\hat{i}_{\mathrm{o}}$ remains unchanged.

In order to verify the above analysis, the cascaded system mentioned in Section III-B is still taken as the example. The Bode plots of the audio-susceptibility transfer functions before and after the PALPVI control strategy is adopted, i.e., $G_{\mathrm{cpl\_vv}}(s)$ and $G^{\mathrm{P}}_{\mathrm{cpl\_vv}}(\mathrm{s})$, are given in Fig. 10. Obviously, their differences are mainly within the medium-frequency range. Considering that there is almost no ac components in this frequency range when the cascaded system operates stably. Therefore, the proposed PALPVI control strategy hardly affects the steady-state output voltage of the CPL in stable operation.

IV. Cases Study and Experimental Verification

A. System Design

In this section, a 48–24–12 V cascaded dc system prototype is built to verify the feasibility and effectiveness of the proposed PALPVI control strategy, and its structure is shown in Fig. 11(a). The switching frequency is 50 kHz. The main parameters are given in Table II. The control is completed with the digital signal processor TMS320F 28335. It should be pointed out that the experimental system shown in Fig. 11(a) only contains two voltage sensors.

The digital realization of $G_{\mathrm{VIR}}(s)$ is shown in Fig. 11(b), here, the backward difference is adopted from the s-domain to z-domain. The coefficients in the difference equation of $G_{\mathrm{VIR}}(z)$ can be calculated by (13), and there are

$$k_1 = -k_2 = a_1 T_s/a_2, \quad k_3 = 2 - a_3 T_s/a_2$$
$$k_4 = a_3 T_s/a_2 - a_4 T_s^2/a_2 - 1 \tag{18}$$
$$a_1 = \pi H_2 D_2 k_{\mathrm{R}} f_{\mathrm{osc}}/Q_{\mathrm{R}}, a_2 = 1$$
$$a_3 = 2\pi f_{\mathrm{osc}}/Q_{\mathrm{R}}, a_4 = (2\pi f_{\mathrm{osc}})^2 \tag{19}$$

where T_s is the sampling period and its value is 20 μs; for k_{R}, to completely eliminate the negative impedance characteristic of the CPL, its value should be greater than 1; here, k_{R} is taken as 2 to reserve a certain stability margin; Q_{R} is taken as 0.707 to ensure a relatively narrow pass-band.

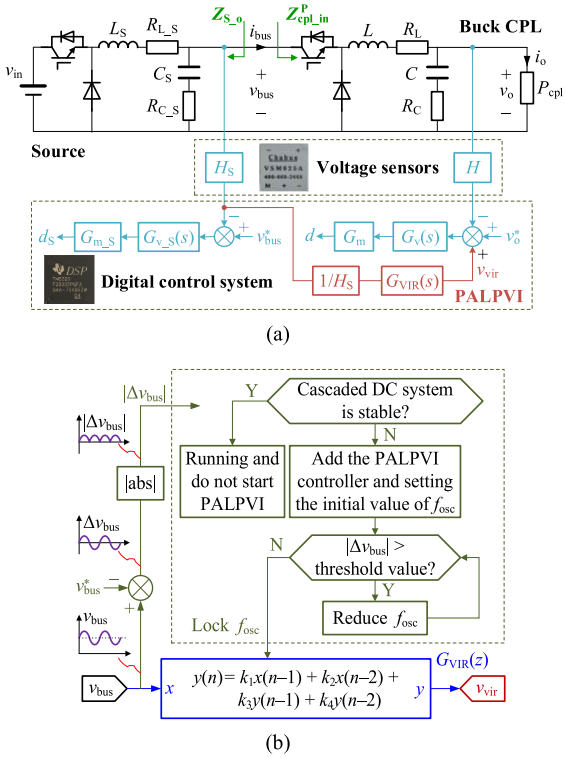


Fig. 11. Realization of the proposed PALPVI control strategy. (a) Experimental system. (b) Realization of $G_{\mathrm{VIR}}(s)$.

According to Fig. 11(b), first, the ac component Δv_{bus} can be obtained by the difference of the bus voltage v_{bus} and its reference v^*_{bus}. If the cascaded system operates stably, the absolute value $|\Delta v_{\mathrm{bus}}|$ contains the switching ripple and is usually very small; while when the cascaded system is unstable, $|\Delta v_{\mathrm{bus}}|$ contains the low-frequency f_{osc} component and cannot be ignored. Hence, the system stability can be judged by comparing $|\Delta v_{\mathrm{bus}}|$ with a threshold value. Generally speaking, the threshold value should be greater than the maximum of the allowable ripple and fluctuation of dc bus voltage when the system operates normally. Here, 2% of the bus voltage is taken as an example, i.e., 0.48 V. When $|\Delta v_{\mathrm{bus}}|$ is greater than the threshold value, the system is considered unstable, and the PALPVI control strategy will start working. Once the PALPVI control strategy works, $G_{\mathrm{VIR}}(z)$ will be calculated based on a preset maximum value of f_{osc}. As mentioned in Section II, $f_{\mathrm{L\_c}} >> f_{\mathrm{osc}}$, hence the maximum value of f_{osc} can be set to $f_{\mathrm{L\_c}}$. If the system is still unstable, it indicates that the current f_{osc} is not the actual system oscillation frequency. So, f_{osc} will be reduced until the cascaded system is stabilized. As soon as the right f_{osc} is found, it will be locked unless the cascaded system oscillates again (such as P_{cpl} increases). Note that, the decreasing value of f_{osc} should be much smaller than the bandwidth of the PALPVI controller. Meanwhile, its value cannot be too small, otherwise the locked f_{osc} may be too far from its actual value to achieve the best control effect. Considering that the oscillation frequency of dc bus voltage is always within the range of 200 Hz–1 kHz. Therefore, the decreasing value is set as the 5% of the minimum of all possible bandwidth, that is, $5\% \times 200/0.707$ Hz $= 14$ Hz.

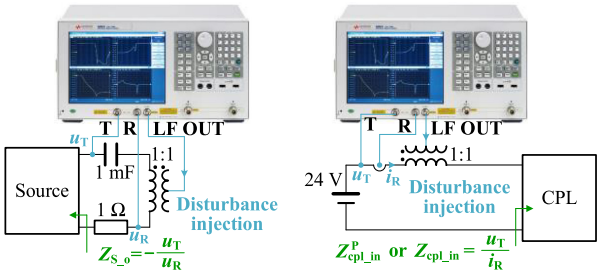


Fig. 12. Impedance measurement methods based on the network analyzer Agilent E5061B. (a) Output impedance. (b) Input impedance.

B. Cases Study

In order to analyze and verify the control effect of the proposed PALPVI control strategy under different power levels, two cases are set, that is, Case 1: $P_{\rm cpl} = 45.6$ W and Case 2: $P_{\rm cpl} = 81.6$ W. The system shown in Fig. 11(a) is simulated in the PLECS, and its experimental prototype is tested by the network analyzer Agilent E5061B. The source output impedance and CPL input impedance are measured under these two cases. The measurement methods based on the Agilent E5061B are given in Fig. 12. For the output impedance measurement circuit shown in Fig. 12(a), the sinusoidal frequency-changeable signal generated by Agilent E5061B is injected into the source output side via an isolation transformer with the turns-ratio of 1:1. The 1 mF capacitor is used to isolate dc current, and the voltage $u_{\rm R}$ of the 1 Ω resistor is equal to the disturbance response current. For the input impedance measurement circuit shown in Fig. 12(b), the sinusoidal frequency-changeable signal is directly injected into the load input side via an isolation transformer with the turns-ratio of 1:1. Different from Fig. 12(a), the air gap must be added in the isolation transformer because the dc current flows through its secondary side. Meanwhile, the magnetic core must be selected with a large size to ensure sufficient excitation inductance at low frequency. The simulation and measurement results are illustrated in Figs. 13 and 14 for the two cases, respectively. Note that these results are the average values of the three measurements.

In Case 1, as shown in Fig. 13(a), before the PALPVI control strategy is adopted, $|Z_{\rm S\_o}(j\omega)|$ intersects $|Z_{\rm cpl\_in}(j\omega)|$ at the frequency about 600 Hz, and at this frequency, the impedance phase difference $\varphi(Z_{\rm S\_o}(j\omega)) - \varphi(Z_{\rm cpl\_in}(j\omega)) = 198^\circ > 180^\circ$. Hence, the cascaded system is unstable and there will be a low-frequency ac oscillation at about 600 Hz in the bus voltage $v_{\rm bus}$. As shown in Fig. 13(b), when the PALPVI control strategy is added, although $|Z_{\rm S\_o}(j\omega)|$ still intersects $|Z^{\rm P}_{\rm cpl\_in}(j\omega)|$, the phase of the CPL input impedance, i.e., $\varphi(Z^{\rm P}_{\rm cpl\_in}(j\omega))$, increases significantly near the intersection frequency and falls within $(-90^\circ, 0^\circ)$, which indicates that the negative impedance characteristic of the CPL near the system oscillation frequency is completely eliminated.

In Case 2, as shown in Fig. 14(a), before the PALPVI control strategy is adopted, $|Z_{\rm S\_o}(j\omega)|$ intersects $|Z_{\rm cpl\_in}(j\omega)|$ at the frequency about 580 Hz, and the impedance phase difference $\varphi(Z_{\rm S\_o}(j\omega)) - \varphi(Z_{\rm cpl\_in}(j\omega)) = 225^\circ > 180^\circ$. Hence, the cascaded system is unstable and there will be a low-frequency ac oscillation component at about 580 Hz in the bus voltage

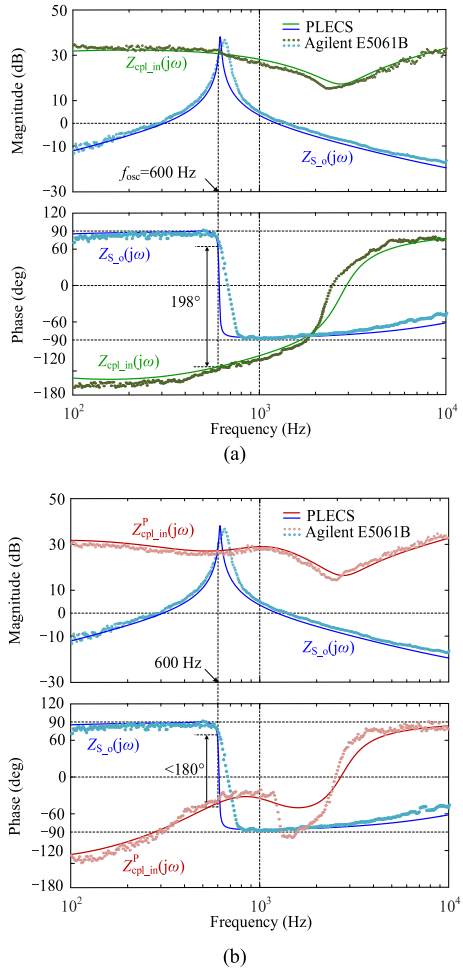


Fig. 13. Impedance frequency characteristics of the cascaded system under case 1. (a) Without PALPVI. (b) With PALPVI.

$v_{\rm bus}$. When the PALPVI control strategy is added, as shown in Fig. 14(b), although $|Z_{\rm S\_o}(j\omega)|$ still intersects $|Z^{\rm P}_{\rm cpl\_in}(j\omega)|$, the phase difference $\varphi(Z_{\rm S\_o}(j\omega)) - \varphi(Z^{\rm P}_{\rm cpl\_in}(j\omega)) < 180^\circ$. Therefore, in this case, the cascaded system can also operate stably with the impedance reshaping.

C. Experimental Verification

In order to further verify the correctness and effectiveness of the proposed PALPVI control strategy, the experimental testing of the two cases are conducted. The experimental results are illustrated in Figs. 15–17, where the waveforms of the bus voltage $v_{\rm bus}$, the CPL output voltage $v_{\rm o}$, and current $i_{\rm o}$ are shown.

In Case 1, before applying the PALPVI control strategy, as shown in Fig. 15(a), the cascaded system is unstable and the low-frequency oscillation appears in $v_{\rm bus}$ at about 602 Hz. Note that this oscillation is not the steady-state ripple. Based on [45], the output voltage ripple of a dc–dc converter arises from the incomplete attenuation of the switching harmonics by the low-pass filter. However, from Fig. 15(a), the oscillation frequency is much lower than the switching frequency and its amplitude is much larger than the steady-state ripple, which means the bus

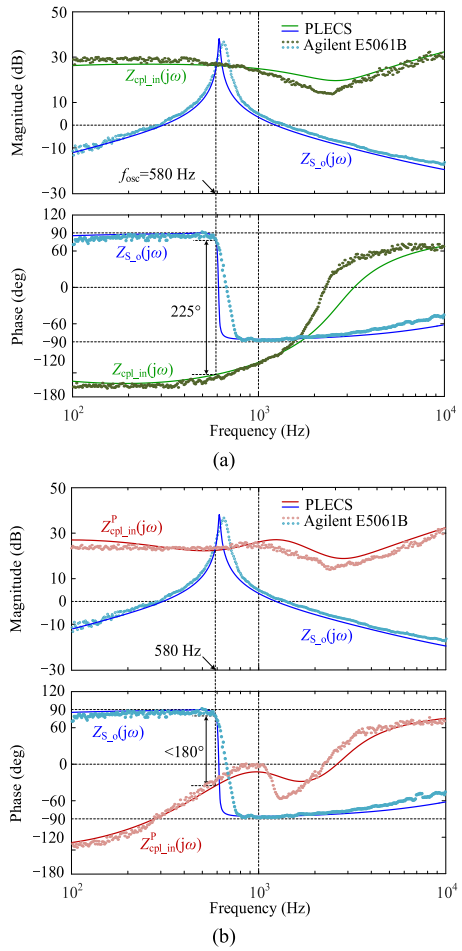


Fig. 14. Impedance frequency characteristics of the cascaded system under case 2. (a) Without PALPVI. (b) With PALPVI.

voltage is not in steady state and the system is unstable. After applying the PALPVI control strategy, the cascaded system can operate stably, as shown in Fig. 15(b). These experimental results are basically the same as the prediction from Fig. 13. When the PALPVI control strategy takes effect, the dynamic waveforms are shown in Fig. 15(c), it can be seen that the proposed PALPVI control strategy can quickly stabilize the system and does not affect the steady-state operation point of the system.

Similarly, the results of Case 2 are provided in Fig. 16. Fig. 16(a) and (b) is the waveforms of the cascaded system without and with the PALPVI control strategy, respectively. It can be seen that, without the PALPVI, the system operates unstably and there is about 574-Hz low-frequency oscillation in $v_{\rm bus}$, but turns stable immediately after the PALPVI is added, which coincides well with the prediction from Fig. 14. The dynamic waveforms shown in Fig. 16(c) further verify the quick and no steady-state error response of the PALPVI control strategy.

Fig. 17 is provided to verify the power adaptability of the PALPVI control strategy. When the system switches between Cases 1 and 2, Fig. 17(a) shows the transient experimental waveforms without the PALPVI control strategy. Obviously, with the increase of $P_{\rm cpl}$, the system oscillation amplitude increases. Fig. 17(b) is the counterpart of Fig. 17(a) after applying the PALPVI control strategy. By comparison, the PALPVI control strategy can suppress the system oscillation under different cases, which confirms the good power adaptability of the proposed PALPVI control strategy.

D. Adaptability of the Proposed PALPVI Scheme Under Different Source Scenarios

According to the design principles and controller function of the proposed PALPVI scheme shown in Section III, different sources only correspond to the different oscillation frequencies and do not affect the other controller parameters. Therefore, it can be predicted that the proposed PALPVI scheme is still effective under different source scenarios. To prove this conjecture, a comparative experiment of Case 2 is implemented, called Case 3 hereinafter. In Case 3, the source is only a 24 V dc power supply and an *LC* filter, as shown in Fig. 18(a). Note that the bus voltage sensor still remains. In this case, the source output impedance can be expressed as

$$Z_{\rm S\_o} = \frac{(sL_{\rm S} + R_{\rm L\_S})(1/sC_{\rm S} + R_{\rm C\_S})}{(sL_{\rm S} + R_{\rm L\_S}) + (1/sC_{\rm S} + R_{\rm C\_S})} \tag{20}$$

where $L_{\rm S} = 5840$ mH, $R_{\rm L\_S} = 0.14\ \Omega$, $C_{\rm S} = 88$ μF, and $R_{\rm C\_S} = 0.23\ \Omega$.

The experimental waveforms are shown in Fig. 18(b). When the PALPVI control strategy is invalid, the low-frequency oscillation occurs at about 186 Hz. While after the PALPVI control strategy is added, the system oscillation is quickly suppressed. Combined with Case 2, it can be concluded that the PALPVI is adaptive to different source scenarios.

E. Impact on the Dynamic Performance of the Load Converter

According to the deduction and analysis in Section III-C, the proposed PALPVI scheme changes the audio-susceptibility $G_{\rm cpl\_vv}(s)$ of the load converter in the medium-frequency range. To further show this negative impact in a straightforward way, Fig. 19 shows the experimental waveforms of the load converter without/with the PALPVI control strategy under Case 2 when its input voltage steps from 24 to 30 V. Note that the frequency $f_{\rm osc}$ in PALPVI is set as 574 Hz according to Fig. 16(a). It can be seen that compared with the original control of the load converter, the PALPVI control strategy only brings a slight increase in overshoot and dynamic response time. According to (16) and Fig. 10, the reason for this result is that the audio-susceptibility $G_{\rm cpl\_vv}(s)$ increases after the PALPVI control strategy is added, which means if a disturbance near frequency $f_{\rm osc}$ appears in $v_{\rm bus}$, this disturbance will transfer from $v_{\rm bus}$ to $v_{\rm o}$ via $G_{\rm cpl\_vv}(s)$, then, a lager disturbance happens in $v_{\rm o}$.

Despite all this, there is still no need to worry about this impact. That is because the dc bus voltage $v_{\rm bus}$ is also stable when the system operates stably. Even if the large amplitude jump of $v_{\rm bus}$ occurs, it will be blocked by the protection devices.

V. Discussion

A. Negative Impact on Converter Dynamic Characteristics

In fact, one of the most concerned problems about the virtual impedance control is its negative impact on the converter dynamic performance, whether for the source converter or load

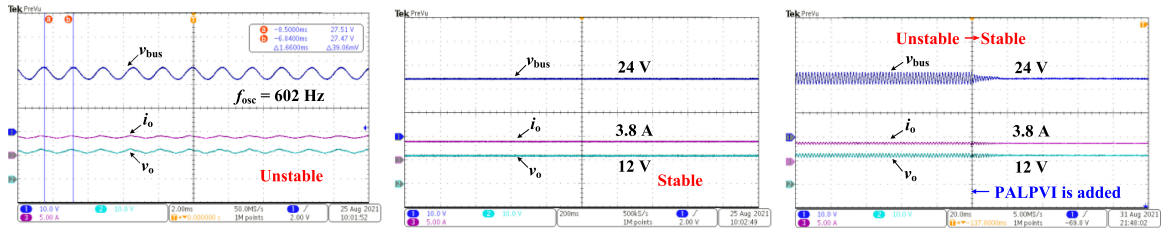


Fig. 15. Experimental waveforms of the cascaded system under Case 1. (a) Before the PALPVI control strategy is added. (b) After the PALPVI control strategy is added. (c) Dynamic switching process.

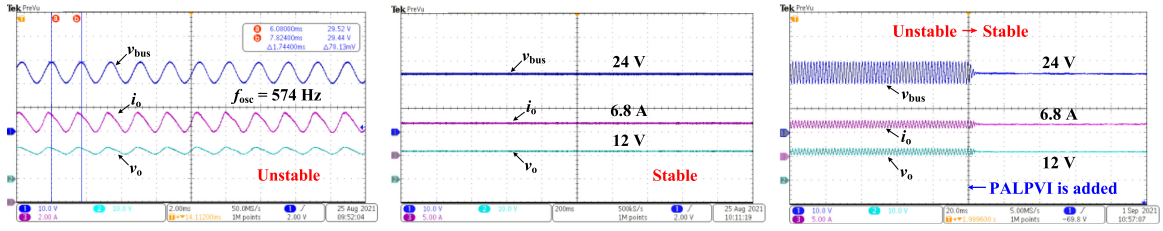


Fig. 16. Experimental waveforms of the cascaded system under Case 2. (a) Before the PALPVI control strategy is added. (b) After the PALPVI control strategy is added. (c) Dynamic switching process.

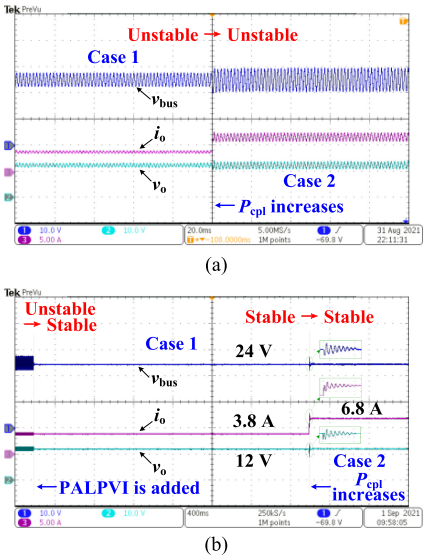


Fig. 17. Dynamic switching experimental waveforms from Case 1 to Case 2. (a) Without the PALPVI control strategy. (b) With the PALPVI control strategy.

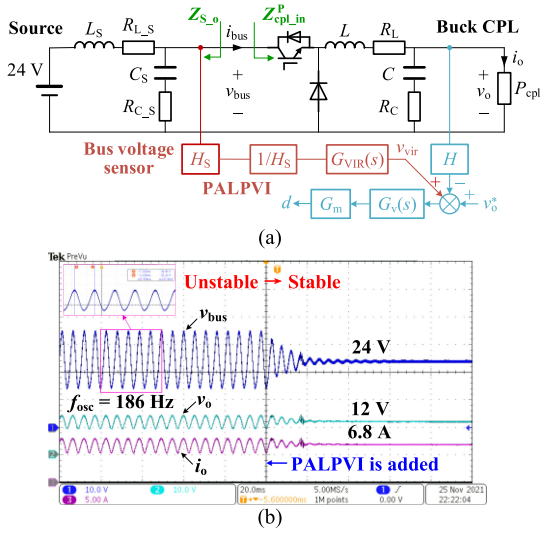
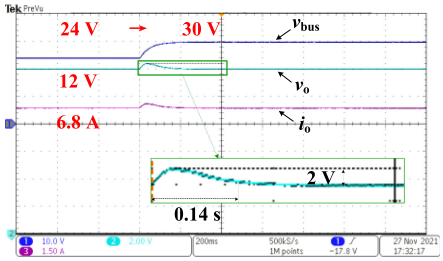


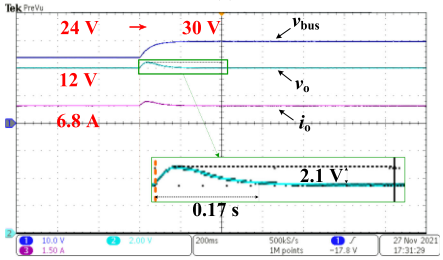
Fig. 18. System and experiment results under Case 3. (a) Experimental system. (b) Dynamic experiment waveforms.

converter. In order to reduce this negative impact, the following two methods are effective.

1) The valid frequency range of the virtual impedance control should be reduced as much as possible.
   As mentioned in [35], [39], [41], [42], [46], and this article, to suppress the cascaded system oscillation at frequency f_{osc}, the virtual impedance control should only adjust the converter impedance around f_{osc}, that is, (f_{osc}–$\Delta f_{osc}/2$, f_{osc}+$\Delta f_{osc}/2$), while it is almost invalid in other frequency ranges. For this purpose, the band-pass filter must be adopted in the impedance reshaping schemes, so that the low-frequency and high-frequency dynamic characteristics of the converter can be well maintained. Hence, the impedance reshaping schemes without a band-pass filter may have more serious negative impact, such as [37] and the direct method proposed in [39].
2) The suitable location and connection way of the virtual impedance can further reduce the negative impact.
   For the input impedance reshaping of the load converter, the LPVI scheme reshapes $Z_{cpl\_in}(s)$, slightly changes $G_{cpl\_vv}(s)$, while remaining $G_{cpl\_ii}(s)$ and $Z_{cpl\_o}(s)$ unchanged. By comparison, the LSVI control strategy completely changes the four closed-loop transfer functions of



(a)



(b)

Fig. 19. Dynamic experimental waveforms of the load converter. (a) Without the PALPVI control strategy. (b) With the PALPVI control strategy.

TABLE III
CONTROLLER ORDERS OF LPVI SCHEMES

Schemes	Orders
The direct method proposed in [39] and the proposed PALPVI scheme	2
The optimal method proposed in [39] and the scheme in [41]	3
The schemes in [35], [42] and [46]	More than 3

the load converter [29]. Therefore, the negative impact of the LPVI on load converter is far less than that of the LSVI.

Note that the above measures are all considered in the PALPVI control strategy; as a result, the proposed scheme has almost no side effect on the dynamic performance of CPL.

B. Implementation Complexity Comparison With Some Existing Schemes

The PALPVI control strategy proposed in this article belongs to the LPVI scheme. Some similar impedance shaping schemes have been discussed in previous literature. To elaborate the features of the PALPVI control strategy, the implementation complexity of these LPVI schemes will be analyzed and compared from the following three aspects:

1) *Controller order:* Obviously, the higher the controller order, the more difficult its digital implementation is. According to [35], [37], [39], [41], [42], [46], and (12), the controller orders of these LPVI schemes are shown in Table III. It can be seen that the proposed PALPVI scheme is one of the two simplest schemes for digital implementation.

2) *Number of sensors required:* For any LPVI scheme, it is known that the bus voltage must be detected and introduced into its output voltage control loop. Therefore, if the frontend source is a bus-voltage-controlled converter, the bus voltage signal can be obtained from the source converter, as shown in Fig 11(a). Even if the source converter is not accessible, only a bus voltage sensor is required. Besides, according to [35], [37], [39], [41], [42], and [46], because the load power appears in the expressions of their compensation controllers, an additional power detection circuit or a current sensor needs to be installed to obtain the load power. By comparison, the compensation controller of the proposed PALPVI scheme, that is, $G_{\mathrm{VIR}}(s)$, is independent of the load power, which means it requires less sensors than the existing LPVI schemes.

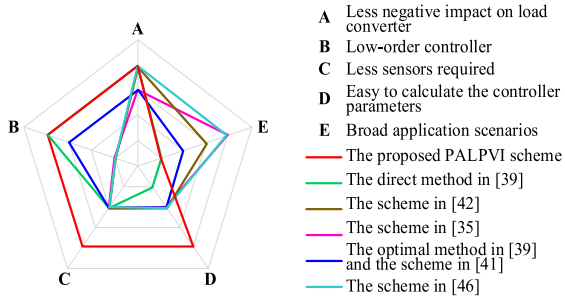


Fig. 20. Comparison of some PALPVI schemes.

3) *Calculation difficulty of the controller parameters:* It should be pointed out that, if the controller parameters of an LPVI scheme is difficult to calculate, its realizability is still poor even if the order of its compensation controller transfer function is low and fewer sensors are required. For example, in the direct method proposed in [39], its compensation controller is only composed of a second-order band-pass filter and a gain coefficient. However, the gain coefficient not only is related to the system oscillation frequency, circuit parameters, control parameters, and load power but also can only be obtained by the difficult complex-valued operation. The similar problem appears in [41] and the optimal method is proposed in [39]. Based on (13), the controller gain coefficients of the proposed PALPVI scheme are constants and easy to design.

In summary, Fig. 20 compares the performance of these LPVI schemes. It can be seen that although the proposed PALPVI control strategy has the application scenario limits, it has the advantages of simple structure and parameter calculation, less sensors, and easy to implement. More importantly, its power adaptability is novel and attractive.

VI. CONCLUSION

In order to eliminate the low-frequency negative impedance characteristic of the buck-type CPL so as to improve the stability of the cascaded dc system, a PALPVI control strategy is proposed in this article, and it has the following features.

1) The compensation controller of the proposed PALPVI scheme is just a two-order band-pass filter independent of the *LC* and control parameters, which is easy to implement and has high reliability.
2) The proposed PALPVI control strategy has strong power adaptability, but does not involve any current sensor or power detection circuit to obtain the load power, which is more cost attractive.

3) The proposed PALPVI scheme only reshapes the input impedance of the buck-type CPL within a very small frequency range around the system oscillation frequency, thus has almost no negative impact on the dynamic performance of the CPL.
4) The proposed PALPVI scheme is effective under different source scenarios.

Finally, the effectiveness of the PALPVI control strategy is verified by experiments.

APPENDIX

This appendix will present detailed expression of $G_{\mathrm{PALPVI}}(s)$ mentioned in Section III. Substituting the transfer functions of Table I, (1) and (2) into (6), there is

$$G_{\mathrm{PALPVI}}(s)=\frac{a_3s^3+a_2s^2+a_1s+a_0}{b_3s^3+b_2s^2+b_1s+b_0} \tag{A.1}$$

where these coefficients can be calculated as

$$\begin{cases} a_3=DV_{\mathrm{bus}}LC \\ a_2=DV_{\mathrm{bus}}C(R_L+R_C)+HG_{\mathrm{m}}V_{\mathrm{o}}V_{\mathrm{bus}}k_{\mathrm{p}}R_CC \\ a_1=DV_{\mathrm{bus}}+HG_{\mathrm{m}}V_{\mathrm{o}}V_{\mathrm{bus}}(k_{\mathrm{p}}+k_{\mathrm{i}}R_CC) \\ a_0=HG_{\mathrm{m}}V_{\mathrm{o}}V_{\mathrm{bus}} \end{cases} \tag{A.2}$$

$$\begin{cases} b_3=G_{\mathrm{m}}P_{\mathrm{cpl}}LCk_{\mathrm{p}} \\ b_2=G_{\mathrm{m}}C[(P_{\mathrm{cpl}}R_L+P_{\mathrm{cpl}}R_C+V_{\mathrm{o}}^2)k_{\mathrm{p}}+P_{\mathrm{cpl}}Lk_{\mathrm{i}}] \\ b_1=G_{\mathrm{m}}[P_{\mathrm{cpl}}k_{\mathrm{p}}+(P_{\mathrm{cpl}}R_L+P_{\mathrm{cpl}}R_C+V_{\mathrm{o}}^2)Ck_{\mathrm{i}}] \\ b_0=G_{\mathrm{m}}P_{\mathrm{cpl}}k_{\mathrm{i}} \end{cases} \tag{A.3}$$

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