A PFM Boost Harvester With System-Level Self-Tuned Maximum Power Point Tracking

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***Abstract*—This article presents a low-overhead energy harvesting and delivery system (EHDS) with pulse frequency modulated (PFM) integrated voltage regulator (IVR) power conversion and self-tuned maximization of system output power. A novel load-inclusive time-based maximum power point tracking (LI-TB-MPPT) is developed to provide centralized tuning of PFM-IVR operation based on both source capabilities and load demand on-the-fly, and a configurable fractional sample and hold circuit provides adaptive harvesting window control. The proposed EHDS enables robust harvesting while relieving the use of high passives, with over two orders of magnitude reduction, at the cost of only slight decrease in end-to-end efficiency compared to prior works. Furthermore, a low-overhead wake-up assist circuit utilizes cold-configuration of harvesting sources for efficient and accelerated cold-start. The proposed EHDS is demonstrated in a 65 nm CMOS process with commercial photovoltaic energy harvesting modules. Using only 1.2 and 1 μH of passives, measured results show a peak 74.9% end-to-end efficiency (simulated up to 85% at 47μH) and a fast startup time of 3.8 ms. Up to 15% increase in conversion efficiency against load and input voltage variations is achieved with LI-TB-MPPT. The results demonstrate a compact solution for self-sustained cost-restricted stand-alone systems.**

***Index Terms*—Cold-start, energy harvesting, maximum power point tracking (MPPT), pulse frequency modulation.**

I. Introduction

SELF-POWERED devices that operate in stand-alone environments are critical foundations for Internet of things applications. One of the key challenges for these end-devices is to provide a robust, yet low-cost, low-overhead system for power management. Scavenging energy from harvesting sources [1], [2] and smart management of power delivery [3]–[5] have become integral parts of energy harvesting and delivery systems (EHDS) for self-powered devices. Compared to power conversion from steady sources, the power that harvesting sources can provide not only depends on the biasing conditions of the transducer but also the strength of the input (light, heat, etc.), which can be highly variable and intermittent/unstable [6], [7]. Therefore, additional measures on top of traditional power delivery systems are required. Cold-start methods [6], [8], [9] allow the main power management unit (PMU) to enter typical operating conditions from power-free ("cold") states by generating sufficient voltage (V_{CTRL}). Maximum power point tracking (MPPT) methods are used to dynamically adapt to variations in harvesting conditions [1], [5], [10]–[13]. Fig. 1 shows a schematic for a typical EHDS.

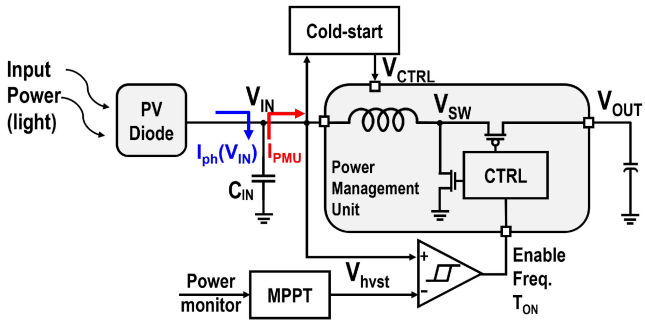

Fig. 1. Schematic of generic EHDS.

However, existing cold-start and MPPT present the following drawbacks for small-scale self-powered systems.

1) *Large overhead:* Devoted auxiliary converters and/or larger harvesting sources are needed to address low-efficiency power conversion during cold-start.
2) *Large passives:* High passives (L/C) are needed to provide input voltage filtering/regulation and to increase conversion efficiency of the PMU.
3) *Load decoupling:* Source-oriented MPPT prioritizes regulation of harvesting voltage and does not consider change in the conversion efficiency of the power management unit (PMU) under variations in load and input power.

In this article, we present a pulse-frequency modulated (PFM) EHDS that uses innovative cold-configuration, adaptive harvesting window control and system-output power evaluation to address these limitations. A self-monitoring wake-up assist (WUA) circuit is designed to bypass low-efficiency harvesting periods to accelerate bootstrap mode cold-start while introducing minimal footprint overhead. A load-inclusive time-based MPPT (LI-TB-MPPT) scheme implements a power evaluation metric derived through PMU output regulation signals. This allows

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LI-TB-MPPT to include the impact of load variations during on-the-fly self-tuning. The output-based power evaluation opens up the opportunity to relieve harvesting voltage regulation restrictions and reduces filtering demand for the harvesting source. This advantage is further exploited by a configurable-fraction fractional sample and hold (FSH) circuit that allows open-circuit-free sampling and control of the harvesting window. Fractions for the FSH circuit are configured along with the PMU switching frequency by the LI-TB-MPPT circuit to optimize system-level harvesting and conversion efficiency for maximum output power. On-the-fly self-tuning and reconfiguration of the EHDS is performed with a standard hill-climbing perturb and observe (P&O) algorithm within LI-TB-MPPT.

In summary, the main contributions of this article include the following.

1) A novel PFM EHDS control scheme is proposed with high tolerance for reduced passives, which contributes to both reduced system cost and shortened wake-up time.
2) A low-overhead time-based output power estimation metric that relieves dependency on harvesting voltage regulation during observation for standard P&O MPPT.
3) A configurable FSH scheme that maximizes utilization of harvesting resources during IDLE periods of PFM operation by controllably increasing harvesting windows.
4) A low area/power overhead WUA circuit that provides further acceleration of bootstrapped cold-start by enabling reliable cross-EHDS cold-configuration.

A test-chip is implemented in a 65 nm CMOS technology node. Full EHDS operation is demonstrated and characterized with commercial photovoltaic (PV) harvesting sources. With a total capacitance/inductance of only 1.2 (input: 0.1 μF) and 1 μH, the proposed system demonstrates a peak end-to-end efficiency of 74.9%. Simulated results project an end-to-end efficiency of up to 85% when only the inductance is increased to 47 μH. The LI-TB-MPPT-controlled FSH fraction tuning achieves a 9% increase in harvested power, and a 15% increase in conversion efficiency is observed with switching frequency tuning. The wake-up assisted cold-start achieves 2$\times$ reduction in cold-start time and 6$\times$ reduction in minimum illumination can be achieved with the WUA circuit.

The rest of this article is organized as follows. Section II outlines the background of prior EHDSs. Section III explains design objectives of this work. Section IV introduces the proposed WUA circuitry and power evaluation/optimization for system-focused MPPT. Section V details the implementation of the design. Section VI presents measurement results and comparison with prior state of the art. Finally, Section VII concludes this article.

II. Background

A. Cold-Start

Cold-start is a unique operation for EHDSs in which the system's control voltage starts from floating/grounded initial conditions and wakes up with harvested power. It is critical for self-powered EHDSs as it enables restoration of operation from power-drained conditions. Bootstrapped cold-start requires voltage-invariant designs to allow boosting from low voltages [9]. Before regulation can be reached, the PMU will be always-ON and continuously draws current from the harvesting source to boost the output voltage (which is connected back to the control voltage of the PMU). During this process, power consumption from control blocks (oscillator, analog comparators, power stage, etc.) within the PMU can be considered as increased load of the EHDS. The additional power burdens bootstrap operation and can result in excessive current drawn from the harvesting node. This reduces the harvesting voltage, and further lengthens cold-start periods.

A common approach is to have a secondary converter that is devoted for cold-start [6] to ensure that control power is decoupled from the load through a two-stage cold-start arrangement. This is usually implemented via switch-capacitor converters as they do not need high-performance voltage/current sensors to perform zero-current sensing [14]. Prior work has also demonstrated one-shot cold-start where only the control voltage of the low-side gate and driver needs to be charged [8] with the charge-pump. However, these designs present significant area overhead from large on-chip capacitance and increased transistor sizing to reduce transistor resistance at low voltages.

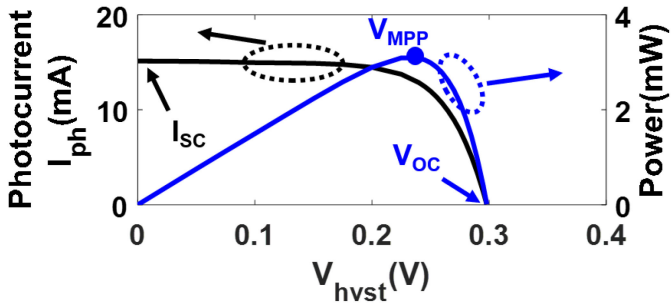


Fig. 2. *I–V* and *P–V* characteristics of PV devices.

B. Maximum Power Point Tracking

In most harvesting sources, there is an optimal operating point where the source generates the maximum power. For example, in a PV module [4], [15], [16], the biasing voltage directly modulates the depletion region [17] and the generated photo current (I_{ph}). Fig. 2 shows a plot of current–voltage and power–voltage characteristics for PV devices under fixed input light intensity.

As input power fluctuates, so does the power-voltage profile and V_{MPP} of the device. Therefore, a critical challenge for EHDS designs is dynamically controlling the PMU at the system level to ensure maximum power can be harvested and delivered. One of the most prevalent topologies used in small scale harvesting systems is the fractional open circuit voltage (FOCV) method [5], [10]. FOCV operates based on the assumption that the V_{MPP} is always close to a fixed fraction of the open circuit voltage (V_{OC}), regardless of variations in input power. Therefore, simple voltage division is sufficient for creating an adequately well reference voltage for MPPT once V_{OC} is obtained. FOCV MPPT benefits from its simplicity, but it also introduces undesired

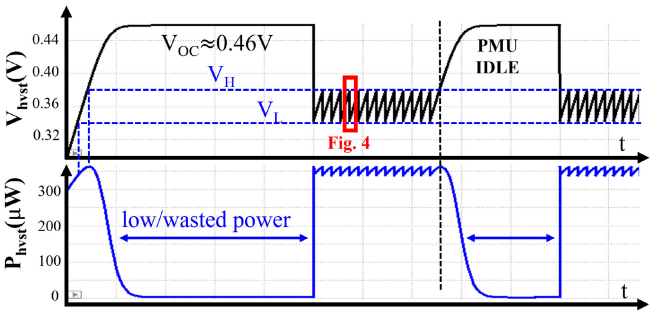


Fig. 3. Transient of single-input single-output PFM boosting. (Highlighted harvesting window in Fig. 4.)

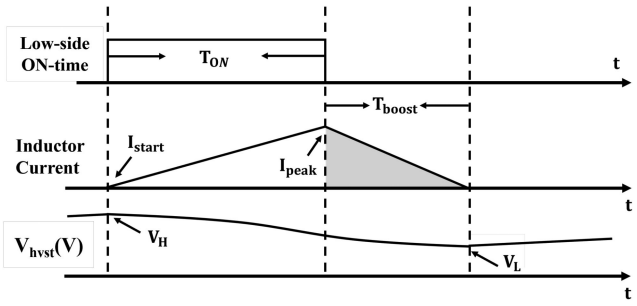


Fig. 4. Current drawn from a single inductor pulse and drop in voltage.

area/wasted-energy overhead due to the need to obtain $\mathbf{V_{OC}}$ [2], [11].

Since the harvesting voltage (V_{hvst}) dynamically varies with both the current generated by the harvesting source and the current drawn by the PMU (see Fig. 1), one can also indirectly modulate the harvesting voltage by carefully controlling the impedance of the PMU. Several different impedance matching techniques have been devised to bias the harvesting source. For example, impedance matching for MPPT in EHDSs can be performed by controlling the PMU duty cycle to modulate the harvesting voltage [6]. At equilibrium, the net increase in harvesting voltage (charged by the harvester) on the input capacitor will be equal to the net decrease (discharged with current drawn by PMU). To interface with low-power PMUs such as pulse frequency modulation (PFM) integrated voltage regulators (IVRs), input hysteresis comparators [3], and switching frequency modulation [8] have both been implemented in prior works. However, due to burst-harvesting periods, the use of high capacitance ($> 10\mu$F) and high inductance ($> 10\mu$H) is often necessary to filter/dampen harvesting voltage ripple for MPPT and reduce current ripple for improved conversion efficiency [4], [6], [8], [13], [18]–[20]. To prevent wasted power when the PMU is idle (see Fig. 3) and/or shortage in harvested power when the PMU is active, design complexity to enable multiple (backup) resources are often necessary [3], [4], [14]. However, while source-oriented MPPT schemes such as FOCV optimize harvesting efficiencies of sources, they cannot capture the conversion efficiency of the PMUs.

C. Dependence on Passive Filtering

Fig. 3 shows an example of the harvesting voltage and power waveforms for a typical PFM EHDS. PFM operation provides superior low-power end-to-end efficiency through allowing PMU-IDLE periods under low load [21]. However, even though average current is low, large input capacitance/inductance are needed to ensure the MPPT window can be successfully regulated under spurious inductor current pulses when the PMU is ACTIVE [5]. A direct impact of this is that large, high-quality passives increase EHDS cost. While output passives depend on load requirements, a theoretical derivation of the minimum requirement of input-filtering passives can be derived as follows. Fig. 4 shows illustrative inductor current and harvesting voltage (highlighted portion in Fig. 3) waveforms with starting current (I_{start}) as zero. Assuming ideal boost regulator behavior, linear approximations can be used to compute inductor current increase/decrease [9]. With an ON-time of T_{on}, the total charge drawn from a single inductor current pulse (Q_{pulse}) is

$$Q_{\text{pulse}} = \frac{I_{\text{peak}}(T_{\text{ON}} + T_{\text{boost}})}{2} \tag{1}$$

where I_{peak} is the peak current and T_{boost} is the boosting period, and represented as

$$I_{\text{peak}} \approx \frac{V_H T_{\text{ON}}}{L} \tag{2}$$

$$T_{\text{boost}} \approx \frac{I_{\text{peak}} L}{V_{\text{OUT}} - V_H} \tag{3}$$

where V_H is the higher threshold of the input hysteresis (see Fig. 3), L is the inductance and V_{OUT} is the output voltage of the PMU. Combining (1) to (3), we can compute Q_{pulse} as

$$Q_{\text{pulse}} \approx \frac{V_H T_{\text{ON}}^2}{2\,L}\left(1 + \frac{V_H}{V_{\text{OUT}} - V_H}\right). \tag{4}$$

To maintain input regulation, Q_{pulse} has to be less than the net input of charge from the source and the input capacitor hysteresis charge

$$Q_{\text{pulse}} \leq I_{ph}(V_H) T_{\text{ON}}\left(1 + \frac{V_H}{V_{\text{OUT}} - V_H}\right) + C_{\text{IN}}(V_H - V_L). \tag{5}$$

When I_{ph} is low (limited by form factor, illumination, etc.), high inductance, input capacitance, and/or fast clocks are required to maintain the above inequality. For example, with an input hysteresis of 20 mV from $V_H = 0.48$V to $V_L = 0.46$V, output voltage of 0.8 V, I_{ph} of 1 mA, and a T_{ON} of 8 μs, it can be approximated that $LC \geq 3.8 \times 10^{-9}$, and therefore $> 10\mu$ of input capacitance and inductance are required.

III. Proposed Approach

This article presents a design that realizes a low-passive, low-footprint, low-cost EHDS that addresses the challenges of high passives and large cold-start overhead mentioned in Section II. While reducing C_{IN} and L, it is inevitable that the system will encounter scenarios where typical levels of input voltage hysteresis (<50 mV) become insufficient for output regulation with increased conversion ratio. To maintain output

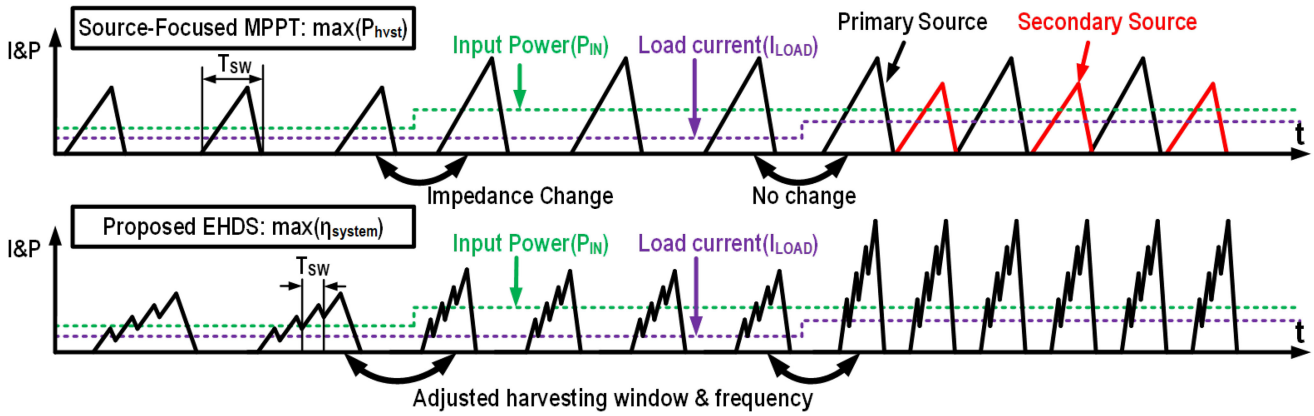


Fig. 5. Conceptual view of the proposed EHDS (tolerates lower L,C) compared to conventional source-focused EHDSs (limited to higher L,C).

regulation, an alternative to adding backup resources (often seen in multi-input–multioutput (MIMO) designs [3]) would be to readjust both the impedance of the PMU and the harvesting operation beyond source-focused MPPT restrictions. Instead of trying to increase EHDS robustness through adding complexity for interfacing with additional resources, the proposed system emphasizes improving harvesting and power delivery efficiency from a single source so that maximum power can be delivered (when required by the load).

Efficiency improvement for low-passive harvesting is made possible by optimizing PMU operation in multiple fronts. In the end, the end-to-end efficiency (η_{ETE}) of an EHDS can be expressed as

$$\eta_{\text{ETE}} = \eta_{\text{hvst}}(P_{\text{src}}, V_{\text{hvst}}) \times \eta_{\text{PMU}}(V_{\text{hvst}}, V_{\text{OUT}}, I_{\text{load}}) \quad (6)$$

where the harvesting efficiency (η_{hvst}) is a function of the power of the input source (P_{src} =light, heat, etc.) and the harvesting voltage. The conversion efficiency of the PMU (η_{PMU}) is a function of harvesting voltage, output voltage (V_{OUT}) and load current (I_{load}) and can also be expressed as

$$\eta_{\text{PMU}} = (P_{\text{hvst}} - P_{\text{con}} - P_{\text{sw}} - P_{\text{ctrl}})/P_{\text{hvst}} \quad (7)$$

where P_{hvst}, P_{con}, P_{sw}, and P_{ctrl} represent the harvested power, power dissipated by conduction loss, and power consumed by switching loss and control circuits, respectively.

As mentioned in Section II, the main bottleneck for cold-start comes from inefficient and possibly unstable harvesting operations before the control voltage enters normal operating ranges (high P_{con}, P_{sw}, and P_{ctrl}). This is addressed to an extent with devoted auxiliary cold-start converters in prior works. The large area overhead from these converters, however, comes from the fact that switch resistance becomes excessively high at low control voltages ($R_{DS,ON} \propto 1/(V_{GS} - V\text{th})$). In this article, we propose utilizing cold-configuration to minimize P_{ctrl}, eliminate P_{sw}, and reduce P_{con} by gating power-hungry blocks in the PMU and enabling autonomous source-stacking to create a temporary high voltage directly.

Fig. 5 illustrates the operation of the proposed EHDS compared to traditional source-focused approaches during normal operation. One of the immediate differences is that the proposed system relies on multi-pulse PFM operation [9] to enhance inductor current build-up when V_{hvst} droops increase with decreased input capacitance. Second, although not shown in the figure, the proposed design will operate with a larger harvesting window to reduce input-hysteresis-induced-P_{SW} under reduced input capacitance. This also increases average P_{hvst} because PMU idle periods can also harvest power to restore V_{hvst}. Third, the system-oriented EHDS controls do not prioritize the source (as in Fig. 3) but adaptively modulates harvesting windows and switching frequency ($1/T_{SW}$) to improve EHDS end-to-end efficiency and support higher load under the same resources. While there does not exist an simple yet accurate expression for $\eta_{\text{PMU}} = f(frequency, V_H - V_L)$, the following will demonstrate the importance of these attributes with two model-simulated test cases. The EHDS model is created by integrating harvesting source characteristics and input voltage transients into a transient-based model for dc–dc PFM BRs [22]. For ease of visualization, we have set the following system parameters: C_{IN}=100 nF, L=2μH, V_{OC}=0.51 V, I_{SC}=2 mA, V_{OUT}=0.8 V, BR current limit=20 mA, and ESR$_{BR}$=4Ω.

A. Frequency Tuning

As the interface between harvesting sources and EHDS output, PMU impedance not only affects harvesting conditions but also the subsequent power conversion. However, traditional source-oriented MPPT approaches often optimize harvesting efficiency of the source and neglect conversion efficiency of the PMU. It has been shown in prior work that oscillator frequency plays a critical role in determining PFM IVR efficiency [9], [22]. Switching frequency for PFM BRs not only affects tradeoffs of switching loss versus conduction loss during the design phase but also inductor current behavior during operation (single-pulse versus multipulse [23]). In certain scenarios, it even determines the maximum load that can be delivered [22].

Fig. 6 shows the average current boosted to the PMU output when different switching frequencies are selected. With the same harvesting window of ~0.1 V, both 16 and 2 MHz cases will have to undergo a restore time of 6μs before the next "packet" of PFM pulses can be activated. The key difference between these two cases is that because 16 MHz enters multi-pulse operation, the inductor current is focused into a shorter "packet." Assuming

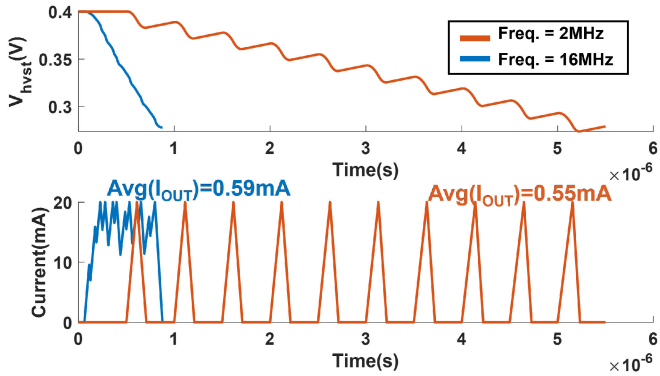


Fig. 6. Impact of different switching frequencies. (Harvesting window $(V_{\max} - V_{\min})$ ~0.1 V).

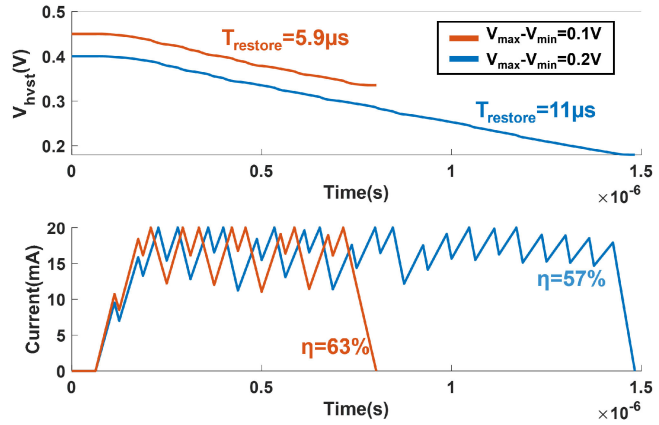


Fig. 7. Impact of different harvesting windows (Frequency =16 MHz).

the EHDS needs to charge an output hysteresis of 50 mV on to 1.1μF output capacitance under 0.5 mA load current, 53 and 18 "packets" are needed for the 16 and 2 MHz cases, respectively. Although a 2-MHz system will exhibit better low-load efficiency, a 16-MHz system can benefit from both reduced ripple losses and the increased 590 mA average output current at high load. Allowing an EHDS to freely reconfigure switching frequency will maximize benefits at varying load. In the proposed system, on-the-fly frequency tuning is made possible by using P&O within a load-inclusive time-based MPPT circuit to control the bias current fed to an analog current-capacitor oscillator [24].

B. Harvesting Window Tuning

As shown in Fig. 6 and (4)–(5), the harvesting window is the main element that determines the amount of charge that is available within a single PFM "packet" under reduced L, C_{IN}, and I_{SC}. Increasing the harvesting window allows reduced switching losses introduced by the input hysteresis. This work exploits this advantage to improve low-passive conversion efficiency of the EHDS. However, different harvesting window sizes can also play a role in determining the system efficiency.

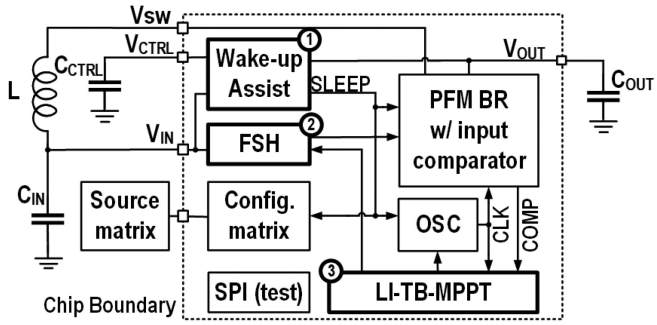


Fig. 8. Schematic of proposed system and target objectives. (a) Cold-start: Wake-up assist. (b) System-focused MPPT: LI-TB-MPPT. (c)V_{OC}-free harvesting voltage control: FSH. (d) Passive dependence reduction: FSH + LI-TB-MPPT.

Fig. 7 shows the impact of selecting different harvesting window sizes and their associated restore times. With a shorter restore time (T_{restore}, time waiting for the input voltage to recharge from $V_{\min}$ to $V_{\max}$), a smaller harvesting window (0.1 V case) generally results in a higher median at low-to-medium load. This also relates to a lower conversion ratio and higher conversion efficiency. On the other hand, the lower $T_{\text{restore}}/(V_{\max} - V_{\min})$ ratio provided with a 0.2 V window indicates that it has a better ability to supply higher loads. In the following section, we will provide detailed derivations of these observations and our approach to embedding adaptive harvesting window control with LI-TB-MPPT into the proposed EHDS.

IV. Proposed Design and System Components

The high-level schematic of the proposed system is presented in Fig. 8. Three main circuits are proposed to realize the proposed approach by assisting and adjusting the main PMU during different phases of harvesting operation. The main PMU consists of a typical PFM boost regulator (BR) [23] with an additional input comparator for harvesting voltage regulation. The proposed blocks are highlighted with bold lines in Fig. 8 and each represent ① wake-up assist circuit (WUA), ② fractional sample & hold (FSH), and ③ load-inclusive time-based MPPT (LI-TB-MPPT).

The key function of the analog WUA is to generate a "SLEEP" signal through monitoring voltage levels of critical nodes within the PMU. This signal is used as a digital reference for cold-configuration of both analog and digital blocks within the system to ensure optimum cold-start performance.

LI-TB-MPPT utilizes timing metrics of PFM BR output regulation to evaluate system efficiency in a manner that includes not only harvesting efficiency of the source, but also conversion efficiency of the PMU and contributions of the load. It implements a P&O algorithm to reconfigure system settings and optimize system power delivery under conversion ratio and load variations.

The FSH is designed as an analog interface between LI-TB-MPPT and the input comparator within the PMU. Instead of relying on a single fixed fraction, such as traditional FOCV approaches, FSH allows multiple discrete fractions to be selected.

The flexibility of configurable fractions allows FSH to perform harvesting voltage sampling without needing to enter V_{OC}.

Low-passive tolerance, which is a key contribution of this work, has been made possible through the joint contribution of both FSH and LI-TB-MPPT circuits. By only requiring timing information of output regulation, LI-TB-MPPT operation is independent of both harvesting voltage variations and PMU operation modes. This means that harvesting window confinements, which is a major limiting factor for inductance and capacitance requirements in traditional source-focused MPPT approaches, can be relieved. This notion is supported in FSH by providing a solution for allowing large harvesting windows to be selected, even when this means that the harvesting source may not be able to restore itself to V_{OC} when the BR is IDLE.

A. Cold-Start: Wake-Up Assist

An advantage of PV harvesting sources is that they can generate relatively high voltage (> 0.2V) in nominal room-light environments. The high V_{OC} from PV modules gives opportunity for using self-powered source configurations to create the necessary kick-start voltage for the main PMU and eliminate the large area overhead associated with the prior need for auxiliary cold-start converters.

A critical challenge for realizing cold-configuration functionality is that the state of digital logic can be hard to determine without explicit RESET triggers. Incorrect cold-configuration of the EHDS can result in system failure. To realize low-overhead cold-start, we propose a WUA circuit that creates a robust "SLEEP" signal even in subthreshold voltages ($<$0.4 V) to guarantee correct initialization of the EHDS during cold-start. This signal is used universally across the EHDS to "assist wake-up operation." For example, the EHDS bypasses low-efficiency switching activity at low voltages completely (PMU is turned OFF) by using the SLEEP signal to bias-gate all analog comparators until the system is ready to enter boot-strapped operation. During this period of time, the WUA internally connects the input voltage (V_{IN}) to the control voltage (V_{CTRL}) for direct, efficient charging (no switching losses from the PMU path). The EHDS also utilizes the SLEEP signal to control harvesting source configuration during cold-start. This ensures that sufficient system-wake-up voltage can be provided by stacking harvesting sources in series when the V_{OC} of a single source is low. Before cold-start is complete, the WUA ensures harvesting sources (when multiple are available) are always configured in series (with SLEEP$=1$) to create a high voltage. After the control voltage is sufficient for typical operation, the WUA reconfigures the source back to its programmed state and connects the system back into bootstrapped mode for higher efficiency.

In this test-chip, the on-chip source configuration matrix has been designed to enable up to three combinations of harvesting sources (stacks of 3, 2 and all parallel) for system characterization coverage, as shown in Fig. 9. A total of 6 on-board photodiodes are integrated on-board to ensure comparable harvested power across configurations. However, this level of complexity and overhead is not necessary for product vehicles. Depending on harvesting source characteristics (mainly V_{OC}) of the end system, WUA cold-start can operate with down to 2, or even a single input source (WUA assists bias-gating and switching-activity bypass). Furthermore, while experiments in this article are performed with off-the-shelf photodiodes for ease-of-access during testing and evaluation of the prototype EHDS, source-configuration can also be embedded into diode-pixels in a similar manner as CMOS active pixel sensor circuits [25] if on-chip harvesting sources are used.

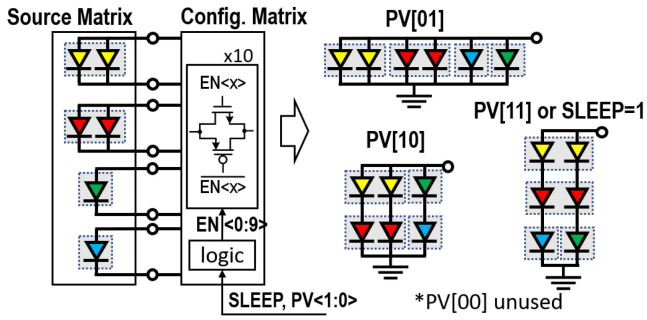


Fig. 9. Possible source configurations.

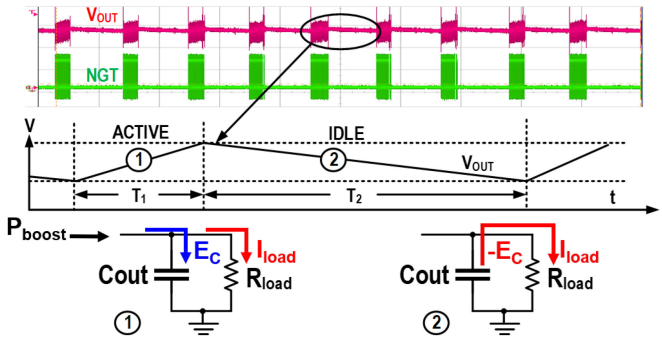


Fig. 10. Boosted-power estimation metric derivation.

B. LI-TB-MPPT: Boosted Power Estimation Metric

The load-inclusive time-based MPPT (LI-TB-MPPT) block is developed based on a fully digital boosted-power estimation metric to evaluate the total output power of the EHDS. The derivation of the metric is illustrated in Fig. 10. The ACTIVE periods (indicated by the switching NGT signal) and IDLE periods are marked as the first and second phases (T_1 and T_2), respectively. During the ACTIVE phase, the net flow of energy (E_1) comes solely from PMU boosted power (P_{boost}). This power is used to supply the load power (P_{load}) and charge the output capacitor with enough energy to reach upper hysteresis (E_C). Assuming that the load current is consistent across this regulation cycle, the energy consumed by the load during the IDLE period (T_2) will be equivalent to the difference in capacitor-stored energy ($E_C = \frac{1}{2}C(V^2_{\text{OUT,max}} - V^2_{\text{OUT,min}})$) at the output. It can then be derived that the boosted power is proportional to $1/T_1 + 1/T_2$ when the hysteresis energy is stable

$$E_1 = P_{\text{boost}}T_1 = E_C + P_{\text{load}}T_1 \tag{8}$$

$$E_2 = E_C = P_{\text{load}}T_2 \tag{9}$$

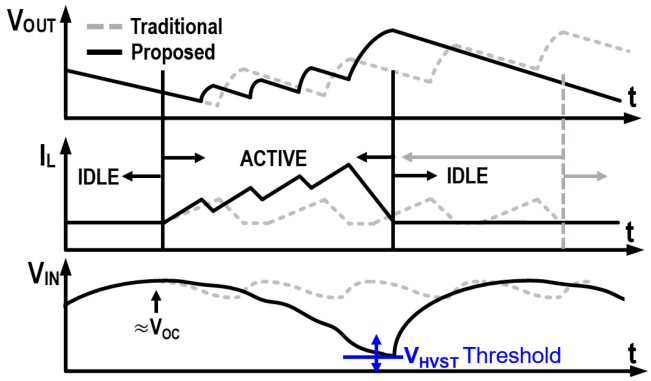


Fig. 11. PFM inductor current and input/output voltage.

$$P_{\text{boost}} = E_C \left(\frac{1}{T_1} + \frac{1}{T_2}\right) \propto \left(\frac{1}{T_1} + \frac{1}{T_2}\right). \tag{10}$$

The power-to-time relationship represented by (10) is the foundation of our LI-TB-MPPT. Not only does it provide a metric for evaluating P_{boost}, it does so while including the effect of output load. This metric is used as a reference while performing P&O [14] for system optimization by implying the following. 1) The faster the output voltage hysteresis is charged under a given load, the more efficient is the EHDS. 2) Decrease in T_2 and increase T_1 under the same system configurations is likely due to an increase in output load (and vice versa).

Performing MPPT with a metric derived from the system output not only ensures maximum power delivered, but it also abides with the objective of relieving high passives by becoming entirely independent of the harvesting operation. The independence of LI-TB-MPPT operation is the key to enabling the EHDS to freely manipulate system variables, both during the design phase and on-the-fly self-reconfiguration.

C. Fractional Sample and Hold: Harvesting-Window Control

Fig. 11 shows an abstraction of current and voltage waveforms during PFM boosting for the proposed system. Starting from an IDLE state for the PMU, V_{OUT} reduces with leakage and/or active current of loading modules. Since the inductor current is close to zero, the harvesting node voltage (V_{IN}) increases with harvested power. For low load conditions (and/or high output capacitance), the idle period is long and V_{IN} can be restored back to V_{OC} with the harvested energy during PMU IDLE. However, as load increases, max(V_{IN}) drops as its charging is cut short by the following PMU ACTIVE period. This also affects the harvesting window applied to the source. Assuming an ideal PV harvesting source (zero series resistance), the harvested current can be expressed as [26]

$$I_{\text{hvst}}(t) = I_{SC} + I_{pv0}(1 - e^{KV_{\text{hvst}}(t)}) \tag{11}$$

where I_{SC} is the short-circuit current of the harvesting device and I_{pv0}, K are device and harvesting condition dependent constants that result in $I_{\text{hvst}} = 0$ @ $V_{hvst} = V_{OC}$. It can then be derived (by solving for $\partial V_{\text{hvst}}(t)/\partial t = I_{\text{hvst}}(t)/C_{\text{IN}}$) that the

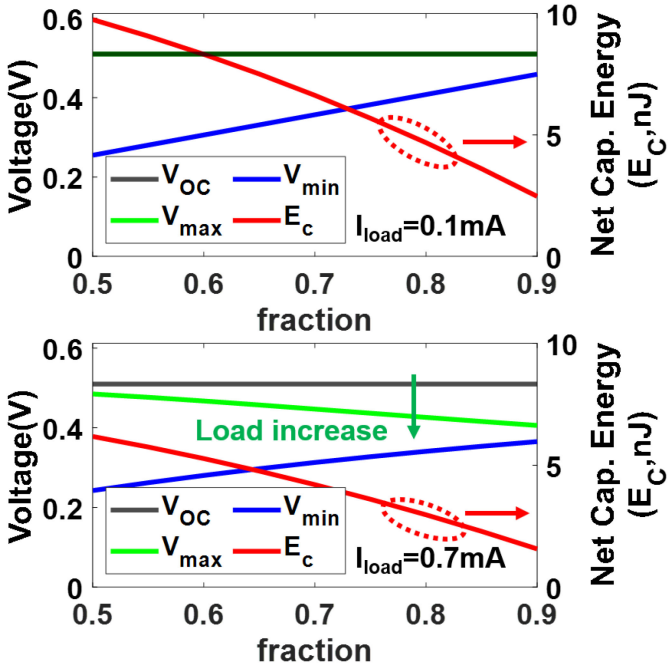


Fig. 12. Maximum/minimum voltage and hysteresis energy for different fractions ($V_{\text{min}}/V_{\text{max}}$) at equilibrium for load current=0.1 mA (top), 0.7 mA (bot). ($V_{OC} = 0.51$ C, $I_{SC} = 1$ mA, $C_{IN} = 100$ nF, and $C_{\text{OUT}} = 1.1\mu$F).

input voltage follows the following curve:

$$V_{\text{hvst}}(t) = \frac{-1}{K} \ln\left(\frac{1}{I_{SC}}\left(I_{pv0} + (I_{SC} - I_{pv0})e^{\frac{-I_{SC}K(t+t_0)}{C_{IN}}}\right)\right) \tag{12}$$

$$t_0 = \left(\frac{-C_{IN}}{I_{SC}K}\right)\left(\ln\left(\frac{I_{SC}e^{-KV_{\text{min}}} - Ipv0}{I_{SC} - I_{pv0}}\right)\right). \tag{13}$$

Based on charge equilibrium at the harvesting node, the integrated value of $I_{\text{hvst}}(t)$ is equal to that of the inductor current, and the hysteresis of stored charge in the input capacitor. We can, thus, derive the maximum input voltage as

$$V_{\text{max}} = V_{OC} - \frac{1}{K} \ln\left(1 + \left(\frac{I_{SC}}{I_{pv0}}e^{KV_{\text{min}}} - 1\right) e^{\frac{-I_{SC}KT_{\text{IDLE}}}{C_{IN}}}\right). \tag{14}$$

The IDLE period T_{IDLE} is purely a function of the load current and output capacitance when the output hysteresis is maintained during dc–dc PFM operation. However, with harvesting window control, the output hysteresis can be limited by the boosted charge from source hysteresis. Therefore, T_{IDLE} also changes with different fractions. Assuming a linear decrease in T_{IDLE} with increased fractions to account for this effect and substituting $V_{\text{max}} \times fraction$ for V_{min} in (14), we can then plot the source regulation metrics when the system reaches equilibrium as shown in Fig. 12.

Going back to the derived equation, (12), we can utilize the transient of harvesting voltage to also derive a transient of harvested power for the input source. This power-transient can then be used to approximate the average input power based on the change in harvesting windows for different fractions under load variations. This is plotted in Fig. 13. As observed, the

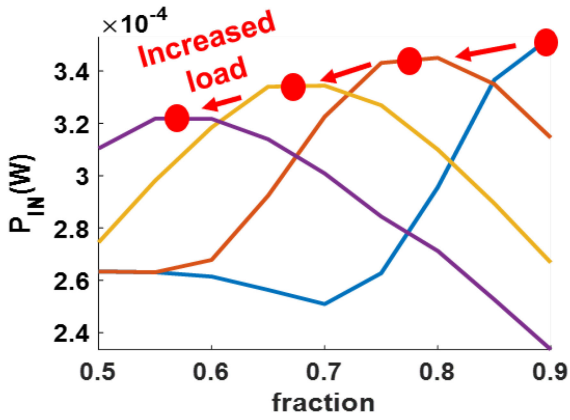


Fig. 13. Shift in maximum input power for different fractions with respect to change in load.

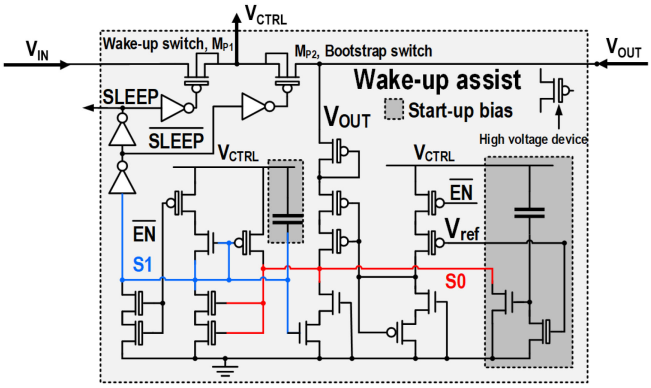


Fig. 14. Analog WUA circuit schematic for robust wake-up configuration.

peak input power shifts to different fractions as the load varies, and a constant fraction can lead to loss in input power and therefore harvesting efficiency. Traditional FOCV approaches neglect the impact of load and force-sample OCV conditions by either disconnecting the PMU [4] or using a dummy cell [27]. The former presents risks in power delivery (therefore requires multisource/storage EHDSs), and the latter has large overhead. In the proposed EHDS, we address this challenge via integrating on-the-fly "fraction configure-ability" into an FSH circuit that allows for OCV-free MPPT tracking, where load-sensing is directly performed with the LI-TB-MPPT circuit.

V. Implementation

A. Wake-Up Assist Circuit

The WUA circuit (see Fig. 14) composes an analog latch that senses two voltages to determine the state of control power for the system. The reference voltage (V_{ref}) is sensed with a voltage detector circuit [4], which is followed by a second stage to detect the output voltage of the EHDS. During cold-start, V_{IN} charges up first through harvested power from the input source. A portion of the power flows through p-n junctions of PMOS transistors and increases the control voltage. As V_{CTRL} increases, MOS capacitors within the highlighted start-up bias circuits initialize nodes S0 (red) to "ground," S1 (blue) to "V_{CTRL}" and connects

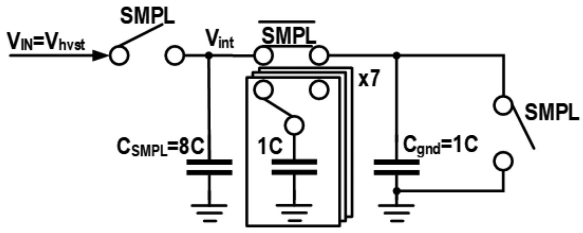


Fig. 15. Sample and hold circuit with configurable fractions through capacitive charge sharing.

V_{CTRL} to V_{IN} via wake-up switch M_{P1}. The two voltage detectors and output latch ensures that these values are maintained and S1 also closely follows the increase in V_{CTRL} to ensure that the digital SLEEP signal outputs a robust "1" even at low control voltages. This is a critical characteristic as the SLEEP signal is used to control digital logic, source configuration and bias gates of analog components. Any offset from the supply rail can propagate and amplify into incorrect configurations, especially at subthreshold voltages (< 0.4V).

The SLEEP signal is also used to: 1) place the regulator in the IDLE mode (bias-gate comparators and oscillator) to reduce V_{CTRL} power and prevent potential input voltage drop from premature switching activity; and 2) configures the PV diodes in series to increase V_{IN} (and the connected V_{CTRL}) during cold-start. Once both V_{ref} and V_{OUT} have become sufficiently high, SLEEP becomes low and the WUA connects V_{CTRL} to V_{OUT} (i.e., enter the bootstrap mode via bootstrap switch M_{P2}). After entering normal bootstrap operation, the regulator is enabled and the source is reconfigured (to prevent over-voltage and reduce series resistance) with a low SLEEP signal. High voltage devices are selectively implemented between every path from V_{CTRL} to ground in the WUA circuit to reduce standby power overhead (<15pW in simulation) and provide high threshold voltage levels.

B. Configurable Fractional Sample and Hold

The FSH circuit is based on a charge-sharing sample and hold circuit. Fig. 15 shows a schematic of the FSH circuit implemented with MOS capacitors and transmission gate switches. The internal voltage (V_{int}) is the voltage that is held and sent to the PFM BR input comparator (see Fig. 8) for harvesting window control. When the sample signal (SMPL) is high, C_{SMPL} is connected to V_{IN} and the grounding capacitor C_{gnd} is drained. When SMPL is low, V_{IN} is disconnected, the charge across C_{SMPL} and C_{gnd} are redistributed, and V_{int} settles at a fraction of V_{IN}, determined by the capacitance ratio between C_{SMPL} and C_{gnd}. Compared to resistor dividers, this topology has the advantage of low static power consumption when providing sufficiently fast sampling speed. To allow fraction configure-ability, seven MOS capacitors can be switched between C_{SMPL} and C_{gnd} to support eight different configurations of sampling fractions (see Fig. 12). The minimum fraction that can be applied to the sampled voltage occurs when all configuration capacitors are connected to C_{gnd}, and the maximum fraction occurs when all capacitors are connected to C_{SMPL}. This flexibility allows the FSH to perform

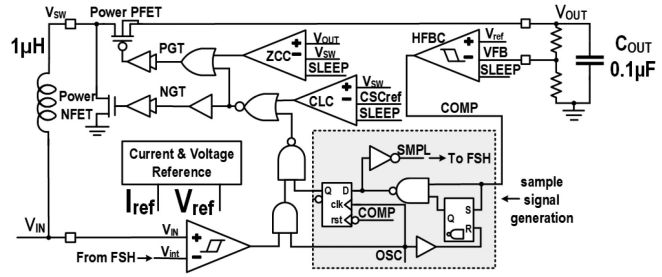


Fig. 16. Main control path with embedded sample (SMPL) signal generation.

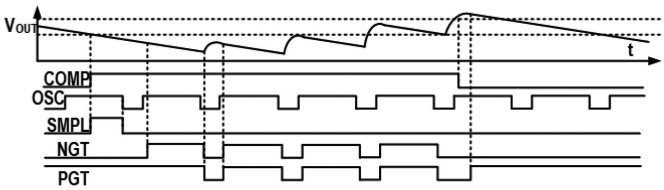


Fig. 17. Waveform for sample signal generation in the PFM control path.

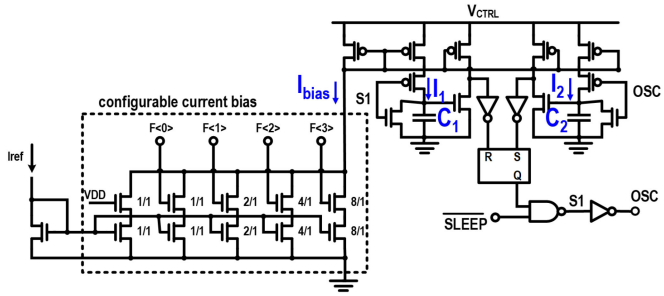


Fig. 18. Configurable frequency oscillator schematic.

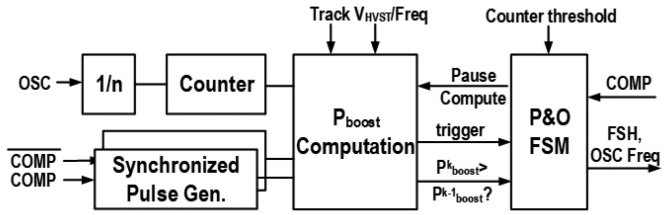


Fig. 19. LI-TB-MPPT block diagram.

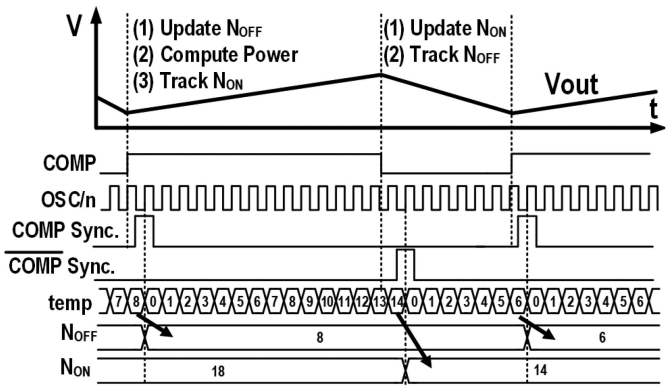


Fig. 20. MPPT operation waveform.

tracking while eliminating the area [4] and disconnection [27] overhead of traditional FOCV approaches. The configuration is updated every regulation cycle by the LI-TB-MPPT circuit to ensure input voltage fluctuations can be tracked on-the-fly, even when increase in load reduces the maximum input voltage as explained in Section IV-C.

C. PFM Control Path

The main control path is shown in Fig. 16. Output regulation is performed by the hysteresis feedback comparator (HFBC), which compares a resistor-divided feedback voltage with the on-chip V_{ref}. The input hysteresis comparator output overwrites oscillator clock to stop the PMU and to prioritize source voltage regulation before the OSC signal is passed to later stages. A zero-current comparator (ZCC) and a current limit comparator (CLC) close the power PFET and power NFET, when the inductor current falls below zero or surpasses a predesigned current limit, respectively. This is done by comparing the switching node voltage V_{SW} with V_{OUT} and another on-chip reference CSC_{ref} in a similar manner as prior works [9]. The CLC senses inductor current through an internal NFET and resistor that is placed in parallel to the low-side power NFET. The current limit is designed to be approximately 20 mA to prevent imposing extensive voltage drop on the input capacitor. Additionally, sample signal generation is embedded in the PFM control path to create a "SMPL" signal before any switching activity begins. The flip-flop blocks OSC signal propagation until sampling is completed (see Fig. 17).

D. Configurable-Frequency Oscillator

A configurable-frequency current-capacitor oscillator is designed for creating switching signals for the PMU and the system clock. Different frequencies can be made though changing the configurable current bias. The advantage of the current-capacitor design is that it delivers a stable duty-cycle robust to process-voltage-temperature variations, which is determined by the ratio of mirrored currents I_1, I_2 and capacitors C_1, C_2 [9]. The impact of frequency variations [24] can be countered through allowing MPPT to tune configurations for the bias current branch when it tracks for maximum output power.

E. Load Inclusive Time-Based MPPT

The block diagram of the LI-TB-MPPT implementation and details of LI-TB-MPPT operation are shown in Figs. 19– 21. The digital synchronization block creates pulses that trigger computation only at rising and falling edges of the COMP signal. The P_{boost} computation engine logs counted clocks during T1 and T2 (as N_{ON} and N_{OFF} in the figure) and computes P_{boost} from these values. Digital threshold checks (for counter overflow and load-change retriggering) are implemented in the MPPT finite state machine before the computed "higher power: $P^{k}_{\text{boost}} > P^{k-1}_{\text{boost}}$" decision is fed to the perturb and observe finite state machine (P&O FSM). In the event of a load-step, not

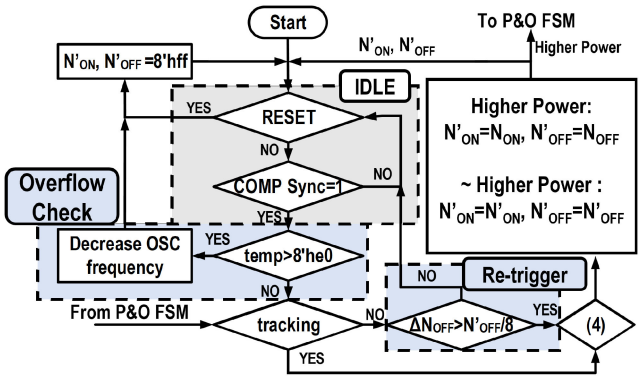
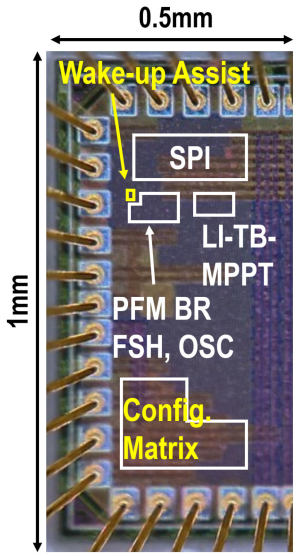


Fig. 21. P_{boost} computation flow diagram with digital threshold checks.



General	
Technology	65nm
OSC(@1V)	6MHz~20.8MHz
Wake-up Assist	
Area	0.000322mm^2
FSH	
Area	0.000133mm^2
Configuration Matrix	
Area	0.0476mm^2
Configurations	3
LI-TB-MPPT	
Area	0.0032mm^2
Clock Division	1/8
Counter Width	8 bits
Search Algorithm	Perturb & Observe

Fig. 22. Chip micrograph and specifications.

only does the PMU conversion efficiency change with IDLE period but also the harvesting voltage recharging is affected, as discussed in Section IV-C. A threshold of $N_{OFF}/8$ is applied for resetting tracking registers under such scenarios.

The P&O FSM implements the following algorithm for hill-climbing. 1) The FSM first attempts a change in EDHS configuration. 2) The output power of the EHDS is compared to prior states with the power-evaluation engine. 3) If "higher power" is observed, the FSM continues changing EHDS configurations in the same direction and re-evaluates. If not, the system converges back and attempts a different change. Decisions to modulate the FSH fraction and oscillator frequency are updated at the beginning of every output regulation cycle during the search for an optimal operating point for the EHDS.

We also simplify the boosted power metric for efficient computation because it is not necessary to obtain the absolute value of the metric for hill-climbing MPPT. Instead, only a single-bit decision is required: whether the computed metric of one state is higher than another. Our first step is to avoid division operations that are used in (10), as they are computation heavy

$$P_{\text{boost}} > P'_{\text{boost}} \iff \left(\frac{1}{T_1}+\frac{1}{T_2}\right) > \left(\frac{1}{T'_1}+\frac{1}{T'_2}\right) \quad (15)$$

$$(15) \Rightarrow T'_1T'_2(T_1+T_2) > T_1T_2(T'_1+T'_2). \quad (16)$$

Next, we perform a second step of conversion by computing intermediate values of $x=(T_1+T_2)/2$ and $y=(T_1-T_2)/2$. To prevent negative values, initial comparison of T_1 and T_2 is performed and the larger value is reassigned to T_1 for computation. Substituting x and y into (16) and rearranging the inequality, we can reach the following:

$$(16) \Rightarrow x' - y'\left(\frac{y'}{x'}\right) > x - y\left(\frac{y}{x}\right). \quad (17)$$

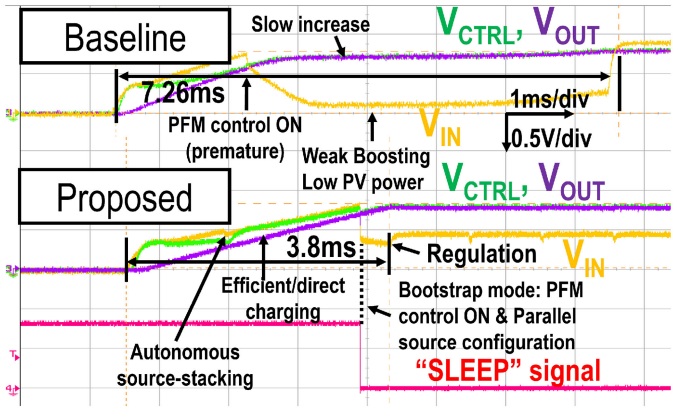
The multiplication and division in $y(y/x)$ is addressed by quantizing the division into powers of $1/2$ and performing bit-shifting for multiplication. The error rate introduced by this binning (with 5% tolerance) is 2.6% for 8-b timing information, with the majority of errors lying in corner cases that have very unbalanced ACTIVE and IDLE periods (which rarely occur in implementation). The synthesized area can be reduced by $2.2\times$ with observation registers added. Without the testing harness, the projected area reduction can be up to $6.1\times$.

VI. Measurement Results

To demonstrate the proposed EHDS, a test-chip is fabricated in 65 nm CMOS (see Fig. 22) and integrated on-board with PV diodes (VBPW34S), where the V_{OC} of a single harvesting photodiode is measured with ~0.25V@380 lx (roomlight) and ~0.48V@36klux.. The integrated EHDS uses a 1μH inductor, an input capacitance (C_{IN}) of 0.1μF, a control voltage capacitance (C_{CTRL}) of 1μF and an output capacitance (C_{OUT}) of 0.1μF. Higher capacitance is added on the control voltage, rather than the output node, to reduce voltage drop from charge sharing with output capacitance when the PMU is switched into bootstrapped mode. Both will serve as decoupling capacitance for V_{CTRL} and V_{OUT} regulation once the system wakes up. The measured switching frequency of the oscillator is 6–20.8 MHz at $V_{\text{CTRL}}=$ 1.0 V, with an average duty cycle of 80%. The relatively high frequency enables reduction in both inductance and C_{IN}.

A. Wake-Up Assisted Cold-Start

Fig. 23 shows measured waveforms and results of bootstrap cold-start with and without the proposed WUA circuit. To highlight benefits of cold-configuration, waveforms from the stack-of-three testcase have been selected to represent baseline bootstrapped wakeup. This is because the proposed WUA also enforces a stack-of-three autonomously during cold-configuration. During baseline experiments, the testing harness overwrites the SLEEP signal and the source matrix is powered externally to ensure a stable configuration is asserted. Only the testing harness is powered externally (for observation) during the measurement for the proposed approach and everything else is free-running from harvested power, including the autonomous source-stacking enabled by the WUA. Even with this slight



Configuration	Wakeup time(@6klux)	Lowest wakeup intensity (klux)
Baseline	7.26ms	6 (3-stack), 17 (2-stack), failed (1-stack)
Proposed	3.8ms	1 (auto-3-stack)

Fig. 23. Measurement waveforms for input voltage, output voltage, control voltage, and SLEEP signal.

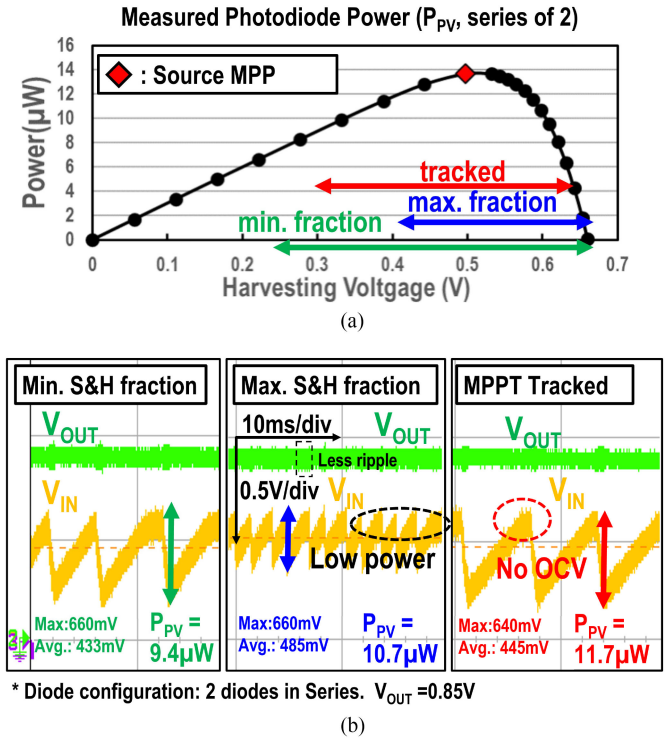


Fig. 24. Measurement waveforms for input voltage with fixed fractions (open-loop) versus with MPPT-tuned fractions (closed-loop). (a) DC power-voltage. (b) Transient measurements.

disadvantage, the proposed wake-up assisted cold-start presents superior performance in all aspects.

In both experiments, V_{CTRL} and V_{OUT} rise with V_{IN} increase initially through drain-to-body p-n junctions of the wake-up switch (see Fig. 14) and the power PFET (see Fig. 16). Low input voltage observed in the baseline measurements that arise from premature switching activity restricts inductor current build-up and results in inefficient boosting. The consequent long-ACTIVE periods further leads to extensive current drawn, even lower input voltage, and, ultimately, slow increase in both V_{CTRL} and V_{OUT}. However, with the proposed WUA, although input voltage increase is slightly delayed before cold-configuration kicks in, this latency is compensated while the output voltage rises quickly after self configurations are complete. From this example, we can directly observe the benefit of connecting V_{CTRL} to V_{IN} for accelerated charging during cold-start. Additionally, with bias-gating of unused PFM control blocks, the bootstrap current of the PMU is also reduced from 42 μA active current (measured from an always ON-state) to 4 μA leakage. After the WUA senses that the EHDS is ready for bootstrapped operation, the SLEEP signal also reconfigures the harvesting source into parallel configurations for bootstrapped operation. Overall, the system achieves 2$\times$ reduction wake-up time (7.26 ms$\rightarrow$3.8 ms) by: 1) enabling robust cold-configuration of harvesting sources in series to create high voltage; 2) direct/efficient charging of control voltage from the input source; 3) avoiding weak-boosting periods before V_{CTRL} reaches nominal operation voltage completely; 4) minimizing PMU power with bias-gating during cold-start. We also measure that the minimum light intensity needed is reduced by at least 6$\times$ with the proposed approach.

B. Fraction Tuning With LI-TB-MPPT

Fig. 24(a) shows the PV power as a function of harvesting voltage when harvesting under roomlight with the source matrix configured in a stack of 2. Fig. 24(b) shows the input and output (regulated at 0.85 V) waveforms when fractions are fixed at minimum, maximum and when it is tracked by LI-TB-MPPT. As explained in Section IV-C, we can observe that different fractions result in different V_{min} and V_{max} pairs when the system reaches equilibrium. Therefore, the harvesting window is successfully controlled by controlling sample and hold fractions in the FSH circuit. Measurement waveforms with minimum and maximum fractions acquired by overwriting MPPT decisions with the testing harness are compared to when closed-loop tracking results. For a low fraction (with more capacitors connected to C_{gnd}, Fig. 15), the PMU is allowed to boost more charge during ACTIVE, which results in a higher ripple in the output voltage, and longer IDLE periods when V_{IN} charges back to V_{OC}. For a high fraction, PMU boosting is cut short by the input comparator and less drop in V_{IN} is observed. This also reduces the output voltage spike and ripple. It can be seen that both minimum and maximum fractions harvest from voltages where PV diodes produce low power due to low voltage ($<$0.4 V) or low current (@$>$0.6 V). Allowing the LI-TB-MPPT to search for an optimum setting avoids such conditions and up to 9% improvement in measured input power is observed.

C. Frequency Tuning With LI-TB-MPPT

Fig. 25 shows transients of the LI-TB-MPPT retuning oscillator frequency on-the-fly. The frequency range of the configurable oscillator (6–20.8 MHz) has been designed for two reasons. The first is to ensure the PMU can enter multipulse operation at high loads for improved efficiency. The second is to limit the input voltage drop (with only 0.1 μF input capacitance) from inductor

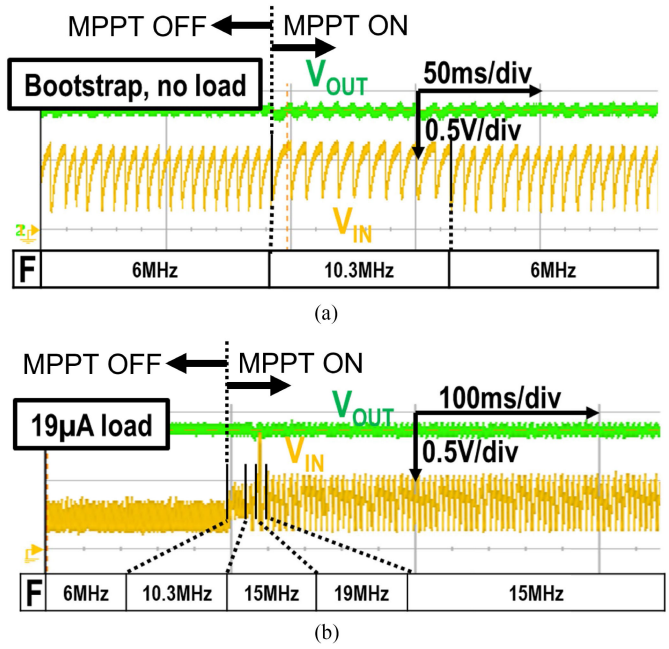


Fig. 25. Measurement waveforms for input voltage with frequency tuning. (a) Self-powered. (b) 19μA load. (F is the switching frequency of the PMU.).

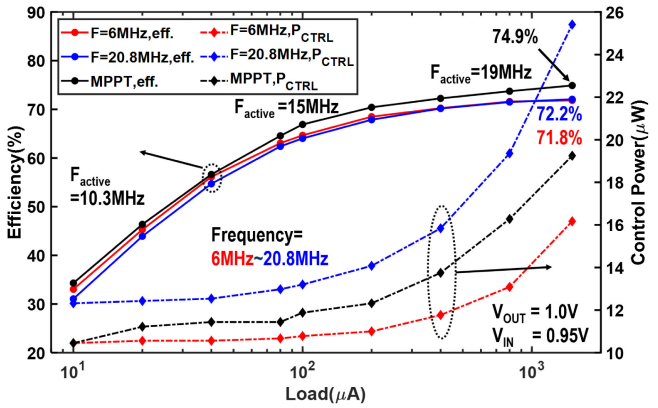


Fig. 26. Measured end-to-end efficiency and system power for MPPT tracking at different loads. (F_{active} is the active switching frequency of the PMU, controlled configuring current bias in Fig. 18 through LI-TB-MPPT.).

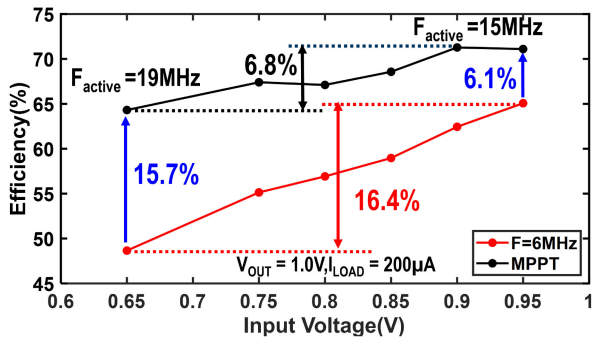


Fig. 27. Measured end-to-end efficiency at different input voltages.

current pulses when the harvested power is low. This experiment is conducted in a two-step process to prevent initiating a retrigger event as shown in Fig. 21. Fig. 25(a) represents the first step where no external load is applied and the EHDS supplies itself with the power boosted from photodiodes that are powered with room light. We can observe that although the EHDS attempts to increase the frequency (F=6 MHz $\rightarrow$10.3 MHz) initially, it converges back after a few regulation cycles as the P&O algorithm finds that the increase in frequency does not provide significant benefit in increasing system performance. Fig. 25(b) also initializes the EHDS with F=6 MHz in open-loop before MPPT tracking is enabled, except in this case, a current sink applies 19 μA load on the output node of the EHDS. The increased load results in shorter IDLE periods and a drop in the input voltage when the frequency is fixed at a configuration of F=6 MHz. When the MPPT is enabled, the EHDS auto-selects a configuration of F=15 MHz after 20 ms.

It can be observed that the P&O search with frequency configuration avoids applying low-voltage biasing conditions to the harvesting source, thus increasing robustness of EHDS operation. Although the same output power is delivered when regulated at the same load, a separate experiment demonstrates that the proposed MPPT approach increases the maximum load/power, at which output regulation is maintained, by 10% (40μW $\rightarrow$ 44μW) under an input intensity of 6klux. Additionally, compared to asynchronous FOCV sampling [6], [27] where tracking response time depends on the sampling frequency, an advantage of integrating sampling into the PFM control path is that input fluctuations can be tracked every regulation cycle and LI-TB-MPPT ensures that output variations can be tracked within a few regulation cycles without needing to enter OCV conditions.

Fig. 26 shows the measured efficiency and PMU power consumption across different loads when the switching frequency is maximum, minimum, and tuned by LI-TB-MPPT. The IDLE frequencies for the first two cases are the same as their active frequencies (F_{active}) but are observed to be auto-selected as 6 MHz across MPPT-tuned measurements. We can observe that both efficiency and power increase with load for all three cases. Although lower frequency reduces power consumption of the PMU for improved end-to-end efficiency at low load, higher frequency produces higher efficiency at high load by reducing ripple loss from spurious single pulse boosting. By allowing the LI-TB-MPPT circuit to modulate the converter frequency during ACTIVE and IDLE periods, MPPT-tuned results always present maximum efficiency. A peak end-to-end efficiency of 74.9% is observed at 1.5 mA load current, which is 2.7% and 3.1% higher than both fixed-frequency configurations.

Fig. 27 shows the LI-TB-MPPT circuit modulating frequency at different input voltages. A change in input voltage not only changes the conversion ratio but also inflicts a direct change in the inductor current slope. The impact of this effect is especially high when the frequency is low as the peak inductor current will be limited by the input voltage in single-pulse operations. Therefore, an increase in frequency is often needed to restore the "boosting ability" and efficiency of the PMU as input voltage decreases. We can observe an efficiency improvement between 6.1% and 15.7% (blue) when the active frequency is tuned by

TABLE I
COMPARISON TO STATE-OF-THE-ART EHDSS

Metric	[18]	[19]	[20]	[6]	[4]	[8]	**This Work**
Technology	350nm	180nm	180nm	180nm	180nm	180nm	**65nm**
Converter Scheme	PFM	DCM	PFM+PSM	BFHC	DCM	DCM	**PFM**
Input Voltage	0.15-0.75V	20-70mV	1.5-2.6V	>129mV**	>0.4V**	>50mV**	**>0.25V****
Output Voltage	1.8-3.3V	0.8-1.1V	1,1.8,3V	0.8,1.1V	1,3V	1.2V	**0.75-1.2V**
Input Capacitance	47µF	1µF	10µF	-	-	-	**0.1µF**
Other Capacitance	15µF	0.2µF	30µF	-	-	1µF	**1.1µF**
Inductance	22µH	47µH	10µH	82µH	47µH	100µH	**1µH**
Frequency	31.2kHz	12.8Hz	10kHz	30kHz	30kHz	8kHz	**6MHz-20.8MHz**
Maximum Efficiency	83%@1.5mW	55%@1.2nW	83%@90µW	84%@67µW	89%@50µW	80%@400µW	**74.9%@1.5mW**
Maximum Power***	2.5mW	4nW	10mW	107µW	1mW	2mW	**2mW**
MPPT	TB	No	Current	FOCV	FOCV	Look-up Table	**2-D LI-TB-MPPT w/ FSH+Frequency**
Tracking Efficiency	96%	-	96%	-	-	-	**85%(source) 99%(system)**
MPPT Area*	-	-	-	$0.03mm^2$	$0.05mm^2$	$0.01mm^2$	$\mathbf{0.0033mm^2}$
Cold-start	No	No	No	Yes	Yes	Yes	Yes
Wake-up Area*	-	-	-	$0.4mm^2$	$0.9mm^2$	$0.96mm^2$	$\mathbf{0.000322mm^2}$**(WUA)** $\mathbf{0.047mm^2}$**(config.)**
Wake-up Time	-	-	-	300s	11s	252ms	**3.8 ms**
EHDS Active Area*	$25mm^2$	$1.53mm^2$	$4.62mm^2$	$1.2mm^2$	$1.5mm^2$	$2.52mm^2$	$\mathbf{0.058mm^2}$

"-": not reported or unavailable, PFM = Pulse frequency modulation, DCM =Discontinuous conduction mode, PSM=Pulse skipping modulation, BFHC= Boost/flyback hybrid converter, TB= Time-based
* Estimated from chip area reported in corresponding reference and proportion of related blocks presented in chip micrographs.
** Including cold-start.
*** Maximum power reported and/or shown in efficiency plots.

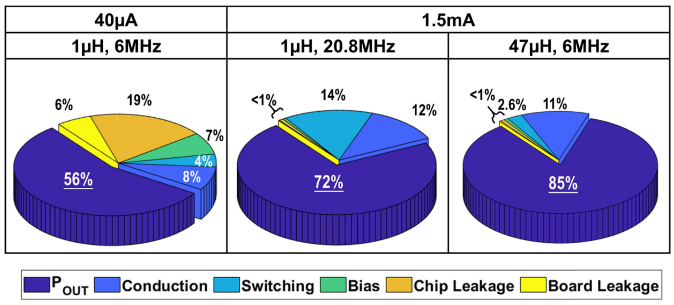


Fig. 28. Breakdown of loss components at 40 μA and 1.5 mA load ($V_{\text{OUT}} = 1.0$ V, and $V_{\text{IN}} = 0.95$ V) with 1 and 47μH inductance.

the LI-TB-MPPT circuit. The variation in efficiency across input voltage is also reduced, from a 16.4% change (red) to 6.8% change (black).

D. Comparison With Prior Works

Table I presents a summary of the EHDS with the designed chip compared with state-of-the-art EHDS implementations in existing literature. This article achieves a peak conversion efficiency of 74.9% with an input capacitance of 0.1 μF and an inductance of 1 μH. While prior works have demonstrated over 80% end-to-end efficiency, it can be seen from the table that these were achieved with passives that are much higher in value. It has been shown in prior work that increased inductance can benefit conversion efficiency [19]. Fig. 28 shows a breakdown of loss components for our EHDS and their impact on the end-to-end efficiency. This breakdown has been constructed based on a PFM-transient loss model [22] and modified to capture the input harvesting window control specific to the proposed EHDS. The total loss due to all the control circuits (i.e., total current drawn from V_{CTRL}) is measured as 31.5 μW, which includes 10.38 μW (9.13 μW due to leakage) for the LI-TB-MPPT and 1.94 μW for the configuration matrix. Its contribution to total loss is included in the model separately as "Bias" power and "Chip Leakage." The conduction loss, switching loss, and board leakage are computed based on both measurement values (clock frequency, duty cycle, output hysteresis, feedback potentiometer, etc.) and simulation data (R_P, R_N, driver slew-rate, and switching energy, etc.). By including the nonideal loss components characterized from both measurement and simulated data, we can see that the modeled end-to-end efficiency matches the measurement results shown in Fig. 26. From the modeled loss breakdown, we can observe that the conversion efficiency at low power (P_{OUT}= 56%@40μ A) is mainly limited by leakage components (25%), and as expected the contribution of conduction loss and switching loss becomes more significant under high power (P_{OUT}= 72%@1.5 mA).

While the proposed design is demonstrated in a low-cost EHDS with reduced passive values, improved efficiency can also be achieved when higher-quality passives are available. Fig. 28 also shows a test case where up to 85% conversion efficiency can be achieved when our EHDS uses a 47 μH inductor (as in reference [4]) and fixed switching frequency of 6 MHz. The gain in efficiency is a result of reduced current ripple and frequency, which is shown in Fig. 29. However, as shown in the figure, the increased inductance also results in a large amount of boosted charge due to the reduced inductor current slope when switching events stop. This additionally requires increased input capacitance and output capacitance to reduce voltage ripple for harvesting and regulation, respectively. Although the proposed system can achieve competitive end-to-end efficiencies when similar passive values are used compared to prior EHDSs, peak efficiency is not the main focus of the design. A key contribution

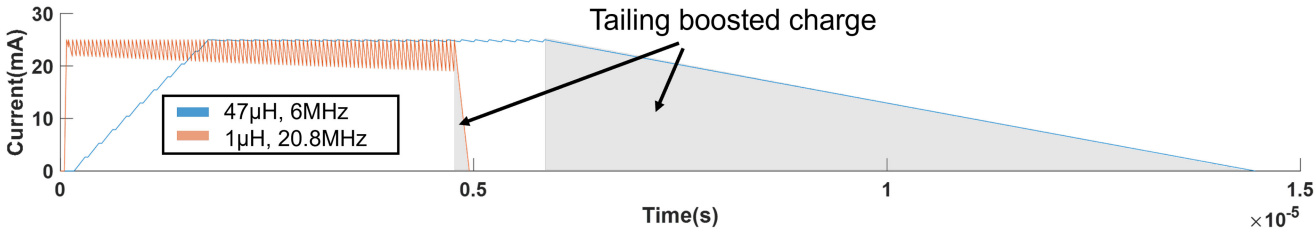


Fig. 29. Simulated inductor current with 1μH at 20.8 MHz and 47μH inductance at 6 MHz, boosting at 1.5 mA load.

of this article is that the proposed system can support high levels of reduction in explicit passive values needed for operation, which ultimately signifies reduced system cost.

The proposed system also presents orders of magnitude lower active area with the proposed MPPT and WUA approaches. When considering the scaling of technology nodes, this article still presents over 3$\times$ reduction. Furthermore, most of the active areas in this EHDS are dominated by the configuration matrix and not the control system as the size of the transmission gates have been designed with an R_{ON} of 0.5 Ω to interface with up to 10 mA harvester current. The size of these gates can be scaled accordingly when strength of harvesting sources change to gain additional area reduction. In addition, the output-based tracking achieves system-level tracking efficiency of up to 99%. The measured line regulation is 11.9 mV/V, the load regulation is 0.174 mV/μA, and the worst-case output ripple is measured at 68 mV. Finally, a wake-up time of 3.8 ms can be attributed to both reduced input/control/output capacitance and the additional 2$\times$ improvement presented in Section VI-A.

VII. Conclusion

This article presents a low-cost, self-tuned PFM EHDS using PV sources. A system-output MPPT approach is proposed for system-efficiency optimization and with a configurable FSH circuit, the harvesting voltage is allowed to drop to lower thresholds when the PMU is active but adaptively controlled with respect to load to ensure it can replenish itself during PMU IDLE periods. In addition, a WUA circuit achieves robust cold-configuration and fast cold-start with little overhead. We demonstrate the proposed EHDS in a 65 nm technology with commercial PV diodes and measured results confirm successful cold-start, MPPT, and only slight efficiency loss (which can be restored if a high inductance is used at increased cost) during power delivery with orders of magnitude lower active area and on-board inductor/capacitor values compared to prior works. These results provide the foundation toward compact, low-cost, self-powered IOT applications.

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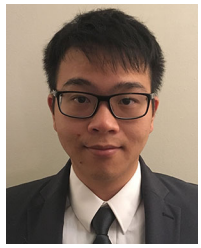

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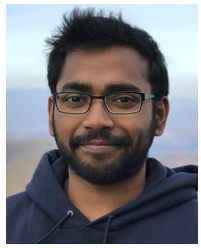

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