A Mixed Conduction Mode-Controlled Bridgeless Boost PFC Converter and Its Mission Profile-Based Reliability Analysis

Zhengge Chen, *Member, IEEE*, Jianping Xu, *Member, IEEE*, Pooya Davari, *Senior Member, IEEE*, and Huai Wang, *Senior Member, IEEE*

***Abstract*—Given the telecom base transceiver station (BTS) load mission profiles, a mixed conduction mode (MCM) control for a bridgeless boost PFC converter (IPOS boost) is proposed to mainly improve its power factor and reduce the input current total harmonic distortion (THD_i) in the light-load conditions. The principle of the MCM control and the efficiency analysis are introduced. Then, the experimental verification is performed to show the control effectiveness and performance improvements. Furthermore, a mission profile-based reliability assessment for the PFC converter is presented to analyze the IPOS boost under the classical average current (AVC) control and the proposed MCM control, along with its conventional boost counterpart under the AVC control. Considering the measured efficiency data and BTS typical mission profiles in a rural area, the analysis results indicate that given 20 years of operation, the accumulated failure of the IPOS boost under the AVC controls is 0.27%, and is further decreased to 0.24% by just the software update with the proposed MCM control. By contrast, the accumulated failure of the conventional boost counterpart under the AVC control is 2.06%, much higher than the IPOS boost.**

***Index Terms*—Base transceiver station (BTS), bridgeless, mission profile, mixed conduction mode (MCM), power factor correction (PFC), reliability analysis, wear-out.**

I. Introduction

In THE power distribution system for the telecom network, ac–dc power factor correction (PFC) converters are extensively used [1], [2]. With the concerns of increased operation electricity bills, many efforts in recent decades have been devoted to the bridgeless topology-related evaluations [3]–[5], derivations [5]–[8], and controls [1] for their efficiency superiority over the conventional topology counterparts. Besides, PFC converter optimization for the high performance in a wide load range is also meaningful [9]–[15]. This article focuses on one bridgeless boost topology for its performance improvement by the control method.

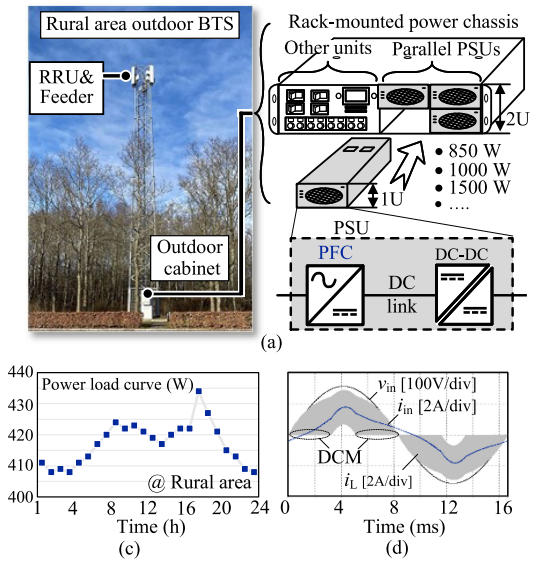

Fig. 1. PFC converter in the power distribution system for base transceiver station (BTS) applications. (a) Typical configurations in rural area. (b) One typical day power load in a rural area [1] with increased power loads in daytime and decreased loads in night. (c) Key simulation waveforms of the input-parallel output-series bridgeless boost (IPOS boost) in a light load.

The IPOS boost and input-parallel output-parallel (i.e., dual boost) bridgeless boost PFC topologies are categorized into two bridgeless groups [7]. Then, along with the conventional boost PFC converter (conventional boost), they are compared with the assumption of being used in the BTS application [see Fig. 1(a)]. The benchmarking results indicate the efficiency superiority of the IPOS boost among other compared converters [7]. And, the IPOS boost with the unique dc split structure also triggers further research interest, as presented in this article.

Given one typical day load mission profile [see Fig. 1(b)] and the power supply unit (PSU) output power ratings, the BTS actually operates in the idle mode most of the time. It means that the PFC converter efficiency, power factor (PF), and input current total harmonic distortion (THD_i) in 20%–40% load condition are critical [1]. Unfortunately, the conventional boost designed in the continuous conduction mode (CCM) operation

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with the classical average current (AVC) control suffers from the deteriorated PF and THD_i in the light-load conditions [16]. This is because that the inductor current enters the discontinuous conduction mode (DCM) operation near the zero-crossing of the ac input [see Fig. 1(c)] and it makes the original CCM control inefficient [17]. This phenomenon is also observed in the IPOS boost [see Fig. 1(c)]. Various types of mixed conduction mode (MCM) controls for the conventional boost are proposed [13], [17]–[22] with the CCM control law applied to the CCM and the DCM law for the DCM, respectively. From the implementation perspectives, these MCM controls can be divided into following two groups, roughly.

1) In the first group, they separately calculate both the DCM and CCM duty cycles, and based on selection rules, one of the calculated duty cycles can be employed [18], [19]. Although this control strategy increases the digital signal processor (DSP) calculations since only one duty cycle is used finally, the advantage is that the conduction mode detection circuit or program is spared and there is no additional material cost.
2) On the contrary, the second group uses conduction mode detection algorithms to avoid the calculations of both the DCM and CCM duty cycles [13], [17], [20]–[22]. However, auxiliary sampling circuits [13], [20] or high-performance controller with internal comparators [21], [22] have to be used for mode detection. The aforementioned MCM controls are implemented in the conventional boost. This article proposes an MCM control for the IPOS boost and adopts the first group control strategy to avoid the extra material cost. Moreover, the DCM duty cycle is fitted to reduce the calculation time.

In the second part of this article, motivated by the high reliability request of the BTS in rural area [23], the IPOS boost and its conventional boost counterpart are targeted for the reliability assessment. Besides, the question of how much the MCM control affects the IPOS boost will be revealed. Until now, many PFC converter reliability-related works [24]–[27] mainly discuss the aluminum electrolytic capacitors (Al-Caps) annihilation for the lifetime compatibility with the light-emitting diode. Because Al-Caps are seen as one of the major fragile parts in power converters [28]. However, how much the lifetime improvement for the converter without Al-Caps is actually not explored quantitatively. Moreover, although many Al-Cap-targeted reliability researches are conducted [28]–[31], the detailed PFC converter level reliability analysis is not seen.

In the other literature [24], [32]–[34], empirical-based component reliability models [35] are used to estimate the PFC converter reliability performance. For example, Ranjbar *et al.* [32] and Abdi *et al.* [33] adopted the fixed failure rates of components from U.S. Military-Handbook-217F to assess the lifetime of PFC converters. Although this method is simple, it suffers from low accuracy [36]. Because these constant failure rates are only statistic results based on random failures observed in the useful life region of the bathtub curve [37] (see Fig. 2), and the component manufacturing technique differences or the real mission profiles are typically not taken into account [24], [34].

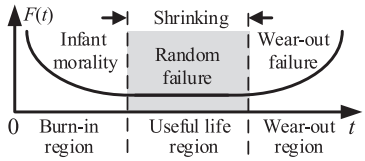

Fig. 2. Classical bathtub curve of a device failure rate $F(t)$ in different regions.

Thus, the PFC converter reliability assessment in the wear-out region, which relates to different topologies, mission profiles, and control strategies [37]–[39], is still not covered. Meanwhile, the shrink of the useful life region, mainly driven by the commercial electronics industry since 1990s [36], has also made the failure rates in the wear-out phase a key role in design and reliability prediction [36], [39].

This article presents a mission profile-based approach for the PFC converter reliability assessment in the wear-out region. The long-term mission profiles and the built electro–thermal models are used to derive the time-dependent accumulated failure of the critical components (i.e., semiconductors and capacitors). Similar approaches have been used to analyze the reliability of a dc–dc converter [40], a microinverter [41], and modular multilevel converters [42]. However, due to the differences in applications, topologies, and controls, the mission profiles and electro–thermal models are significantly different from others [40]–[42].

The major contributions of this article are summarized as follows.

1) An MCM-controlled IPOS boost with reduced DSP calculation time is proposed mainly to improve the light load performance (PF and THD_i).
2) The accumulated failure of three targeted converters is estimated quantitatively by an adapted mission profile-based reliability analysis method for PFC converters.

The rest of this article is organized as follows. In Section II, the MCM control for the IPOS boost is introduced, followed by the power loss analysis. In Section III, the experimental results of the prototype are given. The PFC converter reliability analysis is conducted, and the results are given in Section IV. Finally, Section V concludes this article.

II. MCM-Controlled IPOS Boost

Without any hardware modification in the IPOS boost to increase cost, this part aims to use only the control algorithm to improve the converter performance. Meanwhile, the PSUs in the telecom are commonly required to have the online software update ability, which means that the new control algorithm may also be accessible by the software update for the deployed PSUs in the real field.

A. CCM Operation Control Laws

The CCM control law is based on the AVC control and was introduced in [7]. The CCM operation modes of the IPOS boost in the positive half-line cycle are shown in Fig. 3. According to

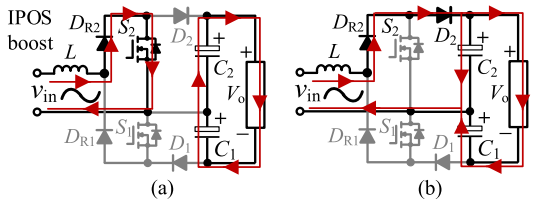

Fig. 3. CCM operation modes. (a) S_2 in ON-state. (b) S_2 in OFF-state.

the operation modes, it can be known that the IPOS boost has the similar model as the conventional boost presented in [43]. Thus, the CCM duty-cycle feedforward (DFF) $d_{\mathrm{ccm,ff}}$ for the IPOS boost is derived. The average switch voltage $v_{\mathrm{S2,avg}}$ across S_2 in the IPOS boost is

$$v_{\mathrm{S2,avg}} = (1 - d_{\mathrm{ccm}})V_{\mathrm{o}}2 \tag{1}$$

where d_{ccm} is the duty cycle for the CCM and V_{o} is the output voltage. Then, to make the compensated average switch voltage close to the input voltage, $d_{\mathrm{ccm,ff}}$ is derived as

$$d_{\mathrm{ccm,ff}} = 1 - 2v_{\mathrm{in}}V_{\mathrm{o}} \tag{2}$$

where v_{in} is the instantaneous input voltage.

B. DCM Operation Control Laws

The average inductor current $i_{\mathrm{L,avg}}$ is seen as the input current i_{in} is

$$i_{\mathrm{in}}(t) = i_{\mathrm{L,avg}}(t) = \frac{T_{\mathrm{S}}d_{\mathrm{dcm}}v_{\mathrm{in}}}{2L}(d_{\mathrm{dcm}} + d_{\mathrm{off}}) \tag{3}$$

where d_{dcm} is the inductor charging duty cycle in DCM, d_{off} is the discharging duty cycle, and T_{S} is the switching cycle. Based on the volt-second balance of the inductor, i.e., $v_{\mathrm{in}}\cdot d_{\mathrm{dcm}} = (1/2V_{\mathrm{o}}–v_{\mathrm{in}})\cdot d_{\mathrm{off}}$, (3) can be re-expressed as

$$i_{\mathrm{L,avg}} = \frac{0.5T_{\mathrm{S}}{d_{\mathrm{dcm}}}^2V_{\mathrm{o}}v_{\mathrm{in}}}{2L(0.5V_{\mathrm{o}} - v_{\mathrm{in}})}. \tag{4}$$

Given (4), the instantaneous input power p_{in} is

$$p_{\mathrm{in}}(t) = v_{\mathrm{in}}(t)\cdot i_{\mathrm{L,avg}}(t) = \frac{0.5T_{\mathrm{S}}{d_{\mathrm{dcm}}}^2V_{\mathrm{o}}{v_{\mathrm{in}}}^2}{2L(0.5V_{\mathrm{o}} - v_{\mathrm{in}})} \tag{5}$$

Then, considering $p_{\mathrm{in}} = v_{\mathrm{in}}\cdot i_{\mathrm{ref}}$, d_{dcm} in (5) is derived as

$$d_{\mathrm{dcm}} = \sqrt{\frac{2L(0.5V_{\mathrm{o}} - v_{\mathrm{in}})p_{\mathrm{in}}}{0.5T_{\mathrm{S}}V_{\mathrm{o}}{v_{\mathrm{in}}}^2}} = \sqrt{\frac{2L(0.5V_{\mathrm{o}} - v_{\mathrm{in}})i_{\mathrm{ref}}}{0.5T_{\mathrm{S}}V_{\mathrm{o}}v_{\mathrm{in}}}} \tag{6}$$

where i_{ref} is the inductor current reference-generated based on the AVC control scheme, and it is

$$i_{\mathrm{ref}} = k_{\mathrm{e}}v_{\mathrm{e}}v_{\mathrm{in}}{V_{\mathrm{in,avg}}}^2 \tag{7}$$

where v_{e} is the output voltage error signal generated from the outer voltage loop, k_{e} is the constant in the AVC control, and $V_{\mathrm{in,avg}}$ is the average input voltage value.

Replacing i_{ref} in (6) with (7), d_{dcm} is re-expressed as

$$d_{\mathrm{dcm}} = \frac{K\sqrt{v_{\mathrm{e}}}}{V_{\mathrm{in,avg}}}\sqrt{1 - \frac{V_{\mathrm{M}}\left|\sin(\omega t)\right|}{0.5V_{\mathrm{o}}}} \tag{8}$$

where $K = (2Lk_{\mathrm{e}}/T_{\mathrm{S}})^{0.5}$ is a constant, V_{M} is the maximum input voltage, and ω is the line angular frequency. Equation (8) can be used to implement the DCM control.

Furthermore, (8) can be fitted to avoid the use of the square root function for the relief of the DSP calculation burden. First, $[1–V_{\mathrm{M}}\sin(\omega t)/(0.5V_{\mathrm{o}})]^{0.5}$ can be fitted by the Taylor series, which was also be employed in [44] and [45], and show effectiveness. The Taylor series use evaluated series at a chosen expansion point a to fit an equation, which is

$$f(x) = f(a) + \frac{f'(a)}{1!}(x-a) + \frac{f''(a)}{2!}(x-a)^2 + \frac{f'''(a)}{3!}(x-a)^3 + \cdots. \tag{9}$$

Assume $\sin(\omega t)$ in (8) as the variable x and then (8) is fitted by the first and second terms of the Taylor series, as

$$\begin{aligned} d_{\mathrm{dcm,f0}} &= \frac{K\sqrt{v_{\mathrm{e}}}}{V_{\mathrm{in,avg}}}\left[\sqrt{1 - \frac{V_{\mathrm{M}}}{0.5V_{\mathrm{o}}}x_0} - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}\frac{(x-x_0)}{\sqrt{1 - \frac{V_{\mathrm{M}}}{0.5V_{\mathrm{o}}}x_0}}\right] \\ &= \frac{K\sqrt{v_{\mathrm{e}}}}{V_{\mathrm{in,avg}}}\left(1 - \frac{V_{\mathrm{M}}}{0.5V_{\mathrm{o}}}x_0\right)^{-\frac{1}{2}}\left(1 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}x_0 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}x\right). \end{aligned} \tag{10}$$

To determine x_0 in (10), ignoring the phase shift between v_{in} and i_{in}, the PF of the IPOS boost determined by the fitted duty cycle $d_{\mathrm{dcm,f0}}$ is derived in (11) shown at the bottom of the next page, where $m = V_{\mathrm{M}}/V_{\mathrm{o}}$ and $d_{\mathrm{f0}} = {D_0}^2/(1–2m\cdot x_0)$.

Based on (11), Fig. 4 shows PF curve with x_0 and m as variables. As indicted in Fig. 4, when $x_0 = 0.865$, PF remains high within the given input voltage range (represented by m).

$$\begin{aligned} \mathrm{PF} = \frac{P}{S} = \frac{P_{\mathrm{in}}}{V_{\mathrm{in\_RMS}}I_{\mathrm{in\_RMS}}} &= \frac{\frac{1}{\pi}\int_0^{\pi}\left[\frac{0.5T_{\mathrm{S}}V_{\mathrm{o}}}{2L}\frac{{V_{\mathrm{M}}}^2|\sin\omega t|^2}{0.5V_{\mathrm{o}} - V_{\mathrm{M}}|\sin\omega t|}d_{\mathrm{f0}}\left(1 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}x_0 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}|\sin\omega t|\right)^2\right]d(\omega t)}{\frac{V_{\mathrm{M}}}{\sqrt{2}}\sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\left(\frac{0.5T_{\mathrm{S}}V_{\mathrm{o}}}{2L}\right)^2\left(\frac{V_{\mathrm{M}}|\sin\omega t|}{0.5V_{\mathrm{o}} - V_{\mathrm{M}}|\sin\omega t|}\right)^2{d_{\mathrm{f0}}}^2\left(1 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}x_0 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}|\sin\omega t|\right)^4\right]d(\omega t)}} \\ &= \frac{\sqrt{\frac{2}{\pi}}\int_0^{\pi}\frac{|\sin\omega t|^2\left(1 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}x_0 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}|\sin\omega t|\right)^2}{0.5 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}|\sin\omega t|}d(\omega t)}{\sqrt{\int_0^{\pi}\frac{|\sin\omega t|^2\left(1 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}x_0 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}|\sin\omega t|\right)^4}{\left(0.5 - \frac{V_{\mathrm{M}}}{V_{\mathrm{o}}}|\sin\omega t|\right)^2}d(\omega t)}} = \frac{\sqrt{\frac{2}{\pi}}\int_0^{\pi}\frac{|\sin\omega t|^2(1 - mx_0 - m|\sin\omega t|)^2}{0.5 - m|\sin\omega t|}d(\omega t)}{\sqrt{\int_0^{\pi}\frac{|\sin\omega t|^2(1 - mx_0 - m|\sin\omega t|)^4}{(0.5 - m|\sin\omega t|)^2}d(\omega t)}} \end{aligned} \tag{11}$$

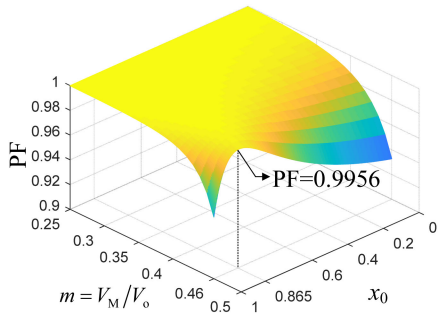

Fig. 4. PF curve, derived by $d_{\mathrm{dcm,f0}}$, with x_0 and m as variables.

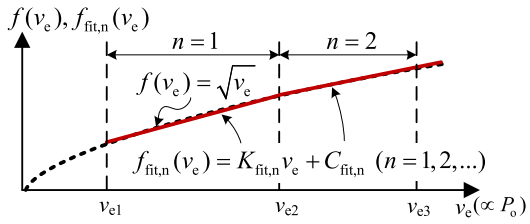

Fig. 5. Theoretical method of fitting $\sqrt{v_e}$ with one or multiple piecewise linear equations in certain v_e ranges.

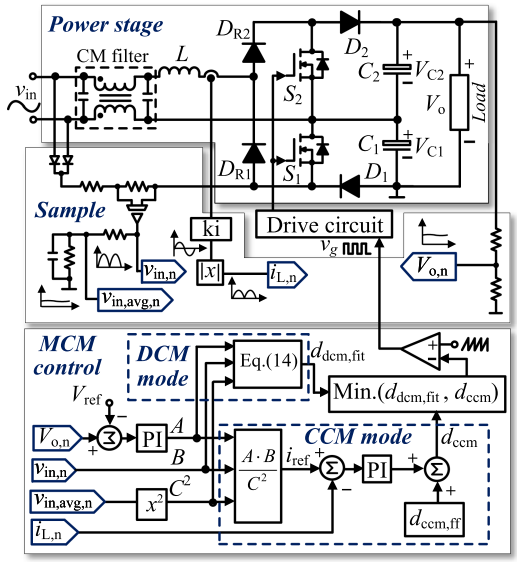

Fig. 6. Control scheme of the MCM controlled IPOS boost with the CCM control law implemented based on the AVC control principle, along with the DFF, and the DCM control law achieved by (14).

Thus, $d_{\mathrm{dcm,f0}}$ is re-expressed as

$$d_{\mathrm{dcm,f1}} = \frac{K\sqrt{v_e}}{V_{\mathrm{in,avg}}}(1 - 0.865\,m - V_M\,|\sin\omega t|V_o). \quad (12)$$

Note that v_{in} is assumed to be the nominal value in the long-term operation, and then m is seen as a constant (=0.389). Thus, $d_{\mathrm{dcm,f1}}$ in (12) is further simplified as

$$d_{\mathrm{dcm,f2}} = \frac{K\sqrt{v_e}}{V_{\mathrm{in,avg}}}\left(1.1618 - \frac{1.7532V_M\,|\sin(\omega t)|}{V_o}\right). \quad (13)$$

Besides, in the digital controller, v_e in (13) is a constant in the steady operation and proportional to the output power ($\propto i_{\mathrm{ref}}$), as indicated in (7). Thus, as shown in Fig. 5, $\sqrt{v_e}$ can be fitted by one linear or piecewise functions $K_{\mathrm{fit,n}}{\cdot}v_e{+}C_{\mathrm{fit,n}}$ in certain v_e ranges. And then, (13) can be re-expressed as

$$d_{\mathrm{dcm,fit}} = \frac{K(K_{\mathrm{fit}}v_e{+}C_{\mathrm{fit}})}{V_{\mathrm{in,avg}}}\left(1.1618{-}\frac{1.7532V_M\,|\sin(\omega t)|}{V_o}\right). \quad (14)$$

It can be seen that by using (14) instead of (8), the DSP calculation burden can be reduced through eliminating the square root function. Thus, the computation time in each switching cycle is reduced. Note that the value of v_e is affected by the control parameters, e.g., k_e in (7). In our case, v_e is around 130 in 100-W load and 460 in 400 W, as observed in the DSP register. Only one linear equation is used finally with $K_{\mathrm{fit}} = 0.024$ and $C_{\mathrm{fit}} = 9.75$.

C. Control Blocks

Fig. 6 shows the MCM control diagram for the IPOS boost. Note that it is identical to that under the AVC control, and thus, there is no increased cost. However, the input voltage sampling circuit of the IPOS boost is slightly different compared to the conventional boost.

Among the MCM control block in Fig. 6, the CCM control principle is based on the AVC control with the CCM DFF for the IPOS boost, different from the DFF of the conventional boost [18]. The DCM control law is (14) oriented, derived directly from the DCM operation, not as the DCM DFF. Besides, instead of using a lookup table, auxiliary circuit, or relatively limited switching frequency, the simplified DCM duty cycle for the IPOS boost is achieved by the Taylor series [44], [45] to reduce the DSP calculation time.

In the proposed MCM control, both the $d_{\mathrm{dcm,fit}}$ and d_{ccm} are calculated during each switching cycle in the DSP. And, the minimal one of $d_{\mathrm{dcm,fit}}$ and d_{ccm} will be chosen finally for the duty cycle d in the next switching cycle, similar to the other MCM controls in [18] and [19].

D. Duty Cycle Selection and Power Loss Analysis

To estimate the power loss between the MCM and AVC controls, for simplifications, assumptions are made as follows.

1) The simplified duty cycle of the MCM control with v_e in (14) is hardly determined, and thus, it is assumed to be the theoretical DCM duty cycle given in (6) for the power loss estimation.
2) When the converter under each control method, the corresponding duty cycle is assumed to be the theoretical expressions in the CCM and DCM without concerns of disturbances.
3) Power losses of the snubber circuits across MOSFETs are not considered, and the input common-mode (CM) choke is seen as the pure resistor.

TABLE I
DESIGN SPECIFICATIONS AND SELECTED COMPONENTS FOR CONVENTIONAL AND IPOS BOOST

Descriptions	Parameters	Components	Topology / Part no. / Quantities
Switching frequency f_S	65 kHz	Inductors L	IPOS: 254* μH, 0077094A7 ×1
Line frequency cycle f_L	60 Hz	(WF ∈ 25% ∼ 40%)	Conv.: 508* μH, 0077730A7 ×1
RMS input voltage V_{in}	110 Vac (90∼135 Vac)	Switches + Heatsinks	IPOS: IPW65R045C7 + SW25-2G (11.4°C/W) ×2
Output voltage V_o	400 V	($T_{cal,S}$∈ 100 ± 2°C)	Conv.: IPW65R045C7 + PA-T21-38E (3.1°C/W) ×1
Output power P_o	850 W	Output capacitors C_X	IPOS: LGG2E152MELB50 (250 V / 1500 μF) ×2
Output voltage ripple $V_{o,rip}$	≤ 10 V @ 850 W	($T_{cal,C}$∈ 95 ± 5 °C)	Conv.: LGG2W391MELB40 (450 V / 390 μF) ×2
RMS input current I_{in}	≤10 A @ 850 W with 90 Vac	Diodes + Heatsinks	IPOS: IDH06G65C5 + SW38-2G (10.2°C/W) ×2
Ambient temperature T_a	-20 °C to 65 °C (T_{am})	($T_{cal,D}$ ∈ 100 ± 2 °C)	Conv.: IDH06G65C5 + SW38-2G (10.2°C/W)×1
Hold-up time t_{hold}	10 ms @ $V_{o,min}$ = 320 V	Rectifier diodes + Heatsinks	IPOS: BU2506 + YB32-4G (6.8°C/W) ×1
Input CM filter	1 mH ×1, 2.2* μF ×2	($T_{cal,DR}$*∈ 135 ± 2°C)	Conv.: PB4006 + PA-T21-38E (3.1°C/W) ×1

∗Note: 1) $T_{cal,DR}$ is set to "135 ± 2°C" since D_R has higher thermal stress ability. 2) By following the same inductor ripple current factor, the IPOS boost can have smaller inductance than the conventional one [7]. 3) Additional parallel CM film capacitors are located in the bottom side of the board.

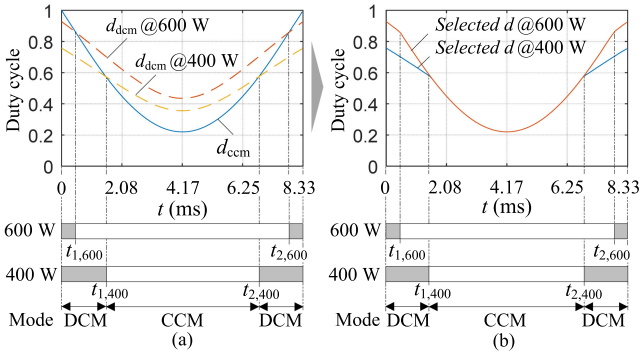

Fig. 7. Examples of theoretical duty cycles at different power loads for the IPOS boost under the MCM control in a half-line cycle. (a) d_{ccm} and d_{dcm}. (b) Selected duty cycle d. Note: The minimal value of the d_{dcm} and d_{ccm} are selected for the final used d in each T_S and here shows the values of d_{dcm}, d_{ccm}, and d in a half-line cycle in two different loads.

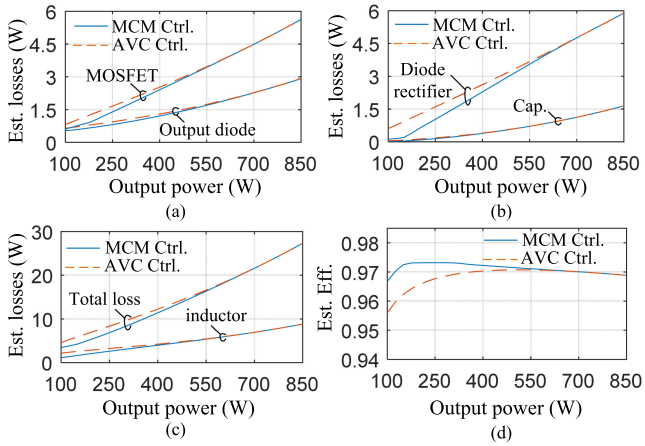

Fig. 8. Estimated component power losses of the IPOS boost under different controls in (a)–(c) and estimated efficiency in (d).

4) The inductance discrepancy of the inductor caused by the "permeability versus dc bias" curve in the Kool Mμ core is not considered [46].

For power loss estimation, Table I gives the design specifications and selected components for the IPOS boost and conventional boost, which follows the same component sizing criteria. Section III has more details.

In one half-line cycle of the ac input, the time period of the converter in the DCM and CCM operations should be clarified for the power loss estimation. In the DCM, the theoretical duty cycle d_{dcm} is given in (6), which is dependent on the power load. In the CCM, the theoretical duty cycle d_{ccm} is

$$d_{ccm} = \frac{0.5V_o - v_{in}}{0.5V_o} \tag{15}$$

which is also the theoretical duty cycle of the AVC control.

Then, based on the DCM and CCM duty cycle expressions in (6) and (15), respectively, along with the specific parameters in Table I, exemplified d_{ccm} and d_{dcm} in one half-line cycle are plotted in Fig. 7(a). Meanwhile, according to the "minimal value" selection criterion, the finally used duty cycle d is shown in 7(b). It can be seen in Fig. 7(b), d_{dcm} is only employed near the zero-crossing of ac input (i.e., near $t = 0$ or 8.33 ms) where the inductor current likely becomes DCM operations in the light loads [see Fig. 1(c)]. In addition, since d_{dcm} is load-dependent, the time instants t_1 and t_2, indicating the DCM and CCM operation periods, also change with power loads.

As shown in Fig. 7, let (6) be equal to (15) (i.e., $d_{ccm} = d_{dcm}$) and considering $v_{in} = V_M \sin(\omega t)$, the time instants t_1 and t_2 for different power load to distinguish the DCM and CCM periods in one half-line cycle can be derived as

$$\begin{cases} t_1 = \sin^{-1}\left(\dfrac{T_S V_o {V_M}^2 - 2LP_oV_o}{2T_S {V_M}^3}\right) \\ t_2 = \pi - \sin^{-1}\left(\dfrac{T_S V_o {V_M}^2 - 2LP_oV_o}{2T_S {V_M}^3}\right). \end{cases} \tag{16}$$

Based on (16), the IPOS boost is considered to operate in the DCM if $t_1 > t \geq 0$ or $t_2 < t \leq T_L/2$ and in the CCM if $t_1 \leq t \leq t_2$ (see Fig. 7).

The component power loss calculations in the DCM are given in the Appendix and the CCM part can be found in [7] and [47]. Combining t_1 and t_2 in (16), the parameters in Table I and the power loss calculation equations, Fig. 8 shows the power loss calculation results. Note that the power loss under the AVC control is estimated by pure CCM duty cycle. As observed in Fig. 8, the MCM control can slightly improve the efficiency in the light-load conditions (max. around 1.0%).

From the control perspective, in the DCM period (near t = 0 or 8.33 ms), the lower d_{dcm} is employed in the MCM control

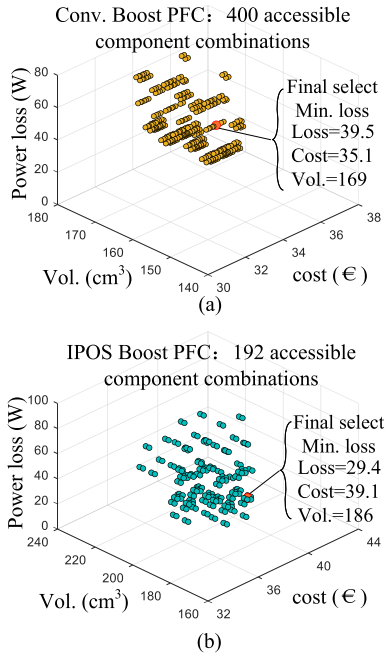

Fig. 9. Criteria-satisfied component combinations for targeted converters. (a) Conventional boost. (b) IPOS boost.

compared with d_{ccm} in the AVC control [see Fig. 7(a)]. Thus, this efficiency improvement can also be perceived as the lower duty cycle in the proposed MCM control contributing to the lower inductor current and power loss. This also explains why this efficiency improvement is gone in the heavy load; since in the heavy load, both the MCM and AVC controls employ the CCM duty cycle. In fact, because the MCM control can lead to low THD_i in the light loads, it means less distorted current flowing into the converter and it also helps the efficiency improvement in the light loads [17].

III. Experimental Validations and Analysis

For comparison consistency, by using the same criteria, the components are selected from the same series of the same manufacturers to avoid the manufacturing technique impacts. Table I gives the selected components based on the built component database [49] and the component criteria [see "components" column]. Fig. 9 shows the criteria-satisfied component combinations for the targeted converters and their performances are estimated by the component-level models.

For each component, key parameters in the datasheet are used to build its cost, volume, and loss-related models. For example, in our case, the MOSFET cost is estimated by using the chip area, as shown in Fig. 10. Then, the chip area can be reflected by the ON-state drain current I_{don} given in the datasheet. Thus, based on the component-level estimation, the converter-level cost, volume, and power loss can be evaluated. This article finally selects the minimal-loss-based component combination for each prototype.

The considered component series are given as follows.

1) The MOSFETs are from Infineon CoolMOS C7 and CP series with the TO-247 package.

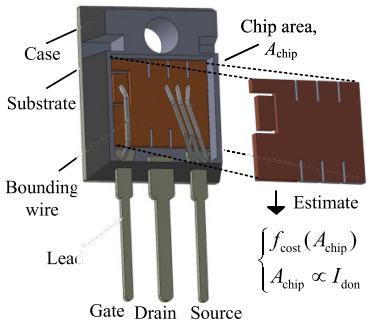

Fig. 10. Key parameter-based component models for converter-level comparison, MOSFET example for building cost model.

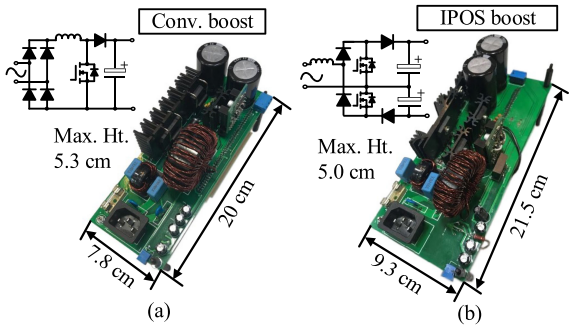

Fig. 11. Built prototypes. (a) Conventional boost. (b) IPOS boost.

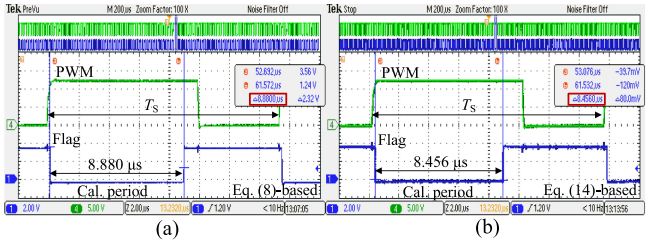

Fig. 12. DSP calculation time comparison (2 µs/div). (a) Equation (8) based MCM control. (b) Equation (14) based MCM control with simplified duty cycle expression. Note: Power stage not operate to avoid the potential sampling time impact.

2) Output diodes are from Infineon CoolSiC G5 with the TO-220 package.
3) Heatsinks are from Aavid with straight and unequal type extruded channel fin and Ohmite *P* series.
4) Toroidal cores are from Magnetics Kool Mμ with the outside diameter sizes between 2.7 and 5.2 cm.
5) Al-Caps are from Nichicon LGG series.
6) Input rectifier diodes from Vishay New isoCink+ diode bridges.

Fig. 11 shows the built prototypes based on Table I. Notably, in Table I, 650-V C7 series MOSFETs are used in the IPOS boost instead of the 500-V P7 series. Because the 500-V MOSFETs have high ON-state resistance and do not satisfy the selection criteria ($T_{\mathrm{cal,S}} \in 100 \pm 2$ °C). Similarly, the Al-Caps are not the same between the converters.

Fig. 12 shows the DSP computation time of using the (8) and (14) based MCM controls, respectively. It shows that the DCM

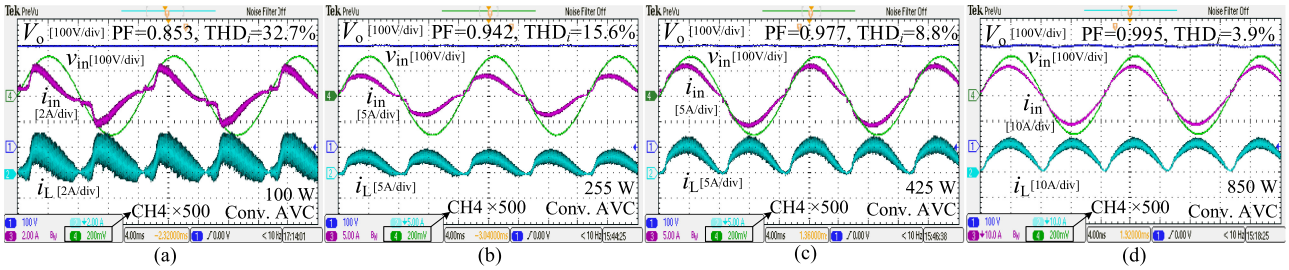

Fig. 13. Waveforms of the Conv. boost under the AVC control in (a) 100; (b) 225 (30% load); (c) 425 (50% load); and (d) 850 W (100% load).

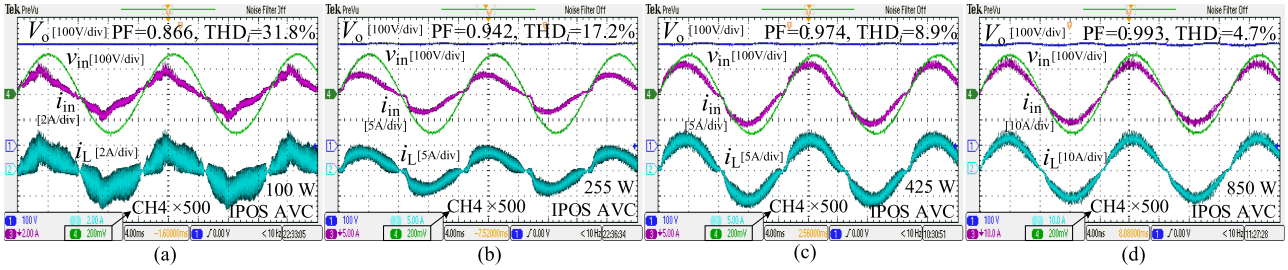

Fig. 14. Waveforms of the IPOS boost under the AVC control in (a) 100; (b) 225 (30% load); (c) 425 (50% load); and (d) 850 W (100% load).

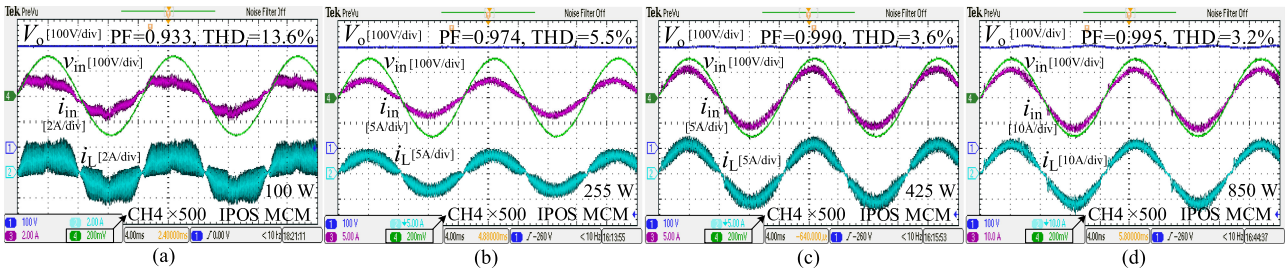

Fig. 15. Waveforms of the IPOS boost under the MCM control in (a) 100; (b) 225 (30% load); (c) 425 (50% load); and (d) 850 W (100% load).

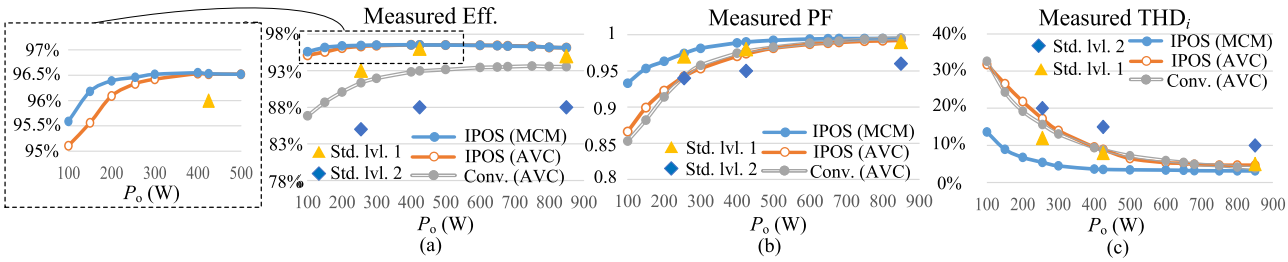

Fig. 16. Measured efficiency, PF, and THD$_i$ of the IPOS boost under the AVC and MCM controls, along with the conventional boost under the AVC control over different loads at 110 VAC input voltage. (a) Efficiency. (b) PF. (c) THD$_i$. Note: Standard level 1 and level 2 are both the requirements in [48] and level 1 is the top-level (more stringent) standard.

duty cycle fitting can reduce the computation time by 424 ns, around 63 time clocks of the employed DSP (150 MHz and 6.67 ns for one time clock).

The MCM control is applied to the IPOS boost prototype and the efficiency, PF, and THD$_i$ are measured by the power analyzer N4L. Figs. 13–15 show the waveforms of the conventional boost under the AVC control, the IPOS boost under the AVC and the MCM controls, respectively. It can be seen that the IPOS boost and conventional boost both under the AVC control have similar PF and THD$_i$ in the different loads. By contrast, the inductor current $i_{\rm L}$ and input current $i_{\rm in}$ of the IPOS boost under the MCM control are more sinusoidal than the IPOS boost under the AVC control.

Fig. 16 shows the measured experimental data over different loads, along with the corresponding standard level 1 and level 2 requirements. Meanwhile, Table II gives the specific measured

TABLE II
MEASURED DATA OF COMPARED CONVERTERS

Loads	Parameters	Conv. AVC	IPOS AVC	IPOS MCM
100 W	PF	0.853	0.866	0.933
	THD_i	32.7%	31.8%	13.6%
	Eff.	86.8%	95.1%	95.6%
225 W (30% load)	PF	0.942	0.942	0.974
	THD_i	15.6%	17.2%	5.5%
	Eff.	91.4%	96.3%	96.5%
425 W (50% load)	PF	0.977	0.974	0.990
	THD_i	8.8%	8.9%	3.6%
	Eff.	93.0%	96.5%	96.5%
680 W (80% load)	PF	0.991	0.990	0.995
	THD_i	5.0%	4.9%	3.2%
	Eff.	93.6%	96.4%	96.4%
850 W (100% load)	PF	0.995	0.993	0.995
	THD_i	3.9%	4.7%	3.2%
	Eff.	93.6%	96.1%	96.1%

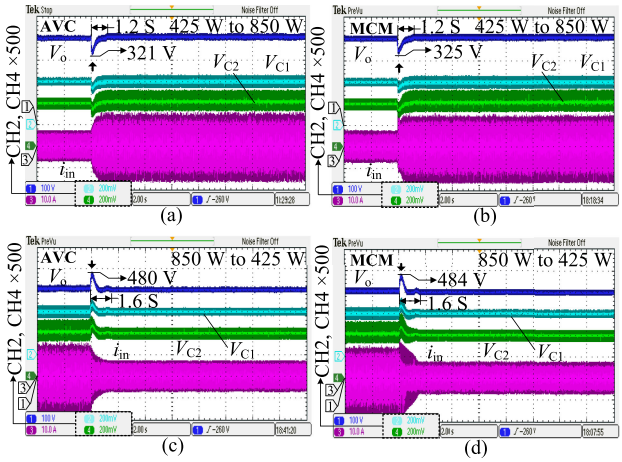

Fig. 17. Load transient test of the IPOS boost with output voltage V_o, capacitor voltages V_{C1} and V_{C2} [100 V/div], input current i_{in} [10 A/div], and time [2 s/div]. (a) 425 to 850 W; and (c) 850 to 425 W test under the AVC control. (b) 425 to 850 W; and (d) 850 to 425 W test under the MCM control.

data of the compared converters in the critical loads. As shown in Fig. 16, it indicates that the IPOS boost and the conventional boost under the AVC control can only satisfy the standard level 2 due to the low PF and poor THD_i in the light loads. By contrast, the IPOS boost under the MCM control with the improved PF and THD_i can meet the stringent standard level 1 requirements (the top-level). Besides, the MCM control slightly increases the efficiency in the light loads (maximum around 0.6%). Note that due to the maximum duty cycle limitation in the reality and the parasitic resonance losses in the DCM [21], the efficiency improvement is not as much as the theoretically predicted in Fig. 8(d). Also, note that due to the biased sampling signals [17], [18], disturbances caused by the switching behavior, etc., the practical PF in the experiment is not close to 1 in the light-load conditions. Fortunately, since it already satisfies the standard level 1, it is still acceptable.

Fig. 17 shows the load transient waveforms of the IPOS boost under the AVC and MCM controls. In the PFC stage, the stable operation after the load transient is more concerned. Thus, the waveforms are shown on a large time scale instead of the switching cycle scale. It can be seen that in both control methods, the voltage overshoot and response time are almost the same. However, the input current i_{in} is different [see Fig. 17(c) and (d)] in the transient period. It is possibly caused by the improper duty cycle d, since a smaller maximum duty cycle limitation (i.e., $d \leq 65\%$, normally $d \leq 91\%$) for the transient period is adopted to suppress V_o overshoot, and it might lead to d switching inappropriately between DCM and CCM in a half-line cycle during the transient period. Anyway, the capacitor voltages V_{C1} and V_{C2} are stable and equal to 200 V before and after the load transient, which means that the automatic balance of the capacitor voltages is not affected by the MCM control. Meanwhile, the output voltage V_o and the input current i_{in} are stable after the load step, and thus, the proposed MCM control for the IPOS boost is effective.

IV. RELIABILITY ANALYSIS

This section mainly presents a mission profile-based reliability analysis approach for the PFC applications, and this reliability analysis procedure is shown in Fig. 18. To implement the analysis, following assumptions are made.

1) A 1-U (=1.75 in) power chassis is assumed in the BTS and two 850-W PSUs operate in a rural area (load mission profile: 400–450 W).
2) The load mission profile in one typical day is considered to repeat within a year.
3) The BTS is assumed in Arizona, USA, and then the one-year ambient temperature data can be used.
4) The component junction/hotspot temperatures are assumed stable in each hour.
5) The interactive thermal impacts between components are not considered for simplicity.
6) The input voltage is considered stable in one year.
7) Al-Caps and semiconductors are seen as critical components and only the wear-out failures described by the corresponding component lifetime models [28], [50] are considered in this article.

A. Mission Profiles and Electro–Thermal Models

Mission profiles and the electro–thermal models are the two vital parts of this approach. Mission profiles mainly reflect the applications and operation condition impacts on the converter reliability. And, the electro–thermal models (details in [7]) reveal the effects of the topology, component (design), and the control method. Thus, they also make the reliability analysis presented in this article different from others [40]–[42]. Note that for the IPOS boost under the MCM control, the required component power loss calculations (needed in Fig. 18 electro–thermal model) can refer to the Appendix.

Extracted from the mission profiles, the power consumption data is sent to the electro–thermal models for calculating the power losses $P_{loss,X}$ of each critical component. Then, the power

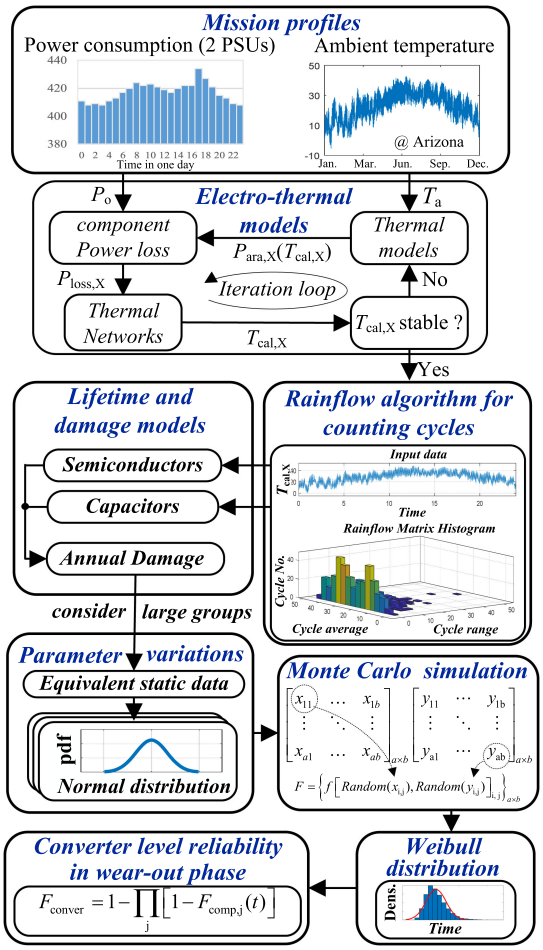

Fig. 18. Reliability analysis procedure and the corresponding mission profiles.

load-dependent efficiency equation $\eta_e(P_o)$ for each topology is used to evaluate the input power P_{in} and the relative input current $i_{in} = P_o/(\eta_e \cdot V_{in})$. Once i_{in} is derived, according to the $P_{loss,X}$ calculation equations [7], [47] and parameters in Table I, $P_{loss,X}$ can be obtained. Afterward, by using the thermal resistant network of the critical component, the calculated junction/hot spot temperature $T_{cal,X}$ is derived. If $T_{cal,X}$ is close to the assumed temperature (T_a+ΔT), then it is seen as stable and sent to the next step for analysis; otherwise, the assumed temperature will be increased to recalculate the thermal-dependent parameters and update $P_{loss,X}$.

B. Annual Damage Calculation

Because the calculated junction/hotspot temperatures over one year are difficult to be used directly in the existing component reliability evaluation models, the rainflow algorithm is employed to identify the thermal cycles and collect the corresponding cycle information, e.g., cycle number n_i for the ith identified cycle, temperature variation $\Delta T_{cal,X,i}$ for the ith identified cycle, etc. Besides, according to [50], a Coffin–Manson law-based MOSFET lifetime model with critical parameters m and α fitted by experimental data is used as

$$N_{f,i} = \alpha \cdot (\Delta T_{cal,X,i})^{-m} \tag{17}$$

where $N_{f,i}$ is the cycle-to-failure under the ith cycle condition. Then, a widely used linear accumulation of the damage model [50]–[52] is adopted to estimate the accumulative damage $D_{mg,semi}$ in one year, which is expressed by n_i and $N_{f,i}$ as

$$D_{mg,semi} = \sum_i (n_i/N_{f,i}). \tag{18}$$

Note that the semiconductors and Al-Caps have different physical structures, wear-out failure mechanisms, failure criteria, etc. Thus, their lifetime models are not identical [28], [40], [50]. Thus, as for the Al-Cap, a popular lifetime evaluation model is used [28] as

$$L_{C,i} = L_{C0} \cdot 2^{\frac{T_0 - T_{hs,i}}{10}} (V_C/V_0)^{-n_0} \tag{19}$$

where L_{C0} is the lifetime under the temperature T_0 and rated voltage V_0, $L_{C,i}$ is the estimated capacitor lifetime of the ith cycle, $T_{hs,i}$ is the mean hot spot temperature identified in the ith cycle, V_C is the applied voltage, and n_0 is the voltage stress exponent. Here, n_0, typically ranging from 3 to 5 [28], is set to 3, as same to [41]. And then, the accumulative damage $D_{mg,cap}$ in one year is

$$D_{mg,cap} = \sum_i (\Delta L_i/L_{C,i}) \tag{20}$$

where ΔL_i is the identified cycle range of the ith cycle.

Fig. 19 shows the calculated temperatures of the key components and their corresponding annual damages (i.e., damage in one year). It can be seen that in the considered mission profiles and the application, the Al-Caps are the weakest part from the converter reliability perspective of view. Besides, the Al-Caps of the IPOS boost under the MCM control receive slightly lower estimated damage than the IPOS boost under the AVC control, much lower than the conventional boost.

C. Parameter Variations and Converter Failure Probability

Probably due to slight differences in microstructures, variations are commonly seen in the real world among individual parameters, test data, measurements, [38], [40], [41], etc. This means that the time-to-failure probability distributions of large group samples have more interest than the fixed time-to-failure of one single sample.

Since the individual parameters, test data, coefficients typically follow the normal (Gaussian or bell-shaped) distribution [38], and the normal distribution can be obtained by specifying the median value and standard deviation. Then, the probability density function (PDF) of the normal distribution can be employed to describe the parameter uncertainties. Thus, each parameter in reliability models in (17) and (19) is updated by PDF for depicting parameter variations. Before the update, the equivalent static data, i.e., the equivalent temperature variation $\Delta T_{cal,X,eqv}$ and capacitor hot spot temperature $T_{hs,eqv}$, need to be determined by the obtained $D_{mg,semi}$ and $D_{mg,cap}$. In fact, $D_{mg,semi}$ and $D_{mg,cap}$ derived in Fig. 19(g) can be seen as the results derived by the equivalent static values. Thus, based on

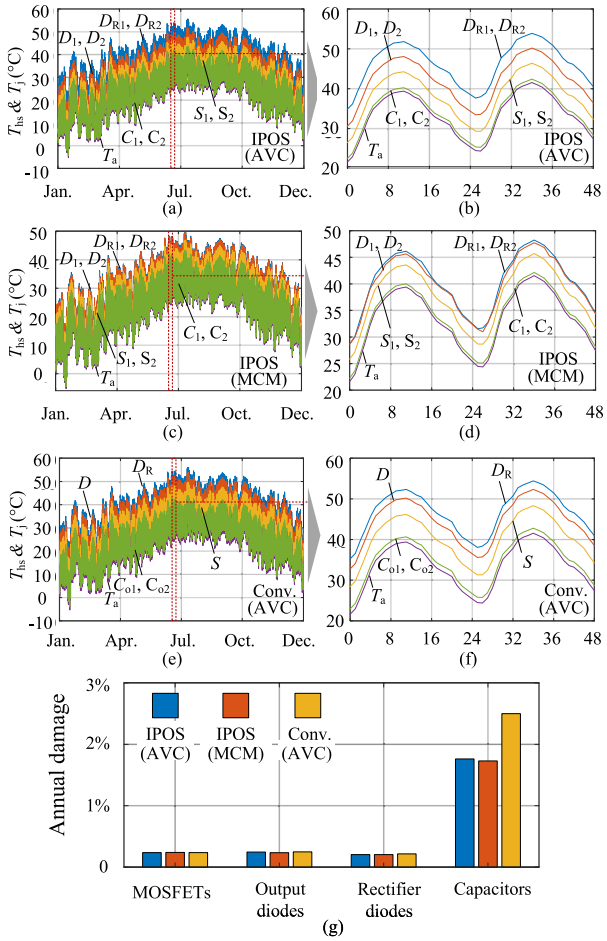

Fig. 19. Calculated junction/hot-spot temperatures of critical components over one year in (a)–(f) and the relative annual damages (per year) in (g).

(17) and (19), $\Delta T_{\mathrm{cal,X,eqv}}$ and $T_{\mathrm{hs,eqv}}$ are

$$\Delta T_{\mathrm{cal,X,eqv}} = \left(\frac{\alpha \cdot D_{\mathrm{mg,semi}}}{365}\right)^{\frac{1}{m}} \tag{21}$$

$$T_{\mathrm{hs,eqv}} = T_0 - 10 \cdot \log_2\left(\frac{8760}{D_{\mathrm{mg,cap}} \cdot L_{\mathrm{C0}} \cdot (V_{\mathrm{C}}/V_0)^{-n_2}}\right) \tag{22}$$

where 365 days are considered as 365 cycles in one year with the corresponding $\Delta T_{\mathrm{cal,X,eqv}}$ to fit the derived $D_{\mathrm{mg,semi}}$ and 8760 h in one year are used with $T_{\mathrm{hs,eqv}}$ to fit $D_{\mathrm{mg,cap}}$.

The reason that cycles and hours are used to obtain the equivalent static variables for semiconductors and Al-Caps, respectively, is that different lifetime models [see (17) and (19)] are employed for their annual damage calculations. By (21) and (22), $\Delta T_{\mathrm{cal,X,eqv}}$ and $T_{\mathrm{hs,eqv}}$ can be derived, respectively. Then, given the 5% variations of each parameter, their PDFs can be obtained as shown in Figs. 20(a) and 21(a).

In addition, the Monte Carlo simulation is conducted to explore the possible results based on the different input parameters from 100 000 samples. Then, the obtained data are fitted by the

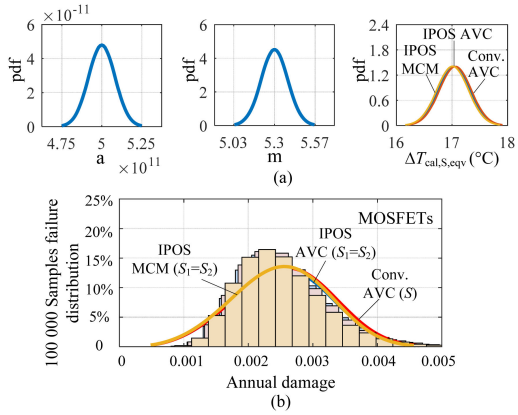

Fig. 20. Reliability analysis of 100 000 MOSFETs in the IPOS boost under the MCM and AVC controls, along with the conventional boost under the AVC control. (a) 5% variations considered in parameter PDFs. (b) Histograms of MOSFET failure distributions.

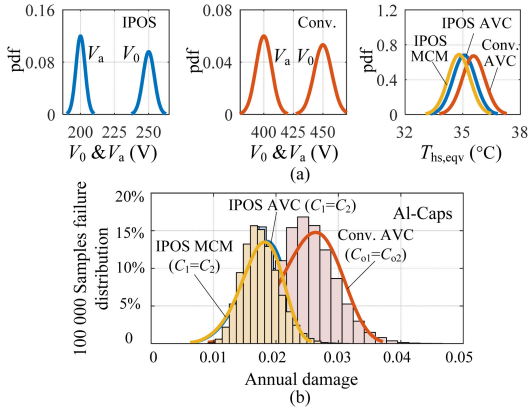

Fig. 21. Reliability analysis of 100 000 Al-Caps in the IPOS under the MCM and AVC controls, along with the conventional boost under the AVC control. (a) 5% variations considered in parameter PDFs (PDFs of L_0, n_0, and T_0 are not shown here for brevity). (b) Histograms of Al-Caps failure distributions.

Weibull distribution [38], [40]–[42], which is

$$f_{\mathrm{comp,j}}(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}}, F_{\mathrm{comp,j}}(t) = 1 - e^{-\left(\frac{t}{\eta}\right)^{\beta}} \tag{23}$$

where β is the scale parameter, η is the shape parameter, and $F_{\mathrm{comp,j}}$ is the corresponding cumulative distribution function of the component j. Figs. 20(b) and 21(b) show the 100 000 MOSFETs and Al-Caps annual damage distributions.

Afterward, the converter-level reliability block diagram (RBD) of the IPOS boost and the conventional boost is shown in Fig. 22. Note that all components in the prototypes are considered in series, because if one fails, the design specifications in Table I cannot be fulfilled. According to the RBD, the converter-level failure function is

$$F_{\mathrm{conver}} = 1 - \prod_{\mathrm{j}} [1 - F_{\mathrm{comp,j}}(t)]. \tag{24}$$

Fig. 23 shows the accumulated failure probability curves of the compared converters and the corresponding components

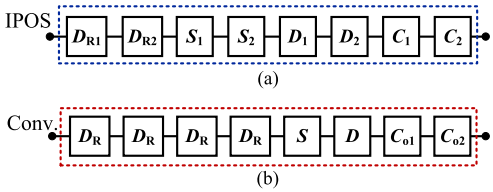

Fig. 22. Considered RBD for converter-level reliability calculations. (a) IPOS boost. (b) Conventional boost.

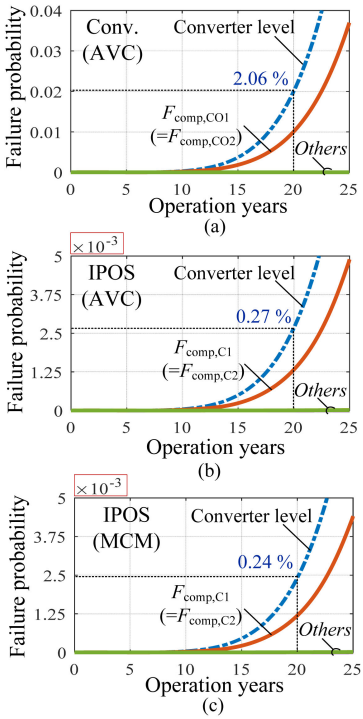

Fig. 23. Estimated accumulated wear-out failure probability curves of the compared converters. (a) Conventional boost under the AVC control. (b) IPOS boost under the AVC control. (c) IPOS boost under the MCM control. Note: here "others" represent the semiconductors.

under the investigated mission profiles in the BTS applications. Note that the $F_{\mathrm{comp,j}}$ curve shown in Fig. 23 only indicates the failure probability of one component j. And, if there are dual components j employed in the converter level, two identical $F_{\mathrm{comp,j}}$ need to be considered in (24) to estimate F_{conver}. As observed in Fig. 23, in this study case, the Al-Caps are the major factors affecting the converter-level accumulated failure in the wear-out phase. Meanwhile, given 20 years designed lifetime, the estimated accumulated failure of the IPOS boost under the MCM control is 0.24%, slightly decreased compared with that of the IPOS boost under the AVC control (0.27%), and much lower than that of the conventional boost (2.06%). Based on the analysis results, there are following two conclusions.

1) *IPOS With AVC Versus Conv. With AVC:* Given the relatively high maintenance cost in rural area, the IPOS boost topology with the lower accumulated failure is an attractive solution compared to the conventional boost. Even though within the same design, the estimated payback period of using the IPOS boost topology instead of the conventional one is 3.9 years in rural area [7].

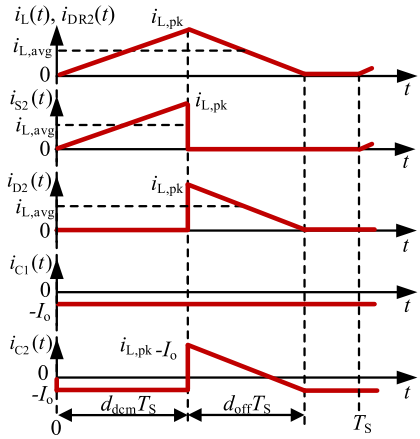

Fig. 24. Key waveforms of the IPOS boost operating in the DCM during the positive half-line period.

2) *IPOS With AVC Versus IPOS With MCM:* The proposed MCM controlled IPOS boost not only shows improved PF and THD$_i$ performance but also the reduced accumulated failure. Even though the accumulated failure is only slightly decreased, it should be noted that it is achieved by only the software update without extra material cost.

V. Conclusion

Combining the BTS load mission profile, an MCM-controlled IPOS boost was proposed to mainly improve the PF and THD$_i$ performance in the light-load conditions. Further analysis also indicated the slightly increased efficiency, and then the experiment test verified the control effectiveness and the improved performance. Besides, based on the typical BTS mission profiles in a rural area, the mission profile-based reliability analysis for the PFC converter was presented to analyze the accumulated wear-out failure of the IPOS boost under the AVC control and the MCM control, along with the conventional boost under the AVC control. The results, considering the wear-out failure of semiconductors and Al-Caps, indicated that within 20 years of operation, the IPOS boost under the MCM control has the accumulated failure of 0.24%, slightly lower than the IPOS boost under the AVC control (0.27%) and much lower than the conventional boost under the AVC control (2.06%). Although the MCM-controlled IPOS boost only decreases 0.03% accumulated failure than the IPOS boost with the AVC control, it requires only software update without additional material cost. In summary, the MCM-controlled IPOS boost PFC converter can be a good candidate for the telecom application in rural area.

Appendix

This part introduces the power loss calculations of the key components in the IPOS boost. Fig. 24 shows the key waveforms in the DCM operation. The switch, inductor, and capacitor rms currents in one switching cycle, i.e., $i_{\mathrm{S2,RMS}}$, $i_{\mathrm{L,RMS}}$, $i_{\mathrm{C1,RMS}}$, and $i_{\mathrm{C2,RMS}}$, are

$$i_{\mathrm{S2,RMS}}^2 = \frac{8T_{\mathrm{S}}^{1/2}p_{\mathrm{in,th}}^{3/2}(0.5V_{\mathrm{o}} - v_{\mathrm{in}})^{3/2}}{3v_{\mathrm{in}}L^{1/2}V_{\mathrm{o}}^{3/2}} \tag{A.1}$$

$$i_{\mathrm{L,RMS}}^2 = \frac{4p_{\mathrm{in,th}}^{3/2} T_{\mathrm{S}}^{1/2} (0.5V_{\mathrm{o}} - v_{\mathrm{in}})^{1/2}}{3v_{\mathrm{in}} L^{1/2} V_{\mathrm{o}}^{1/2}} \tag{A.2}$$

$$i_{\mathrm{C2,RMS}}^2 = i_{\mathrm{D2,RMS}}^2 - I_{\mathrm{o}}^2 = \frac{8p_{\mathrm{in,th}}^{3/2} T_{\mathrm{S}}^{1/2} (0.5V_{\mathrm{o}} - v_{\mathrm{in}})^{1/2}}{3L^{1/2} V_{\mathrm{o}}^{3/2}} - I_{\mathrm{o}}^2 \tag{A.3}$$

$$i_{\mathrm{C1,RMS}}^2 = I_{\mathrm{o}}^2 \tag{A.4}$$

where $p_{\mathrm{in,th}}$ is the theoretical instantaneous input power, i.e., $p_{\mathrm{in,th}} = i_{\mathrm{in}} \cdot v_{\mathrm{in}}$. The output diode and rectifier diode AVCs in one switching cycle, i.e., $i_{\mathrm{D,avg}}$ and $i_{\mathrm{DR2,avg}}$, are

$$i_{\mathrm{D2,avg}} = \frac{2p_{\mathrm{in,th}}}{V_{\mathrm{o}}} \tag{A.5}$$

$$i_{\mathrm{DR2,avg}} = \frac{2p_{\mathrm{in,th}}(0.5V_{\mathrm{o}} - v_{\mathrm{in}})}{V_{\mathrm{o}} v_{\mathrm{in}}}. \tag{A.6}$$

Note that (A.1)–(A.6) are the derived results in one switching cycle, the corresponding rms and AVCs in a half-line cycle can be further derived as

$$i_{\mathrm{X,RMS,L}}^2 = \frac{1}{1/2T_{\mathrm{L}}} \int_0^{1/2T_{\mathrm{L}}} i_{\mathrm{X,RMS}}^2(t)dt, \mathrm{X} \in \{L, S, C\} \tag{A.7}$$

$$i_{\mathrm{Y,avg,L}} = \frac{1}{1/2T_{\mathrm{L}}} \int_0^{1/2T_{\mathrm{L}}} i_{\mathrm{Y,avg}}(t)dt, \mathrm{Y} \in \{D, DR\}. \tag{A.8}$$

REFERENCES

[1] B. Huang, G. Torrico, X. Ma, and Y. Liang, "High efficiency telecom rectifier designed for wireless communication networks," in *Proc. IEEE 33rd Int. Telecommun. Energy Conf.*, 2011, pp. 1–6.

[2] J. W. Kolar, J. Biela, and J. Minibock, "Exploring the pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2% efficiency vs. 7 kW/dm^3 power density," in *Proc. Int. Power Electron. Motion Control Conf.*, 2009, pp. 1–21.

[3] A. F. de Souza and I. Barbi, "A new ZVS-PWM unity power factor rectifier with reduced conduction losses," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 746–752, Nov. 1995.

[4] F. Musavi, M. Edington, W. Eberle, and W. G. Dunford, "Evaluation and efficiency comparison of front end AC–DC plug-in hybrid charger topologies," *IEEE Trans. Smart Grid*, vol. 3, no. 1, pp. 413–421, Mar. 2012.

[5] Z. Chen, B. Liu, Y. Yang, P. Davari, and H. Wang, "Bridgeless PFC topology simplification and design for performance benchmarking," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5398–5414, May 2021.

[6] B. Zhao, A. Abramovitz, and K. Smedley, "Family of bridgeless buck-boost PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6524–6527, Dec. 2015.

[7] Z. Chen, P. Davari, and H. Wang, "Single-phase bridgeless PFC topology derivation and performance benchmarking," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9238–9250, Sep. 2020.

[8] J. C. Salmon, "Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase AC supplies and using either single or split DC rail voltage outputs," in *Proc. Appl. Power Electron. Conf. Expo.*, 1995, pp. 473–479.

[9] Y. Tang, D. Zhu, C. Jin, P. Wang, and F. Blaabjerg, "A three-level quasi-two-stage single-phase PFC converter with flexible output voltage and improved conversion efficiency," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 717–726, Feb. 2015.

[10] J. He, X. Ruan, and L. Zhang, "Adaptive voltage control for bidirectional converter in flicker-free electrolytic capacitor-less AC–DC LED driver," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 320–324, Jan. 2017.

[11] C.-C. Lin and Y.-Y. Tzou, "Green mode control strategy of a PMSM with front-end SEPIC PFC converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 1476–1481.

[12] L. Huang, F. Chen, W. Yao, and Z. Lu, "Flexible mode bridgeless boost PFC rectifier with high efficiency over a wide range of input voltage," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3513–3524, May 2017.

[13] F.-Z. Chen and D. Maksimović, "Digital control for improved efficiency and reduced harmonic distortion over wide load range in boost PFC rectifiers," *IEEE Trans. Power Electron.*, vol. 25, no. 10, pp. 2683–2692, Oct. 2010.

[14] Q. Li, F. C. Lee, M. Xu, and C. Wang, "Light load efficiency improvement for PFC," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2009, pp. 3755–3760.

[15] W.-S. Wang and Y.-Y. Tzou, "Light load efficiency improvement for AC/DC boost PFC converters by digital multi-mode control method," in *Proc. IEEE 9th Int. Power Electron. Drive Syst.*, 2011, pp. 1025–1030.

[16] K. De Gussemé, D. M. van de Sype, A. P. M. van den Bossche, and J. A. Melkebeek, "Input-current distortion of CCM boost PFC converters operated in DCM," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 858–865, Apr. 2007.

[17] S. F. Lim and A. M. Khambadkone, "A simple digital DCM control scheme for boost PFC operating in both CCM and DCM," *IEEE Trans. Ind. Appl.*, vol. 47, no. 4, pp. 1802–1812, Jul./Aug. 2011.

[18] K. De Gussemé, D. M. van de Sype, A. P. M. van den Bossche, and J. A. Melkebeek, "Digitally controlled boost power-factor-correction converters operating in both continuous and discontinuous conduction mode," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 88–97, Feb. 2005.

[19] L. Roggia, F. Beltrame, J. E. Baggio, and J. R. Pinheiro, "Digital control system applied to a PFC boost converter operating in mixed conduction mode," in *Proc. Brazilian Power Electron. Conf.*, 2009, pp. 698–704.

[20] R. K. Tripathi, S. P. Das, and G. K. Dubey, "Mixed-mode operation of boost switch-mode rectifier for wide range of load variations," *IEEE Trans. Power Electron.*, vol. 17, no. 6, pp. 999–1009, Nov. 2002.

[21] H.-S. Youn, J.-S. Park, K.-B. Park, J.-I. Baek, and G.-W. Moon, "A digital predictive peak current control for power factor correction with low-input current distortion," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 900–912, Jan. 2016.

[22] C. W. Clark, F. Musavi, and W. Eberle, "Digital DCM detection and mixed conduction mode control for boost PFC converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 347–355, Jan. 2014.

[23] GSMA, "Closing the coverage gap: How innovation can drive rural connectivity," Accessed: Jul. 17, 2019. [Online]. Available: https://www.gsma.com/mobilefordevelopment/wp-content/uploads/2019/07/GSMA-Closing-The-Coverage-Gap-How-Innovation-Can-Drive-Rural-Connectivity-Report-2019.pdf

[24] S. Allemann, J. Biela, and M. Held, "Reliability comparison of a dual boost and a triangular current mode resonant-transition PFC converter topology," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst.*, 2012, pp. 1–5.

[25] H. Wu, S. Wong, C. K. Tse, S. Y. R. Hui, and Q. Chen, "Single-phase LED drivers with minimal power processing, constant output current, input power factor correction, and without electrolytic capacitor," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 6159–6170, Jul. 2018.

[26] S. Li, S.-C. Tan, C. K. Lee, E. Waffenschmidt, S. Y. Hui, and C. K. Tse, "A survey, classification, and critical review of light-emitting diode drivers," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1503–1516, Feb. 2016.

[27] H. Ma, J. Lai, C. Zheng, and P. Sun, "A high-efficiency quasi-single-stage bridgeless electrolytic capacitor-free high-power AC–DC driver for supplying multiple LED strings in parallel," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5825–5836, Aug. 2016.

[28] H. Wang and F. Blaabjerg, "Reliability of capacitors for DC-link applications in power electronic converters - An overview," *IEEE Trans. Ind. Appl.*, vol. 50, no. 5, pp. 3569–3578, Sep./Oct. 2014.

[29] A. Lahyani, P. Venet, G. Grellet, and P. J. Viverge, "Failure prediction of electrolytic capacitors during operation of a switchmode power supply," *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1199–1207, Nov. 1998.

[30] K. Abdennadher, P. Venet, G. Rojat, J. Rétif, and C. Rosset, "A real-time predictive-maintenance system of aluminum electrolytic capacitors used in uninterrupted power supplies," *IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1644–1652, Jul./Aug. 2010.

[31] B. Sun, X. Fan, C. Qian, and G. Zhang, "PoF-simulation-assisted reliability prediction for electrolytic capacitor in LED drivers," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6726–6735, Nov. 2016.

[32] A. H. Ranjbar, B. Abdi, G. B. Gharehpetian, and B. Fahimi, "Reliability assessment of single-stage/two-stage PFC converters," in *Proc. Compat. Power Electron.*, 2009, pp. 253–257.

[33] B. Abdi, A. H. Ranjbar, J. Milimonfared, and G. B. Gharehpetian, "Reliability comparison of boost PFC converter in DCM and CCM operating modes," in *Proc. Int. Symp. Power Electron., Elect. Drives, Automat. Motion*, 2008, pp. 939–943.

[34] H. Valipour, M. F. Firouzabad, G. Rezazadeh, and M. R. Zolghadri, "Reliability comparison of two industrial AC/DC converters with resonant and non-resonant topologies," in *Proc. 6th Power Electron. Drive Syst. Tech. Conf.*, 2015, pp. 430–435.
[35] Y. Song and B. Wang, "Survey on reliability of power electronic systems," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 591–604, Jan. 2013.
[36] J. W. Harms, "Revision of MIL-HDBK-217, reliability prediction of electronic equipment," in *Proc. Annu. Rel. Maintainability Symp.*, 2010, pp. 1–3.
[37] G. A. Klutke, P. C. Kiessler, and M. A. Wortman, "A critical look at the bathtub curve," *IEEE Trans. Rel.*, vol. 52, no. 1, pp. 125–129, Mar. 2003.
[38] J. W. McPherson, *Reliability Physics and Engineering: Time-to-Failure Modeling*, 1st ed. Cham, Switzerland: Springer, 2013.
[39] H. Wang *et al.*, "Transitioning to physics-of-failure as a reliability driver in power electronics," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 2, no. 1, pp. 97–114, Mar. 2014.
[40] D. Zhou, H. Wang, and F. Blaabjerg, "Mission profile based system-level reliability analysis of DC/DC converters for a backup power application," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 8030–8039, Sep. 2018.
[41] Y. Shen, A. Chub, H. Wang, D. Vinnikov, E. Liivik, and F. Blaabjerg, "Wear-out failure analysis of an impedance-source PV microinverter based on system-level electro-thermal modeling," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3914–3927, May 2019.
[42] Y. Zhang, H. Wang, Z. Wang, F. Blaabjerg, and M. Saeedifard, "Mission profile-based system-level reliability prediction method for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6916–6930, Jul. 2020.
[43] D. M. van de Sype, K. de Gussemé, A. P. M. van den Bossche, and J. A. Melkebeek, "Duty-ratio feedforward for digitally controlled boost PFC converters," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 108–115, Feb. 2005.
[44] Z. Chen, P. Yang, G. Zhou, J. Xu, and Z. Chen, "Variable duty cycle control for quadratic boost PFC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 7, pp. 4222–4232, Jul. 2016.
[45] K. Yao, X. Ruan, X. Mao, and Z. Ye, "Variable-duty-cycle control to achieve high input power factor for DCM boost PFC converter," *IEEE Trans. Ind. Electron.*, vol. 58, no. 5, pp. 1856–1865, May 2011.
[46] Magnetics, "Power cores catalog 2017," 2017. [Online]. Available: https://www.mag-inc.com/Media/Magnetics/File-Library/Product%20Literature/Powder%20Core%20Literature/2017-Magnetics-Powder-Core-Catalog.pdf
[47] L. Huber, Y. Jang, and M. M. Jovanović, "Performance evaluation of bridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.
[48] *48V Rectifier for Telecommunications*, YD/T 731-2018, Ministry of Industry and Information Technology, Beijing, China, 2018.
[49] Z. Chen, P. Davari, H. Wang, "Component database for topology benchmarking with guidelines of how to use it," distributed by IEEE Dataport, 2021, doi: 10.21227/jcdv-c792.
[50] A. Testa, S. de Caro, and S. Russo, "A reliability model for power MOSFETs working in avalanche mode based on an experimental temperature distribution analysis," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3093–3100, Jun. 2012.
[51] M. A. Miner, "Cumulative damage in fatigue," *Trans. ASME. J. Appl. Mech.*, vol. 12, pp. A-159–A-164, Sep. 1945.
[52] S. Russo *et al.*, "Reliability assessment of power MOSFETs working in avalanche mode based on a thermal strain direct measurement approach," *IEEE Trans. Ind. Appl.*, vol. 52, no. 2, pp. 1688–1697, Mar. 2016.

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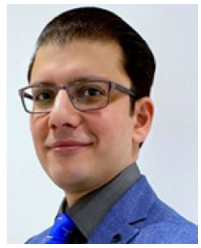

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