A High-Efficiency Fast-Transient LDO With Low-Impedance Transient-Current Enhanced Buffer

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***Abstract*—This article proposes a new low-impedance transient-current enhanced (LTE) buffer, which is applied for low-dropout regulator (LDO) with large off-chip capacitor. The LTE buffer is based on current-shunt feedback technique and two ac coupling networks, which can achieve an extremely low output impedance and high charging/discharging current of the gate of power transistor at load transient response, while maintaining low-quiescent current consumption under the full-load range. In addition to containing the LTE buffer, the proposed LTE-LDO employs recycling-folded-cascode amplifier as the error amplifier, which has the advantage of high loop gain, loop bandwidth, and current efficiency. Meanwhile, simple Miller compensation with a nulling resistor is employed for frequency compensation and a complete small-signal analysis under different load current conditions is given in this article. This design has been implemented in semiconductor manufacturing international corporation 0.18 μm complementary metal–oxide–semiconductor process and the experimental results show that the quiescent current consumption is about 48 μA, and the maximum current efficiency of the LTE-LDO is 99.976%. The measured transient response shows that under the condition of 1 μF load capacitance, when the load current changes to 200 mA/100 ns, the output voltage change is 76 mV.**

***Index Terms*—Comprehensive stability analysis, high efficiency, low-dropout regulator (LDO), low-impedance transient-current enhanced (LTE) buffer, recycling-folded-cascode (RFC).**

I. Introduction

THERE are four major performance requirements of low-dropout regulator (LDO), including low-dropout voltage, high output current, low no-load quiescent current, and small output transient undershoots and overshoots [1]–[5]. In LDO design, the ability to source high load current while achieving low-dropout voltage requires the use of a large size positive channel metal–oxide–semiconductor (PMOS) transistor as the pass device. For the traditional LDO with a large off-chip capacitor, the large gate capacitance of the PMOS pass device creates a low-frequency nondominant pole within the unity-gain frequency of the loop, thereby degrading stability [6]–[11]. In addition, the large gate capacitance of the PMOS pass device will also decrease the slew rate (SR) at the gate of the power transistor, which makes the transient response of LDO worse [12]–[16]. Therefore, a voltage buffer generally needs to be inserted between the error amplifier and the power transistor to isolate the high output resistance of the error amplifier and the large gate capacitance of the power transistor, to improve both the loop stability and transient response for the LDO. Specifically, the typical diagram of the traditional LDO with a large off-chip capacitor using the buffer is shown in Fig. 1 [18].

In the previous works, different kinds of voltage buffers have been proposed [17]–[24]. The most primitive buffer is realized by using a source follower, which is shown in Fig. 2. The output resistance of this buffer is the reciprocal of its transconductance that can be increased by two ways. One is to increase width-to-length ratio of the transistor, but an excessively large size results in a large gate parasitic capacitance, which lowers the position of the pole at the output of the error amplifier. Another is to increase quiescent current, but this causes excessive power consumption. Therefore, this buffer has no advantage in current efficiency. Besides, there are two kinds of commonly used buffer techniques based on source follower. One is the current-shunt feedback-based buffers [18]–[22], specifically, all of them mainly employ impedance attenuation technique, combined with current-shunt feedback, which greatly reduces the output impedance of the buffer. Among them, the most representative is the impedance-attenuated buffer proposed in [18]. However, this kind of buffer adopts adaptive bias technique, consuming large quiescent current under the heavy load condition, thereby resulting in low current efficiency of LDO. Another kind of buffers mainly use ac coupling networks [23], where the most representative is the energy-efficient voltage buffer proposed in [23]. This buffer contains a current-boosting circuit with quick-ON and auto-OFF features so that it can momentarily provide an extra current to charge and discharge the large gate capacitance of the power transistor. Meanwhile, the quiescent current of this buffer remains constantly low under the full-load range, ensuring high-current efficiency for the LDO. However, the output impedance of this kind of buffer is relatively high, resulting that the nondominant pole at the gate of power transistor cannot be effectively separated to a high frequency. Hence, additional equivalent series resistance (ESR) needs to be added to ensure the stability, which increases the transient voltage changes.

Consequently, in order to effectively overcome the previously mentioned buffer challenges, this article proposes a new

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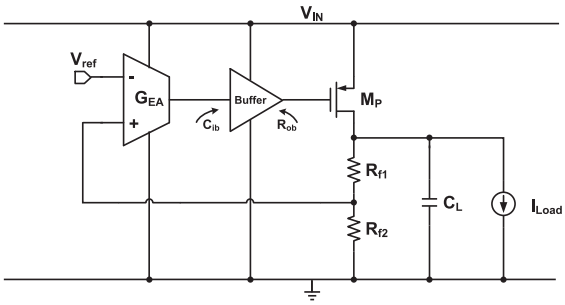


Fig. 1. Conventional block diagram of LDO with buffer.

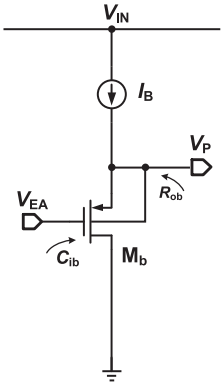


Fig. 2. Schematic of source follower.

low-impedance transient current-enhanced (LTE) buffer. The proposed low-impedance transient current-enhanced buffer (LTE buffer) is designed based on current-shunt feedback technique and two ac coupling networks, which can achieve extremely low output impedance and high charging and discharging current of the gate of power transistor when the load current is switched, while maintaining low-quiescent current consumption under the full-load range. In addition to containing the LTE buffer, the proposed LTE-LDO employs the recycling-folded-cascode (RFC) amplifier as the error amplifier, which has the advantage of high loop gain, loop bandwidth, and current efficiency. As a result, the proposed LTE-LDO can achieve fast transient response and high-current efficiency. At the same time, Miller compensation with a nulling resistor (SMCNR) is used to ensure loop stability for the proposed LTE-LDO. Although SMCNR is commonly used, the stability analysis in the full-load current range has not been mentioned by the previous works. Therefore, by calculating the transfer function of the system under different load current conditions, this article gives a complete small-signal analysis under different load current conditions.

The rest of this article is organized as follows. Section II introduces the proposed LTE buffer about its structure, characteristic, and signal analysis. Section III mainly presents the detailed design and stability analysis under full-load conditions of the proposed LTE-LDO. Sections IV and V give simulation and experimental results and the final conclusion about this approach, respectively. Finally, Section V concludes this article.

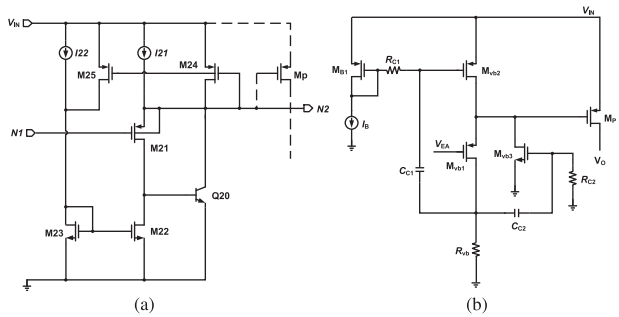


Fig. 3. Traditional buffers (a) with current-shunt feedback and (b) with current-boosting circuit.

II. Proposed LTE Buffer

For traditional LDOs with off-chip large capacitors, the load current is usually relatively large. In order to maintain a low-dropout voltage, the size of the power transistor needs to be designed to be large. This introduces a low-frequency subdominant pole at the output of the error amplifier. When the load current gradually increases, the bandwidth of the loop also increases, so that the nondominant pole is located within the frequency range of the unit bandwidth of the loop, which leads to a stability problem of the loop. In order to increase the phase margin of the loop, one way is to use ESR compensation to make the circuit generate a zero on the left half plane. However, this method will make the transient response worse, especially when the load current jumps greatly, this situation will be more serious. In order to ensure the stability of the loop without deteriorating the transient response, a voltage buffer needs to be added between the error amplifier and the power transistor.

The addition of the voltage buffer separates the output resistance of the error amplifier and the parasitic capacitance of the gate of the power transistor. Since the parasitic capacitance at the input of the buffer is relatively small, the output resistance is also relatively low, so the dominant pole that was originally at low frequency is, thus, converted into two higher frequency poles, which improves the phase margin. And a voltage buffer with the superior performance should not only have extremely low output impedance and be able to push the output pole to high frequencies, but also have a large SR to improve transient response.

The most commonly used two kinds of buffers are shown in Fig. 3. Specifically, Fig. 3(a) shows the impedance-attenuated voltage buffer proposed in [18], which uses current-shunt feedback to reduce the resistance at the output. And its output resistance can be expressed as

$$R_{OUT} = \frac{1}{g_{m21}(1+\beta) + g_{m24}}. \tag{1}$$

Among them, g_{m21} and g_{m24} represent the transconductance of M21 and M24, respectively, and β represent the magnification of Q20. Although this kind of buffer can effectively reduce the output impedance, it adopts the adaptive bias structure, thereby resulting in high-quiescent current consumption under the heavy load condition.

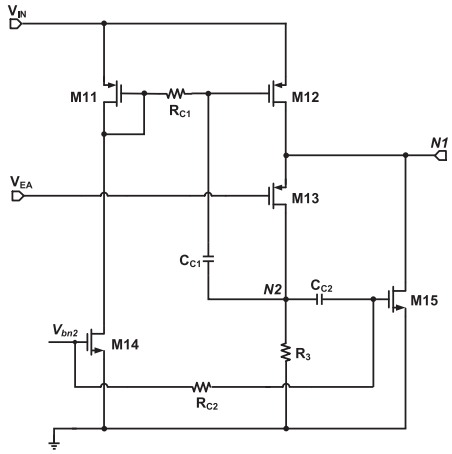


Fig. 4. Schematic of the proposed LTE buffer.

In addition, Fig. 3(b) shows the energy-efficient voltage buffer proposed in [23], which contains a current-boosting circuit with quick-ON and auto-OFF features so that it can momentarily provide an extra current to charge and discharge the large gate capacitance of the power transistor while maintaining low-quiescent current. The output impedance R_{ob}(s) of this buffer can be expressed as

$$R_{\rm ob} \approx \frac{1}{g_{mvb1}(1+\delta R_{vb} g_{mvb2})}. \tag{2}$$

Among them, $\delta = C_{C1}/(C_{\rm gsvb2}+C_{C1})$, this buffer introduces an impedance attenuation factor $\delta R_{\rm vb} g_{\rm mvb2}$, which can reduce the output resistance to a certain extent. However, since $M_{\rm vb3}$ is in the OFF-state in the steady state, parallel feedback cannot be formed. Therefore, the attenuation of the output impedance of the buffer is relatively weak.

Consequently, in order to effectively reduce the output impedance of the buffer under the condition of low-quiescent current, and at the same time increase the charge and discharge current of the gate of the power transistor when the load current is switched, this article proposes a new LTE buffer, the schematic of which is shown in Fig. 4. This buffer mainly includes source follower M13, current mirror load M12, shunt transistor M15, two ac coupling networks (respectively, composed of R_{C1}, C_{C1} and R_{C2}, C_{C2}), resistor R_3, and also includes M11 and M14 providing current for M12 and M15.

When the circuit is in a steady state, C_{C1} and C_{C2} are both in an open state, M11 and M12 form a pair of current mirrors, and the gate voltage of the M12 is equal to the gate voltage of the M11, so the quiescent current flowing through M12 is determined by the ratio of the current mirror and the quiescent current flowing through M11 is determined. The current of the M13 branch is determined by the current flowing through the M12 and M15 branch.

When the load of the LDO changes, there is an over/undershoot at the node N1 since the slow loop response. The variable voltage is fed back to the error amplifier to adjust the gate voltage $V_{\rm EA}$ of M13. Thus, the current through M13 changes, resulting in the voltage of the N2 node changing. The coupling network composed of R_{C1}, C_{C1}, R_{C2}, and C_{C2} will transmit this voltage change to the gates of M12 and M15, respectively. At this time, the voltages at the gates of M12 and M15 are no longer equal to the voltage at the gate terminals of M11 and M14, which will cause transient currents in M12 and M15, thereby effectively increasing the SR at the output. In order to explain in more detail the working principle of this buffer and its role in reducing output impedance and improving transients, the following will analyze the large-signal response process in detail, and give the specific expression of output impedance through small-signal analysis.

A. Large-Signal Analysis

When the output of the LDO switches from a small load current to a large load current, because the loop is too late to respond, the required additional load current is provided by the discharge of the load capacitor. At this time, the voltage on the upper plate of the capacitor drops, and the output voltage will decrease accordingly, resulting in undershoot. This voltage change is transmitted to the positive input of the error amplifier through the feedback network, and is amplified by the error amplifier and then transmitted to the gate of M13, pulling down its gate voltage. At this time, the current flowing through M13 will increase instantaneously. And the voltage at N2 rises accordingly and is coupled to the gate of M12 via C_{C1} so that the flow of M12 is turned OFF instantaneously and fed back to the gate of M15 via C_{C2}, making the current flowing through M15 instantly increased by i_{disch}. Therefore, the addition of two ac coupling networks can significantly enhance the discharge effect of the output of buffer on the gate of MP. This response process of the above large signals can be shown in Fig. 5(a).

When the output of LDO switches from a large load current to a small load current, the output voltage will rise accordingly, generating an overshoot voltage. Meanwhile, the output voltage of the error amplifier will rise, and the gate voltage of M13 will increase, reducing the current flowing through M13. The voltage drop at point N2 pulls down the voltage of the gate of M12 through the coupling of C_{C1}, so M12 will generate additional charging current i_{ch} through the coupling of C_{C2}, which pulls down the voltage of the gate of M15 to make M15 turn OFF instantaneously. Obviously, under the action of C_{C1} and C_{C2}, the charging current of the buffer to the MP can be effectively increased, and this response process of the above large signal can be shown in Fig. 5(b).

From the above-mentioned analysis, it can be seen that when the load current of the LDO changes, the buffer proposed in this article can instantly generate additional charging and discharging current, thereby increasing the SR of the output of the buffer without increasing the quiescent current, and enhancing the charging and discharging speed of the gate of power transistor, to improve the transient response of the LDO.

B. Small-Signal Analysis

When the circuit generates high-frequency signal disturbance, the ac coupling network formed by R_{C1} and C_{C1} couples the high-frequency signal to the gate of M12. In order to make the

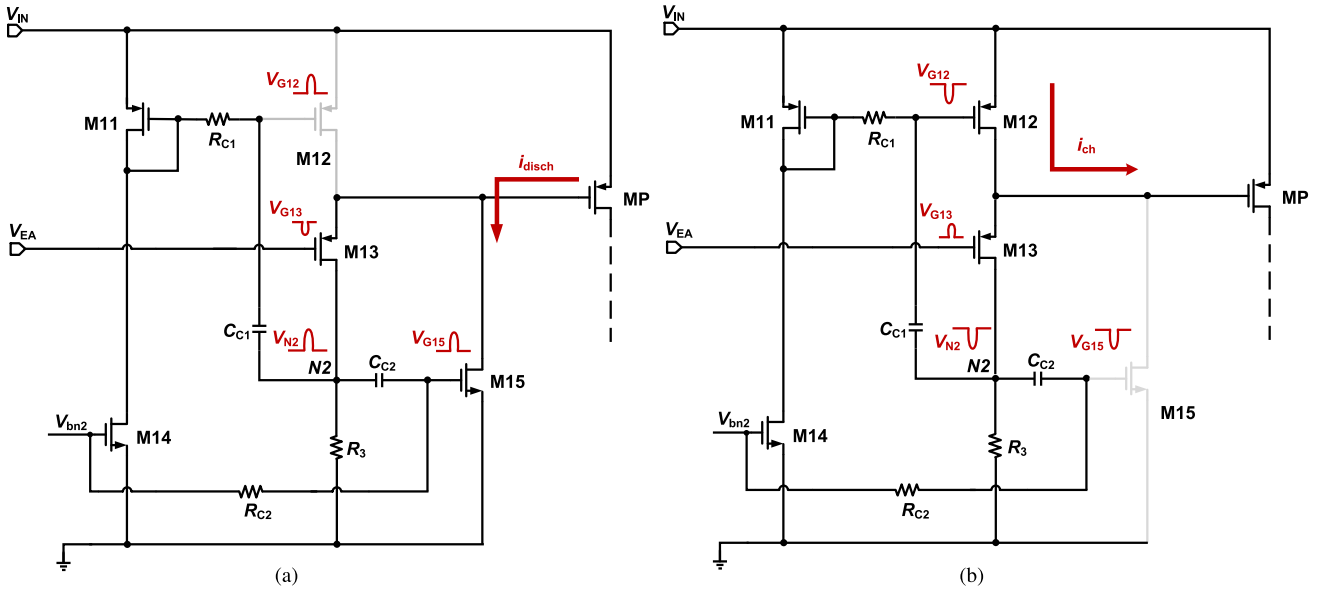


Fig. 5. Large signal response when (a) load current increases and (b) load current decreases.

coupling effect better, the value of R_{C1} will be set relatively large, which is equivalent to an open circuit. At this time, C_{C1} and C_{gs12} are connected in series, where C_{gs12} is the parasitic capacitance between the gate and source of M12. Therefore, the change in the voltage at the gate of M12 is approximately equal to the divided voltage obtained on C_{gs12}. At this time, M12 is not only a bias transistor that provides quiescent current, but also a feedback transistor that transmits high-frequency signals. Similarly, the ac coupling network formed by R_{C2} and C_{C2} will also couple high-frequency signals to the gate of M15. At this time, C_{C2} and C_{gs15} are connected in series, where C_{gs15} is the parasitic capacitance between the gate and source of M15. The change of the voltage at the gate of M15 is approximately equal to the partial voltage obtained on C_{gs15}. At this time, the M15 becomes a parallel feedback transistor. The two feedback loops formed by C_{C1} and C_{C2} can effectively reduce the equivalent output resistance at the output of the voltage buffer. In order to calculate the equivalent output resistance of the buffer, this article gives a small-signal equivalent circuit diagram of the LTE buffer, as shown in Fig. 6.

First, a test voltage V_{test} is added to the output of the buffer and a test current i_{test} will be generated at point N1. The equivalent output resistance can be obtained by dividing the test voltage V_{test} by the current i_{test}. The voltage change of the source of M13 is V_{test}, and the current change is $g_{m13}V_{\text{test}}$. The equivalent resistance R_{N2} of point N2 to ground should be given as follows:

$$R_{N2} = \left(\frac{1}{sC_{C1}} + \frac{1}{sC_{\text{gs12}}}\right) \| \left(\frac{1}{sC_{C2}} + \frac{1}{sC_{\text{gs15}}}\right) \| R_3 = \frac{R_3 s^2 C_A C_B}{s^2 C_A C_B + R_3(s^3 C_A C_{C2} C_{\text{gs15}} + s^3 C_B C_{C1} C_{\text{gs12}})} \tag{3}$$

where $C_A = C_{C1} + C_{\text{gs12}}$, $C_B = C_{C2} + C_{\text{gs15}}$, and the voltage change at point N2 can be obtained by multiplying the current

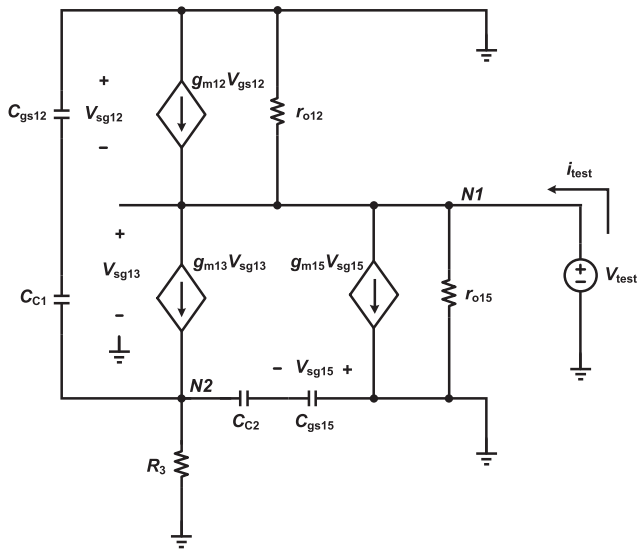


Fig. 6. Small-signal equivalent circuit of LTE buffer.

change $g_{m13}V_{\text{test}}$ with the resistance R_{N2}. The voltage at point N2 is coupled to the gates of M12 and M15 through C_{C1} and C_{C2}, and the voltage change at point N2 is coupled to the gate of M12 and M15, which can be measured by the coupling coefficients α and β, respectively, where

$$\alpha = \frac{C_{C1}}{C_{C1} + C_{\text{gs12}}} \tag{4}$$

$$\beta = \frac{C_{C2}}{C_{C2} + C_{\text{gs15}}}. \tag{5}$$

And the value of i_{test} is the sum of current changes of M12, M13, and M15. Therefore, the equivalent output impedance

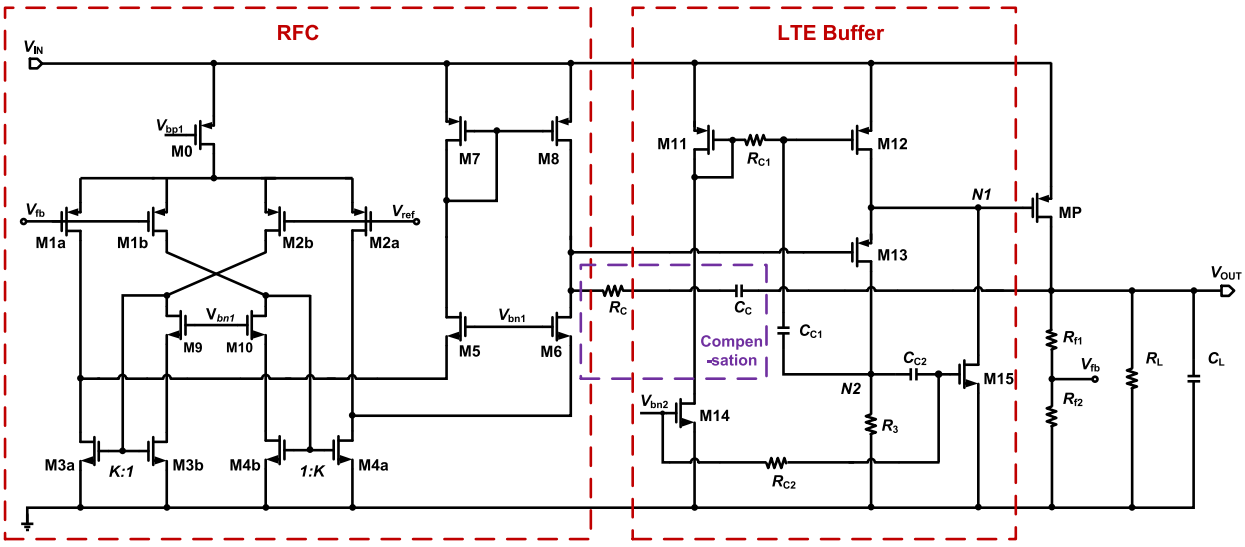


Fig. 7. Schematic of the proposed LTE LDO.

$R_{OB}(s)$ of the LTE buffer should be provided as follows:

$$R_{OB}(s) = \frac{1}{g_{m13}[1+\frac{R_3 s^2 C_A C_B(\alpha g_{m12}+\beta g_{m15})}{s^2 C_A C_B + R_3(s^3 C_A C_{C2} C_{gs15} + s^3 C_B C_{C1} C_{gs12})}]}$$

$$= \frac{1}{g_{m13}[1+R_3(\alpha g_{m12}+\beta g_{m15})]} \frac{1-s/Z_{OB}}{1-s/P_{OB}}. \quad (6)$$

In detail

$$Z_{OB} = \frac{1}{R_3(C_{gs12}+C_{gs15})} \quad (7)$$

$$P_{OB} = \frac{1+R_3(\alpha g_{m12}+\beta g_{m15})}{R_3(C_{gs12}+C_{gs15})}. \quad (8)$$

Because the value of R_3 in this design is relatively small, and C_{gs12} and C_{gs15} are also very small as parasitic capacitances, so both Z_0 and P_0 are at very high frequencies, so the value of the output resistance can be approximately provided as

$$R_{OB} \approx \frac{1}{g_{m13}[1+R_3(\alpha g_{m12}+\beta g_{m15}]}. \quad (9)$$

It can be seen from the above-mentioned equations that the output impedance of the buffer has been significantly attenuated by adding the coupling network composed of R_{C1} and C_{C1} and R_{C2} and C_{C2}. The impedance attenuation factor introduced by LTE buffer is $R_3(\alpha g_{m12}+\beta g_{m15})$. Compared with the buffer proposed in [18], as shown in the previous formula (2), the LTE Buffer proposed in this article can reduce the output impedance more effectively. Nevertheless, it can be obtained from (9) that large transistors M12 and M15 sizes and resistance R_3 effectively reduce the buffer output impedance, and yet according to (7) this cause the Z_{OB} move to the low frequency, resulting in deteriorating loop stability.

Comprehensive analysis shows that the LTE buffer proposed in this article can increase the SR at the output of the buffer during load switching transients, and more effectively reduce the output impedance while maintaining a low-quiescent current within the full-load range. Therefore, compared with the traditional buffers, the buffer proposed in this article achieves a better performance.

III. Proposed LTE-LDO

The proposed LTE-LDO based on the LTE buffer in this article is shown in Fig. 7, where M0–M10 constitute the error amplifier, M11–M15 and R_{C1}, C_{C1}, R_{C2}, and C_{C2} constitute the LTE buffer proposed in this design, and MP constitutes the power stage, R_{f1} and R_{f2} form a feedback network, R_C and C_C form a compensation network, and R_L and C_L are LDO loads.

A. RFC Amplifier

This design uses RFC amplifier as the error amplifier, which can reduce the current consumption to half of the traditional folded cascade (FC) amplifier under the condition of reaching the same loop bandwidth, so that the LDO of this design has higher current efficiency. The schematic of the RFC amplifier is shown in the Fig. 8 [27]. Specifically, M1b, M2b, M3a, M3b, M4a, M4b, M11, M12 together constitute a current recycling path (Recycling Current Path, RCP). With the addition of RCP, the bias current transistor that originally did not transmit small ac signals in the FC is transformed into a signal path for transmitting small ac signals, achieving higher transconductance, loop gain, and SR. At the same time, for frequency compensation, the two cascode transistors of the amplifier output stage are removed in this design to reduce the output impedance of the amplifier.

B. Stability Analysis

This design mainly uses the transfer function H(s) for stability analysis. In order to calculate the transfer function, this article gives the small-signal flow chart of LTE LDO, as shown in Fig. 9. Since the poles contained within the error amplifier are located at very high frequencies, these poles are not taken into consideration in the analysis. Based on the above-mentioned conditions, the first-stage error amplifier can be directly equivalent to a

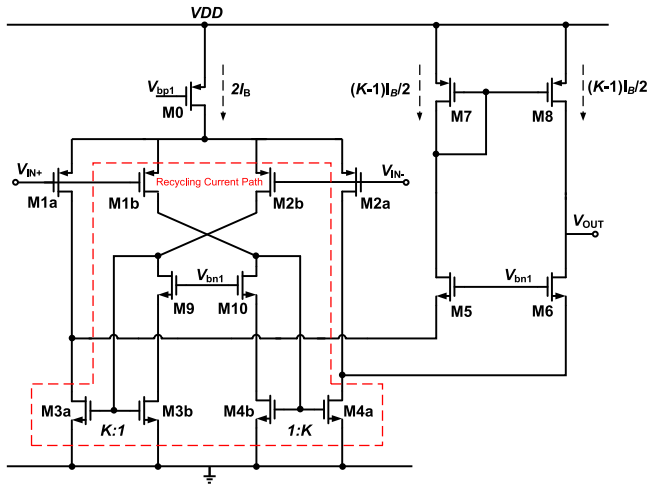


Fig. 8. Schematic of RFC amplifier.

gain stage, and its transconductance is g_{mEA}; the equivalent transconductance of the power transistor is represented by g_{mp}; R_1 and C_1 represent the equivalent output resistance of the error amplifier and the equivalent input capacitance of the LTE Buffer; R_{oeq} and C_L, respectively, represent the equivalent output resistance and load capacitance of the LTE-LDO; B represents the feedback coefficient of the feedback network, and $\mathrm{B} = R_{f1}/(R_{f1} + R_{f2})$.

When calculating system functions, some preconditions need to be clarified:

1) the value of load capacitance C_L and compensation capacitance C_C is much larger than C_1;
2) the equivalent output resistance R_1 of the error amplifier is much larger than the value of the nulling resistor R_C;
3) the value of the nulling resistor R_C is greater than the maximum value of $1/g_{mp}$.

Based on the above-mentioned conditions, the system function can be expressed as

$$H(s) = \frac{-Bg_{\mathrm{mEA}}R_1R_{oeq}g_{mp}[1 + C_C(R_C - \frac{1}{g_{\mathrm{mp}}})s]}{1 + as + bs^2 + cs^3} \tag{10}$$

$$a = R_{oeq}(C_L + g_{\mathrm{mp}}R_1C_C) \tag{11}$$

$$b = R_1R_{\mathrm{oeq}}C_CC_L \tag{12}$$

$$c = R_1R_{\mathrm{oeq}}R_CC_1C_CC_L. \tag{13}$$

It can be seen from the expression of the system function that H(s) has a left plane zero Z_0 and three poles P_0, P_1, P_2. During the change of the LTE-LDO load current, the values of R_{oeq} and g_{mp} are also constantly changing, so the positions of the poles are constantly changing. Therefore, it should be discussed separately, and stability analysis should be carried out under different load current conditions.

1) Light Load Conditions: When the load current is 0, g_{mp} is very small, but the value of R_{oeq} is very large. At this time, there is $R_{\mathrm{oeq}}C_L \gg g_{\mathrm{mp}}R_1R_{\mathrm{oeq}}C_C$, so the value of a is approximately $R_{\mathrm{oeq}}C_L$. At this time, the transfer function *H(s)* should be as follows:

$$\begin{aligned} H(s)|_{I_L=0} &\approx \frac{-Bg_{mEA}R_1R_{\mathrm{oeq}}g_{\mathrm{mp}}[1 + C_C(R_C - \frac{1}{g_{\mathrm{mp}}})s]}{1 + sR_{\mathrm{oeq}}C_L + s^2R_1R_{\mathrm{oeq}}C_CC_L + s^3R_1R_{\mathrm{oeq}}R_CC_1C_CC_L} \\ &\approx \frac{-Bg_{\mathrm{mEA}}R_1R_{\mathrm{oeq}}g_{\mathrm{mp}}[1 + C_C(R_C - \frac{1}{g_{\mathrm{mp}}})s]}{(1 + sR_{\mathrm{oeq}}C_L)(1 + sR_1C_C)(1 + sR_CC_C)}. \end{aligned} \tag{14}$$

At this time, the expressions of P_0, P_1, P_2, Z_0 and the loop bandwidth $\mathrm{GBW_{LTE}}$ are

$$P_0 = -\frac{1}{R_{\mathrm{oeq}}C_L} \tag{15}$$

$$P_1 = -\frac{1}{R_1C_C} \tag{16}$$

$$P_2 = -\frac{1}{R_CC_C} \tag{17}$$

$$Z_0 = -\frac{1}{C_C(R_C - \frac{1}{g_{\mathrm{mp}}})} \tag{18}$$

$$\mathrm{GBW_{LTE}} \approx \frac{Bg_{mEA}R_1g_{mp}}{C_L}. \tag{19}$$

Since C_L is much larger than $Bg_{mEA}R_1g_{\mathrm{mp}}R_1C_C$, it is easy to ensure that the position of P_1 is much higher than the unity gain bandwidth of the system. When the load current is equal to zero, the entire LDO can easily obtain good phase margin. In addition, the value of g_{mp} is relatively small at this time, so the position of the zero on the left plane is relatively high.

2) Heavy Load Conditions: When the load current is very large, g_{mp} is very large, and the value of R_{oeq} is very small. At this time, there is $g_{\mathrm{mp}}R_1R_{\mathrm{oeq}}C_C \gg R_{\mathrm{oeq}}C_L$. Therefore, the value of a is approximately $g_{\mathrm{mp}}R_1R_{\mathrm{oeq}}C_C$, and the transfer function H(s) at this time can be provided in (20) shown at the bottom of the next page.

At this time, the expressions of P_0, P_1, P_2, Z_0 and the loop bandwidth $\mathrm{GBW_{LTE}}$ are

$$P_0 = -\frac{1}{g_{\mathrm{mp}}R_1R_{\mathrm{oeq}}C_C} \tag{21}$$

$$P_1 = -\frac{g_{\mathrm{mp}}}{C_L} \tag{22}$$

$$P_2 = -\frac{1}{R_CC_1} \tag{23}$$

$$Z_0 = -\frac{1}{C_C(R_C - \frac{1}{g_{\mathrm{mp}}})}. \tag{24}$$

Since g_{mp} is very large at this time, P_1 is located at a very high frequency. Therefore, when the load current is very large, there is only one pole within the GBW of the LDO, which can ensure the stability of the system. As the load current continues to increase, the position of P_1 is getting higher and higher, and the position of Z_0 is getting lower and lower, so PM will become larger and larger, and the system will become more stable.

3) Moderate Load Conditions: When the load current is at a medium level, the values of $R_{\mathrm{oeq}}C_L$ and $g_{\mathrm{mp}}R_1R_{\mathrm{oeq}}C_C$ cannot

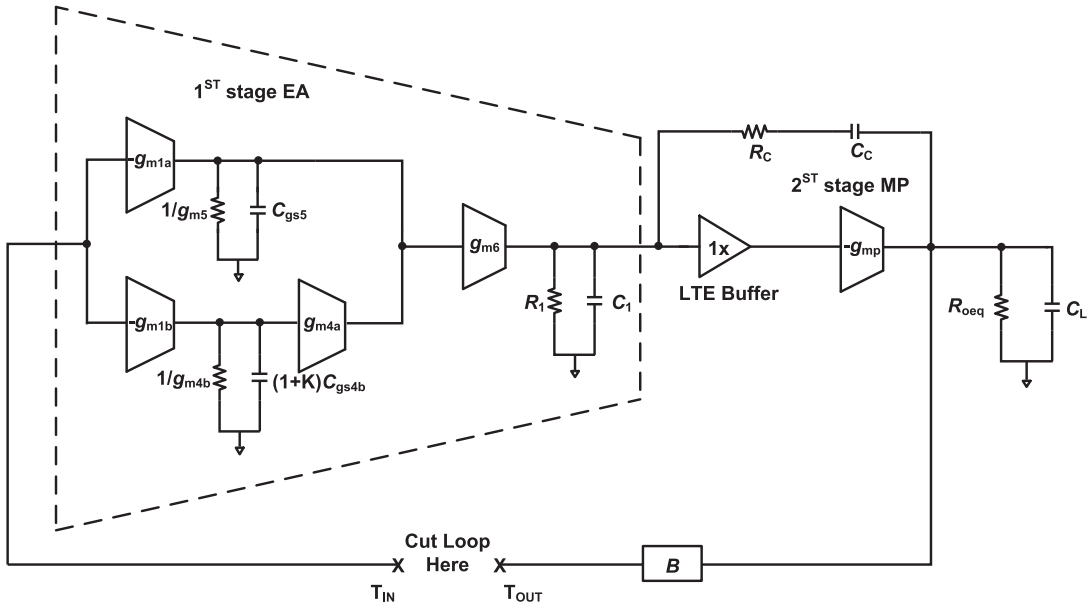


Fig. 9. Small-signal block diagram of the proposed LDO.

be distinguished, so the value of a is $R_{\text{oeq}}(C_L + g_{\text{mp}}R_1C_C)$, and the transfer function H(s) at this time can be shown in (25), shown at the bottom of this page.

At this time, the expressions of P_0, P_1, P_2, Z_0 and the loop bandwidth GBW_{LTE} are

$$P_0 = -\frac{1}{R_{\text{oeq}}(C_L + g_{\text{mp}}R_1C_C)} \tag{26}$$

$$P_1 = -\frac{C_L + g_{\text{mp}}R_1C_C}{R_1C_CC_L} \tag{27}$$

$$P_2 = -\frac{1}{R_CC_1} \tag{28}$$

$$Z_0 = -\frac{1}{C_C(R_C - \frac{1}{g_{\text{mp}}})} \tag{29}$$

$$\text{GBW}_{\text{LTE}} \approx \frac{Bg_{\text{mEA}}R_1g_{\text{mp}}}{C_L + g_{\text{mp}}R_1C_C}. \tag{30}$$

In this case, the PM of the system will be the worst. Therefore, the parameters of the compensation network can be designed according to the worst PM, so that the smallest PM meets the stable conditions to ensure that the system can work normally under various load currents. The expression of PM is provided in the following equation:

$$\begin{aligned}\text{PM} &= 90^\circ - \tan^{-1}\frac{\text{GBW}_{\text{LTE}}}{P_1} + \tan^{-1}\frac{\text{GBW}_{\text{LTE}}}{Z_0} \\ &= 90^\circ - \tan^{-1}\frac{Bg_{\text{mEA}}g_{\text{mp}}C_CC_LR_1^2}{(C_L + g_{\text{mp}}R_1C_C)^2} \\ &\quad - \tan^{-1}\frac{Bg_{\text{mEA}}R_1g_{\text{mp}}C_C(R_C - \frac{1}{g_{\text{mp}}})}{(C_L + g_{\text{mp}}R_1C_C)}.\end{aligned} \tag{31}$$

In order to make the expression of PM more concise, two variables FM_1 and FM_2 are introduced here to assist the analysis, where FM_1 and FM_2 are, respectively

$$\text{FM}_1 = \frac{Bg_{\text{mEA}}g_{\text{mp}}C_CC_LR_1^2}{(C_L + g_{\text{mp}}R_1C_C)^2} \tag{32}$$

$$\text{FM}_2 = \frac{Bg_{\text{mEA}}R_1g_{\text{mp}}C_C(R_C - \frac{1}{g_{\text{mp}}})}{(C_L + g_{\text{mp}}R_1C_C)}. \tag{33}$$

$$\begin{aligned}H(s)|_{I\gg 0} &\approx \frac{-Bg_{\text{mEA}}R_1R_{\text{oeq}}g_{\text{mp}}[1 + C_C(R_C - \frac{1}{g_{\text{mp}}})s]}{1 + sg_{\text{mp}}R_1R_{\text{oeq}}C_C + s^2R_1R_{\text{oeq}}C_CC_L + s^3R_1R_{\text{oeq}}R_CC_1C_CC_L} \\ &\approx \frac{-Bg_{\text{mEA}}R_1R_{\text{oeq}}g_{\text{mp}}[1 + C_C(R_C - \frac{1}{g_{\text{mp}}})s]}{(1 + sg_{\text{mp}}R_1R_{\text{oeq}}C_c)(1 + s\frac{C_L}{g_{\text{mp}}})(1 + sR_CC_1)}\end{aligned} \tag{20}$$

$$H(s) \approx \frac{-Bg_{\text{mEA}}R_1R_{\text{oeq}}g_{\text{mp}}[1 + C_C(R_C - \frac{1}{g_{\text{mp}}})s]}{1 + sR_{\text{oeq}}(C_L + g_{\text{mp}}R_1C_C) + s^2R_1R_{\text{oeq}}C_CC_L + s^3R_1R_{\text{oeq}}R_CC_1C_CC_L} \tag{25}$$

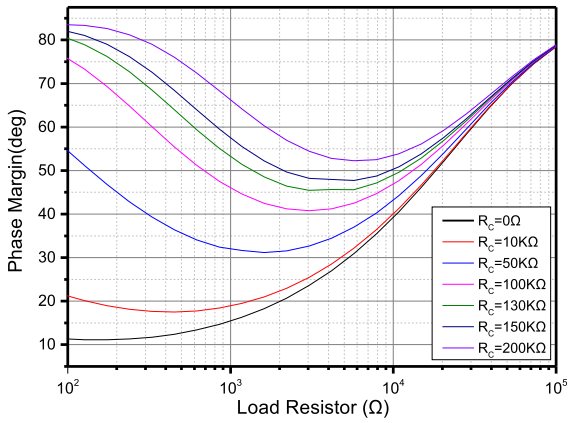


Fig. 10. Changes of PM with load under different R_C conditions.

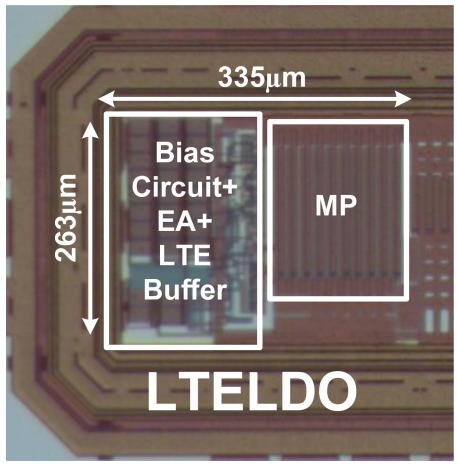


Fig. 11. Layout and photomicrograph of LTE-LDO.

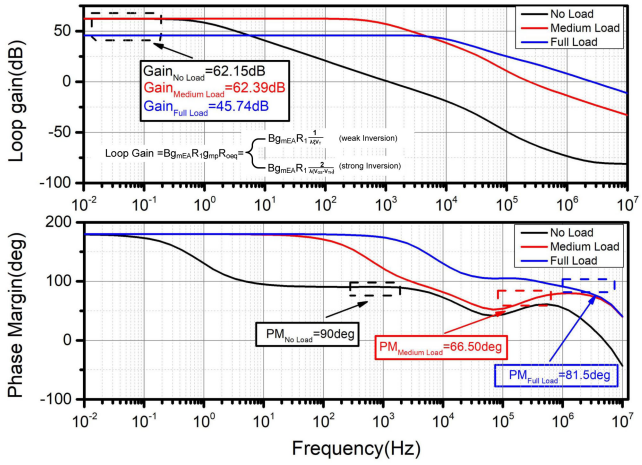


Fig. 12. Simulation of the ac response of LTE-LDO.

Therefore, PM can also be written as

$$\mathrm{PM} = 90^\circ - \tan^{-1}\mathrm{FM}_1 + \tan^{-1}\mathrm{FM}_2. \tag{34}$$

The derivation operation of the above-mentioned formula shows that PM has a minimum value, and the value of the minimum value has a great correlation with the value of R_C. The larger the value of R_C, the larger the value of the minimum value. Fig. 10 verifies the above-mentioned analysis in the form of simulation and gives the change of PM with load under different R_C conditions.

According to the simulation results, the change of PM conforms to the above-mentioned analysis. As the load resistance increases, PM first decreases and then increases, and there is a minimum value. When the load current is very small, that is, the load resistance is very large, the system is very stable, and as the load current continues to decrease, the value of PM will get closer and closer to 90°; when the load current is very large, that is, the load resistance is very small, PM will increase as the load resistance decreases, and the system will become more and more stable. When the load current is at a medium level, PM has the worst condition. The minimum value of PM is related to R_C. Increasing R_C can effectively increase the PM of the system.

IV. Simulation and Experimental Results

The proposed LDO is implemented in a 0.18 μm complementary metal–oxide–semiconductor technology. The input voltage range is 1.8–2.2 V and the output voltage is 1.6 V. The maximum load current is 200 mA and the output is connected to a 1 μF capacitor. The die photo of LTE-LDO is shown in Fig. 11 and the chip area excluding pads is 0.088 mm^2.

Fig. 12 shows the simulation of the ac response of LTE-LDO under no-load, medium-load, and full-load conditions. From the results, the PM of LTE-LDO first decreases and then increases as the load current increases, which is consistent with the theoretical analysis. The PM of the system can satisfy the requirements of stability under no-load, medium-load, and full-load conditions.

Fig. 13 shows the measured line regulation of LTE-LDO under the conditions of load current of 0, 1, and 200 mA. The line regulation of LTE-LDO is 0.725 mV/V and 2.025 mV/V at no-load and full load, respectively, when the input voltage varies from 1.8 to 2.2 V. The output voltage changes by 0.3 mV when the load current is 1 mA, so the line regulation is 0.75 mV/V.

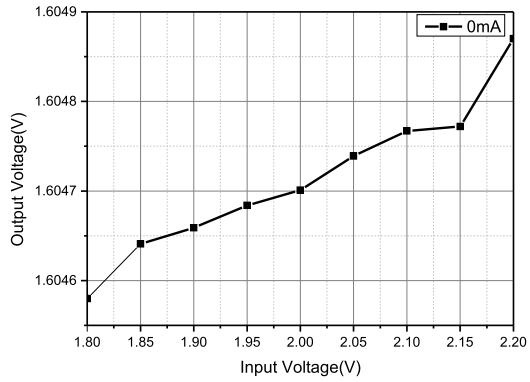
The measured load regulation of LTE-LDO is shown as Fig. 14. The output voltage changes by 42.26 mV when the load current changes in the range of 0–200 mA. Therefore, the load regulation of LTE-LDO is 0.211 mV/mA.

Fig. 15 shows the measured load transient response of LTE-LDO for a load varying from 0 to 200 mA with edge time of 100 ns. The maximum change in output voltage is 76 mV.

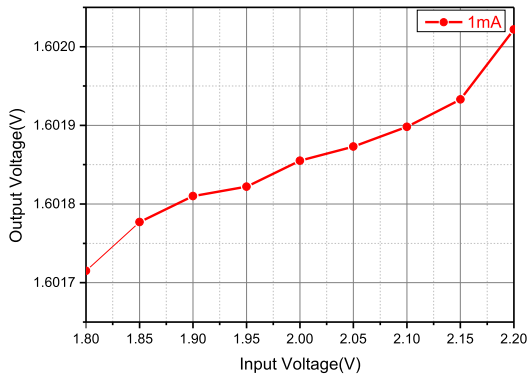
Fig. 16 shows the measured line transient response of LTE-LDO. The overshoot and undershoot at the output are 25.3 mV and 23.4 mV, respectively, when the input voltage changes 0.2 V/100 ns.

Fig. 17 shows the measured PSR of LTELDO at 2 kHz under no-load conditions. It can be calculated that the PSR is -58.72 dB.

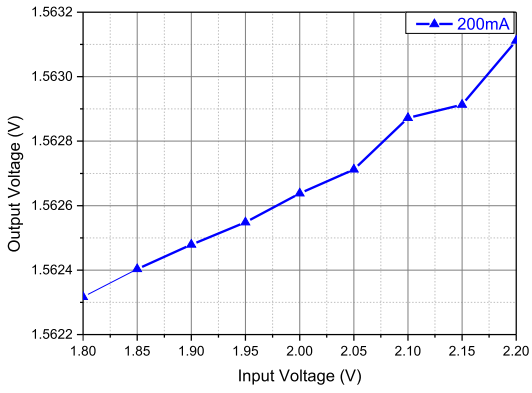
The trend of PSR with frequency can be plotted through measuring PSR at multiple frequencies. Figs. 18 and 19 show the comparison simulation and measurement of PSR under



(a)



(b)



(c)

Fig. 13. Measured line regulation of LTE-LDO at different load currents. (a) Load current = 0 mA. (b) Load current = 1 mA. (c) Load current = 200 mA.

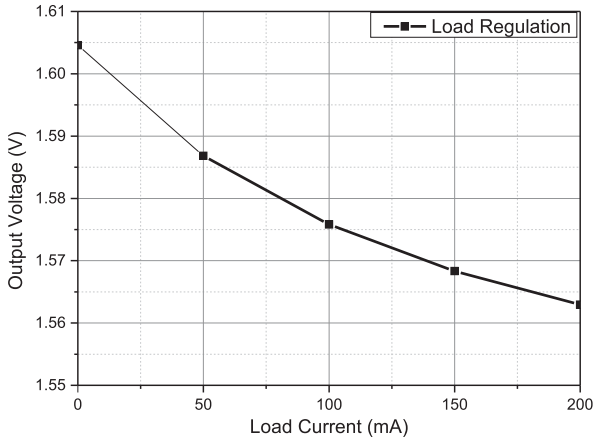


Fig. 14. Measured load regulation of LTE-LDO .

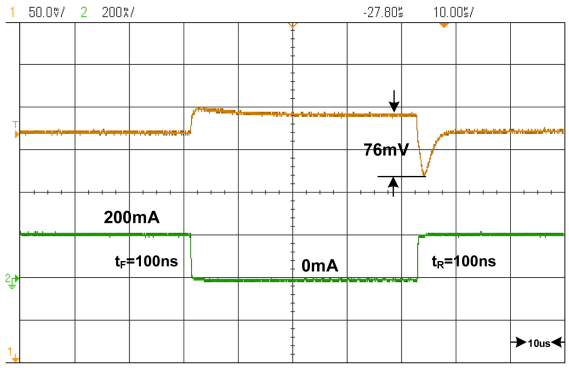


Fig. 15. Measured load transient response of LTE-LDO for a load varying from 0 to 200 mA with edge time of 100 ns.

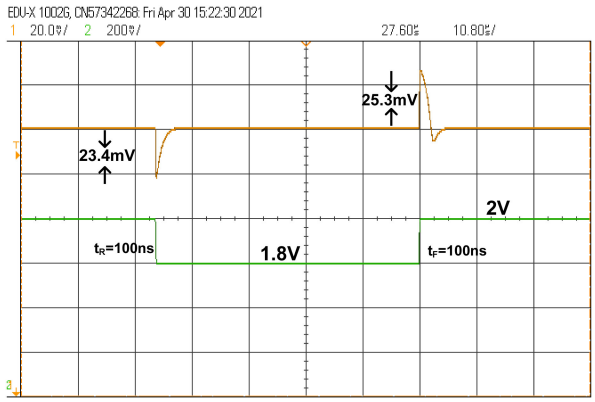


Fig. 16. Measured line transient response of LTE-LDO.

no-load conditions and full load conditions, respectively. It can be obtained from the comparison that the variation trend of the PSR measurement and simulation with the frequency are the same. Table I provides the performance comparison with many previously proposed paper. The current efficiency and other performance must be taken into account to comprehensively describe the performance indicators of all aspects of the LDO. Figure of merit (FoM) can be introduced to reflect the overall performance of the LDO. The formula of FoM is given as

$$FoM = \frac{C_L \Delta V_{o,pp} * I_{Q,ave}}{\Delta I_{load}^2, max} \tag{35}$$

where C_L is the load capacitance and $\Delta V_{o,\mathrm{pp}}$ is the peak-to-peak load transient variation at the maximum load step current $\Delta I_{\mathrm{load,max}}$. The quiescent current increases as the load current increases due to the adaptive-bias technique is adopted in many comparative papers, so there is a range of the quiescent current. In this case, the average value of the quiescent current $I_{Q,\mathrm{ave}}$ is taken into the calculation of FoM to ensure fairness.

The small FoM value proves the high efficiency and excellent performance of the LDO. It can be concluded from

TABLE I
PERFORMANCE COMPARISON WITH PREVIOUS REPORTED LDO

Parameter	[20]	[23]	[25]	[24]	[18]	[26]	This study
Year	2017	2010	2017	2018	2007	2020	2021
Technology	0.13μm	0.35μm	0.18μm	0.25μm	0.35μm	0.18μm	0.18μm
Power transistor type	NMOS	PMOS	PMOS	NMOS	PMOS	PMOS	PMOS
Input Voltage(V)	1.05-2	2	1.4-1.8	1.5-3.3	2.5-5.5	1.4-1.8	1.8-2.2
Dropout Voltage(mV)	29.7	200	200	240	200	200	200
Output Capacitance $C_L(\mu F)$	1	1-10	1	1-47	1	4.7	1
Quiescent Current $I_Q(\mu A)$	14-120	4	1.6-200	1.24-100	20-340	13.5	48
Maximum Load Current(mA)	300	100	50	150	200	150	200
Load Regulation(μV/mA)	6	-	100	-	170	75	211
Line Regulation(mV/V)	0.44	-	5.5	-	2	7.785	2.025
PSR(dB)	-50	-	<-30	>-22	>-45	-30	-79.13
@(Hz)	10K	-	10M	20K	20K	100	100K
$\Delta V_{o,pp}(mV)$	80	55	29	225	54	37	76
Current Efficiency(%)	99.96	99.996	99.6	99.93	99.8	99.991	99.976
Edge Time(ns)	1000	50	10	10	100	500	100
ESR	yes	yes	no	no	no	yes	no
FoM(ps)	59.56	22	1169.28	506.2	243	101.52	91.2

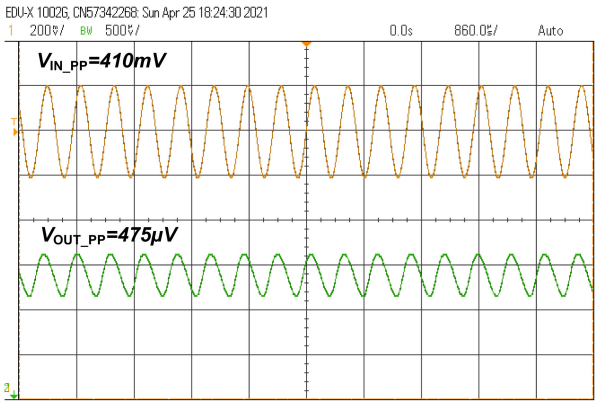


Fig. 17. Measured PSR of LTE-LDO at 2 kHz.

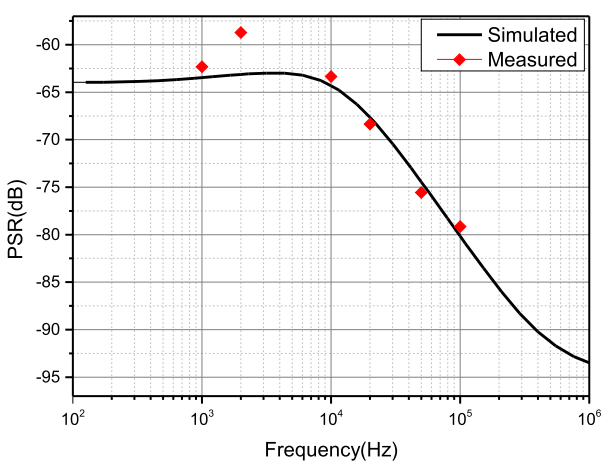


Fig. 18. Comparison simulation and measurement of PSR under no-load conditions ($C_L = 1\ \mu$F and load current = 0 mA).

Table I that most of the previous work needs to increase the quiescent current under heavy load conditions to ensure the loop stability or improve the transient response. However, the

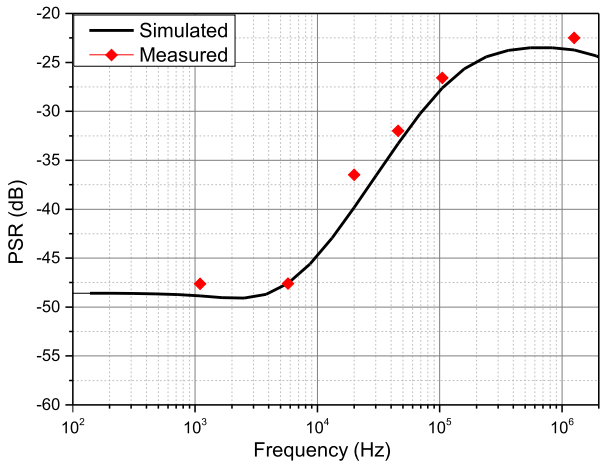


Fig. 19. Comparison simulation and measurement of PSR under full-load conditions ($C_L = 1\ \mu$F and load current = 200 mA).

LTE-LDO proposed in this article can guarantee a low-quiescent current consumption of 48 μA over the entire load current range. Except [23] and [20], the FoM of LTE-LDO is the smallest, which can prove that the LTE-LDO proposed in this article exhibits an excellent performance. An external ESR is required to ensure the stability although [23] and [20] has higher efficiency than LTE-LDO, which increases the cost and complexity of the circuit. The LTE buffer can achieve a very low output resistance while maintaining a low-quiescent current, thereby pushing the pole at the gate of the power transistor to a very high frequency and improving the PM of the system. Moreover, the current-recycling structure is employed in the error amplifier of LTE-LDO, which reduces current consumption while ensuring sufficient bandwidth. Thus, the loop stability of LTE-LDO can be guaranteed without an external ESR. The combination of LTE buffer and current-recycling amplifier realizes the small FoM value of LTE-LDO.

V. Conclusion

In this article, a LDO based on the proposed LTE Buffer with current-shunt feedback and two ac coupling networks has been presented. The LTE-LDO achieves the high-current efficiency and transient enhancement due to the dynamic bias technique and low-output impedance of the LTE buffer. In addition, simple Miller compensation with a nulling resistor is employed for frequency compensation and a complete small-signal analysis under different load current conditions is given in this article. The experimental results and the small FoM in Table I verifies its comprehensive performance and reliability.

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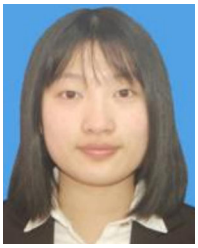

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