# ZVS-Interleaved Synchronous Buck DC–DC Converter With a Coupled Inductor by Varying Switching Frequency and Deadtime

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***Abstract*—This article proposes a fully digital variable switching frequency and deadtime control method for a synchronous rectifier buck dc–dc converter with an inverse coupled inductor. It does not need auxiliary circuits, zero-crossing detection (ZCD), or high-bandwidth sensors. Even in facing the polyline shape of the current in inductors due to the coupling effect, zero-voltage switching (ZVS) can be achieved with the proposed varying switching frequency control to make the turn OFF current be constant. Based on ZVS achievement of the power switches, the deadtime is variable to reduce the conduction loss over body diodes further. The modes and resonant process are analyzed in detail. A 1-kW experimental prototype was built to verify the effectiveness of the proposed control method. The peak efficiency is over 99% in the experimental test.**

***Index Terms*—Inverse coupled inductor, variable deadtime, variable switching frequency, zero-voltage switching (ZVS).**

## I. Introduction

In RECENT years, because of galvanic isolation, soft switching, and high efficiency, the *LLC* resonant converter has been widely used as a dc–dc transformer (DCX) in industrial applications, such as distributed power systems [1], data centers [2], and dc electronic loads [3]. However, it is not suitable for applications with a wide voltage gain range because the gain of DCX is fixed. The sigma structure has been studied to broaden the gain range while retaining the advantages of *LLC*-DCX. It is a quasi-parallel structure composed of *LLC*-DCX converters and dc–dc converters (D2D), such as buck converters [4], [5]. High conversion efficiency and power density can be achieved by this structure, but it is nonisolated and the soft switching of the buck converter is not easy to achieve. In [6], the nonisolated topology in the sigma structure is replaced by a dual active bridge (DAB) converter to realize soft switching and power direction control. However, this converter contains 16 active switches and two transformers. This causes higher cost and more conduction losses. Consequently, two-stage converters are also good choices, in which *LLC*-DCX is used as the isolated stage and a nonisolated converter is used to regulate the output voltage. The synchronous rectification buck converter is commonly used because of its high efficiency and simple structure [7]–[9]. To increase the power density of the converter, high frequency has become a trend because it can reduce the size of the filter capacitor and magnetic components. However, a hard-switching nonisolated converter suffers from a severe reverse-recovery problem caused by the body diode of the switching devices. Increasing the switching frequency leads to higher switching losses and more serious electromagnetic interference. Since previous work mainly focused on the optimization of DCX, the objective of this article is to realize fully soft switching for the second-stage converter to improve the overall conversion efficiency.

Various zero-voltage switching (ZVS) techniques have been developed to solve these problems. One conventional way is to assist the realization of soft switching by adding auxiliary circuits, which can be roughly classified as active-clamping converters [10], [11], zero-voltage-transition converters [12]–[14], and magnetically coupled ZVS converters [15]–[17]. However, the power density and efficiency are limited by the added passive components, switches, and magnetic components. In addition, the reliability of the converter will be reduced because of the complexity of the power circuit and control strategy.

Increasing inductor current ripple is a commonly used method to achieve ZVS without using auxiliary circuits. Its mechanism is to charge and discharge the output capacitors of the switches by changing the direction of the inductor current before commutation. The switching frequency is usually used as a control degree of freedom to increase the inductor current ripple. This method is widely adopted, as in buck–boost converters [18], [19], cascaded dc–dc converters [20], and three-phase inverters [21], [22]. Critical conduction mode (CRM) can be realized with the inductor current zero-crossing detection (ZCD) and a constant deadtime of half a resonant cycle [23], [24]. A CRM technique is an effective way to achieve ZVS and limits unnecessary inductor current ripple. However, the ZVS range depends on the voltage conversion gain and the power flow direction. Since the ZCD circuit is very sensitive to noises, the method of voltage control loop output determining the turn-ON time of the main switch has been successfully implemented without ZCD at all. Thus, the control is robust to noises and the cost is low [9], but there is no inner current tracking loop. Besides, nonlinear inductor [25] and variable coupling coefficient [26]

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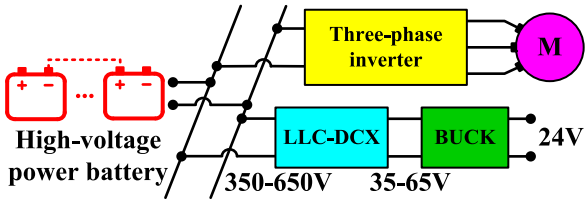


Fig. 1. Application scenario of the proposed converter.

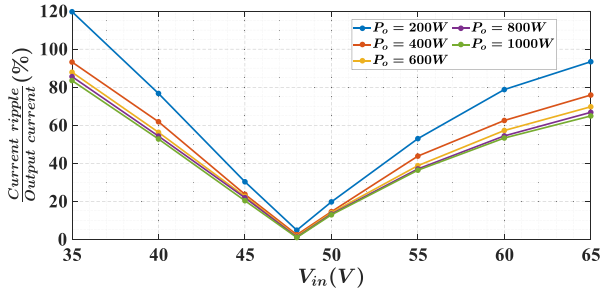


Fig. 2. Current ripple percentage among different output powers at different input voltages.

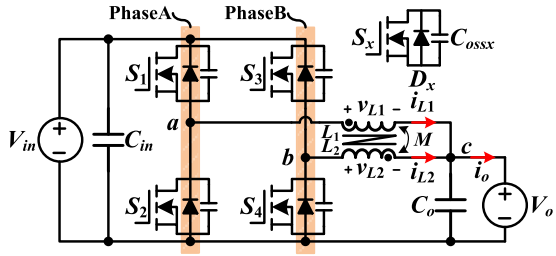


Fig. 3. Interleaved synchronous buck converter with coupled inductor.

ZVS technologies are proposed to optimize the performance of the converter, which increases the cost and complicates the design of magnetic components.

When ZVS is achieved by the current ripple, the peak value of the inductor current is at least twice the average value. Therefore, the interleaved parallel connection is necessary to cancel the current ripple and this leads to a smaller filter capacitor size while the capacity of the converter has been expanded [27], [28]. The power density of interleaved converters can be further improved by coupled inductors because two separate inductors are integrated into one core. In addition, the coupled inductor contributes to the reduction of the volume of the magnetic components [29] and the improvement of the conversion efficiency [30] and dynamic response [31]. Most papers focus on the characteristics of converters with coupled inductors but interleaved SR buck converters using variable switching frequency control with coupled inductors can further improve power density and conversion efficiency.

For interleaved synchronous rectifier (SR) buck with coupled inductors, implementation of soft switching is a challenge because the inductor current of each phase is affected by the state of the other phase due to the coupling. Thus, the current in each inductor is polyline shape instead of the straight line shape. The major contribution of this article is to propose a digital variable switching frequency modulation to deal with this issue. The ZVS range is extended by controlling the constant turn-OFF current. The deadtime is designed to be variable and to reduce conduction loss. In addition, the converter becomes more cost-effective and more reliable because no additional auxiliary circuits, ZCD circuits, and high-bandwidth sensors are needed. Furthermore, the proposed modulation is flexible and easy to be implemented by adding simple digital calculations to traditional fixed switching frequency control.

In this article, the proposed converter is used to provide auxiliary power for image processing, telecommunications, servo systems, and control systems of battery-driven electric vehicles. The system structure is shown in Fig. 1. The two-stage structure converter needs to adapt to the wide input voltage (350–650 V) caused by the load change of the high-voltage power battery. The current ripple percentage among different output powers at different input voltages obtained by simulation is shown in Fig. 2. The more the duty cycle deviates from 0.5, the larger the current ripple. Considering that the small current ripple will reduce the size of the filter capacitor, the *LLC*-DCX is used to step down the battery voltage to 35–65 V.

The rest of this article is organized as follows. The operation principle and operating modes of the proposed topology are explained in Section II. In Section III, the ZVS resonant process, variable switching frequency modulation, and the closed-loop control strategy are given. The experimental verification is provided in Section IV. Section V discusses and compares different ZVS methods. Finally, Section VI concludes this article.

## II. Converter Topology and Mode Analysis

### A. Interleaved Synchronous Buck Converter With a Coupled Inductor

The topology of the interleaved synchronous buck converter with a coupled inductor is shown in Fig. 3. $L_1$ and $L_2$ are the self-inductances of the two inductors and $M$ is the mutual inductance. Two windings with the same turns and wires in the coupled inductor are wound on an EI core so $L_1 = L_2 = L$. The coupling coefficient is defined as $\alpha = M/L$, where $\alpha$ is positive for direct coupling and negative for inverse coupling. Compared with a directly coupled inductor, an inversely coupled inductor has a smaller steady-state current ripple and lower magnetic flux ripple, so an inversely coupled inductor is adopted. $v_{L1}$ and $v_{L2}$ are the voltages applied to the two windings. $i_{L1}$ and $i_{L2}$ are the two inductor currents. Their relationship is given by

$$\begin{cases} v_{L1}(t) = L\frac{di_{L1}(t)}{dt} + M\frac{di_{L2}(t)}{dt} \\ v_{L2}(t) = L\frac{di_{L2}(t)}{dt} + M\frac{di_{L1}(t)}{dt}. \end{cases} \tag{1}$$

Combining the two equations in (1) yields the following:

$$v_{L1}(t) - \alpha v_{L2}(t) = (1-\alpha^2)L\frac{di_{L1}(t)}{dt} \tag{2}$$

where $C_{\text{in}}$ and $C_o$ are the high-frequency filter capacitors on the input side and output side, respectively. Small size $C_o$ is required because the output current ripple is significantly reduced by the interleaving of phase A and phase B. $D_x$ is the body diode of $S_x(x = 1,2,3,4)$, and $C_{\text{oss}x}$ is the output capacitance of $S_x$.

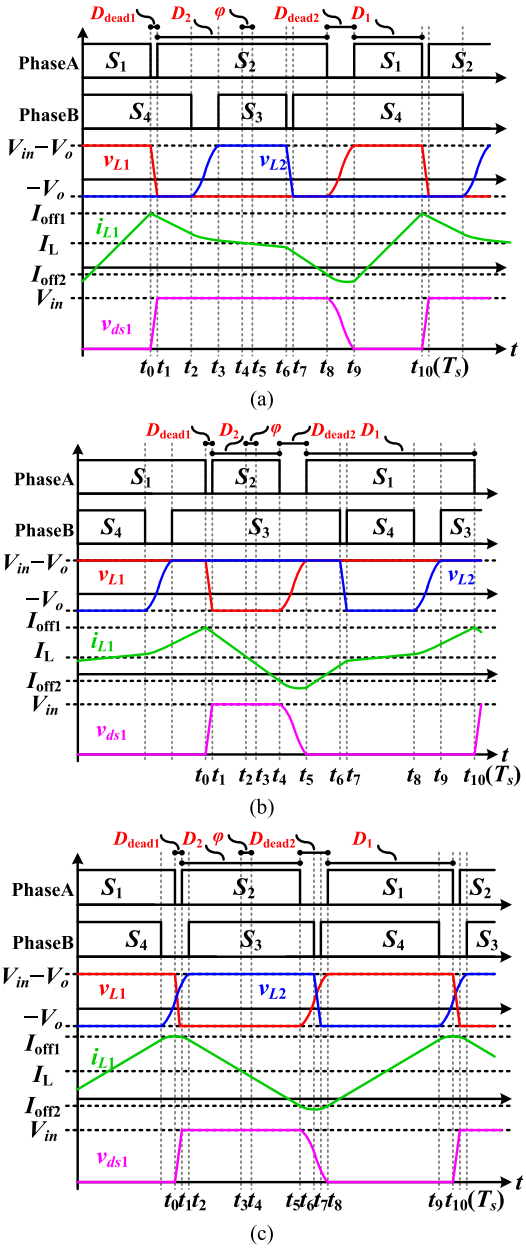


Fig. 4. Typical waveforms considering the resonant process and gate signals of the switches. (a) Mode 1. (b) Mode 2. (c) Mode 3.

### B. Mode Analysis

As shown in Fig. 4, three operating modes can be distinguished because of the unequal deadtime. $D_1$ is the duty cycle of $S_1$ and $S_3$, and $D_2$ is the duty cycle of $S_2$ and $S_4$. The deadtime values are normalized by the switching period $T_s$. $D_{\rm dead1}$ and $D_{\rm dead2}$ are defined according to deadtime $t_{\rm dead1}$ and $t_{\rm dead2}$, respectively. $S_1$ and $S_2$ are 180° phase shifted with $S_3$ and $S_4$, respectively. There is a phase shift $\varphi$ between the centers of gating signals $S_2$ and $S_3$, i.e., $\varphi = (D_{\rm dead2}-D_{\rm dead1})/2$. $I_{\rm OFF1}$ and $I_{\rm OFF2}$ correspond to the inductor current at the turn-OFF instant of $S_1$ and $S_2$, respectively. The boundaries of each mode are specified in Table I. It should be noted out that mode 3 is a transitional mode between mode 1 and mode 2.

TABLE I
MODE BOUNDARY CONDITIONS

| Mode | Boundary conditions |
|---|---|
| 1 | $D_1 \le D_2 - 2\varphi$ |
| 2 | $D_1 > D_2 + 2\varphi$ |
| 3 | $D_2 - 2\varphi < D_1 \le D_2 + 2\varphi$ |

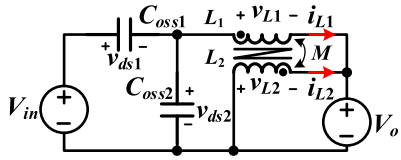


Fig. 5. Equivalent circuit during $t_8$–$t_9$ in mode 1.

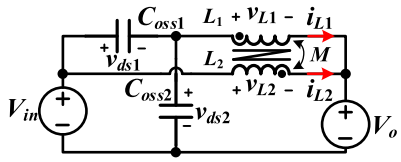


Fig. 6. Equivalent circuit during $t_4$–$t_5$ in mode 2.

## III. CONTROL STRATEGY

### A. ZVS Resonant Process Analysis

During time interval $t_8$–$t_9$ in mode 1, the equivalent circuit is shown in Fig. 5. The voltage across the two inductors can be expressed as follows:

$$\begin{cases} v_{L1}(t) = v_{ds2}(t) - V_o \\ v_{L2}(t) = -V_o. \end{cases} \tag{3}$$

Substituting (3) into (2), one can obtain the resonant process and this can be written as

$$\begin{cases} C_{\rm oss1}\frac{dv_{ds1}(t)}{dt} - C_{\rm oss2}\frac{dv_{ds2}(t)}{dt} = i_{L1}(t) \\ v_{ds2}(t) - (1-\alpha)V_o = (1-\alpha^2)L\frac{di_{L1}(t)}{dt} \\ v_{ds2}(t) = V_{\rm in} - v_{ds1}(t) \end{cases} \tag{4}$$

where $C_{\rm oss1} = C_{\rm oss2} = C_{\rm oss}$. By solving the above differential equations, the expressions of $v_{ds1}(t)$ and $i_{L1}(t)$ are derived as follows:

$$\begin{cases} v_{ds1}(t) = V_{\rm in} - V_o(1-\alpha) \\ \quad + V_o(1-\alpha)\cos(\omega_r t) + I_{\rm OFF2}Z_r\sin(\omega_r t) \\ i_{L1}(t) = V_o(1-\alpha)\sin(\omega_r t)/Z_r - I_{\rm OFF2}\cos(\omega_r t) \end{cases} \tag{5}$$

where $\omega_r = \frac{1}{\sqrt{2C_{\rm oss}L_{\rm eq4}}}$ and $Z_r = \sqrt{\frac{L_{\rm eq4}}{2C_{\rm oss}}}$. The equivalent resonant inductance is defined as $L_{\rm eq4} = L(1-\alpha^2)$ [24].

Fig. 6 shows the equivalent circuit within $t_4$–$t_5$ in mode 2. In the same way, the expressions of $v_{ds1}(t)$ and $i_{L1}(t)$ can be expressed by

During the resonant period, if $v_{ds1}(t)$ becomes negative, the drain–source voltage over $S_1$ will be clamped by the body diode, and then ZVS can be realized. According to (5) and (6), if $V_o/V_{\rm in} \ge 1/[2(1-\alpha)]$ in mode 1 or $V_o/V_{\rm in} \ge 1-1/[2(1-\alpha)]$ in mode 2, ZVS can be guaranteed even if the turn-OFF current equals zero. The deadtime should be appropriately designed to

TABLE II
SYSTEM PARAMETERS

| Symbol | Description | Value |
|---|---|---|
| $V_o$ | Output voltage | 24V |
| $V_{in}$ | Input voltage | 35V-65V |
| $L$ | Self-inductance | 5.9$\mu$H |
| $\alpha$ | Coupling coefficient | -0.21 |
| $C_o$ | Output filter capacitor | 265$\mu$F |
| $C_{in}$ | Input filter capacitor | 120$\mu$F |
| $S_1$, $S_2$, $S_3$, $S_4$ | Switches | IPT015N10N5 |
| $f_{ctr}$ | Control frequency | 100kHz |
| $P_{rate}$ | Rated power | 1kW |

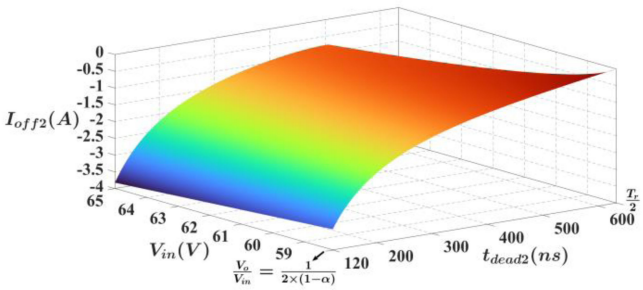


Fig. 7. Turn-OFF current versus the deadtime and input voltage in mode 1.

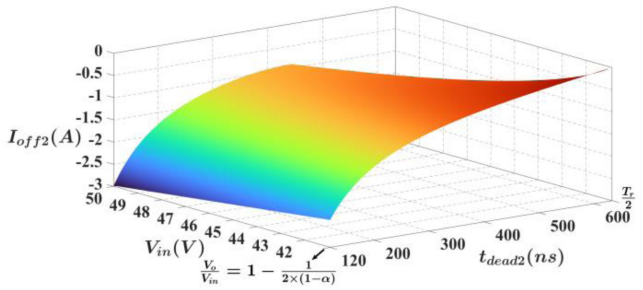


Fig. 8. Turn-OFF current versus the deadtime and input voltage in mode 2.

reduce the additional conduction loss caused by body diodes. In other cases, a negative turn-OFF current is needed to assist the realization of soft switching.

### *B. Variable Deadtime and Switching Frequency Modulation*

The system parameters are shown in Table II. If $V_o/V_{\rm in}<1/[2(1-\alpha)]$ is in mode 1, setting $v_{ds1}(t) = 0$ and one can obtain the turn-OFF current versus the deadtime and the input voltage curve and the three-dimension curve is shown in Fig. 7. Fig. 8 is the case of $V_o/V_{\rm in}<1-1/[2(1-\alpha)]$ in mode 2. The relationship between the turn-OFF current and the deadtime under different input voltages is shown in Figs. 9 and 10, and the minimum turn-OFF current is marked. As shown in the figures, when $V_o/V_{\rm in} = 1/[2(1-\alpha)]$ or $V_o/V_{\rm in} = 1-1/[2(1-\alpha)]$, ZVS can be realized after the end of the half resonant period with $I_{\rm OFF2} = 0$. The minimum required

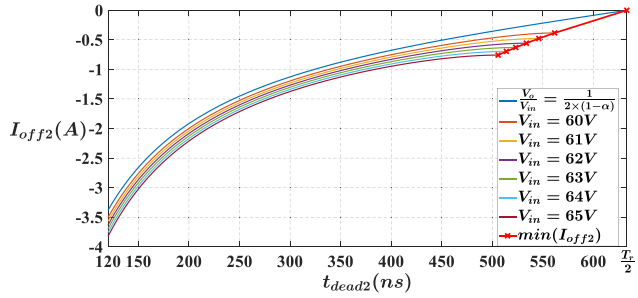


Fig. 9. Relationship between the turn-OFF current and the deadtime under different input voltage levels in mode 1.

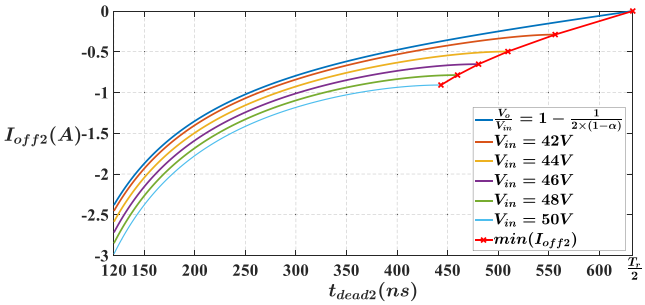


Fig. 10. Relationship between the turn-OFF current and the deadtime under different input voltage levels in mode 2.

turn-OFF current is increased as the input voltage increases. When the turn-OFF current is the same, the required deadtime will become longer as the input voltage increases. It is difficult to control the turn-OFF current and the deadtime at the same time according to the trajectory of the minimum turn-OFF current. Because the turn-OFF current can be controlled by the switching frequency, an implementation-friendly method is to design a constant turn-OFF current while varying the deadtime according to the input voltage.

According to (5) and (6), the relationship between $v_{ds1}(t)$ and $i_{L1}(t)$ in the resonant process can be written.

In mode 1

$$\begin{aligned}&[v_{ds1}(t) - V_{\rm in} + V_o(1-\alpha)]^2 + [Z_r i_{L1}(t)]^2 \\ &= [V_o(1-\alpha)]^2 + (I_{\rm OFF2}Z_r)^2.\end{aligned} \tag{7}$$

In mode 2

$$\begin{aligned}&[v_{ds1}(t) - V_{\rm in} + V_o + \alpha(V_{\rm in} - V_o)]^2 + [Z_r i_{L1}(t)]^2 \\ &= [V_o + \alpha(V_{\rm in} - V_o)]^2 + (I_{\rm OFF2}Z_r)^2.\end{aligned} \tag{8}$$

The resonant process from $t_5$ to $t_8$ in mode 3 is a combination of the resonant processes of mode 1 and mode 2. The state-plane plot is presented in Fig. 11. As seen, the deadtime required by mode 1 or mode 2 is $\theta/\omega_r$, and the deadtime needed by mode 3 is $(\theta_1+\theta_2)/\omega_r+t_{\rm dead1}$. It should be noted that the output capacitance of the MOSFET is nonlinear ($C_{\rm oss} = f(V_{ds})$). The value of the output capacitance will increase with the decrease

$$\begin{cases} v_{ds1}(t) = V_{\rm in} - V_o - \alpha(V_{in} - V_o) \\ \quad + [V_o + \alpha(V_{\rm in} - V_o)]\cos(\omega_r t) + I_{\rm OFF2}Z_r \sin(\omega_r t) \\ i_{L1}(t) = [V_o + \alpha(V_{\rm in} - V_o)]\sin(\omega_r t)/Z_r - I_{\rm OFF2}\cos(\omega_r t) \end{cases} \tag{6}$$

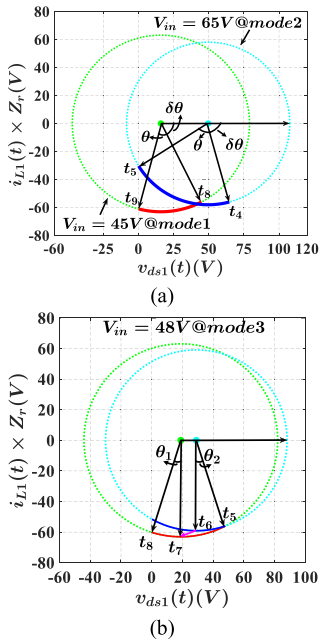


Fig. 11. State-plane plot (a) $V_{\rm in}=65$ V@mode2 and $V_{\rm in}=45$ V@mode1. (b) $V_{\rm in}=48$ V@mode3.

of $V_{ds}$, which will make the resonant period longer, so the margin should be considered in the deadtime.

From the previous analysis, the choice of deadtime is based on the input voltage, so the margin should also be designed according to the input voltage. To simplify the calculation, the deadtime is designed as

$$t_{\rm dead2}=\frac{\theta+\delta\theta}{\omega_r}=\begin{cases}\frac{1}{\omega_r}\arccos\left[\frac{V_o(1-\alpha)-V_{in}}{V_o(1-\alpha)}\right], 0<D_1\le D_2-2\varphi\ (a)\\ \frac{1}{\omega_r}\arccos\left[\frac{(\alpha-1)(V_{in}-V_o)}{V_o+\alpha(V_{in}-V_o)}\right], D_2-2\varphi<D_1<1\ (b)\end{cases}\tag{9}$$

where $\delta\theta$ is the margin. The detailed derivation of the deadtime is given in the Appendix. Due to the frequency modulation, the calculation of the deadtime in mode 3 is the same as that in mode 2, which will be explained in the following.

When $S_2$ is turned ON, $i_{L1}(t)$ is approximately equal to $I_{\rm OFF1}$. Therefore, the relationship between $I_{\rm OFF1}$ and $I_{\rm OFF2}$ can be written as

$$I_{\rm OFF1}+I_{\rm OFF2}\approx 2I_{\rm L}\tag{10}$$

where $I_{\rm L}$ is the average inductor current, and the inductor current at the center point of $S_2$ is close to the average value of the inductor current. The expression of inductor current at mode 1 is given as follows:

$$i_{L1}(t)=\begin{cases}i_{L1}(t_4)+\int_{t_4}^{t}\frac{-V_o-\alpha(V_{\rm in}-V_o)}{L_{\rm eq4}}dt, & t_4\le t<t_6\\ i_{L1}(t_6)+\int_{t_6}^{t}\frac{-V_o+\alpha V_o}{L_{\rm eq4}}dt, & t_6\le t\le t_8\end{cases}\tag{11}$$

where $i_{L1}(t_4)\approx I_{\rm L}$ and $I_{\rm OFF2}=i_{L1}(t_8)$ can be computed as

$$I_{\rm OFF2}=I_{\rm L}-\frac{V_o+\alpha(V_{\rm in}-V_o)}{L_{\rm eq4}}(t_6-t_4)\tag{12}$$

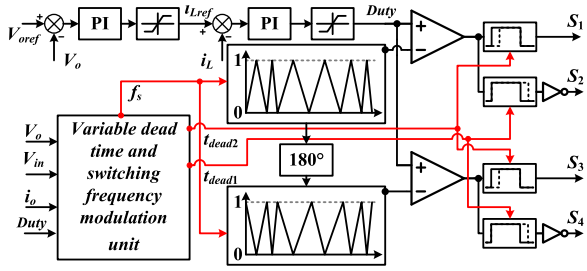


Fig. 12. Closed-loop control block diagram.

where $t_6-t_4=(D_1+2\varphi)T_s/2$, and $t_8-t_6=(D_2-D_1-2\varphi)T_s/2$. The switching frequency $f_s$ can be given by

$$f_s=\frac{\alpha V_{\rm in}\left(D_1+2\varphi\right)+\left(1-\alpha\right)V_oD_2}{L_{\rm eq4}(I_o-2I_{\rm OFF2})}\tag{13}$$

where $I_o$ is the output average current given by $I_o=2I_L$.

The analysis of mode 2 is similar to the analysis of mode 1. It can be seen from Fig. 4 that the frequency calculation of mode 3 is the same as that of mode 2. The switching frequency is given by

$$f_s=\frac{\left[V_o+\alpha(V_{\rm in}-V_o)\right]D_2}{L_{\rm eq4}(I_o-2I_{\rm OFF2})}.\tag{14}$$

### C. Implementation of Closed-Loop Control Algorithm

For the conventional constant switching frequency interleaved SR buck converter, the output voltage and output average inductor current are sampled to achieve closed-loop control. The dc bus voltage needs to be sampled in a two-stage conversion for protection purposes. According to the frequency calculation equation, variable frequency (VF) control can be realized without additional sensors. The modulation wave generation method and closed-loop control are the same as constant switching frequency control, except that the deadtime and switching frequency need to be updated in real time. The closed-loop control block diagram is shown in Fig. 12.

The principle of variable deadtime and switching frequency modulation unit can be easily realized in a digital controller, and the algorithm of this unit is shown in Fig. 13.

## IV. Experimental Results

### A. Prototype

Fig. 14 shows the photograph of the experimental prototype. The system parameters are listed in Table II. MOSFET IPT015N10N5 (100 V, 1.5 mΩ) is used as the switching device in the experimental prototype, which consists of two MOSFETs in parallel to reduce conduction loss. The digital controller is TMS320F28335DSP. The maximum switching frequency value is set at 230 kHz to reduce the switching loss when the transmitted power is lower than 10%. The minimum switching frequency is designed at 24 kHz to avoid saturation of the magnetic core. The control and sampling frequencies are both constant at 100 kHz. Considering the thermal design of surface mount devices, a single-layer metal-core printed circuit board (PCB)

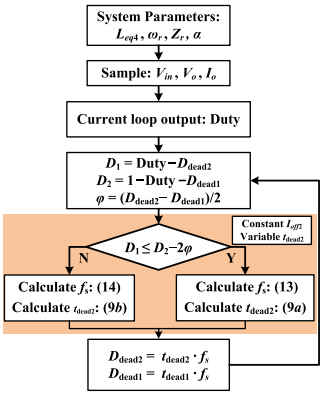


Fig. 13. Algorithm of variable deadtime and switching frequency modulation unit.

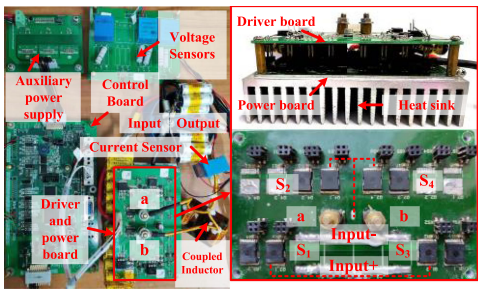


Fig. 14. Schematic diagram of the experimental prototype.

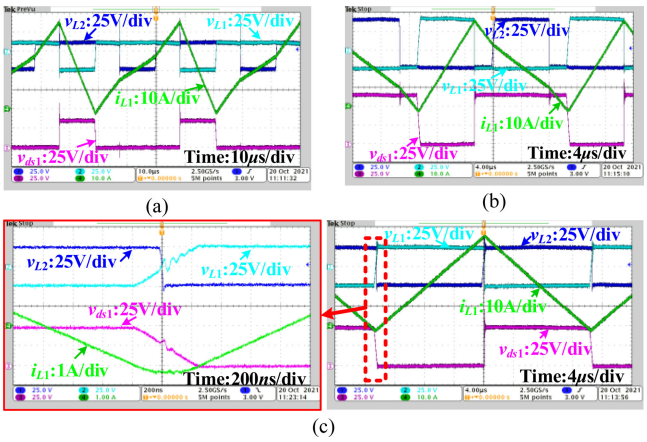


Fig. 15. Steady-state operating waveforms at full load. (a) $V_{\rm in} = 35$ V, $V_o = 24$ V, and $f_s = 24.8$ kHz @mode 1. (b) $V_{\rm in} = 65$ V, $V_o = 24$ V, and $f_s = 47.8$ kHz @mode 2. (c) $V_{\rm in} = 48$ V, $V_o = 24$ V, and $f_s = 35.0$ kHz @mode 3.

is adopted instead of a conventional PCB. Heat can be quickly transferred to the heat sink because it has only a thin inner insulating layer. The drive circuit is designed on top of the power circuit through the connectors.

## B. Operating Waveforms and ZVS Conditions

Fig. 15 illustrates the steady-state operating waveforms of three different modes, which agree well with the theoretical analysis of the modes. The transition mode 3 is shown in Fig. 15(c), the resonant process is zoomed in to display, and ZVS is realized.

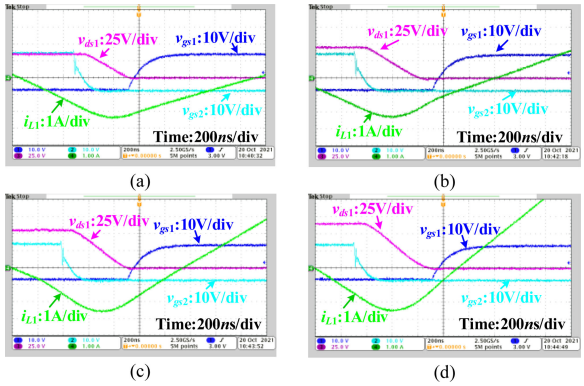


Fig. 16. ZVS conditions at 20% load. (a) $V_{\rm in} = 35$ V, $f_s = 86.7$ kHz, and $t_{\rm dead2} = 450$ ns. (b) $V_{\rm in} = 45$ V, $f_s = 116.5$ kHz, and $t_{\rm dead2} = 633$ ns. (c) $V_{\rm in} = 55$ V, $f_s = 137.6$ kHz, and $t_{\rm dead2} = 543$ ns. (d) $V_{\rm in} = 65$ V, $f_s = 159.5$ kHz, and $t_{\rm dead2} = 633$ ns.

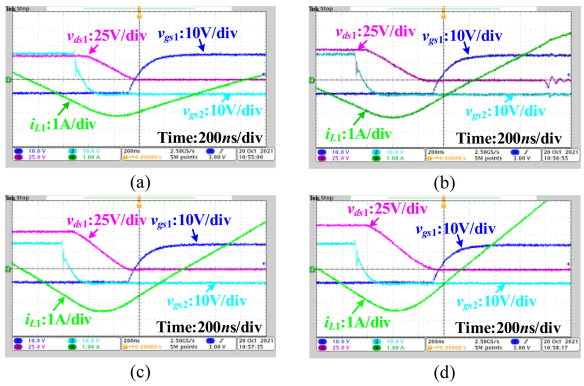


Fig. 17. ZVS conditions at full load. (a) $V_{\rm in} = 35$ V, $f_s = 24.8$ kHz, and $t_{\rm dead2} = 450$ ns. (b) $V_{\rm in} = 45$ V, $f_s = 33.8$ kHz, and $t_{\rm dead2} = 633$ ns. (c) $V_{\rm in} = 55$ V, $f_s = 41.0$ kHz, and $t_{\rm dead2} = 543$ ns. (d) $V_{\rm in} = 65$ V, $f_s = 47.8$ kHz, and $t_{\rm dead2} = 633$ ns.

The ZVS conditions of $S_1$ at 20% load and full load are shown in Figs. 16 and 17, respectively. The turn-OFF current is set to $-2$ A to ensure that the soft switching is fully realized in view of the nonlinearity of the junction capacitance, parasitic resistance in the resonant tank, and sampling errors. It can be seen that the turn-OFF current is controlled at nearly $-2$ A, and ZVS is realized because the drain–source voltage over $S_1$ is decreased to zero before the gate drive voltage is higher than the threshold voltage.

As shown in Fig. 18, the switching frequency at different loads and input voltages is measured experimentally. It can be seen that the switching frequency increases as the load is reduced, and the lowest switching frequency (24.8 kHz) appears at the lowest input voltage at full load.

## C. Conversion Efficiency and Loss Breakdown

The conversion efficiency measured in the experiment is shown in Fig. 19. $P_o$ is the output power. As shown in the figure, high efficiency can be achieved with the proposed frequency modulation. The measured efficiency remains above 96.5% from 10% load to full load. The peak efficiency exceeds 99% at around

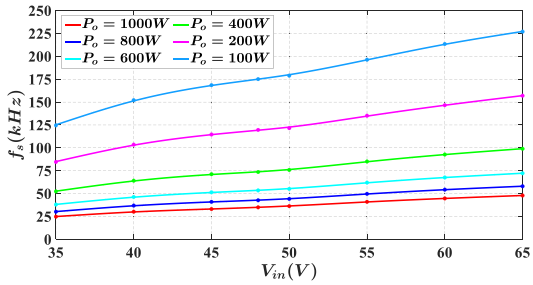


Fig. 18. Switching frequency versus input voltage and loads.

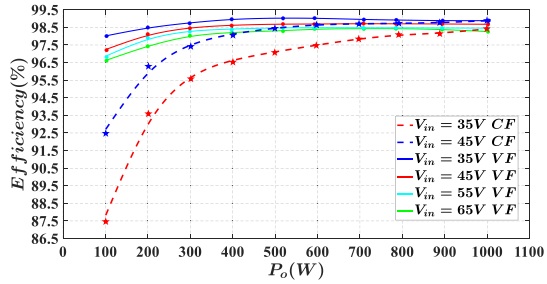


Fig. 19. Conversion efficiency over wide load range at different input voltages.

60% load when the input voltage is 35 V. It must be pointed out that the loss of auxiliary power supply is not included in the efficiency calculation. For a fair comparison, the efficiency of the same topology with constant frequency (CF) control at the identical experimental prototype is also shown in Fig. 19. The switching frequency $f_s$ is set to 24.8 kHz and the deadtime $t_{\text{dead2}}$ is set to 450 ns so that all switches can achieve ZVS with CF control at different loads. Compared with CF control, the efficiency of VF control improved significantly as the load is reduced. Because the current ripple of VF control is smaller than that of CF control, this will reduce conduction loss and core loss. The efficiency curves at 55 and 65 V input voltages are not drawn because the core is saturated due to the large current ripple. Therefore, a larger core is needed with CF control. From this aspect, the volume of the magnetic element can be reduced with VF control.

Fig. 20 gives the major power loss analysis at different loads and input voltage levels. Loss breakdown includes conduction and switching losses of MOSFETs, core, and copper losses of the coupled inductor. Due to the stray loss caused by the resistance of the wires and connectors, the predicted loss is a little lower than the measured loss. As shown in the figure, the core and copper loss of the coupled inductor account for a large proportion. Therefore, efficiency can be further improved by optimizing the coupled inductor. The turn-ON loss of the switching devices is eliminated because ZVS is achieved, the turn-OFF loss increases as the input voltage increases. The core loss is higher under high input voltage because of the higher switching frequency. As a result, efficiency is higher at low input voltage.

### D. Dynamic Response

When 90% of the load power changes at 35-V input, the dynamic response of the proposed converter is shown in Fig. 21. It can be seen that the dynamic response of VF control is fast and the overshoot or undershoot of the output voltage is relatively

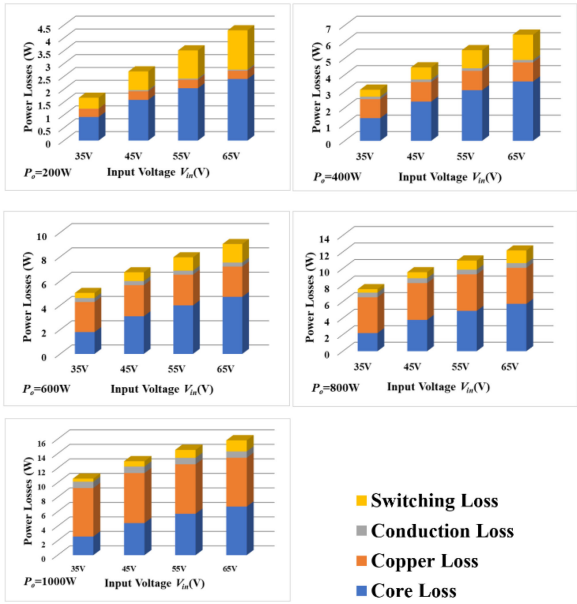


Fig. 20. Major losses breakdown.

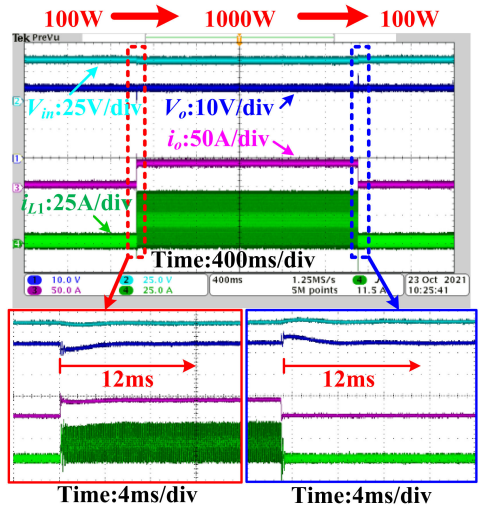


Fig. 21. Load transient response.

small. ZVS will be temporarily lost during the transition due to the delay caused by the low-pass filter in the voltage and current sampling.

It is worth mentioning that the proposed control strategy has the capability of current limiting, and the experimental result is shown in Fig. 22(a). The output current limit value is set at 45 A. When the load resistance is changed from 1.152 to 0.36 Ω by the electronic load, the output current is quickly limited to 45 A for protection, and the output voltage drops from 24 to 16.2 V. As shown in Fig. 22(b), ZVS can still be achieved in this condition. In the case of current limiting, the switching frequency versus output voltage at different input voltages is shown in Fig. 23. The switching frequency required to achieve soft switching decreases as the output voltage decreases, and ZVS will be lost when the switching frequency exceeds the lower limit. It should be pointed out that the current limit is a fault state, which will not operate for a long time in the application.

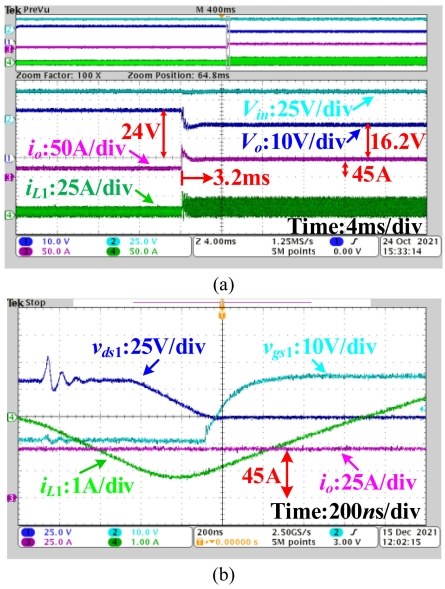


Fig. 22. Experimental results of the current limiting function. (a) Dynamic response. (b) ZVS condition.

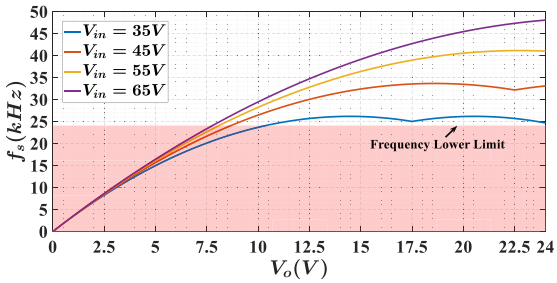


Fig. 23. Switching frequency versus output voltage in the case of current limit.

TABLE III
COMPARISON OF DIFFERENT ZVS METHODS

| | ZVS method in [9] | CRM [24] | Variable coupled inductor [26] | This paper |
|---|---|---|---|---|
| additional elements | None | ZCD | ZCD + Control winding | None |
| Soft switching range | Full input voltage range | Partial ZVS and ZCS | Wide input voltage range | Full input voltage range |
| Control complexity | Easy | Moderate | Difficult | Easy |
| Current limiting capability | Unknow | Unknow | Unknow | Yes |
| Maximum power | 200W | 1.2kW | 60W | 1kW |
| Peak efficiency | 96% (Two-stage) | 98.5% | 96% | 99% |

## V. COMPARISON AND DISCUSSION OF ZVS METHODS

A comparison of the different ZVS methods proposed for an interleaved dc–dc converter with a coupled inductor is shown in Table III. The comparison is made in terms of additional elements, soft-switching range, control complexity, current limiting capability, and peak efficiency. Extra elements or ZCD are required in [24] and [26], which will increase the complexity and cost. The soft-switching range of CRM is limited by the voltage conversion gain, and the ZVS range of the variable coupling coefficient method is restricted by the limitations of the magnetic structure in terms of the maximum and minimum coupling coefficients. In addition, a lookup table is needed to control the dc bias current when implementing variable coupling coefficients. In [9], the turn-ON time of the main switch is obtained by the voltage regulator, the turn-ON time of the SR switch is calculated in real time, and the deadtime is fixed (half the resonant period), which is easily realized by a digital controller. It can be seen that the proposed variable switching frequency modulation has the current limiting capability and is verified by experiments, which is important for the protection of the converter in practice.

## VI. CONCLUSION

In this article, a fully digital variable switching frequency and deadtime control method is proposed for the SR buck dc–dc converter with an inverse coupled inductor. It does not require any auxiliary circuits, ZCD, or high-bandwidth sensors. Three modes are distinguished, and the resonant process in different modes is analyzed in detail. According to the analysis, only by adding simple frequency and deadtime calculations, variable switching frequency and deadtime closed-loop control can be realized based on conventional CF control. ZVS can be achieved for all power switches within a wide load range despite input voltages. Even in facing the polyline shape of the current in inductors due to the coupling effect, constant turn-OFF current is realized to ensure that ZVS can be achieved in the entire input voltage range, and the deadtime is variable as well according to the input voltages to reduce the conduction loss in body diodes based on ZVS achievement. A 1-kW experimental prototype was established to verify the performance of the proposed control method. The experimental results show that the high conversion efficiency can be maintained over a wide load range. The peak efficiency is over 99%. Compared with the CF control method, the conversion efficiency is significantly improved at light loads. Besides, fast dynamic performance and current limiting capability can be realized with the proposed method.

## APPENDIX

When $0 < D_1 \le D_2 - 2\cdot\varphi$, setting $I_{\mathrm{OFF2}} = 0$, and $v_{ds1} = 0$ in (5), the equation can be rewritten as

$$0 = V_{\mathrm{in}} - V_o(1-\alpha) + V_o(1-\alpha)\cos(\omega_r t_{\mathrm{dead2}}). \tag{15}$$

According to (15), $t_{\mathrm{dead2}}$ can be calculated as

$$t_{\mathrm{dead2}} = \frac{1}{\omega_r}\arccos\left[\frac{V_o(1-\alpha) - V_{\mathrm{in}}}{V_o(1-\alpha)}\right], 0 < D_1 \le D_2 - 2\varphi. \tag{16}$$

When $D_2 - 2\cdot\varphi < D_1 < 1$, setting $I_{\mathrm{OFF2}} = 0$, and $v_{ds1} = 0$ in (6), the equation can be rewritten as

$$0 = V_{\mathrm{in}} - V_o - \alpha(V_{in} - V_o) + [V_o + \alpha(V_{\mathrm{in}} - V_o)]\cos(\omega_r t_{\mathrm{dead2}}). \tag{17}$$

According to (17), $t_{\mathrm{dead2}}$ can be expressed as

$$t_{\mathrm{dead2}} = \frac{1}{\omega_r} \arccos\left[\frac{(\alpha-1)(V_{\mathrm{in}}-V_o)}{V_o+\alpha(V_{\mathrm{in}}-V_o)}\right],\ D_2-2\varphi<D_1<1. \tag{18}$$

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