Three-Switch Common Ground Step-Down and Step-Up Single-Stage Grid-Connected PV Inverter

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***Abstract*—This article proposes the first three-switch common ground single-phase photovoltaic (PV) inverter which can support reactive power to the ac grid. The proposed step-down/step-up transformerless PV inverter totally eliminates leakage current and is suitable for use in any ON- or OFF-grid applications which require active and reactive power support. The proposed converter also features a low number of active semiconductor devices, low voltage, and current stresses, acceptable grid side current quality, and high efficiency. The performance of the proposed PV inverter is evaluated for dc to ac single-phase grid connected inverter. The converter uses a direct power dead-beat controller in the inner loop which has a smooth, accurate, and fast response. Experimental results for a 500-W, 100 V_{dc}, and 180 V_{dc} to 110 V_{rms} prototype are provided in a closed-loop system in the presence of the proposed direct power dead-beat controller. The results from the prototype validate the theoretical analysis and the applicability of the proposed structure. The converter exhibits the capability for step-down/step-up dc to ac power conversion and demonstrates a peak efficiency of 97.5% and 96.8% in the 180 and 100 V_{dc}, respectively.**

***Index Terms*—Buck–boost operation, common ground inverter, reactive power capability (RPC), transformerless photovoltaic (PV) inverter.**

I. Introduction

TRANSFORMERLESS string and micro photovoltaic (PV) inverters have the advantages of small volume, light weight, low cost, and high efficiency. However, removing the galvanic isolation leads to direct electrical connection between the PV panels and the utility grid, resulting in leakage current, which increases grid side current harmonics, system losses, and potential saturation of the core of the other distributed transformers in the network and may cause safety issues [1], [2].

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This undesirable leakage current is a consequence of the variable high frequency common mode voltage, which exists between the neutral point of the ac grid and the parasitic capacitor of the PV array [3]. According to the IEC 62109-2-2011 standard, if a monitored value of residual current exceeding 30 mA is detected, the PV system shall disconnect from the main grid within 0.3 s [4]. In recent years, with increasing application of transformerless grid connected PV inverters, the search for new topologies which mitigate leakage current has become a subject of interest. As shown in [5] and [6], the best solution for removing the leakage current from a transformerless PV inverter is the common ground structure.

In addition to reducing the leakage current, other desirable requirements for a grid connected PV converter include the following:

1) the ability to provide reactive power to the grid as required by standards, such as IEEE 1547-2018 [7];
2) a low component count which leads to lower costs and losses;
3) buck–boost capability for wider application;
4) low semiconductor voltage and current stress.

With regard to common ground inverters, the first such inverter, referred to as the *Karschny*-inverter, was proposed in [8]. The *Karschny*-inverter is based on a flying inductor current source inverter, has five active switches, and is capable of stepping up the input dc voltage which makes it an appropriate solution for a micro PV inverter. However, the inability to support reactive power provision to the ac grid limits the use of the *Karschny*-inverter to applications in OFF-grid PV inverters.

Another five-switch inverter has been proposed in [9] which is diode-less and has reactive power capability (RPC). This converter uses a flying capacitor cell to supply the output ac load with positive and negative voltages by switching a capacitor to the output terminal at positive and negative half cycles, respectively. However, this capacitor is charged directly by the input voltage, and, therefore, the voltage gain ratio of this converter is given by the duty ratio D so that it can operate only as a step-down PV inverter.

A buck–boost voltage gain, i.e., $D/(1-D)$, five-switch PV inverter has been proposed in [10] which utilizes the conduction of the body diodes of three main switches during the operation modes. The converter in [11] uses MOSFET switches in the structure of [10] and offers the dual-mode switching strategy during the positive half cycle. However, again, due to the inability of the flying inductor based converters in [10] and [11] to inject

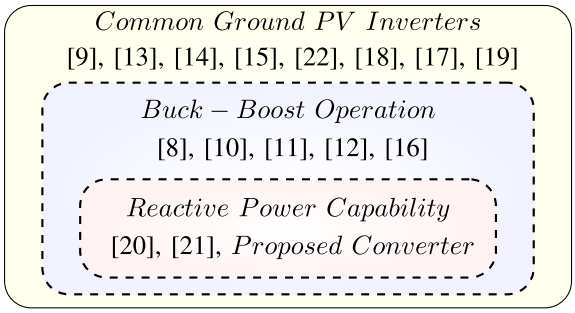

Fig. 1. Categorization of common ground PV inverters.

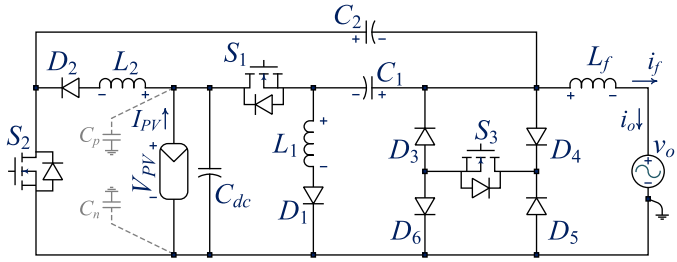

Fig. 2. Proposed three-switch common ground PV inverter.

or absorb reactive power, they are not suitable for connection to the ac network.

Four-switch common ground inverters have been proposed in [12]–[15]. Those in [13]–[15] are flying capacitor converters which need the input dc voltage level to be higher than the peak value of ac grid side voltage; in other words, they are all step-down converters.

Recently, the three-switch PV inverter has been proposed in [16]. The voltage gain ratio of the converters in [16] (and also in [12]) is $(1-2D)/(D-D^2)$ and is therefore lower and more sensitive than the buck–boost voltage gain ratio. If an external disturbance enters a power converter, then a steady-state error due to this disturbance will appear. Hence, having a more sensitive voltage gain ratio results in more steady-state error to be corrected by the controller. Moreover, the application of both converters in [12] and [16] is limited to only the OFF-grid PV inverters since they are incapable of meeting the volt-var settings required by IEEE 1547-2018 [7].

The converter in [17] has three switches and three diodes; however, due to the fact that the voltage gain ratio is limited to being step-down only, with no RPC, this converter can only work as an OFF-grid buck inverter. The step-down converter in [18] has four switches and two diodes and again it is unable to support reactive power. The step-down converter in [19] has six active switches where two body diodes of the switches have been used during the operation modes.

As shown in Fig. 1, the only common ground inverters with both RPC and buck–boost capability are those in [20] and [21], which have utilized six and seven switches, respectively. The high active switch count adds complexity to switch driving and control algorithms complicated, and, moreover, the output voltage level of converter in [21] is limited to twice the input dc voltage.

The contribution of this article is to propose a common ground inverter capable of buck–boost operation and reactive power provision which requires only three switches. In addition, the circuit has a low semiconductor device power (SDP) stress and a relatively simple structure. The maximum total voltage stress (TVS) of semiconductor devices is shown to be $V_{\rm PV}/(1-D)$ and the minimum SDP is $7.4P_{\rm out}$. As a result, the proposed converter uses power switches with a low rated power, which can improve the efficiency. In summary, the converter proposed in this work is the first three-switch common ground (TSCG) PV inverter with buck–boost and RPC and with lower SDP than all previously published common ground PV inverters.

In addition to control the inverter, a direct instantaneous power dead-beat controller (DP-DBC) is adopted for the direct instantaneous power regulation which offers accurate, fast, and smooth operation under different states of operation.

The rest of this article is organized as follows. The proposed structure is presented in Section II. Section III is devoted to the practical considerations and design calculations for the proposed converter. A comprehensive comparison to the previous state-of-the-art converters is presented in Section IV, the DP-DBC controller implementation is given in Section V, and the experimental verification is provided in Section VI. Finally, Section VII concludes this article.

II. Proposed Converter Operation Analysis

Fig. 2 shows the proposed PV common ground inverter structure. $V_{\rm PV}$ and v_o denote the PV voltage and the ac output voltage sides, respectively. The proposed inverter consists of three inductors L_1, L_2, and L_f, three capacitors C_1, C_2, and C_{dc}, three switches S_1, S_2, and S_3, and six diodes D_1, D_2, D_3, D_4, D_5, and D_6. The body diodes of switches do not conduct during a complete switching period (T_s). The pulsewidth modulation (PWM) signals and implementation scheme is shown in Fig. 3. The step-down and step-up modes during positive and negative half cycles of grid side voltage in continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are shown in Figs. 4 and 5. Moreover, the steady-state operation modes during the negative power region (NPR) is shown in Fig. 6. The detailed analysis of each mode are as follows.

A. Positive Half Cycle Operation Mode

A PV source and the output ac is connected to the $V_{\rm PV}$ and v_o sides, respectively. Two states for CCM (three states for DCM) operation modes are defined as follows.

State 1 CCM and DCM $[0-t_1]$: In this interval and according to Fig. 4(a), S_1 is turned ON while S_2 is turned OFF. In this period, L_f is charged by the input dc source $V_{\rm PV}$ and the released energy from C_1. Moreover, L_1 is charged by $V_{\rm PV}$. Thus, the current through L_1 increases, whereas the energy of L_f is increased from the input source and C_1. According to the typical time-domain waveforms in Fig. 7(a), the derived current and voltage equations

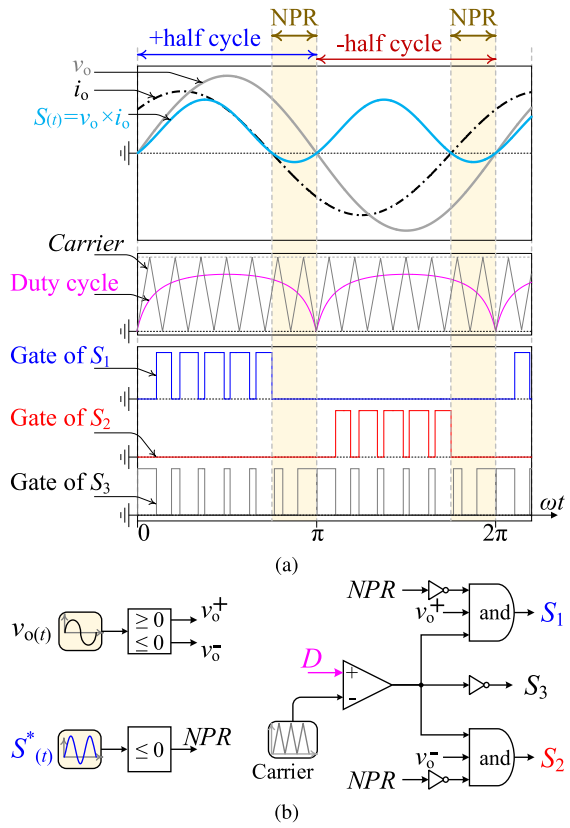

Fig. 3. (a) PWM signals. (b) Implementation scheme.

are

$$\begin{cases} v_{L1} = L_1 \frac{di_{L1}}{dt} = V_{PV} \\ v_{Lf} = L_f \frac{di_o}{dt} = V_{PV} - v_o + V_{C1}. \end{cases} \tag{1}$$

State 2 CCM $[t_1 - T_s]$, DCM $[t_1 - t_2]$: Contrary to state 1, during this interval as shown in Fig. 4(b), S_1 and S_2 are turned OFF,whereas the diodes D_3 and D_5 are conducting and S_3 is turned ON. The inductor L_1 releases its energy into the capacitor C_1, and the energy of L_f is released to the v_o side

$$\begin{cases} v_{L1} = L_1 \frac{di_{L1}}{dt} = -V_{C1} \\ v_{Lf} = L_f \frac{di_o}{dt} = -v_o. \end{cases} \tag{2}$$

By applying volt-second balance on L_1 and L_f, we have

$$D(V_{\text{PV}}) + (1-D)(-V_{C1}) = 0 \tag{3}$$

$$D(V_{\text{PV}} - v_o + V_{C1}) + (1-D)(-v_o) = 0 \tag{4}$$

where D represents the duty cycle of S_1.

By using (3), the average voltage across C_1 is

$$V_{C1} = \frac{D}{1-D} V_{\text{PV}}. \tag{5}$$

From (4) and (5), the voltage conversion ratio of the proposed converter during CCM operation mode for positive half cycle can be calculated as follows:

$$M_{(\text{CCM})} = \frac{v_o}{V_{\text{PV}}} = \frac{D}{1-D}. \tag{6}$$

State 3 DCM $[t_2 - T_s]$: According to Fig. 4(c), in this mode, the current through inductor L_1 meets zero at time t_2 and the current through L_f does not meet zero before the end of the switching period. At the end of this interval, a complete period T_s has been passed.

Considering these intervals, one can define d_1 as the duty cycle where the current of L_1 becomes zero. In this regard, according to a typical DCM waveform in Fig. 7(a), the voltage across the inductors can be defined as

$$v_{L1} = \begin{cases} +V_{\text{PV}} & 0 \le t < DT_s \\ -V_{C1} & DT_s \le t < (D+d_1)T_s \\ 0 & (D+d_1)T_s \le t < T_s \end{cases} \tag{7}$$

$$v_{Lf} = \begin{cases} +V_{\text{PV}} - v_o + V_{C1} & 0 \le t < DT_s \\ -v_o & DT_s \le t < T_s. \end{cases} \tag{8}$$

Again applying the volt-second balance on L_1, the voltage of the capacitor is

$$V_{C1} = \frac{D}{d_1} V_{\text{PV}}. \tag{9}$$

As a result, the DCM voltage gain transfer ratio during the positive half cycle can be obtained as

$$M_{(\text{DCM})} = \frac{v_o}{V_{\text{PV}}} = \frac{Dd_1 + D^2}{d_1}. \tag{10}$$

B. Negative Half Cycle Operation Mode

In this mode, the power flows from V_{PV} side to the grid side during the negative half cycle. Two states for CCM (three states for DCM) operation are defined as follows.

State 1 CCM and DCM $[0 - t_1]$: In this interval and according to Fig. 5(a), S_1 is turned OFF while S_2 is turned ON. In this period, L_f is charged by the released energy from C_2. Moreover, L_2 is charged by V_{PV}. Thus, the current through L_2 increases, whereas the energy of L_f is increased from C_2. According to the typical time-domain waveforms in Fig. 7(a), the derived current and voltage equations are

$$\begin{cases} v_{L2} = L_2 \frac{di_{L2}}{dt} = +V_{\text{PV}} \\ v_{Lf} = L_f \frac{di_o}{dt} = -v_o - V_{C2}. \end{cases} \tag{11}$$

State 2 CCM $[t_1 - T_s]$ and DCM $[t_1 - t_2]$: Contrary to state 1, during this interval as shown in Fig. 5(b), S_1 and S_2 are turned OFF, whereas the diodes D_4 and D_6 are conducting and S_3 is turned ON. The inductor L_2 releases its energy into the capacitor C_2. Similarly, the energy of L_f is released to the v_o side

$$\begin{cases} v_{L2} = L_2 \frac{di_{L2}}{dt} = +V_{\text{PV}} - V_{C2} \\ v_{Lf} = L_f \frac{di_o}{dt} = -v_o. \end{cases} \tag{12}$$

By applying volt-second balance on L_2 and L_f, we have

$$D(V_{\text{PV}}) + (1-D)(V_{\text{PV}} - V_{C2}) = 0 \tag{13}$$

$$D(-v_o - V_{C2}) + (1-D)(-v_o) = 0. \tag{14}$$

By using (13), the average voltage across C_2 can be determined as

$$V_{C2} = \frac{1}{1-D} V_{\text{PV}}. \tag{15}$$

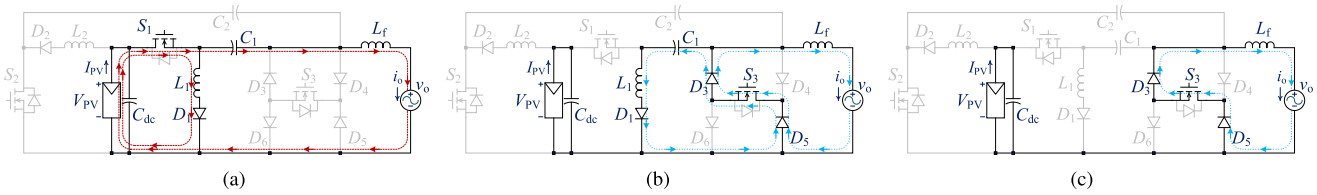

Fig. 4. Equivalent circuit of the proposed converter during the positive half cycle. (a) State 1. (b) State 2. (c) State 3.

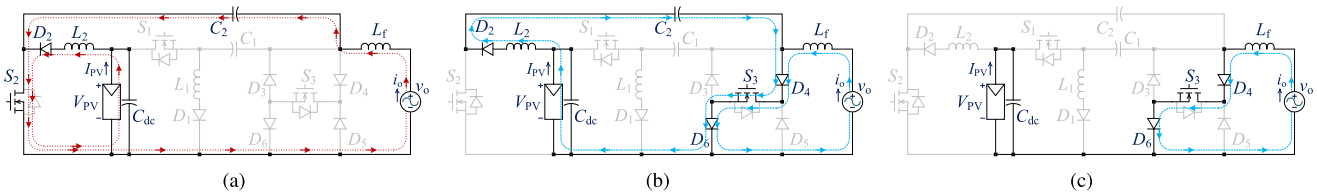

Fig. 5. Equivalent circuit of the proposed converter during the negative half cycle. (a) State 1. (b) State 2. (c) State 3.

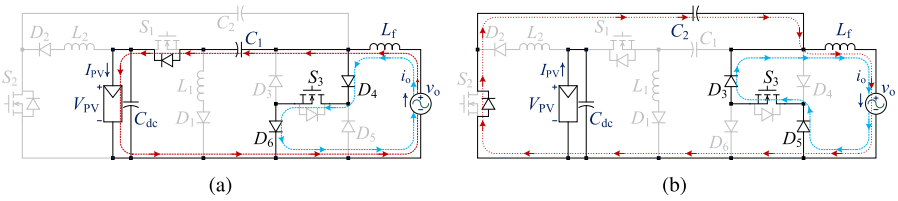

Fig. 6. Equivalent circuit of the proposed converter during NPR operation. (a) Mode 1. (b) Mode 2.

From (14) and (15), the voltage conversion ratio of the proposed converter during CCM operation for negative half cycle operation can be calculated as follows:

$$M_{(\mathrm{CCM})} = \frac{v_o}{V_{\mathrm{PV}}} = -\frac{D}{1-D}. \tag{16}$$

State 3 DCM $[t_2 - T_s]$: According to Fig. 5(c), in this mode, the current through inductor L_2 meets zero at time t_2 and the current through L_f does not meet zero before the end of the switching period. At the end of this interval, a complete period T_s has been passed.

Considering these intervals, one can define d_2 as the duty cycle where the current of L_2 becomes zero. In this regard, according to a typical DCM waveform in Fig. 7(b), the voltage across the inductors can be defined as

$$v_{L2} = \begin{cases} +V_{\mathrm{PV}} & 0 \le t < DT_s \\ V_{\mathrm{PV}} - V_{C2} & DT_s \le t < (D+d_2)T_s \\ 0 & (D+d_2)T_s \le t < T_s \end{cases} \tag{17}$$

$$v_{Lf} = \begin{cases} -v_o - V_{C2} & 0 \le t < DT_s \\ -v_o & DT_s \le t < T_s. \end{cases} \tag{18}$$

Now the volt-second balance is applied on L_2 so that the voltage of the capacitor is

$$V_{C2} = \frac{D+d_2}{d_2} V_{\mathrm{PV}}. \tag{19}$$

As a result, the DCM voltage gain transfer ratio during the negative half cycle can be obtained as

$$M_{(\mathrm{DCM})} = \frac{v_o}{V_{\mathrm{PV}}} = -\frac{Dd_2 + D^2}{d_2}. \tag{20}$$

C. Negative Power Region Operation Modes

During the positive half cycle of the grid voltage and when the instantaneous value of i_o is negative [as shown in Fig. 6(a)], when S_1 is ON and S_3 is OFF (State 1), the current through L_f increases in the circuit consisting of C_1, V_{PV}, and the antiparallel diode of S_1. During State 2 when S_1 is OFF and S_3 is ON, the negative current can flow in the freewheeling circuit consisting of S_3, D_4, and D_6.

During the negative half cycle of the grid voltage and when the instantaneous value of i_o is positive [as shown in Fig. 6(b)], when S_2 is ON and S_3 is OFF (State 1), the current can increase and flow through L_f in the circuit consisting of C_2 the antiparallel diode of S_2. During State 2 when S_2 is OFF and S_3 is ON, the negative current decreases and flows through the freewheeling circuit consisting of S_3, D_3, and D_5.

Hence, by using the proposed switching strategy, the proposed converter can inject or absorb reactive power to the ac grid while preserving the quality of the grid current. Therefore, the proposed converter can satisfy the volt-var setting requirements of standards, such as IEEE 1547-2018.

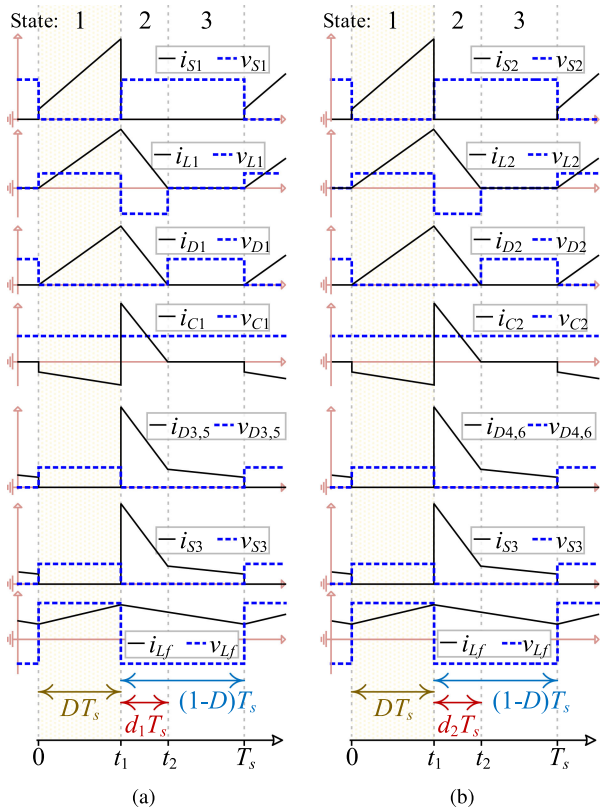

Fig. 7. Time-domain waveforms. (a) Positive half cycle. (b) Negative half cycle.

III. Design Considerations

A. Duty Cycle Calculation

The duty cycle during the CCM and DCM modes can be calculated according to the PV side and output side voltages, and the duty cycle will be time dependent due to the ac output voltage of the inverter.

From (6) and (16), the duty cycle of the proposed converter in the CCM mode is

$$D = \frac{|v_o|}{|v_o| + V_{\text{PV}}}. \tag{21}$$

The current ripple of inductors L_1 and L_2 can be obtained as follows:

$$\Delta i_{L1} = \frac{V_{\text{PV}}}{f_s L_1} D,\ \Delta i_{L2} = \frac{V_{\text{PV}}}{f_s L_2} D \tag{22}$$

where f_s is the switching frequency.

Under DCM operation, the average current of L_1 and L_2 can be obtained as

$$I_{L1} = \frac{D + d_1}{2} \Delta i_{L1},\ I_{L2} = \frac{D + d_2}{2} \Delta i_{L2}. \tag{23}$$

Therefore, d_1 and d_2 for DCM modes can be calculated as

$$d_1 = \frac{2 I_{L1} f_s L_1}{D V_{\text{PV}}} - D,\ d_2 = \frac{2 I_{L2} f_s L_2}{D V_{\text{PV}}} - D. \tag{24}$$

B. Semiconductors Rating

The average (over a switching cycle) ON-state current and average OFF-state voltage across the switches and the diodes can be expressed as

$$\begin{cases} I_{S1} = I_{L1} + I_o = (\frac{D}{1-D} + 1) I_o = \frac{1}{1-D} I_o \\ I_{S2} = I_{L2} + I_o = (\frac{D}{1-D} + 1) I_o = \frac{1}{1-D} I_o \\ I_{D1} = I_{D2} = \frac{D}{1-D} I_o \\ I_{D3} = I_{D4} = I_{D5} = I_{D6} = I_{S3} = \frac{1}{1-D} I_o \end{cases} \tag{25}$$

$$\begin{cases} V_{S1} = V_{C1} + V_{\text{PV}} = (\frac{D}{1-D} + 1) V_{\text{PV}} = \frac{1}{1-D} V_{\text{PV}} \\ V_{S2} = V_{C2} = \frac{1}{1-D} V_{\text{PV}} \\ V_{D1} = V_{D2} = 0 \\ V_{D3} + V_{D5} + V_{S3} = V_{D4} + V_{D6} + V_{S3} = \frac{1}{1-D} V_{\text{PV}}. \end{cases} \tag{26}$$

Therefore, the average total current stress (TCS) and TVS of semiconductor devices during the positive (P) and negative (N) half cycle is

$$P: \begin{cases} \text{TCS} = (D)(I_{S1} + I_{D1}) + (1-D)(I_{D3} + I_{D5} + I_{S3}) \\ \qquad = \frac{D^2 - 2D + 3}{1-D} I_o \\ \text{TVS} = (1-D) V_{S1} + (D)(V_{D3} + V_{D5} + V_{S3}) \\ \qquad = \frac{1}{1-D} V_{\text{PV}} \end{cases} \tag{27}$$

$$N: \begin{cases} \text{TCS} = (D)(I_{S2} + I_{D2}) + (1-D)(I_{D4} + I_{D6} + I_{S3}) \\ \qquad = \frac{D^2 - 2D + 3}{1-D} I_o \\ \text{TVS} = (1-D) V_{S2} + (D)(V_{D4} + V_{D6} + V_{S3}) \\ \qquad = \frac{1}{1-D} V_{\text{PV}}. \end{cases} \tag{28}$$

Furthermore, it is useful to compare the total active switch stress and active switch utilization of candidate converter approaches. In a good design, the voltages and currents imposed on the semiconductor devices are minimized, while the load power is maximized. If a converter contains n active semiconductor devices, the average total switching device power (SDP) stress can be defined as

$$\text{SDP}_{\text{avg}} = \sum_{j=1}^{n} V_j I_j / P_{\text{out}} \tag{29}$$

where V_j and I_j are the average voltage and current over a switching cycle, applied to switch j.

Therefore, the SDP_{avg} of the proposed converter is

$$\text{SDP}_{\text{avg}} = \frac{3 - 2D}{D(1-D)}. \tag{30}$$

C. Passive Components Design

The grid side filter inductor, i.e., L_f, is designed according to the ac source voltage and the desired current ripple Δi_o as

$$L_f \geq \frac{v_o (1-D) T_s}{\Delta i_o}. \tag{31}$$

The value of inductors L_1 and L_2 can be determined according to the boundary of DCM mode. Thus, from $M_{(\text{DCM})}$ and (24),

the following equation can be derived:

$$L_1 = L_2 \leq \frac{DV_{\text{PV}}}{2I_{L1}f_s}. \tag{32}$$

The voltage of C_1 (or C_2) should be a constant value within a switching period. Therefore, the resonant frequency created by elements L_f, C_1, and L_1 (or C_2 and L_2) during the positive (or negative) half cycle, i.e., f_r, must be much higher than the grid frequency f_g and lower than the switching frequency f_s. Now, C_1 (or C_2) can be expressed as

$$C_{1,2} = \frac{1}{(2\pi f_r)^2(L_f + L_{1,2})};\ f_g < f_r < f_s. \tag{33}$$

C_{dc} is the equivalent dc-link capacitance of the converter and is calculated considering the permissible voltage ripple across the dc-link (ΔV_{dc}) and the grid frequency as follows:

$$C_{\text{dc}} = \frac{P_{\text{PV}}}{2\pi f_g V_{\text{PV}} \Delta V_{\text{dc}}}. \tag{34}$$

As an example of the choice of components for the inverter considering 20 kHz as the switching frequency, $V_{\text{PV}} = 100$ V, ΔV_{dc}=5%, $v_o = 110\ V_{\text{rms}}$, and a maximum current ripple of L_f of 2 A, the critical passive components are $L_f = 2.9$ mH, $L_1 = L_2 = 208\ \mu$H, $C_1 = C_2 = 8.6\ \mu$F, and $C_{\text{dc}} = 0.98$ mF.

IV. Comparison of the Proposed Inverter to the State-of-the-Art

Some general information on the characteristics of the main common ground PV inverters and the proposed inverter are provided in Table I.

The main point of Table I is that the proposed converter has the lowest active switch count without any limitation of the voltage gain ratio or ability to support reactive power. The proposed converter has only three switches and the use of their body diodes is not required. The total semiconductor counts of buck–boost voltage gain ratio converters, i.e., the proposed converter [8], [10], [11], are 9, 7, 5, and 8, respectively. Although the total semiconductor device count of [8], [10], and [11] is lower than the proposed converter, they are not able to meet the requirements of IEEE 1547-2018 in terms of reactive power provision.

The voltage gain ratio and sensitivity of the voltage gain comparisons are made between the proposed converter and the main common ground PV inverters in Fig. 8. A higher value of sensitivity means that the voltage gain changes more for a given change in duty cycle. In other words, the variation in output voltage of the digitally controlled converter will be greater for a more sensitive voltage gain converter. Therefore, a converter with more sensitive voltage gain may require a more accurate control system with a high resolution microcontroller.

The gain voltage of the PV inverters, such as [9], [13]–[15], is D. Therefore, the use of those converters is limited only to step-down applications. Although the voltage gain of [21] is $2D$ so that it is capable of stepping up the input voltage, the output voltage is obviously limited to twice the input voltage. The converter of [22] is not able to step up the input voltage during the negative half cycle and it has a very sensitive voltage gain

TABLE I
Comparison Among the Main Common Ground Inverters

Ref.	Number of Elements†	Semi. at state 1,2,3,4	High Freq S at +, − half cycles	$M_{(CCM)}$ RPC?	Main test results
Proposed	3 S 0 BD 6 D 3 L, 3 C	1 S, 1 D 1 S, 3 D 1 S, 1 D 1 S, 3 D	2, 2	$\frac{D}{1-D}$ *yes*	100,180V_{dc},110V_{ac} 500W, 20kHz η_{max}:96.8, 97.5% THD:3.2, 3%
[8]	5 S 1 BD 2 D 2 L, 2 C	3S,1D,1BD 2 S, 2 D 3 S, 1 BD 2 S, 1 D	2, 1	$\frac{D}{1-D}$ *no*	NA
[9]	5 S 3 BD 0 D 1 L, 2 C	2 S, 1 BD 2 S, 1 BD 2 S 1 S, 1 BD	5, 5	D *yes*	400V_{dc},220V_{ac} 500W, 20kHz η_{max} :NA THD:2.1%
[12]	4 S 4 BD 0 D 3 L, 3 C	2 S 2 S	2, 2	$\frac{(1-2D)}{D(1-D)}$ *no*	60V_{dc}, 110V_{ac} 300W, 50kHz η_{max}:94.2% THD:4.3%
[13]	4 S 2 BD 2 D 2 L, 4 C	2 S, 1 D 1S,1BD,1D 2 S, 1 D 1S,1BD,1D	2, 4	D *yes*	400V_{dc},220V_{ac} 500W, 24kHz η_{max}:97.4% THD:2.1%
[10]	5 S 3 SBD 0 D 2 L, 2 C	2 S 2 S, 2 SBD 2 S 2 S, 1 SBD	2, 2	$\frac{D}{1-D}$ *no*	200V_{dc},220V_{ac} 200W, 20kHz η_{max}:96% THD:NA
[14] I,II	4 S 0 BD 1 D 1 L, 3 C	2 S, 1 D 2 S, 1 D 2 S 2 S, 1 D	2, 2	D *yes*	400V_{dc},230V_{ac} 1kW, 50kHz η_{max}:99.2% THD:2%
[14] III	4 S 2 BD 0 D 1 L, 3 C	1 S 2 S, 2 BD 1 S 2 S, 2 BD	3, 3	D *no*	400V_{dc},230V_{ac} 1kW, 50kHz η_{max}:97.8% THD:2%
[21]	7 S 2 BD 1 D 1 L, 3 C	2 S 2S,1BD,1D 2 S, 1 D 3 S, 1 BD	4, 5	$2D$ *yes*	180V_{dc},220V_{ac} 500W, 25kHz η_{max}:98.1% THD:2.1%
[15]	4 S 3 BD 0 D 2 L, 2 C	1 S, 1 BD	4, 4	D *yes*	180V_{dc},110V_{ac} 2kW, 20kHz η_{max}:96.5% THD:3.3%
[16]	3 S 1 BD 1 D 4 L, 4 C	2 S, 1 BD 1 S, 1 D	3, 3	$\frac{(1-2D)}{D(1-D)}$ *no*	38V_{dc}, 110V_{ac} 280W, 40kHz η_{max}:93% THD:2.9%
[22]	2 S 1 BD 1 D 3 L, 3 C	2 S, 1 BD 1 S, 1 D	2, 2	$\frac{(1-2D)}{(1-D)}$ *no*	50V_{dc}, 100V_{ac} 180W, 100kHz η_{max}:95% THD:3.82%
[20]	6 S 0 BD 2 D 3 L, 4 C	3 S 2 S, 2 D 3 S 3 S, 2 D	4, 4	$\frac{(D+D^2)}{(1-D)}$ *yes*	50V_{dc}, 110V_{ac} 400W, 20kHz η_{max}:96.4% THD:3.5%
[11]	5 S 0 BD 3 D 2 L, 2 C	2 S, 1 D 2 S, 2 D 2 S 2 S, 1 D	2, 2	$\frac{D}{1-D}$ *no*	130V_{dc},110V_{ac} 500W, 20kHz η_{max}:98.81% THD:4.28%
[17]	3 S 0 BD 3 D 3 L, 2 C	2 S 2 D 2 S 2 D	1, 2	$1-2D$ *no*	180V_{dc},110V_{ac} 350W, 20kHz η_{max}:96.8% THD:2.32%
[18]	4 S 0 BD 2 D 3 L, 2 C	1 S 1 S, 1 D 2 S 1 S, 1 D	1, 1	D *no*	180V_{dc},110V_{ac} 350W, 37kHz η_{max}:98.55% THD:2.53%
[19]	6 S 2 BD 0 D 3 L, 3 C	1 S 1 S, 1 BD 2 S 1 S, 1 BD	1, 2	D *yes*	200V_{dc},120V_{ac} 1kW, 50kHz η_{max}:98.22% THD:2.3%

† S: switch, BD: body diode, SBD: series body diode, D: diode, L: inductor, C: capacitor.

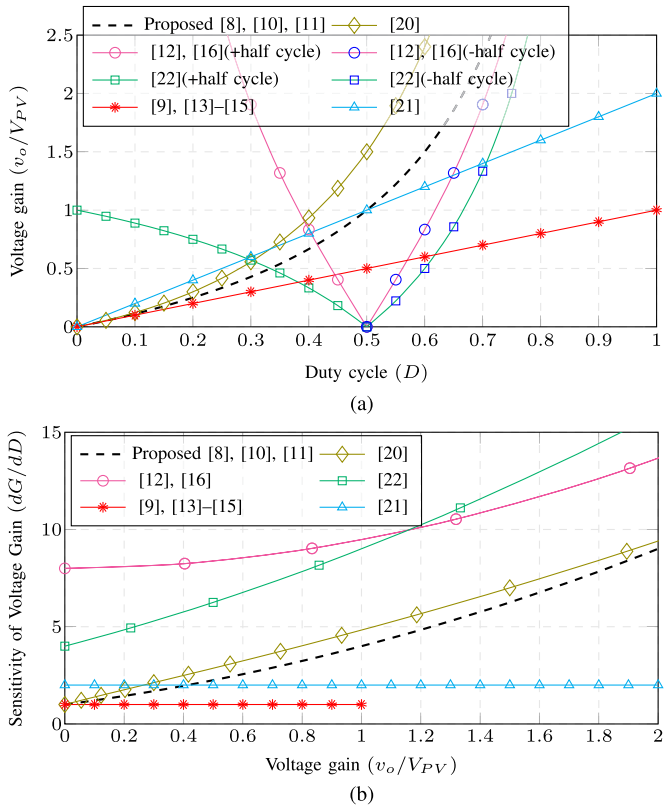

Fig. 8. (a) Voltage gain ratio. (b) Voltage gain sensitivity comparison.

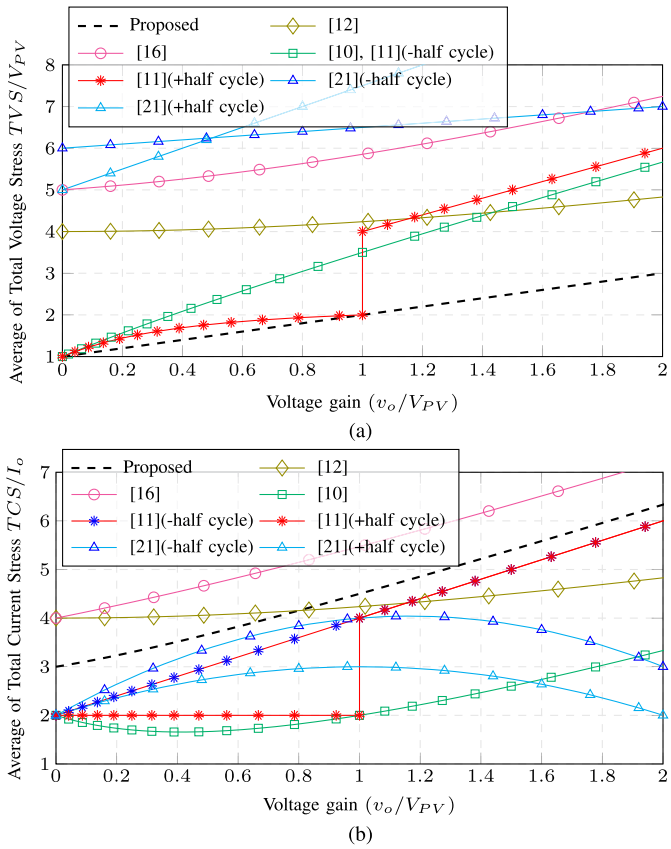

Fig. 9. (a) Average voltage. (b) Current stress versus voltage gain.

ratio. The converters in [12] and [16] have the ability of step-up operation, but the voltage gain is lower and more sensitive than the proposed converter. As shown in this figure, the converter in [20] does have a higher gain than the proposed converter which is also more sensitive. Clearly, the voltage gain ratio of the proposed converter is the same as that of [8], [10], and [11] and is unlimited for any value of PV side voltage and has a very low sensitivity of voltage gain with respect to duty cycle.

Based on the volt-var requirements of IEEE 1547-2018, even during the normal operation, a grid connected distributed energy resource (DER) should be able to inject or absorb reactive power. Therefore, the converters in [8], [10]–[12], [14] type-3 [16], [22] would need to be improved to have reactive power provision capability (RPC) so that they can be used as DER grid connected inverters.

Another comparison can be made between the proposed converter and its main competitors based on normalized averaged TVS (TVS/$V_{\rm PV}$) and normalized averaged TCS of semiconductor devices (TCS/I_o) as shown in Fig. 9. Hence, the proposed converter offers the lowest TVS/$V_{\rm PV}$. Also, TCS/I_o of the proposed converter is lower than the converter in [16] and lower than the TCS of converter in [12] at the voltage gains lower than 0.8. It must be mentioned that the TCS/I_o of converters in [10], [11], and[21] is lower than the proposed converter. However, the converter in [21] cannot achieve a voltage gain greater than 2 and converters in [10]–[12] are not able to support reactive power for the ac grid.

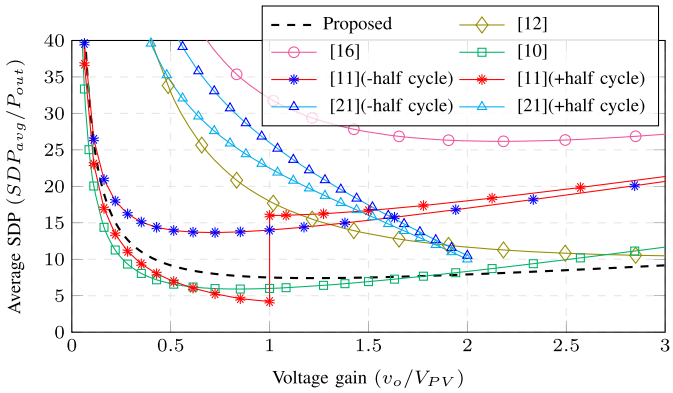

Fig. 10. Average SDP versus voltage gain.

It is also useful to compare the SDP of the proposed converter and the main competitor approaches. The SDP of a converter should be as low as possible to reduce the cost of the semiconductor devices. As it was mentioned in [23], in a good converter design, the voltage and current imposed on a semiconductor device are minimized, while the output power is maximized. Fig. 10 shows the SDP curves of the other reported converters and the proposed converter versus voltage gain. It is clear that the proposed converter has the lowest SDP compared with the other PV inverters.

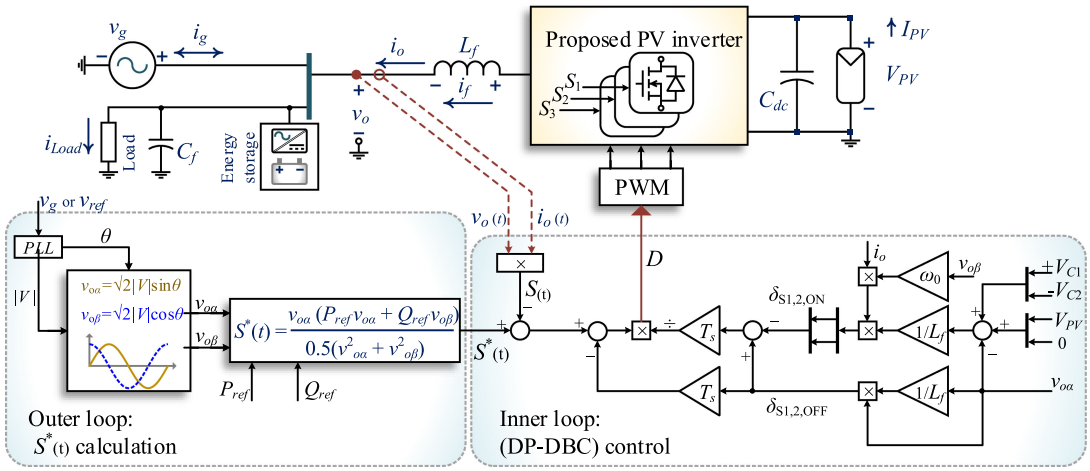

Fig. 11. Proposed DP-DBC control system.

Furthermore, as will be shown later, the measured maximum efficiency is 97.5% for the proposed converter. Therefore, the proposed converter presents a good balance between the component count, voltage gain range, semiconductor device ratings, common ground between PV side, and the output terminals and efficiency, which makes it a very practical solution for a PV power converter unit.

V. Control System Design

The control of the proposed inverter includes the control of output active and reactive powers. The overall diagram of the proposed control system is shown in Fig. 11. The reference value of active and reactive powers is calculated by the maximum power point tracking loop [24] and the volt-var setting, respectively.

In the outer loop, the grid or reference voltage is fed to the phase-locked loop to determine the phase and the amplitude of the voltage, i.e., θ and $|V|$. By using $|V|$ and θ and based on references of P_{ref} and Q_{ref}, the reference value of instantaneous power can be obtained. Based on the instantaneous power theory [25], the reference power can be obtained as follows:

$$S^*(t) = \frac{2v_{o\alpha}}{v_{o\alpha}^2 + v_{o\beta}^2} \times (P_{\text{ref}} v_{o\alpha} + Q_{\text{ref}} v_{o\beta}). \tag{35}$$

In the control system, a fast digital, simple yet efficient DP-DBC concept is adopted for both half cycles as the inner loop.

The single-phase instantaneous power can be calculated as

$$S(t) = v_o(t) \times i_o(t). \tag{36}$$

The derivative of S with respect to time can be expressed as

$$\frac{dS(t)}{dt} = \frac{di_o(t)}{dt} v_o(t) + \frac{dv_o(t)}{dt} i_o(t). \tag{37}$$

Assuming sinusoidal grid voltages, $\alpha - \beta$ components of the output voltage, $v_{o\alpha}$ and $v_{o\beta}$, can be expressed as

$$\begin{cases} v_{o\alpha} = V_m \sin \omega_0 t \\ v_{o\beta} = V_m \cos \omega_0 t \end{cases} \tag{38}$$

where V_m represents the phase voltage amplitude and ω_0 is the grid angular frequency. Note that, in the case of a single-phase system, $v_{o\alpha}$ is taken as the actual output voltage and $v_{o\beta}$ is generated by introducing a quarter period phase shift.

Taking the derivative from (38) with respect to time, the derivative of $S(t)$ can be obtained

$$\frac{dS(t)}{dt} = \frac{di_o(t)}{dt} v_{o\alpha}(t) + \omega_0 v_{o\beta}(t) i_o(t). \tag{39}$$

In the positive half cycle, when S_1 is ON, the voltage across L_f can be determined as

$$v_{Lf} = L_f \frac{di_o}{dt} = V_{\text{PV}} + V_{C1} - v_o. \tag{40}$$

Therefore, the slope of power S during S_1 ON-state ($\delta_{S1,\text{ON}}$) is

$$\delta_{S1,\text{ON}} = \frac{dS(t)}{dt} = \frac{V_{\text{PV}} + V_{C1} - v_{o\alpha}}{L_f} v_{o\alpha} + \omega_0 v_{o\beta} i_o. \tag{41}$$

When S_1 is OFF and S_3 is ON, the inductor voltage is

$$v_{Lf} = L_f \frac{di_o}{dt} = -v_o \tag{42}$$

and OFF-state slope of S during S_1 OFF-state ($\delta_{S1,\text{OFF}}$) can be expressed as

$$\delta_{S1,\text{OFF}} = \frac{dS(t)}{dt} = \frac{-v_{o\alpha}}{L_f} v_{o\alpha} + \omega_0 v_{o\beta} i_o. \tag{43}$$

Similarly, in the negative half cycle, when the switch S_2 is ON, the voltage across L_f can be expressed as

$$v_{Lf} = L_f \frac{di_o}{dt} = -V_{C2} - v_o \tag{44}$$

and when S_2 is OFF and S_3 is ON, the inductor voltage is

$$v_{Lf} = L_f \frac{di_o}{dt} = -v_o. \tag{45}$$

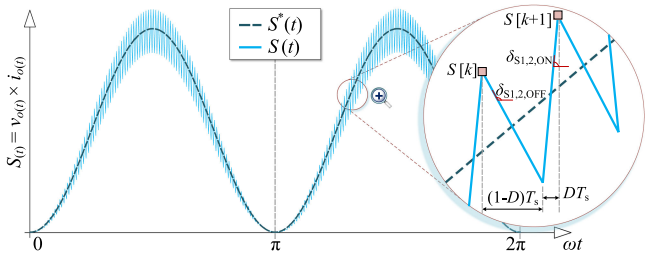

Fig. 12. Variation of instantaneous power $S(t)$.

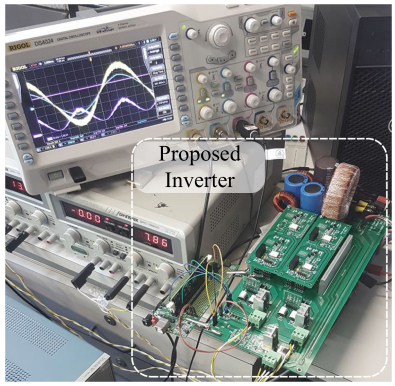

Fig. 13. Experimental prototype of the proposed converter.

TABLE II
EXPERIMENTAL TEST CONDITIONS AND PARAMETERS

Parameters	Values
Rated power (P_{out}):	500 [W]
Switching frequency (f_s):	20 [kHz]
Grid side voltage (v_g):	110 [V] and 50 [Hz]
PV side voltage (V_{PV}):	100 [V] and 180 [V]
Inductors L_1, L_2 and L_f:	0.2 [mH], 0.2 [mH] and 3.5 [mH]
Capacitors C_1, C_2 and C_{dc}:	330 [μF], 330 [μF] and 1 [mF]
MOSFET switches:	IPW60R017C7
Diodes:	STTH30L06C
Microcontroller:	Piccolo TMS320F28035

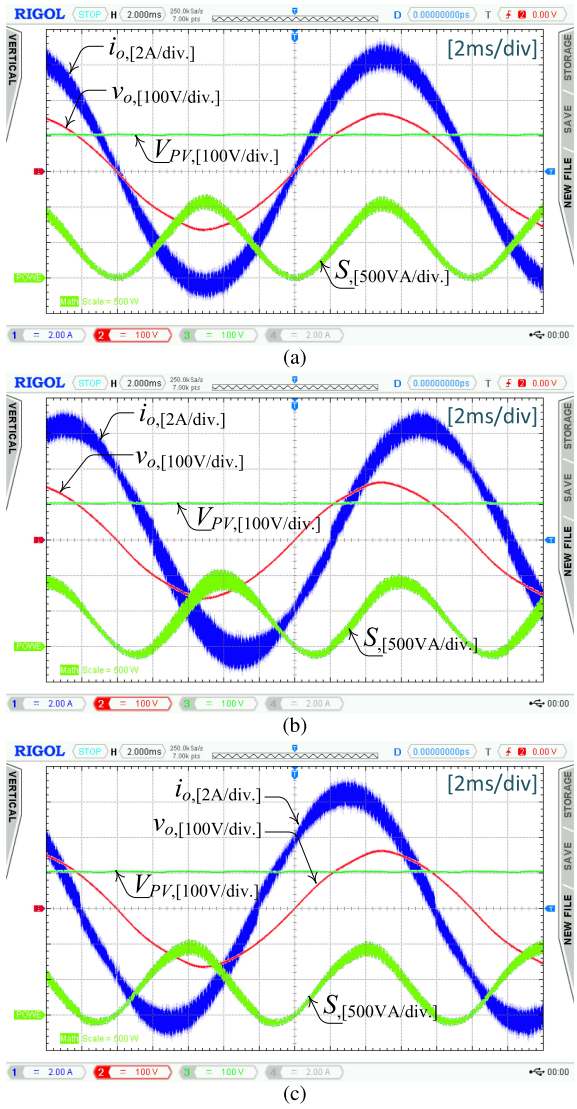

Fig. 14. Waveforms of V_{PV}, v_o, and i_o and output instantaneous power (S) for (a) $P_{\text{ref}} = 500$ W and $Q_{\text{ref}} = 0$ Var (PF $= 1$), (b) $P_{\text{ref}} = 400$ W and $Q_{\text{ref}} = 300$ Var (PF $= 0.8$ lagging), and (c) $P_{\text{ref}} = 400$ W, $Q_{\text{ref}} = 300$ Var (PF $= 0.8$ leading).

The current slope of S during S_2 ON-state ($\delta_{S2,\text{ON}}$) and OFF-state ($\delta_{S2,\text{OFF}}$) can be expressed as

$$\delta_{S2,\text{ON}} = \frac{dS(t)}{dt} = \frac{-V_{C2} - v_{o\alpha}}{L_f} v_{o\alpha} + \omega_0 v_{o\beta} i_o \tag{46}$$

$$\delta_{S2,\text{OFF}} = \frac{dS(t)}{dt} = \frac{-v_{o\alpha}}{L_f} v_{o\alpha} + \omega_0 v_{o\beta} i_o. \tag{47}$$

As shown in Fig. 12, and based on predictive control theory [26]–[35], the instantaneous power S at the next sampling time ($S[k+1]$) can be calculated from its current value ($S[k]$), using the slopes in (40), (42), (45), and (46), i.e.,

$$S[k+1] = S[k] + \delta_{S1,2,\text{ON}} t_{\text{ON}} + \delta_{S1,2,\text{OFF}} (1 - t_{\text{ON}}) \tag{48}$$

where t_{ON} is the S_1 (or S_2) ON-state dwell time.

The controller is intended to eliminate the error S_e between the reference instantaneous power (S^*) and $S[k+1]$, which translates to

$$\begin{aligned} S_e = S^* - S[k+1] = 0 \Rightarrow \\ S^* - S[k] - \delta_{S1,2,\text{ON}} D T_s - \delta_{S1,2,\text{OFF}} (1 - D) T_s = 0. \end{aligned} \tag{49}$$

Then, t_{ON} and, consequently, the optimal duty cycle can be obtained as

$$D = \frac{(S^* - S[k]) - \delta_{S1,2,\text{OFF}} T_s}{(\delta_{S1,2,\text{ON}} - \delta_{S1,2,\text{OFF}}) T_s} \tag{50}$$

$$P: \; D = \frac{L_f (S^* - S[k]) + (v_{o\alpha}^2 - L_f \omega_0 v_{o\beta} i_o) T_s}{(V_{\text{PV}} + V_{C1}) v_{o\alpha} T_s} \tag{51}$$

$$N: \; D = \frac{L_f (S^* - S[k]) + (v_{o\alpha}^2 - L_f \omega_0 v_{o\beta} i_o) T_s}{-V_{C2} v_{o\alpha} T_s}. \tag{52}$$

The grid side inverter instantaneous power controller aims to track the P_{ref} and Q_{ref} and shape the grid side current denoted as

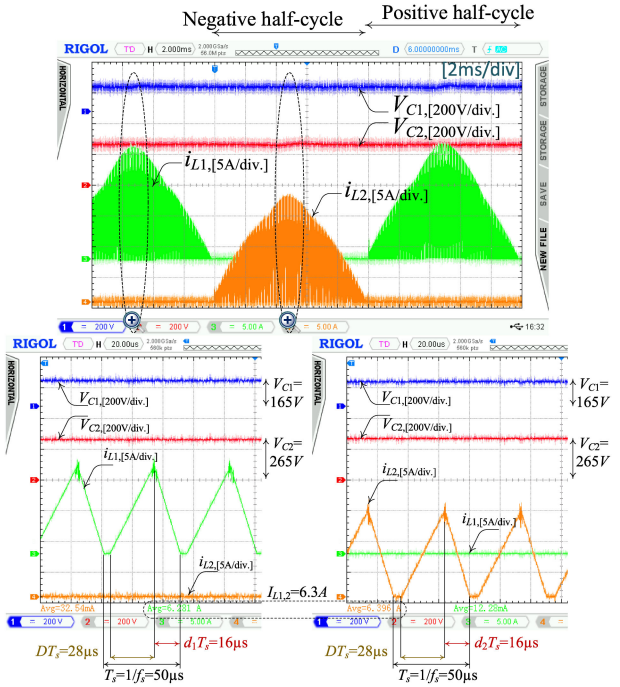

Fig. 15. $i_{L1,2}$ and $V_{C1,2}$ during DCM positive and negative half cycles.

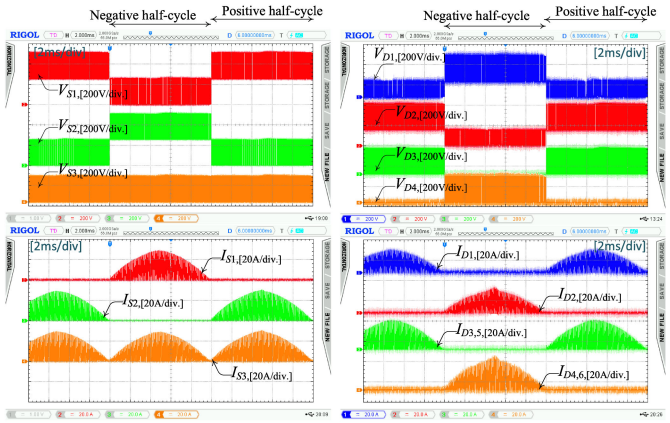

Fig. 16. Voltage and current waveforms of switches and diodes.

i_o as a pure sinusoid. As shown in Figs. 11 and 12, the simple dead-beat instantaneous power controller achieves this goal.

VI. Experimental Verification

To confirm the feasibility of the proposed common ground PV inverter, a laboratory hardware prototype shown in Fig. 13 has been implemented. The specifications of the proposed converter and component parameters are presented in Table II.

Fig. 14(a) illustrates the performance of the proposed converter grid connected, under unity power factor mode, steady-state operation, and with output power references of 500 W and 0 Var. It can be seen that the input PV side voltage is 100 V and the current of the grid is 4.54 A. Fig. 14(b) and (c) shows the steady-state operation under 0.8 lagging and leading

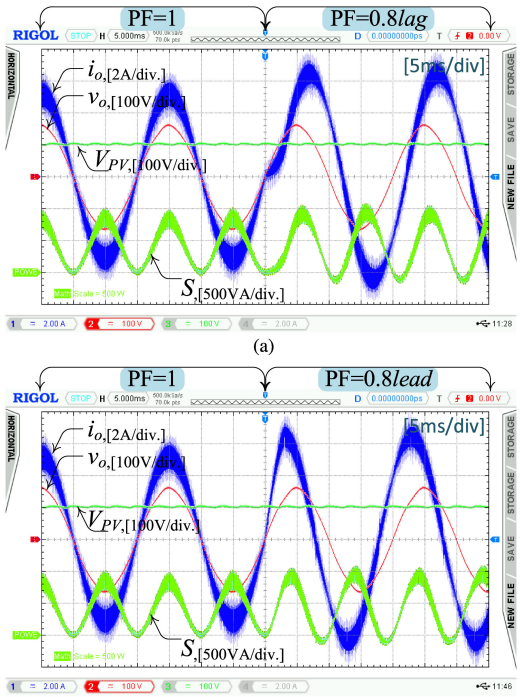

Fig. 17. Transient waveforms from unity to (a) 0.8 lagging and (b) 0.8 leading power factors.

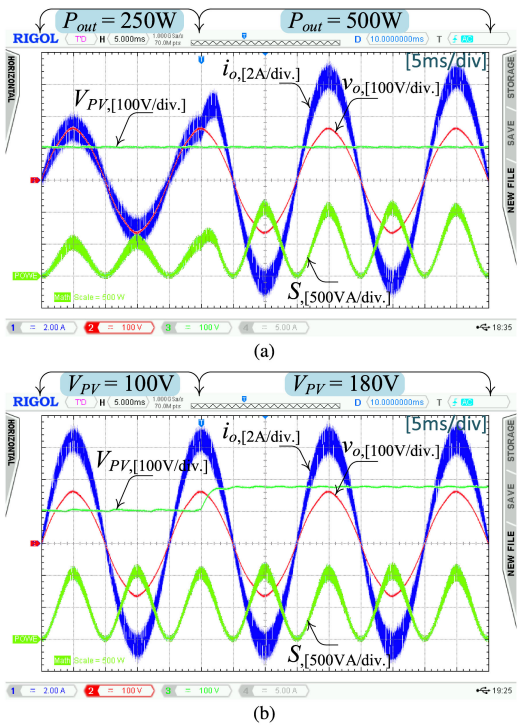

Fig. 18. Transient waveforms in response to (a) step power jump from half-load to full-load and (b) V_{PV} jump from 100 to 180 V.

power factor, respectively (or 400 W and ±300 Var as the output power references). It is clear from Fig. 14 that TSCG generates highly sinusoidal current even considering that the grid voltage is somewhat harmonically distorted.

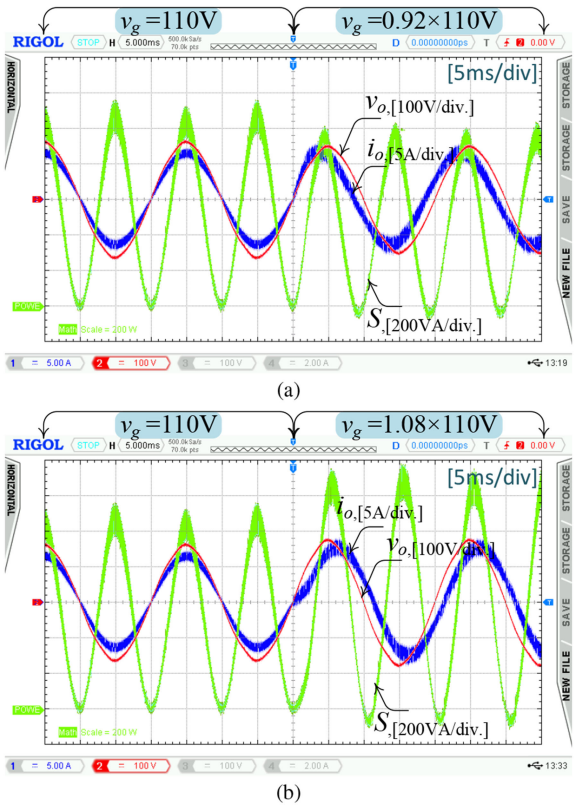

Fig. 19. Waveforms of operation performance based on volt-var setting of IEEE 1547 for (a) +0.08 and (b) −0.08 changes of the grid voltage.

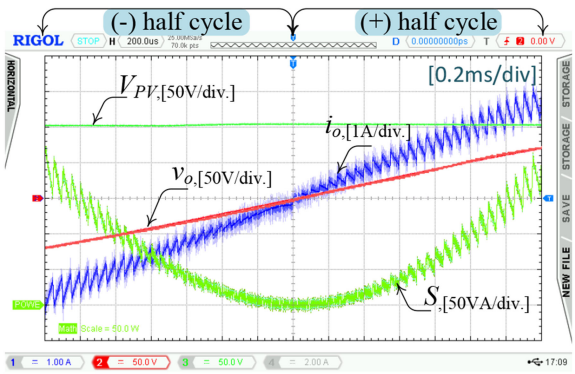

Fig. 20. Zoomed-in view of transient from negative to positive half cycles.

The voltage and current of the passive and active components are shown in Figs. 15 and 16, respectively. These waveforms validate the operation principle of the proposed converter which is explained in detail in Section III.

The DCM operation of TSCG during the positive and the negative half cycles are shown in Fig. 15. The values of $V_{C1,2}$, $V_{\rm PV}$, and v_o with respect to D, d_1, and d_2 confirm the DCM voltage gains of (10) and (20).

The transient performance of the proposed PWM and control system has been investigated experimentally and the results are shown in Fig. 17. A fast and smooth transient response from unity power factor to 0.8 lagging is shown in Fig. 17(a) and from unity power factor to 0.8 leading is shown in Fig. 17(b).

The transient response to a step change in the reference output power and the PV side dc voltage are presented in Fig. 18(a) and (b), respectively. Clearly, a fast-dynamic current performance is achieved and the step change in the PV voltage has almost no effect on the output current waveform. This verifies that the DP-DBC controller, as already expected, offers a high dynamic performance in response to any changes in the references, inputs, and other disturbances.

As already mentioned, the proposed converter should be capable of following the volt-var setting of IEEE 1547. Fig. 19 shows the performance of the proposed converter and control system when the grid side voltage is increased or decreased by ±0.08 of rated voltage. Based on the volt-var setting, the proposed converter injects or absorbs 44% of the nameplate power when the grid voltage level is decreased or increased, respectively. In this case, grid voltage has been increased and decreased to 118.8 and 101.2 $V_{\rm rms}$, respectively; therefore, the proposed converter absorbs and injects 220 Var to the ac grid.

With a closer look at the current waveform, one can detect a very smooth mode transition from the negative to positive half cycle as shown in Fig. 20. This ensures that the total harmonic distortion (THD) of the proposed converter current remains lower than 5%, and, in fact, the THD of injected grid side current is 3.2%. Fig. 21(a) and (b) shows the zoomed-in view of the grid side current and instantaneous power for 0.8 lagging and leading power factors, respectively. Again the grid

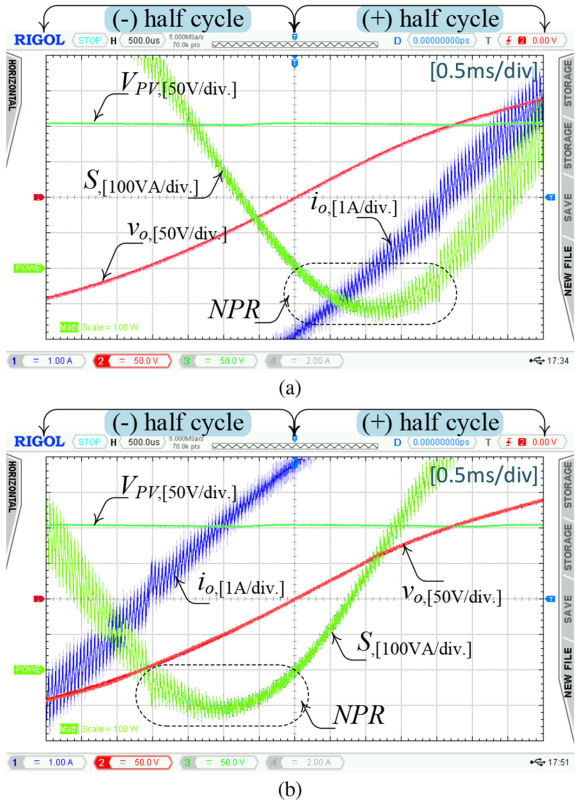

Fig. 21. NPR of (a) lagging and (b) leading power factor.

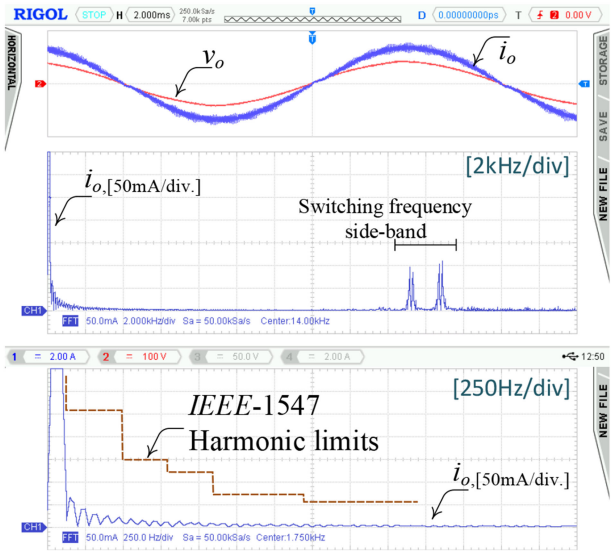

Fig. 22. Harmonic spectrum of the grid side current at the rated power.

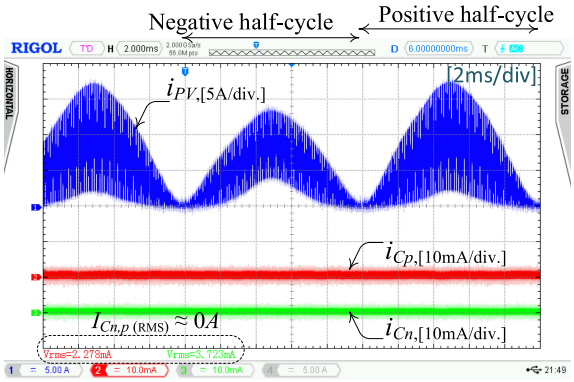

Fig. 23. Leakage and the PV side current waveforms.

current experiences a negligible distortion at transitions from the negative to the positive half cycles of current and in the NPR regions. The measured grid side current harmonic spectrum under rated output power level is shown in Fig. 22. Clearly, the grid current harmonic components are lower than IEEE 1547 limitations.

Based on the approach used in [10] and [21], the measured leakage current waveform through the parasitic capacitors at the positive (C_p) and negative (C_n) terminals of the PV side are shown in Fig. 23. As we expect, the leakage current of the proposed common ground inverter is zero.

Measured peak efficiencies of 96.8% and 97.5% are achieved for the proposed converter when $V_{\rm PV} = 100$ and 180 V, respectively, and these peak efficiencies occur at 300 W loading which can be seen from Fig. 24(a). The power loss breakdown of the proposed converter at the rated power is presented in Fig. 24(b). It can be seen that a large portion of the losses is attributed to the power loss of $S_{1,2,3}$.

The sensitivity analysis based on the mismatch of inductance value (i.e., ΔL_f) and THD of the injected current is shown in Fig. 25. As can be seen in this figure, even while considering

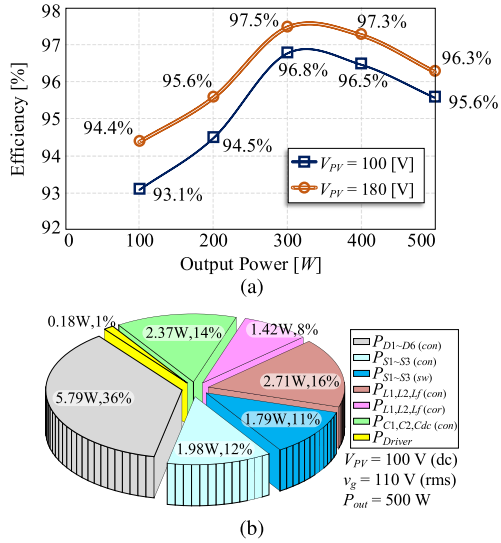

Fig. 24. Proposed converter. (a) Efficiency curve. (b) Loss break down.

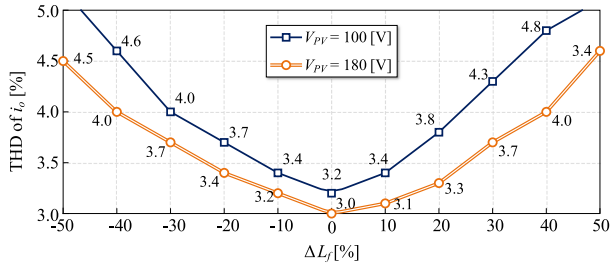

Fig. 25. THD of i_o versus the mismatch value of L_f.

$\pm 50\%$ error in the estimated value of L_f, the proposed converter performs as well as a standard grid connected inverter.

VII. Conclusion

In this article, the first TSCG PV inverter with the capability of supporting reactive power provision to the ac grid is presented. This converter also has the benefits of using a low number of active switches. The proposed converter has utilized a direct power dead-beat controller which ensures smooth and accurate control for the grid side power. Active and reactive power regulation has been successfully demonstrated using the developed prototype. The prototype converter has a maximum efficiency of 97.5% and 96.8% at $V_{\rm dc} = 180$ and 100 V, $V_{\rm rms} = 110$ V, $P_{\rm out} = 500$ W, and $f_s = 20$ kHz. The measured waveforms from the prototype have validated the analysis and operation of the proposed converter. The advantages of the proposed converter in terms of common grounding, consequent mitigation of the leakage current issue, and supporting reactive power to the ac grid by using of only three active switches makes it a versatile topology compared to previously published converters. The use of more diodes or passive components is a drawback for the proposed converter. However, the lower active switch count means that the proposed converter can be implemented with a lower complexity control

system, and a lower count of auxiliary driver circuits and fault protection circuits, and a lower switching losses.

REFERENCES

[1] R. Teodorescu, M. Liserre, and P. Rodriguez, *Grid Converters for Photovoltaic and Wind Power Systems*. New York, NY, USA: Wiley, 2011.

[2] K. Alluhaybi, I. Batarseh, and H. Hu, "Comprehensive review and comparison of single-phase grid-tied photovoltaic microinverters," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1310–1329, Jun. 2020.

[3] Y. Chen, D. Xu, and J. Xi, "Common-mode filter design for a transformerless ZVS full-bridge inverter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 2, pp. 405–413, Jun. 2016.

[4] *Safety of Power Converters for Use in Photovoltaic Power Systems—Part 2: Particular Requirements for Inverters*, IEC International Standard 62109-2:2011, 2011.

[5] H. Xiao and X. Wang, *Transformerless Photovoltaic Grid-Connected Inverters*. Singapore: Springer, 2021.

[6] H. Xiao, "Overview of transformerless photovoltaic grid-connected inverters," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 533–548, Jan. 2021.

[7] *IEEE Standard for Interconnection and Interoperability of Distributed Energy Resources With Associated Electric Power Systems Interfaces*, IEEE Standard 1547:2018, 2018.

[8] K. Dietrich, "German Patent Wechselrichter," Patent DE 19 642 522 (C1), Apr. 1998.

[9] Y. Gu, W. Li, Y. Zhao, B. Yang, C. Li, and X. He, "Transformerless inverter with virtual dc bus concept for cost-effective grid-connected PV power systems," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 793–805, Feb. 2013.

[10] M. Tofigh Azary, M. Sabahi, E. Babaei, and F. Abbasi Aghdam Meinagh, "Modified single-phase single-stage grid-tied flying inductor inverter with MPPT and suppressed leakage current," *IEEE Trans. Ind. Electron.*, vol. 65, no. 1, pp. 221–231, Jan. 2018.

[11] N. Gao *et al.*, "MOSFET-switch-based transformerless single-phase grid-tied inverter for PV systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi: 10.1109/JESTPE.2021.3064587.

[12] A. Kumar and P. Sensarma, "New switching strategy for single-mode operation of a single-stage buck-boost inverter," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5927–5936, Jul. 2018.

[13] J. F. Ardashir, M. Sabahi, S. H. Hosseini, F. Blaabjerg, E. Babaei, and G. B. Gharehpetian, "A single-phase transformerless inverter with charge pump circuit concept for grid-tied PV applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5403–5415, Jul. 2017.

[14] Y. P. Siwakoti and F. Blaabjerg, "Common-ground-type transformerless inverters for single-phase solar photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 65, no. 3, pp. 2100–2111, Mar. 2018.

[15] X. Xu, M. Su, Y. Sun, B. Guo, H. Wang, and G. Xu, "Four-switch single-phase common-ground PV inverter with active power decoupling," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 3223–3228, Mar. 2022.

[16] A. Sarikhani, M. M. Takantape, and M. Hamzeh, "A transformerless common-ground three-switch single-phase inverter for photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8902–8909, Sep. 2020.

[17] Z. Yao, Y. Zhang, and X. Hu, "Transformerless grid-connected PV inverter without common mode leakage current and shoot-through problems," *IEEE Trans. Circuits Syst. II*, vol. 67, no. 12, pp. 3257–3261, Dec. 2020.

[18] Z. Yao and Y. Zhang, "A doubly grounded transformerless PV grid-connected inverter without shoot-through problem," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 6905–6916, Aug. 2021.

[19] Y. Xia, J. Roy, and R. Ayyanar, "A single stage common ground three-level PV inverter with integrated power decoupling," *IEEE Open J. Power Electron.*, vol. 1, pp. 227–237, Jul. 2020.

[20] P. K. Chamarthi, M. S. El Moursi, V. Khadkikar, K. H. A. Hosani, and T. H. M. El-Fouly, "Novel step-up transformerless inverter topology for 1-ϕ grid-connected photovoltaic system," *IEEE Trans. Ind. Appl.*, vol. 57, no. 3, pp. 2801–2815, May/Jun. 2021.

[21] N. Vosoughi, S. H. Hosseini, and M. Sabahi, "A new single-phase transformerless grid-connected inverter with boosting ability and common ground feature," *IEEE Trans. Ind. Electron.*, vol. 67, no. 11, pp. 9313–9325, Nov. 2020.

[22] J. Jiang, S. Pan, J. Gong, F. Liu, X. Zha, and Y. Zhuang, "A leakage current eliminated and power oscillation suppressed single-phase single-stage nonisolated photovoltaic grid-tied inverter and its improved control strategy," *IEEE Trans. Power Electron.*, vol. 36, no. 6, pp. 6738–6749, Jun. 2021.

[23] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Berlin, Germany: Springer International Publishing, 2020.

[24] H. Heydari-doostabad, R. Keypour, M. R. Khalghani, and M. H. Khooban, "A new approach in MPPT for photovoltaic array based on extremum seeking control under uniform and non-uniform irradiances," *Sol. Energy*, vol. 94, pp. 28–36, 2013.

[25] H. Akagi, E. H. Watanabe, and M. Aredes, *Instantaneous Power Theory and Applications to Power Conditioning*. New York, NY, USA: Wiley, 2017.

[26] J. Rodriguez and P. Cortes, *Predictive Control of Power Converters and Electrical Drives*. New York, NY, USA: Wiley, 2012.

[27] M. A. Abbaszadeh, M. Monfared, and H. Heydari-doostabad, "High buck in buck and high boost in boost dual-mode inverter (Hb2DMI)," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4838–4847, Jun. 2021.

[28] H. Heydari-doostabad and M. Monfared, "An integrated interleaved dual-mode time-sharing inverter for single-phase grid-tied applications," *IEEE Trans. Ind. Electron.*, vol. 66, no. 1, pp. 286–296, Jan. 2019.

[29] S. H. Hosseini, R. Ghazi, and H. Heydari-Doostabad, "An extendable quadratic bidirectional DC-DC converter for V2G and G2V applications," *IEEE Trans. Ind. Electron.*, vol. 68, no. 6, pp. 4859–4869, Jun. 2021.

[30] A. Pourfaraj, M. Monfared, and H. Heydari-doostabad, "Single-phase dual-mode interleaved multilevel inverter for PV applications," *IEEE Trans. Ind. Electron.*, vol. 67, no. 4, pp. 2905–2915, Apr. 2020.

[31] H. Heydari-doostabad and R. Ghazi, "A new approach to design an observer for load current of UPS based on Fourier series theory in model predictive control system," *Int. J. Electr. Power Energy Syst.*, vol. 104, pp. 898–909, Jan. 2019.

[32] H. Heydari-doostabad, S. H. Hosseini, R. Ghazi, and T. O'Donnell, "Pseudo dc-link EV home charger with a high semiconductor device utilization factor," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2459–2469, Mar. 2022.

[33] H. Heydari-doostabad and T. O'Donnell, "A wide range high voltage gain bidirectional DC-DC converter for V2G and G2V hybrid EV charger," *IEEE Trans. Ind. Electron.*, vol. 69, no. 5, pp. 4718–4729, May 2022.

[34] H. Heydari-doostabad, M. R. Khalghani, and M. H. Khooban, "A novel control system design to improve LVRT capability of fixed speed wind turbines using STATCOM in presence of voltage fault," *Int. J. Electr. Power Energy Syst.*, vol. 77, pp. 280–286, May 2016.

[35] M. Pourmahdi, H. Heydari-doostabad, R. Ghazi, and T. O'Donnell, "Buck-boost common ground bridgeless PFC (CGBPFC) rectifies with positive/negative output," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1272–1282, Feb. 2022.