Systematic Analysis and Characterization of Extreme Failure for IGCT in MMC-HVdc System—Part I: Device Structure, Explosion Characteristics, and Optimization

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***Abstract*—Explosion proof of power devices is important for the safe operation of high voltage direct current power transmission system based on modular multilevel converter (MMC-HVdc). Comparison of the main commercial power devices' structures shows that the integrated gate commutated thyristor (IGCT) has the simplest housing structure, which is suitable for withstanding the extreme fault in the MMC-HVdc system. Explosion proof tests of IGCT are carried out with different distribution of destruction positions under the extreme failure in the MMC-HVdc system. The maximum surge current of IGCT is between 600 and 700 kA when 18 mF capacitor with 4500 V is discharged. IGCT with evenly distributed destruction positions shows excellent explosion proof, while IGCT with edge focusing destruction positions shows poor explosion proof. Further thermal analysis with simulation shows that IGCT's ceramic shell may suffer a huge transient thermal stress when the destruction positions focus on the edge areas. A designed gas pressure tolerance test shows that the gas pressure is in the safe area which IGCT can withstand under the extreme failure. This means that the thermal stress can be regarded as the main cause of IGCT's explosion phenomenon. Based on the explosion mechanism, an optimized IGCT with controlled punch-through design in the central area is proposed to avoid the edge area destruction under the extreme failure. And explosion proof experiment of optimized IGCT validates its excellent explosion proof under the extreme failure in the MMC-HVdc system.**

***Index Terms*—Device structure, explosion characteristics, extreme failure, integrated gate commutated thyristor (IGCT), modular multilevel converter (MMC), optimization.**

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I. Introduction

THE technology of high voltage direct current power transmission system based on modular multilevel converter (MMC-HVdc) is applied widely in recent years [1], [2]. And the reliability and safety are very important for MMC-HVdc system. During the operation of the MMC-HVdc system, a kind of extreme fault may happen when the faulty submodule loses control totally. The extremely high fault current brings great challenge for the explosion proof design of the devices.

In the early MMC-HVdc projects, the insulated gate bipolar transistor (IGBT), especially the plastic module IGBT (PMI) is commonly applied due to its low cost and loss. However, the explosion proof of PMI cannot be guaranteed, which may affect the safe operation of the MMC-HVdc system [3]–[5]. Considering this problem, recent MMC-HVdc projects adopt press-pack injection enhanced gate transistor (IEGT) or StakPak IGBT widely. And some tests are carried out to verify the explosion proof under large surge current [6]–[8].

Recent years, the integrated gate commutating thyristor (IGCT) becomes a promising high power semiconductor device and attracts much attention in applications of the MMC-HVdc system [9]–[13] due to its lower voltage drop and loss, smaller manufacture cost, and higher reliability compared to IEGT and IGBT [14]–[16]. Besides, IGCT inherits thyristor's advantages like high surge current capability and double-side cooling characteristics. As a result, IGCT is suitable for the application of the MMC-HVdc system [17].

When an MMC submodule loses the controlling of all the power devices and bypass switch due to the controlling communication or hardware failure in the MMC-HVdc system, an extreme fault may happen. During this fault, the voltage of the dc-link capacitor will be charged to a much higher value than the normal working voltage until the power devices break down due to the high overvoltage. Then, the huge energy stored in the capacitor will discharge through the destroyed devices.

The usual solution for the extreme fault in the MMC-HVdc system is using a kind of protection thyristor [18], [19], but the construction cost increases and the controlling becomes more complex. With the technology development of fast recovery

TABLE I
COMPARISON OF THE MAJOR CHARACTERISTICS OF THREE KINDS OF 4.5 kV COMMERCIAL HIGH POWER SEMICONDUCTOR DEVICES

Table head	IGCT	Press-pack IEGT	StakPak IGBT
Manufacturer	ABB	Toshiba	ABB
Code	5SHY 65L4521	ST3000GXH31A	5SNA 3000K452300
Type	Asymmetric	Asymmetric	Reverse conducting
U_{CES}/U_{DRM}	4.5 kV	4.5 kV	4.5 kV
$I_C/I_{T(D)}$	≥3 kA	3 kA	3 kA
I_{CM}/I_{TGQM}	6.5 kA	6 kA	6 kA
E_{on}	2.5 J	12 J	15.5 J
E_{off}	17 J	20 J	15.1 J
Test condition (E_{on}, E_{off})	V_{DC}=2.8 kV, $I_{T(D)}$=3 kA, Tvj= 140 °C	V_{DC}=2.8 kV, I_C=3 kA, Tvj= 150 °C	V_{DC}=2.8 kV, I_C=3 kA, Tvj= 125 °C
$V_{on\text{-}state}$	1.8 V	2.6 V	3.65 V
Test condition ($V_{on\text{-}state}$)	$I_{T(D)}$=3 kA, Tvj= 140 °C	I_C=3 kA, U_{GE}=15 V, Tvj= 150 °C	I_C=3 kA, U_{GE}=15 V, Tvj= 125 °C
Surge current	High	Low	Low
Drive power	High	Low	Low

diode (FRD) [20], the protection thyristor can be saved in IGCT-based MMC-HVdc system. In this situation, the lower IGCT needs to guarantee the explosion proof under the extreme failure in the MMC-HVdc system. However, due to lack of understanding of the mechanism of IGCT's explosion mechanism, the explosion characterization of IGCT under the extreme failure in the MMC-HVdc system has not been clarified.

Considering the situation above, this article gives the systematic analysis and characterization of IGCT's explosion proof under the extreme failure in the MMC-HVdc system. Section II analyzes the characteristics of IGCT for the MMC-HVdc system and introduces the extreme failure in IGCT based MMC-HVdc system. Section III gives the basic operating principle of IGCT and its structure, as well as the comparison with IEGT and IGBT's structures. Section IV gives IGCT's explosion characteristics with different distribution of destruction positions under extreme failure in the MMC-HVdc system. Section V proposes the explosion mechanism of IGCT under extreme failure in the MMC-HVdc system based on the thermal and gas pressure analysis. Section VI proposes a kind of optimized IGCT with a controlled punch-through area in the center based on the explosion mechanism and gives experiment validation of optimized IGCT's excellent explosion proof under the extreme failure in the MMC-HVdc system. Finally, Section VII concludes this article.

II. EXTREME FAILURE IN IGCT BASED MMC-HVDC SYSTEM

A. Characteristics of IGCT and Comparison With IEGT, IGBT

With the development of renewable energy sources such as onshore and offshore wind farms, MMC technology with large capacity becomes one of the best solutions for the flexible HVdc transmission. As a result, press-pack devices with higher blocking voltage and ON-state current level are preferred instead of PMIs in the MMC system with large capacity. There are mainly three kinds of high-power press-pack devices which are suitable for MMC-HVdc application, including IGCT, press-pack IEGT, and StakPak IGBT. Detailed characteristics of the devices with 4.5 kV rated blocking voltage are compared in Table I and the photographs of them are shown in Fig. 1.

Till now the maximum turn-OFF current (I_{TGQM}) of the commercial 4-inch IGCT is 6.5 kA with 4.5 kV blocking voltage (U_{DRM}). The turn-ON loss (E_{on}) and turn-OFF loss (E_{off}) are 2.5 and 17 J, respectively, when IGCT works under 3 kA with 2.8 kV dc-link voltage and 140 °C junction temperature. The ON-state voltage ($V_{\mathrm{on\text{-}state}}$) of IGCT is only 1.8 V under 3 kA with the junction temperature of 140 °C. Besides, IGCT has large surge current capability, which means that IGCT can ride through the fault current in some situations. And the inherited manufacture technology from thyristor makes the cost of IGCT lowest among high power devices with similar rated parameters. Though the high power of IGCT's gate driver is one of the shortcomings, the low working frequency in MMC system helps mitigate the negative effects.

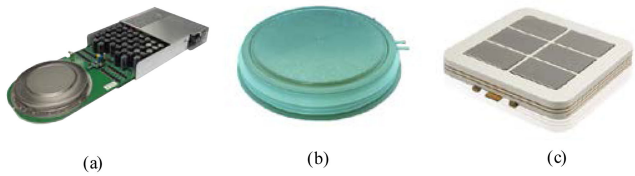

Fig. 1. Photographs of main high-power semiconductors for the MMC-HVdc system. (a) IGCT. (b) Press-pack IEGT. (c) StakPak IGBT.

Compared with IGCT, press-pack IEGT and StakPak IGBT also have large turn-OFF current capability (I_{CM}) with high blocking voltage (U_{CES}). The turn-OFF loss of press-pack IEGT and StakPak IGBT is similar to that of IGCT under 3 kA with 2.8 kV dc-link voltage and their maximum junction temperatures. But their turn-ON loss is obviously larger than that of IGCT due to longer turn-ON time. Another disadvantage of press-pack IEGT and StakPak IGBT is their ON-state voltages with 2.6 and 3.65 V, respectively, which are about 1.5 and 2 times of IGCT's ON-state voltage under the similar test condition. Besides, the surge current capability of press-pack IEGT and StakPak IGBT is low, which means that they may get destroyed under a large fault current.

Based on the contrastive analysis above, IGCT is a promising power device for the MMC-HVdc system due to its high blocking voltage and large current level. Besides, the lower device loss, larger surge current, and smaller manufacture cost compared to IEGT and IGBT make IGCT competitive in the application of the MMC-HVdc system.

B. Analysis of the Extreme Failure in IGCT Based MMC-HVdc System

The typical IGCT-MMC submodule (IGCT-SM) based on the half-bridge topology is illustrated in Fig. 2. For IGCT-SM,

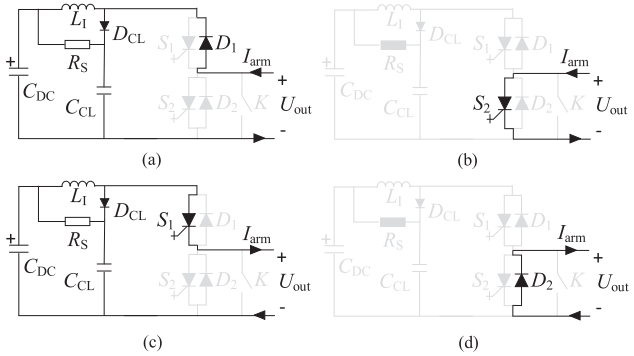

Fig. 2. Illustration of current paths during IGCT-SM's different operation states. (a) $I_{\rm arm} > 0$ and $U_{\rm out} > 0$. (b) $I_{\rm arm} > 0$ and $U_{\rm out} \approx 0$. (c) $I_{\rm arm} < 0$ and $U_{\rm out} > 0$. (d) $I_{\rm arm} < 0$ and $U_{\rm out} \approx 0$.

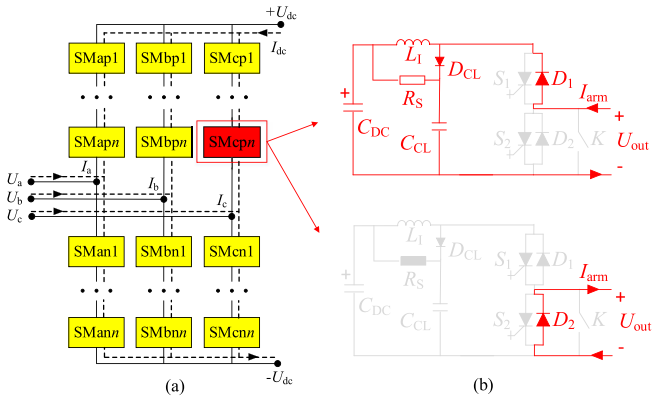

Fig. 3. Illustration of the extreme failure in IGCT-SM. (a) Schematic of IGCT based MMC system and the IGCT-SM which loses control of S_1, S_2, and K. (b) Current paths in the IGCT-SM which loses control of S_1, S_2, and K.

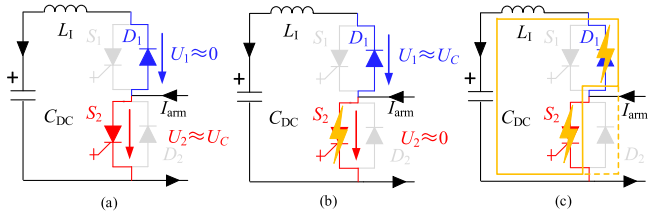

Fig. 4. Illustrative diagram of IGCT-SM's shooting through process under the extreme failure. (a) Right before the occurrence of S_2's breakdown. (b) Instant after S_2's breakdown. (c) Oscillation process after D_1's breakdown.

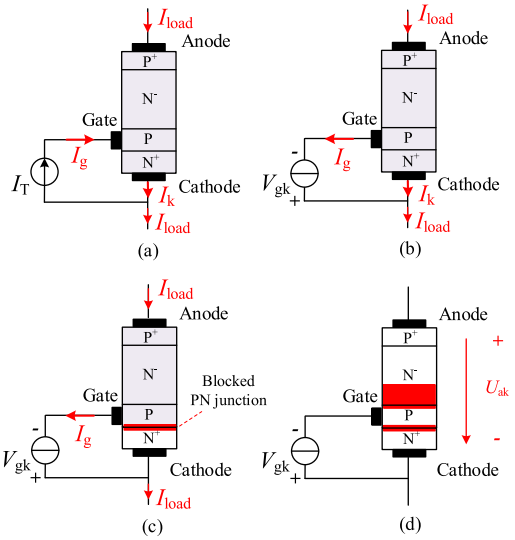

Fig. 5. Illustration of IGCT's operating principle. (a) Current paths during turn-ON process of IGCT. (b) Current paths during commutating process of IGCT. (c) Current paths of the PNP transistor structure in IGCT. (d) Blocking state after turn-OFF process of IGCT.

S_1 and S_2 are IGCTs, meanwhile D_1 and D_2 are freewheeling diodes matched with S_1 and S_2. $C_{\rm DC}$ is the dc-link capacitor. $L_{\rm I}$ is the anode inductor, which is used to protect D_1 and D_2 from being destroyed by the high di/dt rate during the reverse recovery period. $D_{\rm CL}$, $R_{\rm S,}$ and $C_{\rm CL}$ make up the clamping circuit, which is used to limit the overvoltage caused by $L_{\rm I}$ when IGCT turns OFF. K represents the bypass switch of IGCT-SM. $I_{\rm arm}$ represents the arm current and $U_{\rm out}$ represents the output voltage of IGCT-SM. According to the directions of $I_{\rm arm}$ (the direction flowing into IGCT-SM is prescribed as positive) and $U_{\rm out}$, the operation states of IGCT-SM can be divided into four modes. The current paths of these operation states are shown in Fig. 2(a)–(d).

The voltage of $C_{\rm DC}$ is usually controlled at a stable level through certain operating mode controlling strategies among different IGCT-SMs in the whole MMC system. The strategies depend on the controlling of S_1 and S_2 in the IGCT-SMs. When an IGCT-SM loses the controlling of S_1, $S_{2,}$ and K in the worst case due to the communication or hardware failure, $I_{\rm arm}$ can only conduct through D_1 or D_2, as shown in Fig. 3. $U_{\rm a}$, $U_{\rm b}$, and $U_{\rm c}$ represent the voltages of MMC system's ac-side, while $I_{\rm a}$, $I_{\rm b,}$ and $I_{\rm c}$ represent the ac currents. $U_{\rm dc}$ represents the voltage of MMC system's dc-side and $I_{\rm dc}$ represents the dc current. When this failure happens, $C_{\rm DC}$'s voltage $U_{\rm C}$ will be increased continuously by $I_{\rm arm}$ through D_1. It is noticed S_2's voltage U_2 is nearly $U_{\rm C}$ because D_1 is conducting and D_1's voltage U_1 is nearly zero, as shown in Fig. 4(a). When U_2 increases, S_2 will break down at the voltage which is higher than its rated blocking voltage. After that, D_1 will experience the reverse recovery process and $U_{\rm C}$ is almost suffered by D_1, as shown in Fig. 4(b). However, this exceeds D_1's safe operation area and D_1 will break down immediately after S_2. Finally, a dangerous shoot-through fault forms with destroyed D_1 and S_2 and the main discharging loop of $C_{\rm DC}$ is shown in Fig. 4(c). After this extreme failure, IGCT-SM will mainly be bypassed by D_2 and the destroyed S_2.

During the extreme failure, IGCT must withstand a large fault current without any crack of the housing package to ensure the safe operation of the whole system. And this brings great challenge for the design of IGCT.

III. Device Structure of IGCT

A. Operating Principle of IGCT

IGCT is improved from the thyristor, which is controlled by an integrated gate driver. The operating principle is illustrated in Fig. 5. When IGCT turns ON, the gate driver performs like a current source and applies the trigger current $I_{\rm T}$ at the gate

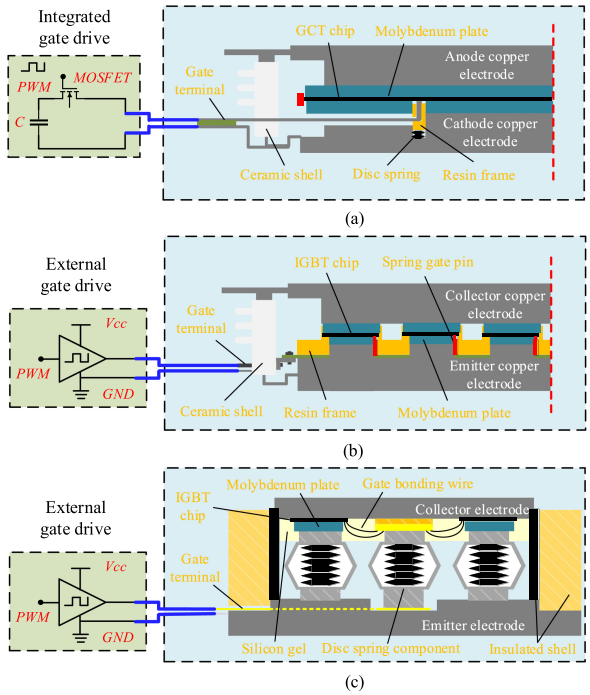

Fig. 6. Cross-sectional structures of main high power semiconductor devices. (a) Structure of IGCT. (b) Structure of press-pack IEGT. (c) Structure of StakPak IGBT.

terminal. Then I_{T} will stimulate the co-amplification effects of PNP and NPN structures in IGCT. Then, IGCT can conduct the load current I_{load} with rather low impedance. Fig. 5(a) shows the current path when IGCT turns ON, including I_{load}, the gate current I_{g}, and the cathode current I_{k}. When IGCT turns OFF, the gate driver performs like a voltage source and applies the reverse voltage V_{gk} between the gate and cathode terminals. Then, I_{k} is commutated to the gate terminal in rather short time with the help of V_{gk}, as shown in Fig. 5(b). After the commutation process, the PN+ junction between the gate and cathode terminals is reverse biased and the PNPN thyristor structure in IGCT is converted to the PNP transistor structure, as shown in Fig. 5(c). The PNP transistor cannot sustain I_{load} singly and it will turn OFF gradually with the building of IGCT's anode—cathode voltage U_{ak}, which is shown in Fig. 5(d). Then, the turn OFF process of IGCT is completed.

B. Structure of IGCT and Comparison With IEGT, IGBT

Fig. 6(a) shows the cross-sectional structure of IGCT and Fig. 7(a) gives the detailed illustration based on the decomposed device. As shown in Fig. 6(a), IGCT is composed of the integrated gate driver, the housing package components, and the internal GCT chip. The GCT chip is a whole wafer with thousands of GCT cells arranged in concentric circles on its surface, which forms the cathode working area and flow the working current, as shown in Fig. 7(a). The GCT chip is in the middle, with the cathode and anode molybdenum plates on its both sides and the molybdenum plates have similar thermal expansion coefficient with silicon as well as low resistance. Then they are in contact with the anode and cathode copper electrodes, forming a sandwich-like structure. The gate area of the GCT chip is an annular area in the middle position and an annular gate terminal is lead out of the housing package through a special designed gate contacting metal ring with disc springs below. Due to the insulation and moisture-proof considerations, an annular ceramic shell with pleated skirt design is used to connect the anode electrode, the gate terminal, and the cathode electrode. After the housing package is sealed and filled with insert gas, the inside area forms an isolated area. Finally, the gate terminal of the housing package is tightly connected with the integrated gate driver.

Different from IGCT integrated with a gate driver, IGBT (including press-pack IEGT and StakPak IGBT) is usually matched with an external gate drive. Another significant difference is that the IGBT chip is hard to be made on a single wafer due to its high requirement to the manufacture process. As a result, there are many independent IGBT chips paralleled inside a device and these IGBT chips work together to guarantee the working current capability. However, there are differences in the detailed structures of these two kinds of devices though multiple IGBT chips are packaged.

Fig. 6(b) shows the cross-sectional structure of press-pack IEGT and Fig. 7(b) gives the detailed illustration based on the decomposed device. In press-pack IEGT, each IGBT chip is matched with a single collector molybdenum plate and a single emitter molybdenum plate. Then, the molybdenum plates are in contact with the anode and cathode copper electrodes, forming a similar press-pack structure like IGCT. The gate area is usually at the corner in a single IGBT chip and other areas performing emitter function. All the gate areas are connected to the gate terminal plate through spring gate pins and finally a needle-like gate terminal is lead out of the housing package. Besides, a special resin frame is placed among the IGBT chips to fix and isolate them. Like the design of IGCT, an annular ceramic shell with pleated skirt design is also used to connect the collector electrode and the emitter electrode. After the housing package is sealed and filled with insert gas, the inside area also forms an isolated area.

Fig. 6(c) shows the cross-sectional structure of StakPak IGBT and Fig. 7(c1)–(c3) gives the detailed illustration based on the decomposed device. In StakPak IGBT, the emitter side of each IGBT chip is matched with a special designed disc spring structure besides the molybdenum plate. Compared with press-pack IEGT, these disc spring structures make StakPak IGBT have better tolerance of uneven pressure. And different from the gate connecting methods through spring gate pins in press-pack IEGT, the gate areas of IGBT chips in StakPak IGBT are connected to a conductive plate through the bonding wires, which is similar to the method in plastic module IGBT. The emitter surface of IGBT chips are then covered by the silicon gel to prevent moisture and surface pollution. The collector sides of IGBT chips in StakPak IGBT are soldered to the collector electrode, which can help fix IGBT chips.

Based on the comparison above, the structure of IGCT is simplest, which is composed of only a single chip and

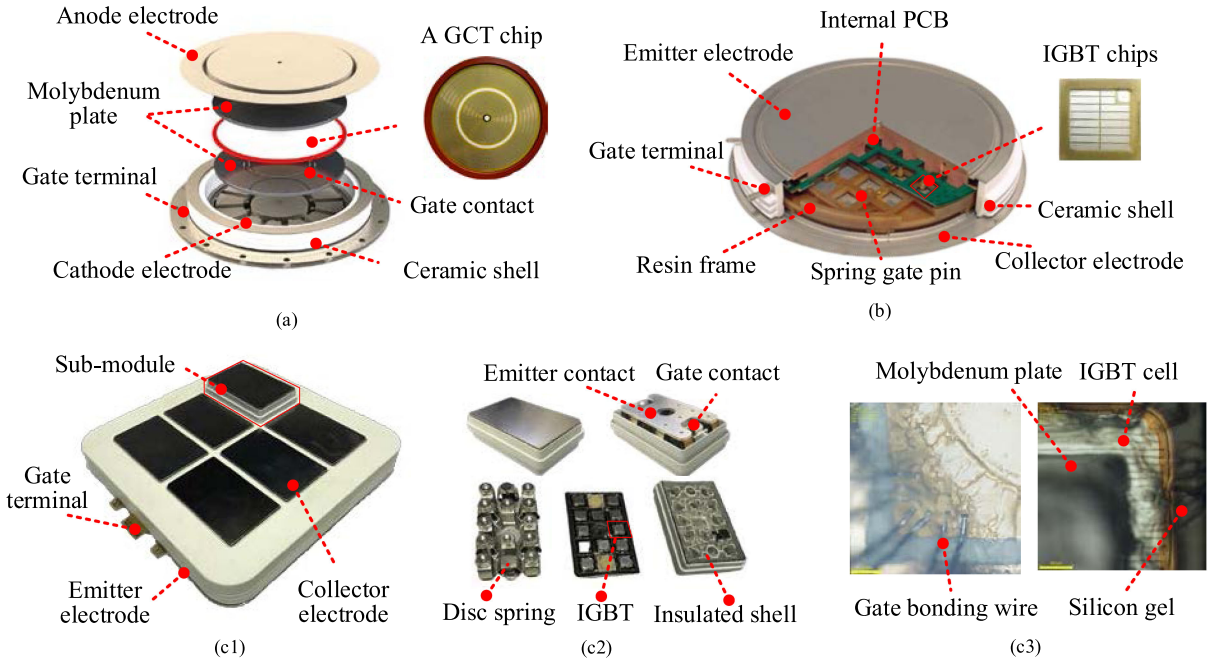

Fig. 7. Detailed illustration based on the decomposed devices. (a) Illustration of an IGCT and the internal GCT chip. (b) Illustration of a press-pack IEGT and the internal IGBT chips. (c1)–(c3) Illustration of a StakPak IGBT and the internal IGBT chips.

several metal plates among three kinds of main high power semiconductor devices. And this structure of IGCT is very suitable for withstanding the extreme fault in MMC-HVdc.

IV. Explosion Characteristics of IGCT Under the Extreme Failure in MMC-HVdc System

To study the explosion characteristics of IGCT under the extreme failure in MMC-HVdc, a test circuit is built to generate the high surge current which is similar to that of the extreme failure. The photograph and circuit schematic diagram of the test platform are shown in Fig. 8. The test platform includes the dc capacitor C_{DC}, the anode inductor L_{I}, the IGCT device under test (DUT), the thyristor *T,* and the discharge switch K_2 which ensures the reliable discharging of C_{DC}. The dc source is connected to C_{DC} through another switch K_1. Besides, a regular monitor and a high-speed camera are placed near the test circuit to ensure the safe experiment and capture the transient photographs when IGCT is destroyed.

A. Evenly Distributed Destruction Positions in IGCT Under the Extreme Failure in MMC-HVdc System

When a MMC submodule loses control totally, the working current will charge the dc capacitor continuously until a conductive loop is formed by the destruction of the lower IGCT in the faulty MMC submodule. Then, the conductive loop helps discharge the energy of the dc capacitor to ensure the safe operation of the MMC system.

To simulate the explosion characteristics of IGCT under the extreme fault, *DUT* and *T* are triggered at the same time when the 18 mF dc capacitor is charged over 4000 V. Fig. 9(a) shows the current and voltage waveforms of the dc capacitor when IGCT

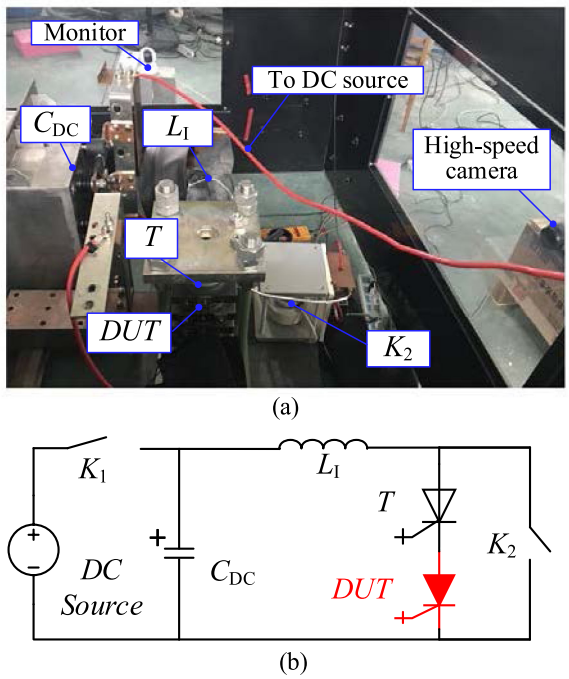

Fig. 8. Illustration of the circuit for testing the explosion proof of IGCT under the extreme failure in the MMC-HVdc system. (a) Photograph of the test system. (b) Circuit schematic diagram of the test system.

is destroyed considering the current limiting effects of the anode inductor in IGCT-MMC submodule, the largest surge current is about 700 kA and the maximum I^2t is about 66.1 $\mathrm{MA^2s}$. After the experiment, the housing package of the destroyed IGCT is well without any crack. The GCT chip inside IGCT shows that there

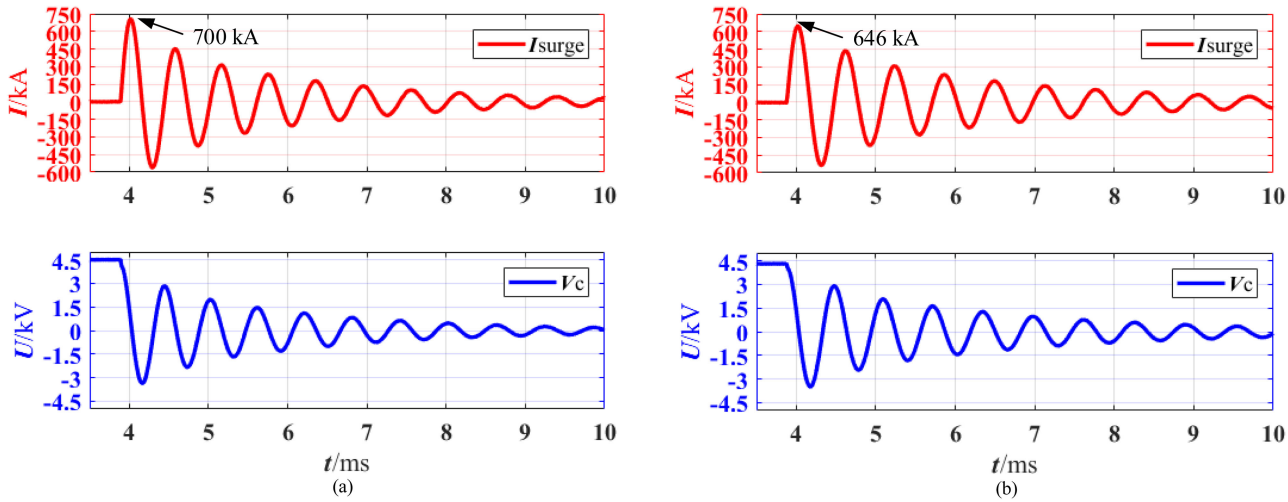

Fig. 9. Current and voltage waveforms of the dc capacitor when IGCT is destroyed. (a) Results of the first tested sample. (a) Results of the second tested sample.

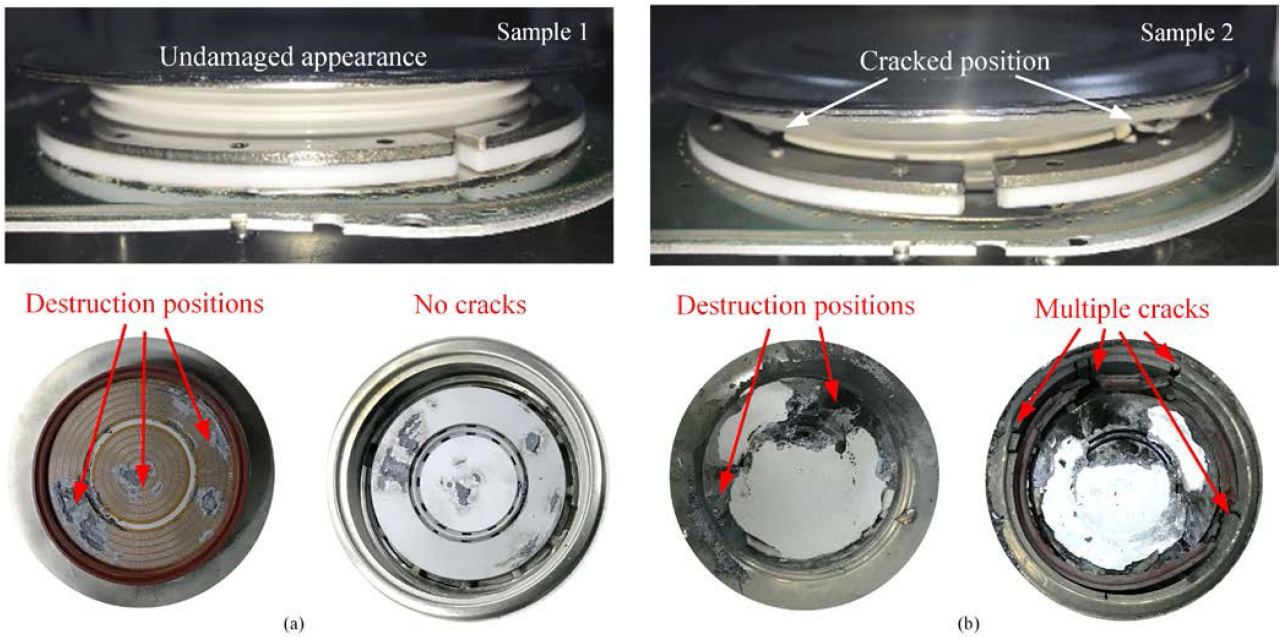

Fig. 10. Comparison of the housing packages' appearances and the destruction positions of the destroyed chips after explosion tests. (a) Photograph of the first tested sample. (b) Photograph of the second tested sample.

exist several destruction positions which are evenly distributed, as shown in Fig. 10(a). This result shows that after the device is triggered, the carriers are evenly distributed in the working GCT cells. As the surge current increases, several positions achieve the thermal limitation at the same time and get melted due to the huge heat.

B. Edge Focusing Destruction Positions in IGCT Under the Extreme Failure in MMC-HVdc System

In another test, a weak area is created at the edge area of *DUT* by a low-energy high-voltage pulse. And a similar surge current is injected to *DUT*. Fig. 9(b) shows that the maximum current of destroyed IGCT is about 646 kA and the maximum I^2t is about 60.5 MA^2s. Different from the first tested IGCT, the housing packages of this IGCT gets cracked. And the destruction positions is focusing in the edge areas of IGCT after test, as shown in Fig. 10(b). It is noted that cracked positions are corresponding to the destruction areas in the chip.

This result shows the possible explosion risks of IGCT under extreme failure in the MMC-HVdc system when IGCT is destroyed without external triggering.

V. Explosion Mechanism of IGCT Under the Extreme Failure in MMC-HVdc System

The explosion phenomenon of IGCT is a complex process which is related to electrical, thermal, chemical, and mechanical

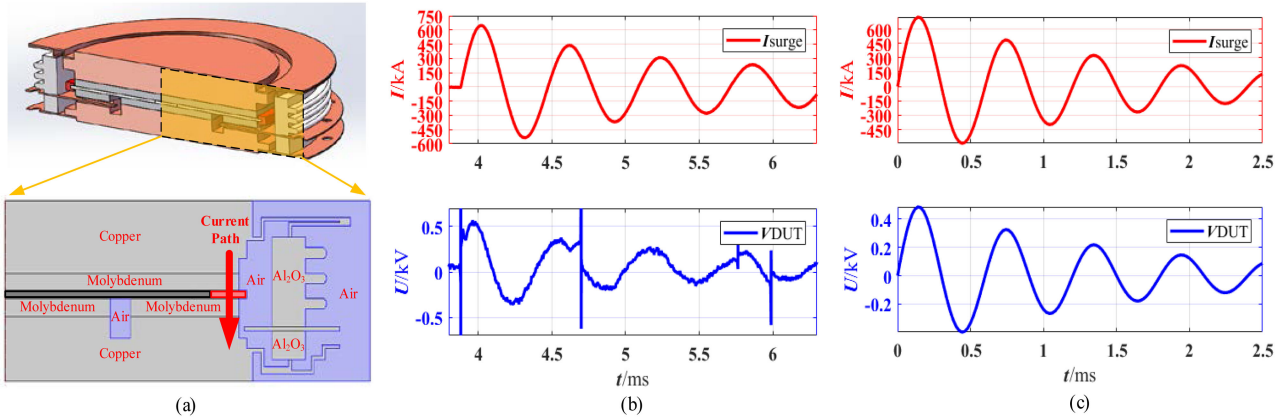

Fig. 11. Proposed 2-D simulation model based on the structure of IGCT. (a) Illustration of the 3-D structure and 2-D cross section of IGCT. (b) Experimental results of IGCT's fault current and voltage. (c) Fitted results of IGCT's fault current and voltage.

factors. Before the housing package of IGCT breaks, the ceramic shell, as the weakest part of the whole housing package, suffers a huge stress which exceeds its stress limit. This huge stress may come from several aspects. First, the surge current which flows through the chips inside the device produces huge heat. Then, the heat transfers to the ceramic shell and causes the temperature rise of the inside surface of the ceramic shell. Due to the poor thermal conductivity of ceramics, there will be a huge temperature gradient in short time and a large thermal stress is produced on the ceramics shell. Besides, during the heat transferring process, some organic materials may be decomposed into carbides and nitrides to add the gas density under high temperature. Meanwhile, the gas inside the device will be heated. As a result, the gas pressure will increase. This pressure stress may be another factor which causes the rupture phenomenon of the housing package. However, the detailed rupture mechanism has not been clarified.

A. *Thermal Stress Analysis of IGCT*

According to the experimental results, the current density distribution may be an important factor for the explosion phenomenon. To verify the transient temperature change on the ceramic shell under different destruction positions, a two-dimensional (2-D) model is built in COMSOL, as shown in Fig. 11(a). The fault current and voltage are estimated as the following formula according to the experiment results, as shown in Fig. 11(b) and (c):

$$I_{\text{surge}} = 800e^{-\frac{t}{0.0015}} \sin\left(\frac{2\pi t}{0.0006}\right)[\text{kA}]. \tag{1}$$

Then, four different destruction positions are simulated to compare the transient temperature change. The results show that the temperature near the ceramics surface changes little when the destruction positions are located inside the chip. And as the destruction positions move toward the edge area of the chip, the temperature change increases. And the increasing thermal stress on the shell may exceed the stress limitation and finally cause the device's rupture. Fig. 12 gives the comparison of temperature changes near the ceramics surface and when the destruction area

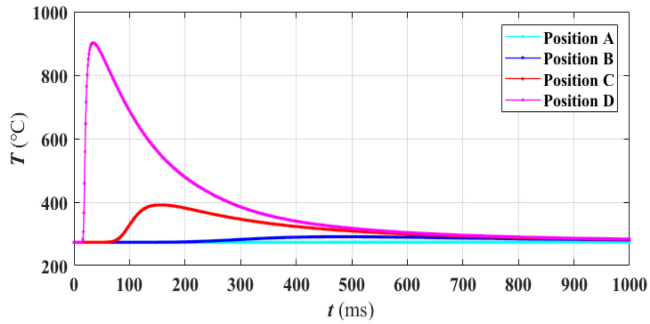

Fig. 12. Temperature changes near the inside surface of the ceramic shell under different destruction positions when IGCT suffers the same surge current and voltage drop under the extremes fault.

is located in the edge area of the chip, the temperature difference is more than 600 °C, which is more than the critical temperature change of the ceramic shell [21].

Fig. 13 gives the comparison of heat diffusion process with different destruction positions in the chip. When the destruction positions are located inside the chip, the transient heat caused by the large surge current can be fully conducted through the molybdenum plates and copper electrodes and the inside gas can obtain little heat. As a result, the temperature change is little near the inside surface of the ceramic shell. While when the destruction positions are in the edge areas of the chip, the huge heat produced by the surge current will spread into the internal gas inside quickly before it is conducted by the molybdenum plates and copper electrodes and a sharp temperature change will happen near the inside surface of the ceramic shell. And when the thermal stress is larger than the intrinsic strength of ceramics, cracks will occur and develop quickly until the ceramic shell collapses.

This result can explain that when IGCT is triggered under the extreme fault, the housing package will maintain stable due to the evenly distributed destruction positions which reduce thermal stress near the inside surface of the ceramic shell. And the focused destruction positions on the edge areas of IGCT will cause great thermal stress on the ceramics shell which causes

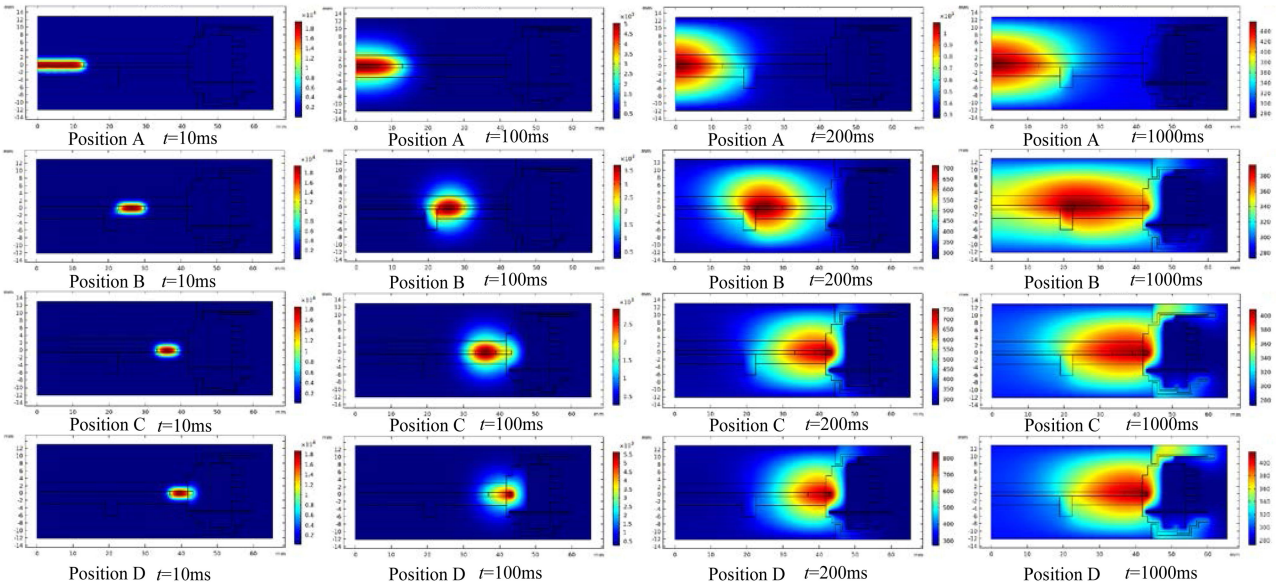

Fig. 13. Comparison of temperature distribution inside IGCT at four time points (10, 100, 200, and 1000 ms) when the destruction positions are different under the same surge current and voltage drop (positions A to D show the destruction areas move from the center area to the edge area).

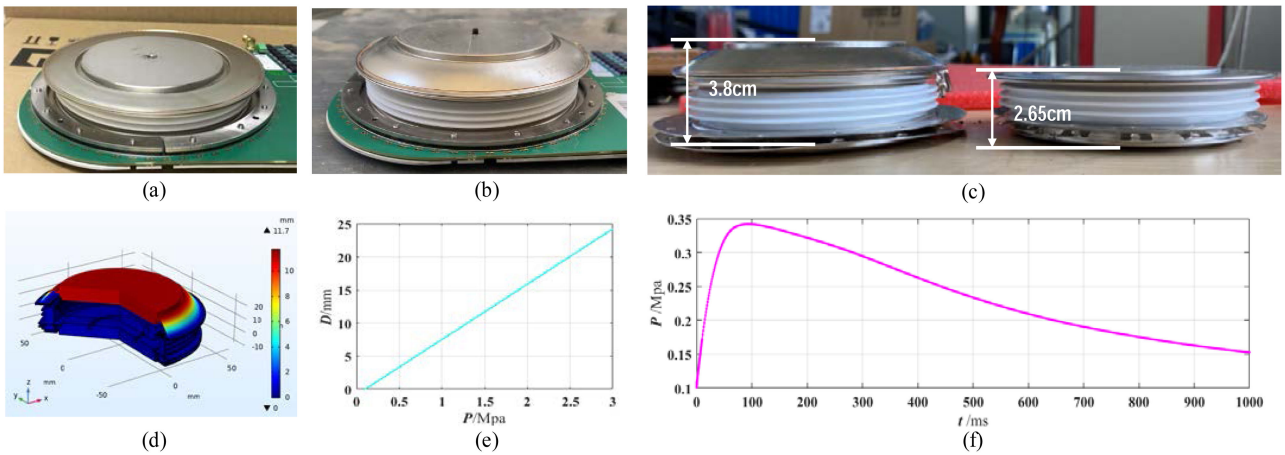

Fig. 14. Gas pressure tolerance test and simulation. (a) Appearance of IGCT before test. (b) Appearance of IGCT after test. (c) Expanded deformation of IGCT after test. (d) 3-D model of IGCT's deformation under gas pressure. (e) Relationship between the expanded deformation and different gas pressures. (f) Changing trends of the gas pressure following time when the destruction area is located in the edge area of IGCT.

the rupture of the ceramics shell part which is corresponding to the destruction positions.

B. Gas Pressure Analysis of IGCT

Another factor which may affect the explosion proof of IGCT is the gas pressure inside. The transient pressure depends on the transient temperature and the amounts of the gas. To verify the effects of the gas pressure on the explosion characteristics of IGCT, a gas pressure tolerance test is carried out using an IGCT housing package. The preinstalled organic resin frame inside IGCT is heated to be decomposed into carbide and nitride gas, which will increase the gas amount inside IGCT.

After 6 h continuous heating, the sample is taken out from the press-fit valve string. The expanded shell compared with the normal shell proves the increase of internal gas in IGCT, as shown in Fig. 14(a) and (b). Although it is difficult to measure the pressure inside IGCT due to its fully sealed structure, the pressure can be estimated from the expansion deformation of the anode electrode, as shown in Fig. 14(c). The expansion deformation simulation is illustrated in Fig. 14(d) and the results in Fig. 14(e) under different pressure show that the housing package of IGCT can withstand more than 1.5 Mpa without rupture after releasing the pressure. Considering the volume changes of the gas inside IGCT, the maximum pressure can achieve more than 2.0 Mpa before releasing the pressure.

C. Explosion Mechanism of IGCT

According to the simulation results in Section V-A, the gas temperature will achieve the largest value when the destruction positions are located in the edge area of the chip. Then, the

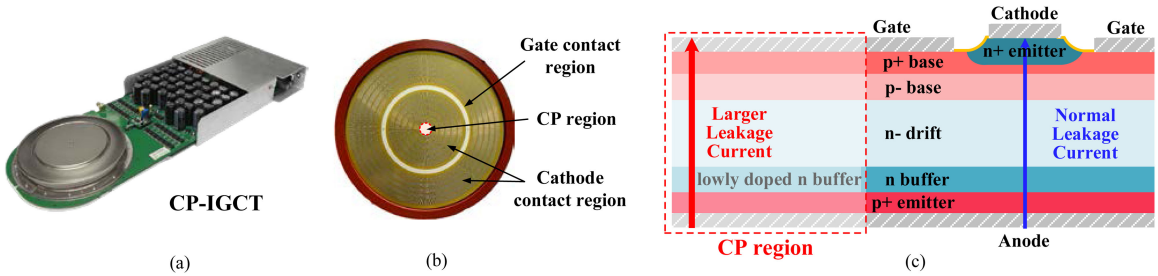

Fig. 15. Illustration of the proposed controlled punch-through IGCT (CP-IGCT). (a) CP-IGCT device. (b) Chip with CP area. (c) Doping design and leakage current path in CP-IGCT.

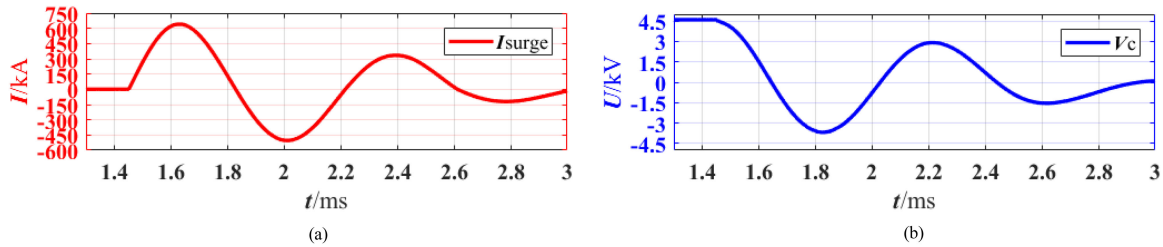

Fig. 16. Results of the extreme failure experiment with the optimized CP-IGCT. (a) Fault current. (b) Voltage of the dc capacitor.

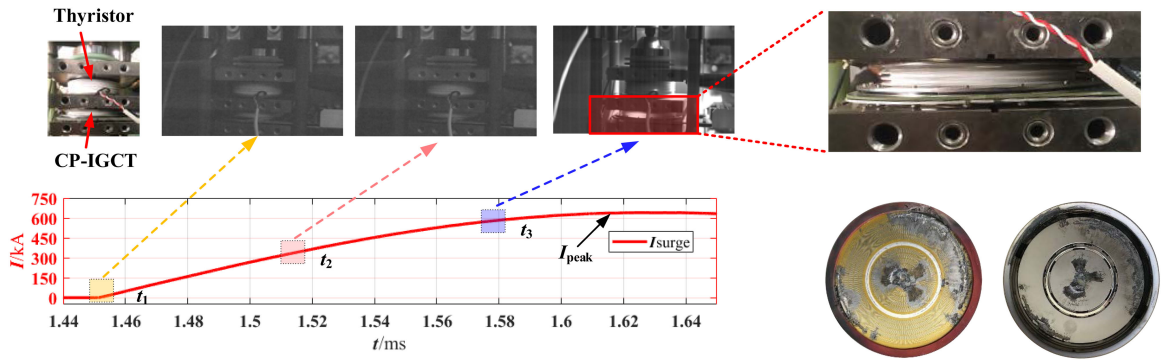

Fig. 17. States of the housing package and inside chips after the shoot-through test of CP-IGCT under the overcharged dc capacitor. (a) Series of photographs taken by the high-speed camera at different time points before the surge current achieves the peak value. (b) Housing package after test. (c) Inside chips.

curve of the gas pressure following the time is plotted when the destruction positions are focused on the edge areas of the device, as shown in Fig. 14(f). It can be noticed that the maximum gas pressure is below 0.35 Mpa, which is lower than the tested gas pressure which IGCT can withstand. This result can prove that the transient thermal stress on the ceramic shell is the main factor of IGCT's explosion proof. Because the transient thermal stress is related to the destruction positions distribution in the chip when IGCT is destroyed, the current distribution of IGCT during the destruction period is a key factor.

VI. Optimization of IGCT's Explosion Proof Under the Extreme Failure in MMC-HVdc System

A. Current Distribution Optimization of IGCT Under the Extreme Failure in MMC-HVdc System

According to the analysis above, the current distribution of IGCT during the destruction period is of vital importance for the explosion proof of IGCT. When IGCT loses control under the extreme failure in the MMC-HVdc system, IGCT cannot be triggered. As a result, a voltage weak point needs to be created in IGCT to ensure the destruction position of the destroyed IGCT. A kind of easy designed way is to create this weak point in the central area of IGCT.

Based on this principle, a controlled punch-through IGCT (CP-IGCT) is brought up with a special design in the central area of GCT chip [22]. The lowly doped n buffer layer in the controlled punch-through area (CP-area) results in larger leakage current than the normal area when the GCT chip is applied around the critical breakdown voltage. Moreover, the critical breakdown voltage of the GCT chip is usually thousands of volts. Thus, the leakage current with hundreds of milliamps can generate several kilowatts of instantaneous power in the central CP-area. Unlike the situation where the whole GCT chip can suffer several kilowatts of power and maintain thermal balance during the ON-state period, the area CP-area only occupies a few percent of the entire chip and the instantaneous power density is quite large. As a result, the central area will achieve the thermal

breakdown limit of silicon lattice in short time. Meanwhile, the situation where the central area breaks down earlier than other areas of the chip can avoid the first destruction of the edge areas of IGCT.

The illustration of the designed CP-IGCT is shown in Fig. 15(a) and (b). The doping design and leakage current path is shown in Fig. 15(c).

B. Experimental Validation of the Explosion Proof of Optimized IGCT Under the Extreme Failure in MMC-HVdc System

To validate the explosion proof of optimized IGCT, the test without triggering signal is carried out under similar conditions. The dc capacitor is charged to about 4500 V and the maximum surge current is over 640 kA and the maximum I^2t is about 77.8 MA^2s, as shown in Fig. 16.

When the IGCT sample is destroyed, the high-speed camera is triggered synchronously for taking series of photographs and the interval between two photographs is about 50 μs. The photograph at t_3 shows that the housing package of the CP-IGCT still remains stable when the surge current is near the peak current, as shown in Fig. 17(a). And Fig. 17(b) shows that the appearance of the CP-IGCT is of no difference compared with the IGCT before test. The destruction positions are focused in the central area, as well as some other inside destruction areas shown in Fig. 17(c).

This means that the central area gets damaged first due to the thermal accumulation caused by the larger leakage current in this area when the device suffers an overvoltage. As a result, the excellent explosion proof of CP-IGCT under the overvoltage fault without triggering is verified.

However, the protection voltage of the controlled breakdown devices (such as the protection thyristor) are limited below 4.5 kV [19] (which is usually around 4.3 or 4.4 kV) to ensure the fully controlled power devices and FRDs will not get destroyed first. Then, the reliable discharging of the over charged capacitor can be realized through the controlled breakdown devices. In fact, the controlled breakdown voltage of the CP region of IGCT can be adjusted during a wide range using different fabrication parameters of the lowly doped n buffer layer [22]. The controlled breakdown voltage can be designed above 4.5 kV. In this situation, the rated voltage of the used fully controlled power devices and FRDs need to be increased to 4.7 kV or higher values.

VII. Conclusion

This article gives the systematic analysis and characterization of IGCT's explosion proof under the extreme failure in the MMC-HVdc system.

During the extreme failure, the device must withstand a large fault current without any crack of the housing package to ensure safety. Comparison of the main commercial power devices shows that IGCT has the simplest structure and is suitable for withstanding the extreme failure in the MMC-HVdc system.

Explosion proof tests show that IGCT with evenly distributed destruction positions has excellent explosion proof while IGCT with edge focusing destruction positions has poor explosion proof. The maximum surge currents of tested IGCT are both between 600 and 700 kA with the discharging of 18 mF/ 4500 V capacitor. The thermal simulation shows that IGCT's ceramic shell may suffer a huge transient thermal stress when the destruction positions focus on the edge areas and the thermal stress is decreased greatly when the destruction positions move into the inner regions of the chip. Besides, a designed gas pressure tolerance test shows that the gas pressure is in the safe area which IGCT can withstand under the extreme failure. This means that the thermal stress can be regarded as the main cause of IGCT's explosion phenomenon.

Based on the explosion mechanism, an optimized IGCT with controlled punch-through design in the central area is proposed to avoid the edge area destruction under the extreme failure. And explosion proof experiment of optimized IGCT validates its excellent explosion proof under the extreme failure in the MMC-HVdc system.

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