Switching Characteristic Analysis and Application Assessment of SiC MOSFET With Common Source Inductance and Kelvin Source Connection

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***Abstract*—SiC MOSFETs with packages of common source inductance (TO-247-3) and kelvin source connection (TO-247-4) are both widely used devices in the existing power conversion. Transient analysis of switching characteristics reveals some evaluation mistakes and misguidance design by using the conventional test circuit due to the difference packages. However, the more precise gate characteristic of TO-247-3 SiC MOSFET can be obtained by using TO-247-4 device package. Based on the unique feature, this article provides an improved evaluation method to get a comprehensive comparison of TO-247-3 and TO-247-4 SiC MOSFET commutation as the active and passive switch devices in the typical half-bridge circuit. The results indicate that 4-PIN SiC MOSFET has both advantages of low switching loss and reduced d*v*/d*t*. Furthermore, this article first reveals that the widely used drive design for TO-247-3 MOSFET with active miller clamped drive IC has a potential irrational circuit defect. Mathematical model analysis and experiment test have been accomplished to verify the superiority of the improved evaluation method. TO-247-4 SiC MOSFET is more promising in application of high efficiency, high frequency as well as strict EMI requirement.**

***Index Terms*—Common source inductance (CSI), device package, silicon carbide (SiC) MOSFET , switching characteristic, TO-247.**

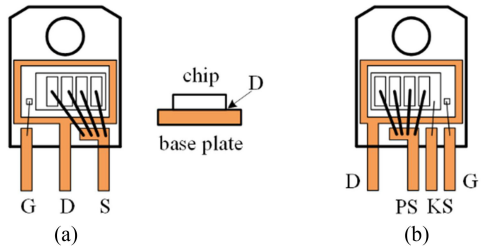

Fig. 1. Internal structure of SiC MOSFET. (a) TO-247-3. (b) TO-247-4.

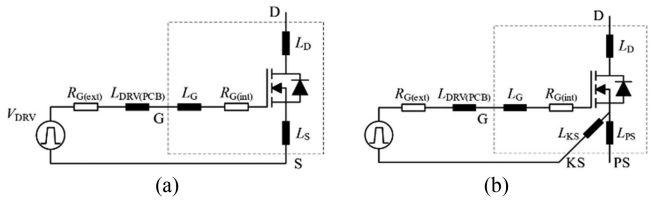

Fig. 2. Equivalent circuit of SiC MOSFET. (a) TO-247-3. (b) TO-247-4.

I. Introduction

With the great development in wafer fabrication and device manufacturing technology, commercial silicon carbide (SiC) MOSFET demonstrates superior performances including high breakdown electric field, low specific ON-state resistance, fast switching speed and high junction temperature capability, which enables power conversion to be higher efficiency, power density and more reliability [1], [2]. However, due to the significant increment of switching speed, the undesired influences caused by power device common source inductance (CSI) become more prominent [3]. In order to ensure good switching performance at high frequency, several improved package forms with kelvin source (KS) connection such as TO-247-4, TO-263-7, ThinPAK8x8, TOLL, DDPAK, and so on, under the consideration of different voltage, current rating and special applications have been launched [4].

Commonly used packages of SiC MOSFET are TO-247-3 and TO-247-4, and their internal structures are shown in Fig. 1. SiC MOSFET chips are thin cubes, with G and S electrodes on the upper surface and D electrode at the backside. The chip is soldered on the metal base. D electrode is leaded to a pin connected with the base, S electrode is leaded to one pin by several bonding wires to conduct the large current. G electrode is leaded to a pin by only one thin bonding wire due to the low driving current. When analyzing the switching process of SiC MOSFETs, printed circuit board (PCB) layout, device package pin and bonding wire are considered as inductance, and the equivalent circuit of TO-247-3 SiC MOSFET is shown as Fig. 2(a).

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It is obvious that L_S makes the power stage and the driving circuit coupling with each other, and the undesired influence on gate drive signal is generated by power stage during the switching commutation process. Compared with TO-247-3, there are two sources in TO-247-4 package, which are KS and power source (PS). KS pin is connected to S electrode with a thin bonding wire. The order and distance of pins are also varied. When using the TO-247-4 package, the drive circuit is connected between G and KS pins, and the main circuit is connected between D and PS pins, as shown in Fig. 2(b).

CSI has effects on both switching process and crosstalk, both of which represent switching characteristics. In the existing research articles, there are two types of description when explaining CSI effects on the switching process. The one focuses on effects of parasitic parameters on switching characteristics indexes [5]–[7]. Although switching process has also been given, effects in each stage of switching process is not illustrated combined with practice waveform. Meanwhile, although these research articles guide the device design and application, the basic theory is not clear enough. The other proposes more detailed device equivalent circuit model considering many parasitic parameters [8]–[10], with the aim of describe these effects by systematized mathematical modeling. Although the practice waveform has been explained precisely, it is not friendly in application, since the relationships between measured waveforms and parasitic parameters are too complicated to comprehend. Some application notes have tried to find description balancing theory and practice [11]–[13], but still not explained it clearly in theory. Another issue should be pointed out is that, the existing research articles have concluded that TO-247-4 package makes it possible to reduce the switching energy of SiC MOSFET s [14] and avoid self-turn-ON ringing [10]. However, switching characteristics has been only compared with a same driving resistance, which means that the compared devices may not on their best design, and causes the conclusion not convincing.

Crosstalk is also a general concerned phenomenon in SiC MOSFET applications, but relevant research articles focused more on the modeling [15]–[18] and the suppression method [19]–[23], less about the CSI effects on crosstalk. Modeling of crosstalk in [15] has considered CSI, but not detailed analyzed its effects, and the estimation of CSI effects on measurement in experiment was inaccurate. CSI effects on crosstalk combining only simplified waveforms and lacking detailed analysis, and not considered CSI effects on measurement were described in [24]. Therefore, CSI effects on crosstalk should be analyzed comprehensively and in detail, and more accurate measurement methods are worthy of further study.

To provide a fairer comparison and more accurate estimation on CSI effects, this article provides detailed explanation of the switching process and crosstalk based on simulation waveforms, and compares switching characteristics of SiC MOSFET with TO-247-3 and TO-247-4 packages. To obtain more accurate measurement results, an improved method is proposed to compare these two packages with one same TO-247-4 device. Experiment of devices with different driving resistance has been accomplished to verify and get more conclusions.

The rest of this article is organized as follows. Research background and objects are introduced in Section I. The influence on both switching process and crosstalk caused by CSI is illustrated in Sections II and III, respectively. Section IV presents an improved comparative method of switching characteristic between TO-247-3 and TO-247-4 SiC MOSFET. In Section V, the corresponding experimental results are provided, and detailed discussion is carried out to reveal the essential advantage of packages with KS connection. Finally, Section VI concludes this article.

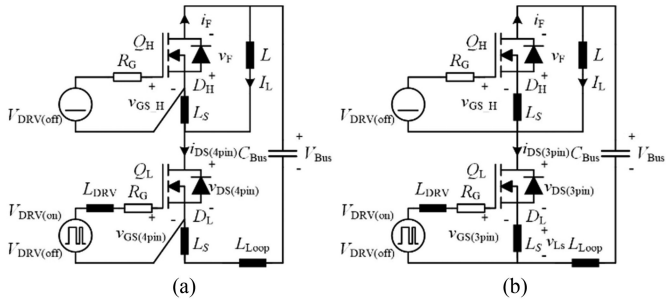

Fig. 3. Equivalent circuit of switching process of SiC MOSFET. (a) TO-247-4. (b) TO-247-3.

II. Switching Process Analysis

Switching process explanation of SiC MOSFET is necessary to evaluate switching characteristics, which is analyzed first according to the simulation results. Then, CSI effects on switching characteristics can be obtained.

The typical switching process of SiC MOSFET in the most application can be simplified and described as the half bridge circuit supplying the inductive load, as shown in Fig. 3. For circuit with TO-247-4 devices shown in Fig. 3(a), L is the load inductor, $C_{\rm Bus}$ is the bus capacitor, $R_{\rm G}$ is the drive resistor, $L_{\rm Loop}$ is the equivalent series inductance in power commutation circuit, $L_{\rm DRV}$ is the equivalent series inductance in drive circuit, $Q_{\rm H}$ and $Q_{\rm L}$ are the upper and lower SiC MOSFET, and $D_{\rm H}$ and $D_{\rm L}$ are body diode of $Q_{\rm H}$ and $Q_{\rm L,}$ respectively.

The typical waveforms of turn-ON process are shown in Fig. 4(a). Before t_0, both $Q_{\rm L}$ and $Q_{\rm H}$ are in the OFF-state, $v_{\rm GS(QL)} = V_{\rm DRV(off)}$, $v_{\rm GS(QH)} = V_{\rm DRV(off)}$, $i_{\rm DS} = 0$. I_L freewheels through $D_{\rm H}$, causing a voltage drop $V_{\rm F}$. $v_{\rm DS}$ maintains $V_{\rm Bus}$. According to the operation principle, the turn-ON process can be divided into three stages. $L_{\rm DRV}$ is ignored in order to simplify the analysis, since it has seldom effects on switching waveform in power stage. But in order to get more meaningful waveforms, $L_{\rm DRV}$ is considered in simulation.

Stage 1 [$t_0 \le t < t_1$]: At t_0, the driving voltage rapidly changes from $V_{\rm DRV(off)}$ to $V_{\rm DRV(on)}$. $C_{\rm iss}$ is charged by $i_{\rm G}$, which can be divided into two parts, $i_{\rm CGS}$ charging $C_{\rm GS}$ and $i_{\rm CGD}$ charging $C_{\rm GD}$

$$V_{\rm DRV(on)} = v_{\rm GS} + i_{\rm G} \cdot R_{\rm G} \tag{1}$$

$$i_{\rm G} = i_{\rm C_{GS}} + i_{\rm C_{GD}} = C_{\rm GS} \cdot {\rm d}v_{\rm GS}/{\rm d}t + C_{\rm GD} \cdot {\rm d}v_{\rm GD}/{\rm d}t. \tag{2}$$

Since $Q_{\rm L}$ is still in OFF state, and $v_{\rm DS}$ keeps as $V_{\rm Bus}$. Thus, $C_{\rm GS}$ and $C_{\rm GD}$ maintain constant and ${\rm d}v_{\rm GS}/{\rm d}t = {\rm d}v_{\rm GD}/{\rm d}t$. According to (1) and (2)

$$V_{\rm DRV(on)} = v_{\rm GS} + C_{\rm iss} \cdot {\rm d}v_{\rm GS}/{\rm d}t \cdot R_{\rm G}. \tag{3}$$

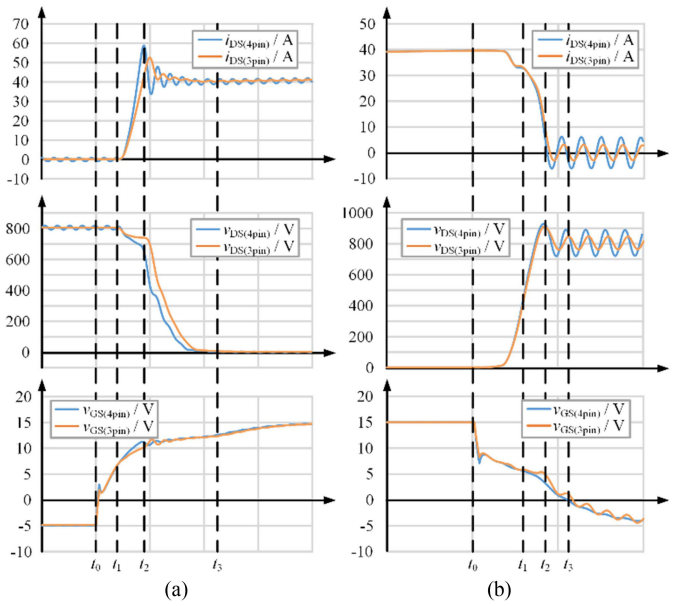

Fig. 4. Switching process of SiC MOSFET (IMZ120R030M1H type MOSFET, $I_{\mathrm{L}} = 40\,\mathrm{A}$, $V_{\mathrm{Bus}} = 800\,\mathrm{V}$, $V_{\mathrm{DRV(on)}} = 15\,\mathrm{V}$, $V_{\mathrm{DRV(off)}} = -5\,\mathrm{V}$, and $L = 100\,\mu\mathrm{H}$). (a) Turn ON. (b) Turn OFF.

By solving (3), v_{GS} is

$$v_{\mathrm{GS}}(t) = V_{\mathrm{DRV(on)}} - (V_{\mathrm{DRV(on)}} - V_{\mathrm{DRV(off)}})e^{-\frac{t-t_0}{R_{\mathrm{G}} \cdot C_{\mathrm{iss}}}}. \tag{4}$$

At t_1, v_{GS} reaches $V_{\mathrm{GS(th)}}$, and t_0-t_1 is defined as $t_{\mathrm{d(on)}}$.

Stage 2 [$t_1 \le t < t_2$]: v_{GS} exceeds $V_{\mathrm{GS(th)}}$, Q_{L} starts turning ON. Since Q_{L} is working in saturate region, i_{channel} is controlled by v_{GS} obeying

$$i_{\mathrm{channel}} = K \cdot (v_{\mathrm{GS}} - V_{\mathrm{GS(th)}})^2. \tag{5}$$

Here, K is a coefficient determined by power device parameter.

Obviously, i_{channel} consists of i_{DS}, i_{CGD}, and i_{CDS}. Since v_{DS} is still in the high voltage, C_{GS} and C_{GD} are still small value. Besides, $|\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|$ is small, so i_{DS} dominates in i_{channel}

$$i_{\mathrm{DS}} \approx i_{\mathrm{channel}}. \tag{6}$$

With I_{L} gradually freewheeling through Q_{L}, i_{DS} increases rapidly. $\mathrm{d}i_{\mathrm{DS}}/\mathrm{d}t$ generates the significant voltage drop on the inductance of the power commutation circuit L_{loop}, which causes v_{DS} to decrease

$$\Delta v_{\mathrm{DS}} = L_{\mathrm{loop}} \cdot \mathrm{d}i_{\mathrm{DS}}/\mathrm{d}t. \tag{7}$$

Since $C_{\mathrm{GD}} \ll C_{\mathrm{GS}}$, Δv_{DS} affects v_{GS} little, v_{GS} still basically satisfies (4), which can be rewritten as

$$v_{\mathrm{GS}}(t) = (V_{\mathrm{DRV(on)}} - V_{\mathrm{GS(th)}}) \cdot (1 - e^{-\frac{t-t_1}{R_{\mathrm{G}} \cdot C_{\mathrm{iss}}}}) + V_{\mathrm{GS(th)}}. \tag{8}$$

Combining (5)–(8), $|\Delta v_{\mathrm{DS}}|$ increases with the gradually growing of $\mathrm{d}i_{\mathrm{DS}}/\mathrm{d}t$.

After i_{DS} exceed I_{L}, D_{H} enters in reverse recovery, which causes an obvious current overshoot in i_{DS} waveform, and v_{GS} continues increasing.

Stage 3 [$t_2 \le t < t_3$]: At t_2, i_{DS} reaches the peak value, D_{H} starts to turn OFF, and v_{DS} starts to decline rapidly. i_{channel} still consists of i_{DS}, i_{CGD}, and i_{CDS}. C_{DS} and C_{GD} significantly increase with the decline of v_{DS}. i_{CGD} and i_{CDS} approach or even exceed i_{DS}, therefore, i_{DS} is much lower than i_{channel}

$$i_{\mathrm{channel}} = i_{\mathrm{DS}} + C_{\mathrm{GD}} \cdot \mathrm{d}v_{\mathrm{GD}}/\mathrm{d}t + C_{\mathrm{DS}} \cdot |\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|. \tag{9}$$

Since SiC MOSFET has the significant drain induced barrier lowering effect, $V_{\mathrm{GS(th)}}$ increases as v_{DS} decreases. According to (5), to maintain channel current, C_{GS} should be charged to improve v_{GS}, which is called miller ramp.

Since $|\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t| \gg |\mathrm{d}v_{\mathrm{GS}}/\mathrm{d}t|$, i_{CGD} can be simplified as

$$\begin{aligned} i_{\mathrm{C_{GD}}} &= C_{\mathrm{GD}} \cdot \mathrm{d}v_{\mathrm{GD}}/\mathrm{d}t = C_{\mathrm{GD}} \cdot \mathrm{d}(v_{\mathrm{GS}} - v_{\mathrm{DS}})/\mathrm{d}t \\ &\approx C_{\mathrm{GD}} \cdot |\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|. \end{aligned} \tag{10}$$

It suggests that $\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t$ is controlled by the charging speed of C_{GD}. When v_{DS} is high, C_{GD} is basically constant, whereas when v_{DS} is low, C_{GD} rapidly increases as v_{DS} decreases, especially when $v_{\mathrm{GD}} < 0\,\mathrm{V}$. It causes that $|\mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t|$ is basically constant when v_{DS} is high, whereas significantly reduces when v_{DS} is low.

Meanwhile, i_{DS} oscillates with a amplitude decayed, which generates corresponding oscillation of v_{DS}. v_{GS} also oscillates due to the charging current through C_{GD}. Therefore, all of them have the same oscillating frequency. At t_3, v_{DS} declines to $V_{\mathrm{DS(on)}}$, and the turn-ON process ends. v_{GS} achieves $V_{\mathrm{DRV(on)}}$ on the effect of i_{G}.

The circuit with TO-247-3 devices shown in Fig. 3(b) is similar to Fig. 3(a), with the only difference that there is CSI L_{S} in Fig. 3(b). Since CSI effects during switching process are mainly caused by v_{LS} generated by $\mathrm{d}i_{\mathrm{DS}}/\mathrm{d}t$, CSI effects in turn-ON process are mainly reflected into *Stages 2* and *3*. Because of the oscillating i_{DS}, it also affects *Stage 4*.

Stage 2 [$t_1 \le t < t_2$]: Q_{L} starts conducting, and $i_{\mathrm{DS(3pin)}}$ rapidly increases, which generates a voltage drop v_{LS} on L_{S}, with a polarity from upper to bottom. So, $v_{\mathrm{GS(3pin)}}$ is calculated with

$$v_{\mathrm{GS(3pin)}} = V_{\mathrm{DRV(on)}} - R_{\mathrm{G(ext)}} \cdot i_{\mathrm{G}} - L_{\mathrm{S}} \cdot \mathrm{d}i_{\mathrm{DS(3pin)}}/\mathrm{d}t. \tag{11}$$

According to (11), v_{LS} reduces the effective driving voltage of $V_{\mathrm{DRV(on)}}$, which has a negative feedback effect to make $v_{\mathrm{GS(3pin)}}$ lower than $v_{\mathrm{GS(4pin)}}$. Since at this stage, SiC MOSFET is saturated, $\mathrm{d}i_{\mathrm{DS(3pin)}}/\mathrm{d}t$ is smaller than $\mathrm{d}i_{\mathrm{DS(4pin)}}/\mathrm{d}t$, and then it causes the voltage drop $v_{\mathrm{DS(3pin)}}$ is lower than $v_{\mathrm{DS(4pin)}}$, and at the same time, it causes the diode reverse recovery current lower.

Stage 3 [$t_2 \le t < t_3$]: Since the rising speed of $i_{\mathrm{DS(3pin)}}$ is slower during the former process, and body diode reverse recovery current is less, so the oscillation amplitude of $i_{\mathrm{DS(3pin)}}$ also decreases at this stage, and the voltage drop on L_{loop} is also lower, which causes the oscillation amplitude of $v_{\mathrm{DS(3pin)}}$ and $v_{\mathrm{GS(3pin)}}$ decreasing. Meanwhile, v_{LS} also weakens the oscillation of $v_{\mathrm{GS(3pin)}}$.

During this process, the rising speed of $v_{\mathrm{GS(3pin)}}$ is influenced by v_{LS} little, so the declined speed of $v_{\mathrm{DS(3pin)}}$ is similar to the one of $v_{\mathrm{DS(4pin)}}$.

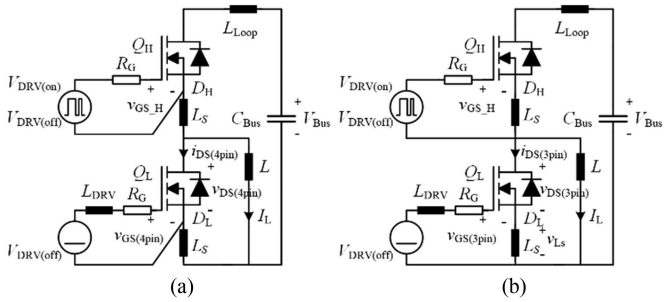

Fig. 5. Equivalent circuit of crosstalk of SiC MOSFET. (a) TO-247-4. (b) TO-247-3.

Stage 4 [$t_3 \le t$]: SiC MOSFET completely conducts, and $i_{\mathrm{DS(3pin)}}$ oscillates with a decayed amplitude, which is smaller than $i_{\mathrm{DS(4pin)}}$. So, the oscillation amplitude of $v_{\mathrm{DS(3pin)}}$, $v_{\mathrm{GS(3pin)}}$ is smaller than $v_{\mathrm{DS(4pin)}}$, $v_{\mathrm{GS(4pin)}}$.

The typical waveforms of turn-OFF process are shown in Fig. 4(b). Before t_0, D_{H} conducts positively. The conduction current is I_{L}, and the terminal voltage is the conduction voltage drop of D_{H}. v_{GS} of Q_{L} is equal to $V_{\mathrm{DRV(on)}}$, so Q_{L} is in the ON-state. i_{DS} is I_{L}, and v_{DS} is $V_{\mathrm{DS(on)}}$. D_{H} is in the OFF-state, withstanding V_{Bus}. The influence of L_{S} in switching-ON process is mainly reflected into *Stages 2–4*.

Stage 2 [$t_1 \le t < t_2$]: i_{DS} starts decreasing, and generates a voltage drop v_{LS} with a polarity from bottom to upper. v_{LS} weakens the driving capability of $V_{\mathrm{DRV(off)}}$, which has a negative feedback effect. Since $\mathrm{d}i_{\mathrm{DS(3pin)}}/\mathrm{d}t$ is smaller, $v_{\mathrm{GS(3pin)}}$ is a little bit higher than $v_{\mathrm{GS(4pin)}}$, and the declined speed of $i_{\mathrm{DS(3pin)}}$ is a little bit slower than $i_{\mathrm{DS(4pin)}}$.

Stage 3 [$t_2 \le t < t_3$]: At t_2, $v_{\mathrm{DS(3pin)}}$ reaches V_{Bus}, the body diode of the other MOSFET starts conducting, and I_{L} commutate rapidly to the body diode of the other MOSFET. Compared with the former interval, the declined speed of $i_{\mathrm{DS(3pin)}}$ is faster. So v_{LS} is higher, and $v_{\mathrm{GS(3pin)}}$ is obvious higher than $v_{\mathrm{GS(4pin)}}$, which causes the declined speed of $i_{\mathrm{DS(3pin)}}$ is slower than $i_{\mathrm{DS(4pin)}}$ in this interval, and the rising speed of $v_{\mathrm{DS(3pin)}}$ and its peak value are lower than those of $v_{\mathrm{DS(4pin)}}$.

Stage 4 [$t_3 \le t$]: SiC MOSFET is completely in OFF-state. Since the effect of former process, the oscillation amplitude of $i_{\mathrm{DS(3pin)}}$ is lower than $i_{\mathrm{DS(4pin)}}$, so the oscillation amplitude of $v_{\mathrm{DS(3pin)}}$, $v_{\mathrm{GS(3pin)}}$ is lower than $v_{\mathrm{DS(4pin)}}$ and $v_{\mathrm{GS(4pin)}}$, respectively.

III. Crosstalk Analysis

Crosstalk is a common phenomenon that the commutation process of a switch has an effect on v_{GS} of the complementary switch. Therefore, it also reflects switching characteristics in half bridge applications. Crosstalk is analyzed first according to the simulation results, and CSI effects on crosstalk can be obtained.

The equivalent circuits of crosstalk shown as Fig. 5 are similar to Fig. 3. Since driving signal is added on the gate of Q_{H}, crosstalk occurs on Q_{L}, and L is in parallel with Q_{L}. The typical waveforms of crosstalk during turn-ON process are shown in

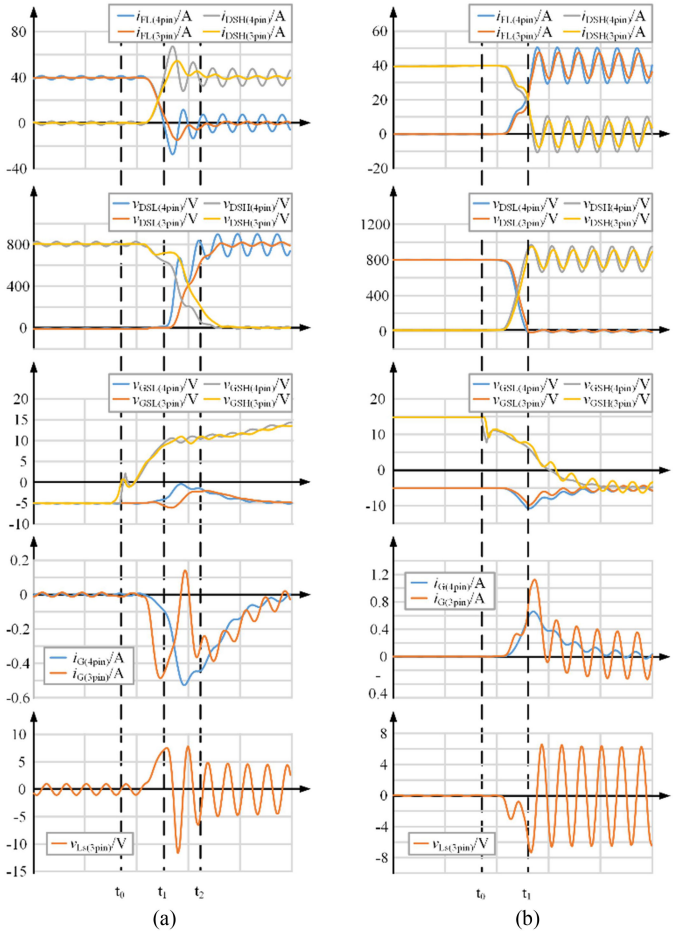

Fig. 6. Crosstalk of SiC MOSFET (IMZ120R030M1H type MOSFET, $I_{\mathrm{L}} = 40\,\mathrm{A}$, $V_{\mathrm{Bus}} = 800\,\mathrm{V}$, $V_{\mathrm{DRV(on)}} = 15\,\mathrm{V}$, $V_{\mathrm{DRV(off)}} = -5\,\mathrm{V}$, and $L = 100\,\mu\mathrm{H}$). (a) Turn ON. (b) Turn OFF.

Fig. 6(a). Q_{L} remains OFF, Q_{H} turns ON, and D_{L} enters in reverse recovery. v_{DS} increases from V_{F} to V_{Bus}. Since v_{GS} of Q_{L} maintains $V_{\mathrm{DRV(off)}}$, in this process, v_{GD} also increases from V_{F}-$V_{\mathrm{DRV(off)}}$ to V_{Bus}-$V_{\mathrm{DRV(off)}}$. Therefore, the varying v_{DG} generates a displacement current i_{miller} through C_{GD}, whose amplitude is determined as

$$i_{\mathrm{miller}} = C_{\mathrm{GD}} \cdot \mathrm{d}v_{\mathrm{DS}}/\mathrm{d}t. \tag{12}$$

i_{miller} flows into drive circuit through C_{GD}, and generates voltage drop on R_{G} and L_{DRV}. Meanwhile, i_{miller} charges C_{GS}. Under the combination of these two factors, v_{GS} increases according to (13), and an upward spike appears

$$v_{\mathrm{GS}} = V_{\mathrm{DRV(off)}} + R_{\mathrm{G}} \cdot i_{\mathrm{G}} + L_{\mathrm{DRV}} \cdot \mathrm{d}i_{\mathrm{G}}/\mathrm{d}t. \tag{13}$$

Stage 1 [$t_0 \le t < t_1$]: At t_0, Q_{H} starts turn-ON, i_{F} starts decreasing from the load current, and v_{DS} is determined by V_{F}, increasing with the drop of i_{F}. Although v_{DS} varies slowly with a small amplitude, v_{GS} still increases obviously because of the large C_{GD}.

Stage 2 [$t_1 \le t < t_2$]: At t_1, D_{L} starts withstanding the reverse voltage, and v_{DS} rapidly increases. Although C_{GD} decreases

with the increase of $v_{\rm DS}$, d$v_{\rm DS}$/dt is still large, so $v_{\rm GS}$ rapidly increases during this stage.

Stage 3 [$t_2 \le t$]: $v_{\rm GS}$ gradually falls back to $V_{\rm DRV(off)}$. Since $v_{\rm DS}$ oscillates with attenuation after reaching $V_{\rm Bus}$, $v_{\rm GS}$ is accompanied by shock during the falling process.

Since CSI effects of crosstalk are mainly caused by $v_{\rm LS}$ generated by d$i_{\rm CGS}$/dt and d$i_{\rm F}$/dt, and d$i_{\rm F(3pin)}$/dt plays a leading role in $v_{\rm LS}$, CSI effects in turn-ON crosstalk are mainly reflected into stages 1 and 2. During these stages, $v_{\rm LS}$ and $v_{\rm GS(3pin)}$ are, respectively,

$$v_{\rm Ls} = (\mathrm{d}i_{\rm C_{GS}}/\mathrm{d}t + \mathrm{d}i_{\rm F}/\mathrm{d}t) \cdot L_{\rm S} \tag{14}$$

$$v_{\rm GS(3pin)} = V_{\rm DRV(off)} + R_{\rm G} \cdot i_{\rm G} + L_{\rm DRV} \cdot \mathrm{d}i_{\rm G}/\mathrm{d}t - v_{\rm Ls}. \tag{15}$$

Stage 1 [$t_0 \le t < t_1$]: At t_0 moment, $Q_{\rm H}$ starts turn-ON, $i_{\rm F(3pin)}$ rapidly decreases from load current, and $v_{\rm DS(3pin)}$ increases with it. According to (15), the increase of $v_{\rm DS(3pin)}$ lift $v_{\rm GS(3pin)}$ up, while the decrease of $i_{\rm F(3pin)}$ pulls down on $v_{\rm GS(3pin)}$, and they are acting in opposite directions. At this stage, the decrease of $i_{\rm F(3pin)}$ plays a leading role, so $v_{\rm GS(3pin)}$ is pulled down below $V_{\rm DRV(off)}$.

Stage 2 [$t_1 \le t < t_2$]: At t_1 moment, $D_{\rm L}$ is starting at the opposite voltage, $v_{\rm DS(3pin)}$ rapidly increases, and $i_{\rm F(3pin)}$ increases from reverse recovery current, and $v_{\rm GS(3pin)}$ is lifted up by both of these two effects.

The simulation waveform of $L_{\rm S}$ on turn-ON crosstalk is shown in Fig. 5. It can be seen that $L_{\rm S}$ makes the upward peak of the turn-ON crosstalk waveform smaller, with difference shapes.

The typical waveforms of turn-OFF crosstalk are shown in Fig. 6(b). $Q_{\rm L}$ keeps OFF, $Q_{\rm H}$ switches OFF, and $D_{\rm L}$ starts freewheeling. The voltage $v_{\rm DS}$ of $Q_{\rm L}$ decreases from $V_{\rm Bus}$ to $V_{\rm F}$. In this process, $v_{\rm DG}$ also rapidly decreases from $V_{\rm Bus}$-$V_{\rm DRV(off)}$ to $V_{\rm F}$-$V_{\rm DRV(off)}$. Therefore, the varying $v_{\rm DG}$ generates a displacement current $i_{\rm miller}$ through $C_{\rm GD}$, whose amplitude is determined by (12). $i_{\rm miller}$ flows from drive circuit through $C_{\rm GD}$, generating voltage drop on $R_{\rm G}$ and $L_{\rm DRV}$, and discharging $C_{\rm GS}$. Under the combination of these two factors, $v_{\rm GS}$ decreases according to (13), and a downward spike appears.

CSI effects in turn-OFF crosstalk are also mainly reflected into stages 1 and 2, and $v_{\rm LS}$ and $v_{\rm GS(3pin)}$ are described as (14) and (15).

Stage 1 [$t_0 \le t < t_1$]: At t_0 moment, $Q_{\rm H}$ starts turn-OFF, $v_{\rm DS(3pin)}$ rapidly decreases from $V_{\rm Bus}$ to $V_{\rm F}$, and $i_{\rm F(3pin)}$ increases. According to (15), the decrease of $v_{\rm DS(3pin)}$ pulls down on $v_{\rm GS(3pin)}$, while the increase of $i_{\rm F(3pin)}$ lift $v_{\rm GS(3pin)}$ up, and they are acting in the opposite directions. At this stage, the decrease of $v_{\rm DS(3pin)}$ plays a leading role, so $v_{\rm GS(3pin)}$ is pulled down below $V_{\rm DRV(off)}$.

Stage 2 [$t_1 \le t$]: $v_{\rm GS(3pin)}$ gradually falls back to $V_{\rm DRV(off)}$. Since $v_{\rm DS(3pin)}$ oscillates with attenuation after reaching $V_{\rm Bus}$, $v_{\rm GS(3pin)}$ is accompanied by oscillation during the fall.

IV. Improved Comparative Measurement Method

Double pulse test is widely used to verified the former analysis, where an accurate measurement is essential. The most obvious method is to take two TO-247-4 and TO-247-3 package devices using the same type SiC MOSFET chip and test them, respectively. Fig. 7 shows their test circuits, where R_G is the driving resistance, and $L_{\rm S}$ is the CSI between measurement points.

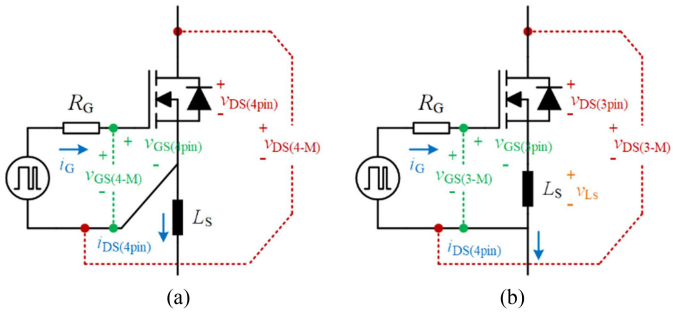

Fig. 7. Equivalent circuits of traditional test method. (a) Turn ON. (b) Turn OFF.

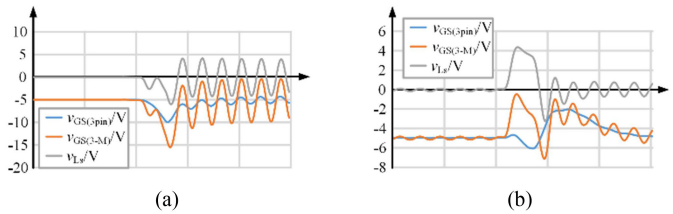

Fig. 8. Simulation waveforms by traditional test method. (a) TO-247-4. (b) TO-247-3.

The measured $v_{\rm GS(4\text{-}M)}$ and $v_{\rm DS(4\text{-}M)}$ for TO-247-4 package devices are similarly equal to the actual $v_{\rm GS(4pin)}$ and $v_{\rm DS(4pin)}$. However, for the TO-247-3 package device, the measurement of $v_{\rm GS(3\text{-}M)}$ and $v_{\rm DS(3\text{-}M)}$ contains a significant voltage drop on CSI caused by a sharply changed $i_{\rm DS}$, leading to the measurement results misleading to the analysis of $v_{\rm GS(3pin)}$ and $v_{\rm DS(3pin)}$, shown as (16) and (17). According to Fig. 8, the CSI effects on measured $v_{\rm GS(3\text{-}M)}$ is nonnegligible

$$v_{\rm GS(3-M)} = v_{\rm GS(3pin)} + L_{\rm S} \cdot \mathrm{d}i_{\rm DS}/\mathrm{d}t \tag{16}$$

$$v_{\rm DS(3-M)} = v_{\rm DS(3pin)} + L_{\rm S} \cdot \mathrm{d}i_{\rm DS}/\mathrm{d}t. \tag{17}$$

In addition, the difference of parasitic parameters in these two measurement circuits also affects the testing results, leading to the comparison not rigorous. Although Infineon has designed a specific PCB package [10], where SiC MOSFET with both two packages can be used to eliminate effect caused by parasitic parameters on PCB, the measured SiC MOSFET chip is not the same, and the difference of device parameters still affects the testing results.

In order to improve the measurement accurate, a test scheme is proposed to compare the influence of CSI on the switching characteristics of SiC MOSFET using the same TO-247-4 package device, including test methodology of both 4-in-3 test and 4-in-4 test.

A. 4-in-4 Test

In the circuit setting, the jumper resistance R_1 is disconnected, whereas R_2 is short-connected. The power stage is connected to

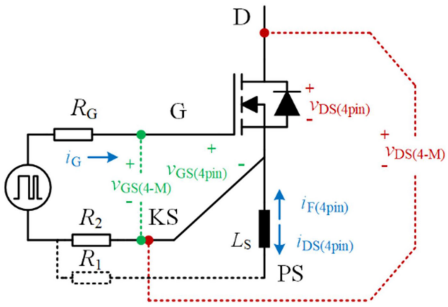

Fig. 9. Proposed comparative test circuit of 4-in-4 SiC MOSFET.

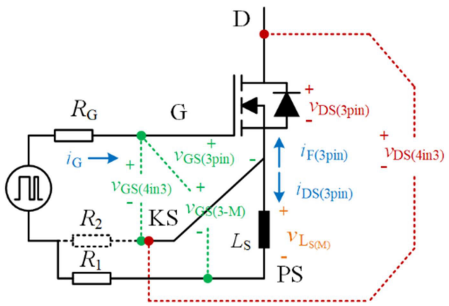

Fig. 10. Proposed comparative test circuit of 4-in-3 SiC MOSFET.

pin D and pin PS, and the drive circuit is connected to pin D and pin KS. In terms of measurement, the measuring point of v_{GS} is G pin and KS pin, and that of v_{DS} is D pin and KS pin. The circuit wiring and test points are the same as when using TO-247-4 packaging devices, as shown in Fig. 9. This method is called the 4-in-4 test. $v_{GS(4pin)}$ and $v_{DS(4pin)}$ are actual gate voltage and drain-source voltage when using TO-247-4 packages, and $v_{GS(4\text{-}M)}$ and $v_{DS(4\text{-}M)}$ are measurement results.

B. 4-in-3 Test

In the circuit setting, R_1 is short-connected, whereas R_2 is disconnected. The power stage is connected to pin D and pin PS, and the drive circuit is connected to pin G and pin PS, with KS pin dangling. In terms of measurement, select the measuring point of $v_{GS(3\text{-}M)}$ is G pin and PS pin, and the measuring point of $v_{DS(3\text{-}M)}$ is D pin and PS pin, which are the same as measured using the TO-247-3 package device. Select the measuring point of $v_{GS(4in3)}$ is G pin and KS pin, and the measuring point of $v_{DS(4in3)}$ is D pin and KS pin, to excluded the influence of $v_{LS(M)}$ to obtain more accurate v_{GS} and v_{DS}. The connection mode of this circuit is to connect TO-247-4 package device to work in the form of TO-247-3 package. This method is called 4-in-3 test, as shown in Fig. 10. The measurement of $v_{GS(3\text{-}M)}$, $v_{GS(4in3)}$ and $v_{DS(4in3)}$ follow (16), (18), and (19), respectively

$$v_{GS(4in3)} = v_{GS(3pin)} \tag{18}$$

$$v_{DS(4in3)} = v_{DS(3pin)}. \tag{19}$$

By using 4-in-3 test and 4-in-4 test, the inductance of the power stage and the drive loop with the same chip is compared. The CSI effects on v_{GS} measurement is also eliminated.

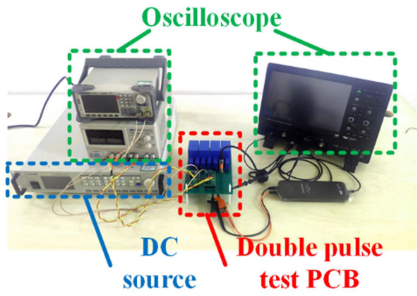

Fig. 11. Double pulse test experimental setup.

V. Experimental Verification and Analysis

In this section, both switching process and crosstalk of SiC MOSFET are verified by experiment, using measurement method presented in Section IV. Further analysis is accomplished to conclude the advantages of TO-247-4 package in switching characteristics without CSI effects on both switching process and crosstalk. Meanwhile, the significant effect on measurement caused by CSI is also pointed out.

A. Switching Process

As shown in Fig. 11, double pulse test experiments based on IMZ120R030M1H type MOSFET has been accomplished, with $I_L = 40$ A, $V_{Bus} = 800$ V, $V_{DRV(on)} = 15$ V, $V_{DRV(off)} = -5$ V, and $L = 100\,\mu$H. To eliminate errors induced by the test equipment, TPP1000, a 10x passive probe with 1 GHz bandwidth, is adopted for v_{GS} measurement, and TPP0850, a 50x high voltage probe with 800 MHz bandwidth, is adopted for v_{DS} measurement. Magnet ring to the oscilloscope-connected line is added to eliminate the common mode disturbance. The waveforms of both turn-ON and turn-OFF process are obtained by 4-in-3 and 4-in-4 tests, respectively, as shown in Fig. 12. Consistent with the analysis and simulation results, when i_{DS} is varying, v_{LS} is generated and reduces the effective driving voltage of $V_{DRV(on)}$ and $V_{DRV(off)}$. Therefore, $v_{GS(3pin)}$ varies slower than $v_{GS(4pin)}$, which has a negative feedback effect on i_{DS} to suppress its variation. During turn-ON process, CSI reduces the increasing speed of v_{GS} in *Stages 2 and 3*, reduces the increasing speed and spike of i_{DS} in *Stage 2*, suppresses the oscillation of v_{GS} and i_{DS}, but does not influence the decreasing speed of v_{DS} in *Stage 3*. During turn-OFF process, CSI reduces the decreasing speed of v_{GS} and i_{DS} in *Stage 3*, and suppresses the oscillation of v_{GS} and i_{DS}. Thus, it can be seen that CSI reduces the swithcing speed of SiC MOSFET.

The declined switching speed makes the switching energy increases, which enlarges losses in applications. When R_G is 8 Ω, E_{on} and E_{off} of TO-247-4 device are 896.4 and 202.2 μJ, respectively, whereas E_{on} and E_{off} of TO-247-3 device are 1278.5 and 236.2 μJ, respectively. According to Table I, when i_{DS} changes, switching energy of TO-247-4 device is always lower than that of TO-247-3 device, and the difference grows as i_{DS} growing. It can be obtained that with the same R_G, the switching speed of TO-247-4 package is faster and the switching

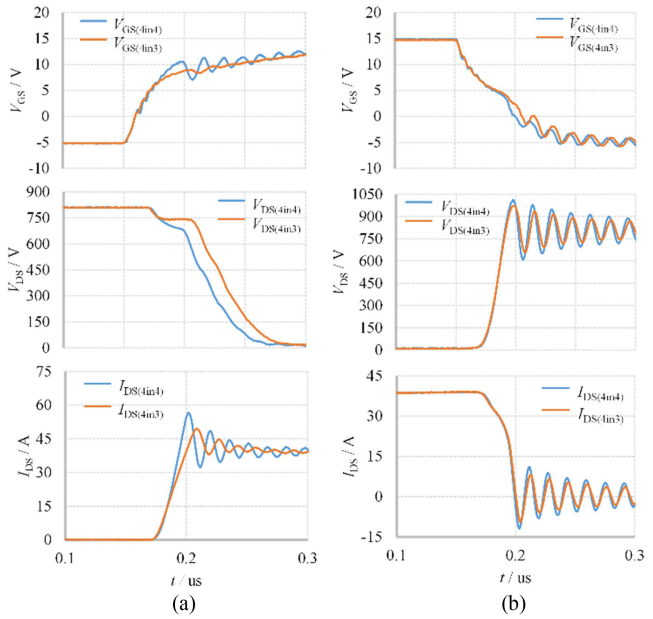

Fig. 12. Test waveform of switching process obtained by 4-in-3 and 4-in-4 tests. (a) Turn ON. (b) Turn OFF.

TABLE I
INFLUENCE OF CSI ON SWITCHING LOSS OF SIC MOSFET

i_{DS} (A)	E_{on} (μJ)			E_{off} (μJ)		
	4in4	4in3	Decline	4in4	4in3	Decline
10	311.5	342.5	9%	13.4	14.2	5%
20	486.3	588.7	17%	39.8	53.9	26%
30	671.2	895.8	25%	110.6	138.6	20%
40	896.4	1278.5	30%	202.2	236.2	14%

TABLE II
SWITCHING LOSS OF SIC MOSFET WHEN R_G REDUCES

$R_G(\Omega)$	E_{on} (μJ)		E_{off} (μJ)	
	4in4	4in3	4in4	4in3
5	437.5	929.3	122.6	155.0
6	594.2	1145.8	167.8	171.4
7	724.3	1229.7	192.4	207.2
8	896.4	1278.5	202.2	236.2

loss is lower than that of TO-247-3 package, which is main advantage always mentioned by manufactures.

However, the switching speed of SiC MOSFET is heavily influenced by R_G. Therefore, it is easy to think out that if R_G of the TO-247-3 package is smaller than that of the TO-247-4 package, the switching speed of the TO-247-3 package is able to be equal to or even exceed that of the TO-247-4 package. As given in Table II, when R_G reduces to 5 Ω, E_{on} and E_{off} of TO-247-3 device are 929.3 and 155.0 μJ, respectively, which is close to TO-247-4 device with an 8 Ω R_G. However, TO-247-4 package makes it possible for SiC MOSFET to achieve much higher switching speed than TO-247-3 package by reducing R_G. Therefore, to obtain a comprehensive conclusion, TO-247-4 and TO-247-3 packages should be compared with the similar switching energy rather than the same R_G. TO-247-4 device with an 8 Ω R_G and TO-247-3 device with a 5 Ω R_G have been

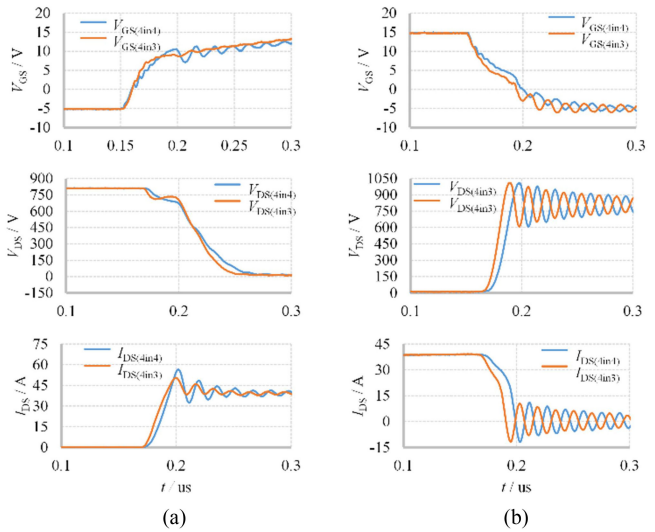

Fig. 13. Comparison between TO-247-4 and TO-247-3 devices with similar switching energy. (a) Turn ON. (b) Turn OFF.

TABLE III
INFLUENCE OF CSI ON dv_{DS}/dt OF SIC MOSFET

i_{DS} (A)	$dv_{DS(on)}/dt$ (V/ns)			$dv_{DS(off)}/dt$ (V/ns)		
	4in4	4in3	Rate	4in4	4in3	Rate
10	36.4	35.0	1.0	28.6	28.50	1.0
20	32.8	31.4	1.0	48.5	46.4	1.0
30	30.3	28.7	1.0	56.8	51.3	1.1
40	28.2	26.3	1.1	58.9	53.2	1.1

compared. Fig. 13 shows the switching waveforms. It can be found that the latter one has a higher dv_{DS}/dt, which induces more severe electromagnetic interference (EMI) and crosstalk issue. It means that switching loss cannot be reduced simply by reducing R_G without any negative effects. In some special applications, switching loss is even sacrificed to ensure that the device satisfy EMI standard.

The effect of CSI on dv_{DS}/dt under the same R_G is given in Table III, whose data are from the test in Table I. Manufacturers generally emphasize TO-247-4 package provides much faster switching speeds and reduced switching losses. Taking the results in Table I, Fig. 10 and Table II into account, the more comprehensive conclusion is that TO-247-4 package makes the switching speed of SiC MOSFET faster and switching losses lower without significantly increasing dv_{DS}/dt, which means both switching speed and EMI requirement are achieved.

B. CSI Effects on Switching Process Measurement

The results of $v_{GS(4in3)}$ and $v_{GS(3\text{-}M)}$ in 4-in-3 test are shown in Fig. 14. Since $v_{GS(3\text{-}M)}$ contains $v_{LS(M)}$ while $v_{GS(4in3)}$ does not, during the turn-ON process, there is a significant positive spike of $v_{GS(3\text{-}M)}$ when i_{DS} rapidly increases, and during the turn-OFF process, there is a significant negative one when i_{DS} rapidly decreases. The oscillation of $v_{GS(3\text{-}M)}$ is always obviously higher than $v_{GS(4in3)}$.

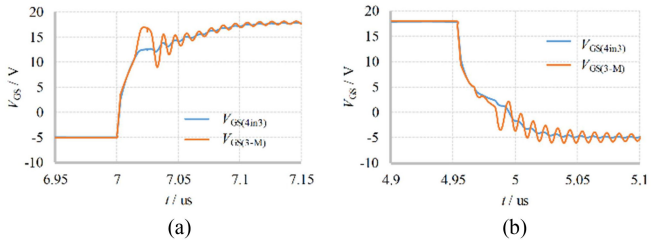

Fig. 14. Comparison between measured $v_{GS(3\text{-}M)}$ and $v_{GS(4in3)}$ of switching process. (a) Turn ON. (b) Turn OFF.

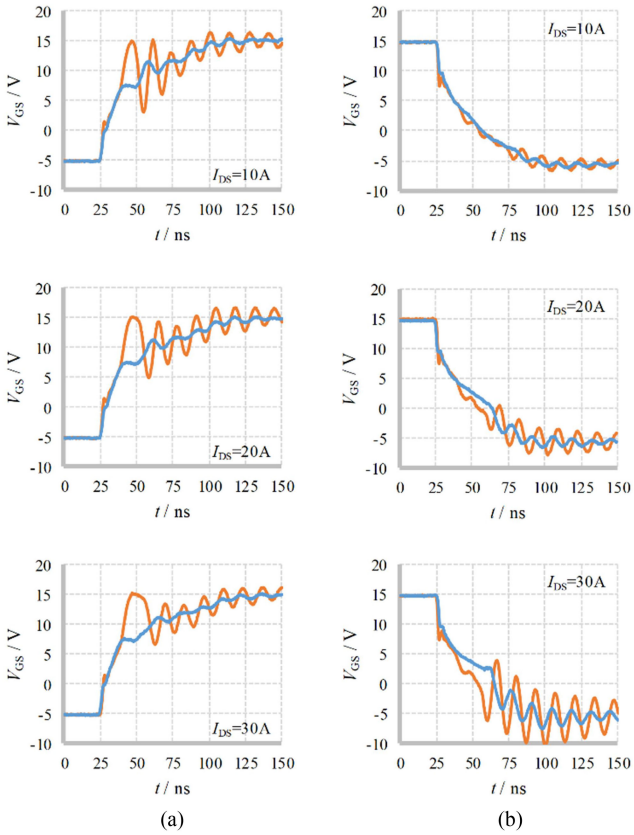

Fig. 15. Influence of L_S on measurement with different turn-ON current (Blue: $v_{GS(4in3)}$, Orange: $v_{GS(3\text{-}M)}$). (a) Turn ON. (b) Turn OFF.

Test conditions also influences the measurement accuracy. To obtain further analysis about CSI effects on measurement, experiments with different load current and R_G has been carried out. As the results shown in Figs. 15 and 16, the former differences between $v_{GS(3\text{-}M)}$ and $v_{GS(4in3)}$ are more obvious when load current is higher and driving resistance is lower.

C. Crosstalk

The waveforms of crosstalk during both turn-ON and turn-OFF process are obtained by 4-in-3 and 4-in-4 tests respectively, as shown in Fig. 17. Consistent with the analysis and simulation results, when C_{DS} is charging or discharging, v_{LS} is generated, which can be considered as a voltage source added on $V_{DRV(off)}$. During turn-ON process, crosstalk of TO-247-4 package devices

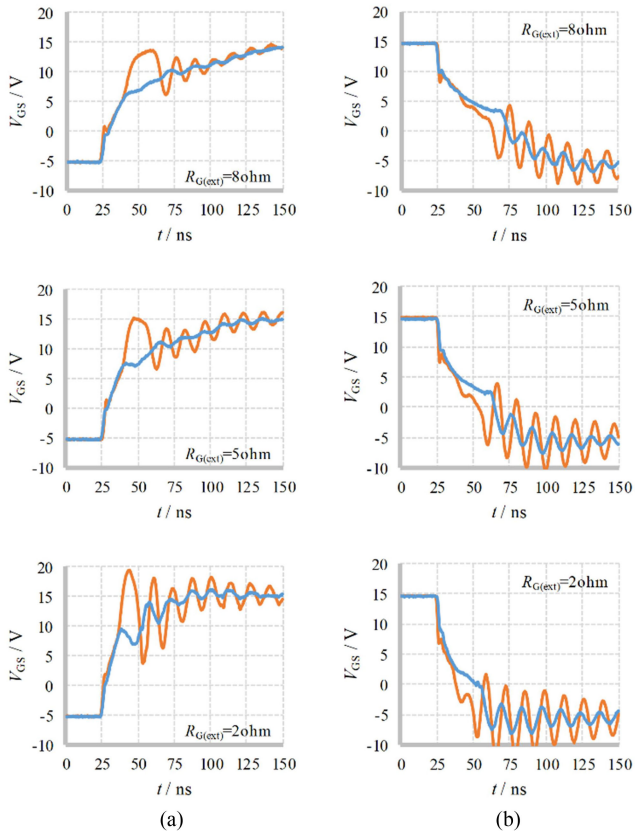

Fig. 16. Influence of L_S on measurement with different drive resistor (Blue: $v_{GS(4in3)}$, Orange: $v_{GS(3\text{-}M)}$). (a) Turn ON. (b) Turn OFF.

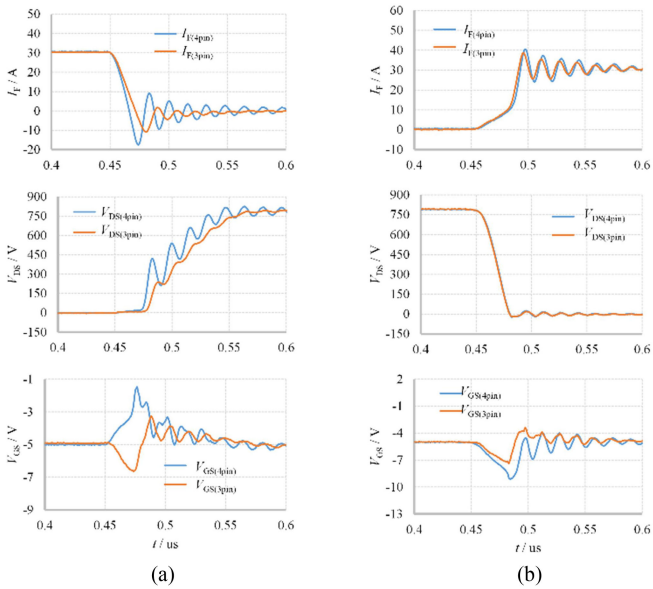

Fig. 17. Test waveform of crosstalk obtained by 4-in-3 and 4-in-4 tests. (a) Turn ON. (b) Turn OFF.

is a positive spike of v_{GS} which may trigger on it, whereas crosstalk of TO-247-3 package device is a negative spike of v_{GS} which may breakdown it. During turn-OFF process, crosstalk of devices with both TO-247-4 and TO-247-3 package is a negative spike of v_{GS} which may breakdown them. Although the crosstalk

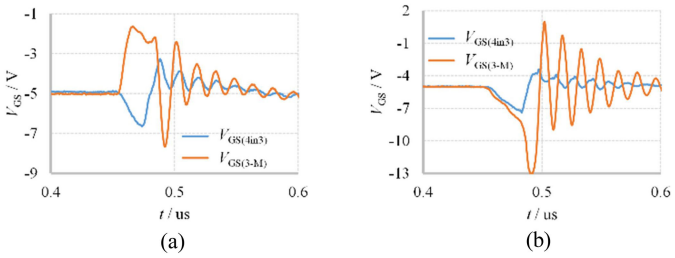

Fig. 18. Comparison between measured $v_{GS(3\text{-}M)}$ and $v_{GS(4in3)}$ of crosstalk. (a) Turn ON. (b) Turn OFF.

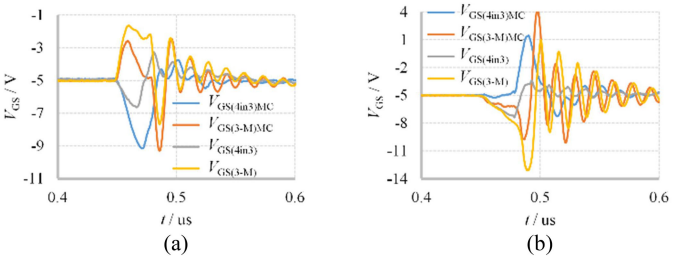

Fig. 19. Influence of L_S on AMC. (a) Turn ON. (b) Turn OFF.

amplitude of TO-247-3 package device is always smaller than that of TO-247-4 package device, which means that CSI makes crosstalk less serious, it still needs to be eliminated to protect the gate of devices from negative voltage breakdown.

D. CSI Effects on Crosstalk Measurement

The results of $v_{GS(4in3)}$ and $v_{GS(3\text{-}M)}$ in 4-in-3 test are also compared. Since $v_{GS(3\text{-}M)}$ contains $v_{LS(M)}$ while $v_{GS(4in3)}$ does not, the measured $v_{GS(3\text{-}M)}$ is significantly different from $v_{GS(4in3)}$ in both amplitude and shape, as shown in Fig. 18. During the turn-ON process, $v_{GS(4in3)}$ contains a negative spike in stage 1, but $v_{GS(3\text{-}M)}$ contains an obvious positive spike, which does not conform to theoretical analysis. During the turn-OFF process, the amplitude of $v_{GS(3\text{-}M)}$ spike is quite larger than $v_{GS(4in3)}$, although they both contain a negative spike in stage 1. Besides, the oscillation of $v_{GS(3\text{-}M)}$ is always larger than $v_{GS(4in3)}$. Therefore, $v_{GS(3\text{-}M)}$ seriously misjudge the condition of crosstalk.

Active miller clamping (AMC) is one of the commonly used method to eliminate crosstalk. It is integrated into IC controllers, consisting of comparator, MOSFET $S_{MC(int)}$ and logic control circuit. During turn-ON crosstalk, when v_{GS} is lifted to the threshold voltage of the comparator $V_{th(MC)}$, the output of comparator flips and $S_{MC(int)}$ turns ON, connecting gate with the ground to suppress the turn-ON crosstalk. During turn-OFF crosstalk, when v_{GS} is lower than -0.7 V, $D_{MC(int)}$, the body diode of $S_{MC(int)}$, turns ON to suppress the turn-OFF crosstalk.

However, the premise for AMC to operate as designed is the correct detection of v_{GS}. Crosstalk is significantly alleviated by AMC when using TO-247-4 device, but not when using TO-247-3 device, according to waveforms of $v_{GS(3\text{-}M)}$ and $v_{GS(4in3)}$ shown in Fig. 19. Therefore, it is no sense to research

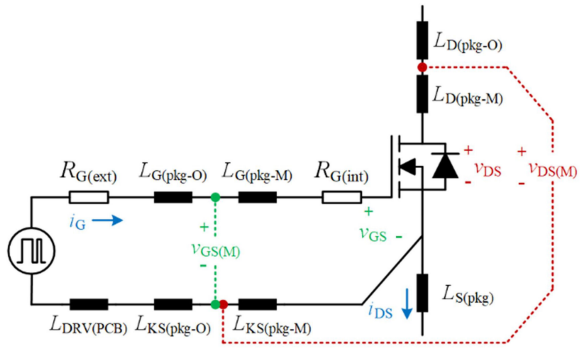

Fig. 20. More detailed equivalent circuit of SiC MOSFET measurement.

the results of AMC using TO-247-3 package device since the wrong detection of v_{GS}.

E. Discussion of Improved Measurement Method

The former analysis has ignored some parasitic parameters in packages and the PCB circuit. Fig. 20 shows more detailed equivalent measurement circuit in which $R_{G(int)}$ is the internal gate resistance, $L_{G(pkg\text{-}O)}$ and $L_{KS(pkg\text{-}O)}$ are the parasitic inductance of G pin and KS pin outside the package, $L_{G(pkg\text{-}M)}$ and $L_{KS(pkg\text{-}M)}$ are the parasitic inductance of G pin and KS pin inside the package, $L_{DRV(PCB)}$ is the parasitic inductance of drive circuit in PCB, and $L_{S(pkg)}$ is the parasitic inductance of S pin.

Although it is able to eliminate part of the effects of parasitic parameters by measuring signals as closed to the root of pins as it can be, there is still some inductance and resistance inside the package which is not able to eliminate in the experiment. It means that the circuit between the measuring points of $v_{GS(M)}$ includes $L_{G(pkg\text{-}M)}$ and $L_{KS(pkg\text{-}M)}$, and the circuit between the measuring points of $v_{DS(M)}$ includes $L_{D(pkg\text{-}M)}$ and $L_{KS(pkg\text{-}M)}$, according to Fig. 20. Varying currents through the inductance between measuring points generate voltage drop, which is also measured as a part of measured voltage. Besides, SiC MOSFET has internal gate resistance $R_{G(int)}$, and i_G also generates a voltage drop on it, which is also measured. So the measured $v_{GS(M)}$ and $v_{DS(M)}$ still have derivation from the actual v_{GS} and v_{DS} of chips, which can be calculated as

$$v_{GS(M)} = v_{GS} + i_G \cdot R_{G(int)} + (L_{G(pkg-M)} + L_{KS(pkg-M)}) \cdot di_G/dt \quad (20)$$

$$v_{DS(M)} = v_{DS} + L_{D(pkg-M)} \cdot di_{DS}/dt + L_{KS(pkg-M)} \cdot di_G/dt. \quad (21)$$

Therefore, although parasitic parameters between measuring points do not influence the analysis of both switching process and crosstalk, they still have influences on the measurement results of v_{GS} and v_{DS}. The actual waveforms of v_{GS} and v_{DS} are able to be calculated according to (20) and (21) with measured signals and parasitic parameters already known, but it is not practical.

VI. Conclusion

In this article, by comparing the same SiC MOSFET with TO-247-4 and TO-247-3 packages, CSI effects on switching process and crosstalk are discussed, combined with simulation waveforms. CSI reduces the switching speed and enlarges the switching energy, which is unexpected in application. Although it can be improved by reducing driving resistance, EMI issue is more severe.

Besides, CSI induces considerable spikes and oscillations in v_{GS} measurement, especially with high load current and low driving resistance. It gets worse that the crosstalk detection is absolutely wrong due to CSI. There should be always negative v_{GS} spikes in both turn-ON and turn-OFF crosstalk when CSI has been considered, but an opposite spike in turn-ON crosstalk, significantly severe spike in turn-OFF crosstalk and more considerable oscillations are detected, which may disable the AMC.

An improved measurement method is proposed to eliminate the effect of CSI voltage on the measured v_{GS}, and simplify comparison these two packages with a same TO-247-4 device. TO-247-4 device makes the switching speed faster and switching losses lower without significant EMI increase. Besides, TO-247-4 package guarantees the correct v_{GS} measurement in practice, which is essential for gate driving correction.

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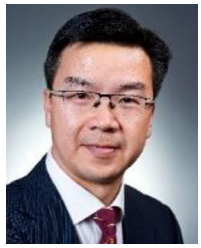

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