Static Analysis of a Digital Peak Current Mode Control DC–DC Converter Using Current–Frequency Conversion

Yudai Furukawa, *Member, IEEE*, Yuichiro Shibata, *Member, IEEE*, Haruhi Eto, *Member, IEEE*,
Ilhami Colak, *Senior Member, IEEE*, and Fujio Kurokawa, *Fellow, IEEE*

***Abstract*—The purpose of this article is to discuss the design guideline and design chart of the digital peak current mode dc–dc converter using a current–frequency conversion by analyzing its static characteristics. The operation of the proposed method is expressed by equations, and the relationships between controller parameters are derived. This discussion reveals the relationships between the peak current instruction value and the output voltage or peak current, which are necessary for designing the proposed method. Then, the design guideline and design chart are given. The validity of the static characteristic analysis is demonstrated by a prototype, whose design follows the design guideline. An appropriate operation in the steady and static state is also indicated by the experiment. As a result, the validity of the static characteristics and the design guideline of the proposed method can be verified.**

***Index Terms*—Current-frequency conversion, dc–dc power converters, digital control, peak current mode control.**

I. INTRODUCTION

DIGITAL control for switching power supplies is attracting attention because it has advantages over analog control, such as flexibility, cooperative control according to the situation, and easy tuning [1]–[8]. The digital control has the issue that the delay time due to A–D conversion time and processing time reduces the stability of the switching power supply. Therefore, a control method that can significantly improve stability is required.

A peak current mode control (PCMC) is well known as a switching power supply control method that can improve stability and is widely used in analog control [9]–[19]. The PCMC utilizes the comparator as the voltage mode control (VMC) does. The immunity of the comparator to noise is one of the drawbacks of analog control. The PCMC replaces a carrier signal in a VMC with a reactor current to improve stability. In the PCMC, the real-time property of current detection is very important and high accuracy is not required. An output voltage of switching power supplies is accurately regulated through a voltage loop as well as the VMC. This control algorithm improves the stability.

Many papers have been reported that implement the PCMC in digital control [20]–[52]. From these papers, the PCMC in digital control can be roughly divided into two types: a complete digital control method [20]–[33] and a hybrid analog–digital control method in which analog circuits and digital circuits coexist [34]–[52]. There are two methods in the complete digital control methods. The one is a method using an A–D converter (ADC) for detecting a peak current of the reactor current and the output voltage [20]–[22]. The other is a peak current prediction method [23]–[33]. These methods have delay times in both the voltage loop and the current loop, and therefore they are called a voltage and current delayed type here. The hybrid analog–digital control method includes a method using a D–A converter (DAC) [34]–[44], a method using a resistor–capacitor (*RC*) integrator circuit [45], and a method using a voltage-controlled oscillator (VCO) [46]–[52]. These methods have the delay time only in the voltage loop, and therefore they are called voltage delayed type here.

The complete digital control method is described. The method using ADC [20]–[22] needs sufficiently fast ADC with respect to the switching frequency, which leads to an increase in cost. Moreover, no matter how a high-speed ADC is used, A–D conversion time and processing time always occur. Thus, the delay time cannot be resolved, and a design that takes this effect into consideration is required. For the same reason, it is difficult to apply it to high-frequency switching power supplies and applications that require a quick response. There is also a delay in limiting the overcurrent. A peak current prediction method [23]–[33] has been proposed that does not need a high-speed ADC, such as direct detection using the ADC. The delay time is not eliminated and has the same drawbacks as the method using ADC since this method predicts the peak current. In the first place, its system configuration is different from the PCMC. The prediction accuracy deteriorates due to parameter variations, prediction model errors, and noise. It is not possible to get the

---

Manuscript received July 28, 2021; revised November 25, 2021; accepted January 15, 2022. Date of publication January 25, 2022; date of current version March 24, 2022. Recommended for publication by Associate Editor D. Vinnikov. *(Corresponding author: Yudai Furukawa.)*

Yudai Furukawa is with Fukuoka University, Fukuoka 814-0180, Japan (e-mail: yudai@fukuoka-u.ac.jp).

Yuichiro Shibata is with the Department of Computer and Information Sciences, Nagasaki University, Nagasaki 852-8521, Japan (e-mail: shibata@cis.nagasaki-u.ac.jp).

Haruhi Eto is with Nagasaki University, Nagasaki 852-8521, Japan (e-mail: haruhi-eto@awa.bbiq.jp).

Ilhami Colak is with the Faculty of Engineering and Architecture, Nisantasi University, 25370 Istanbul, Turkey (e-mail: ilhcol@gmail.com).

Fujio Kurokawa is with the Institute for Innovative Science and Technology, Nagasaki Institute of Applied Science, Nagasaki 851-0193, Japan (e-mail: kurokawa_fujio@nias.ac.jp).

Digital Object Identifier 10.1109/TPEL.2022.3145811

actual peak current value because it is a peak current prediction. These two methods cannot realize the most important real-time current detection and strive to accurately detect the current. Therefore, their concepts are different from the original concept of the PCMC, which is that the current detection needs real-time property and does not need high accuracy.

To deal with the issue of current detection in the digital control, hybrid analog–digital control methods have been proposed [34]–[52]. These methods do not use the ADC for the current detection, and the real-time current detection is achieved with various ideas. The method using the DAC [34]–[44] has the same current detector with the analog control and the real-time current detection can be achieved. The voltage loop is a general configuration of digital control, which uses the ADC. The output digital value of the digital controller in the voltage loop, such as the PID controller, can be utilized for getting a real peak current value. It is converted into the analog signal by the DAC so that the delay time occurs. The delay time by the A–D conversion also exists. This method has the same drawbacks as the analog control, which is the comparator is vulnerable to noise.

A method for peak current detection using a simple digital circuit without using the DAC and comparator has been proposed [45]–[52]. In [45], only the vicinity of the peak value of the reactor current is taken into the *RC* integrator circuit, and the time until the output voltage of the *RC* integrator circuit reaches an arbitrary threshold voltage is detected. The timing of starting current detection is adjusted by the calculation result of the digital controller, which has the general configuration using the ADC, in the voltage loop. This method detects the reactor current in real time, although the response to sudden changes may be delayed because it is a very short time for the current detection. It is difficult to grasp the peak current value in this method. The control system of this method has a different configuration from the PCMC in the first place.

There are two methods for detecting voltage and the reactor current using the VCO instead of the ADC: counting the pulse signal from the VCO [46]–[48] and detecting the frequency by giving a phase difference to the pulse signal from the VCO [49]–[52]. The VCO is an element that outputs the pulse signal with a frequency proportional to its input voltage. It is cheaper and more cost-effective than the ADC [47]. It has immunity to noise as it internally integrates its input voltage for a short time to generate a pulse signal.

The method that counts the pulse signal from the VCO utilizes the counted value as the digital value of the detected signal [46]–[48]. When the target value is set as a digital value after the VCO as in [47], the digital value to be captured will change significantly due to the influence of the temperature characteristics of the VCO. For this reason, it is necessary to set the target voltage before the VCO and increase the gain of the error amplifier as in [48]. A high-frequency VCO and a high clock frequency for counting are required to increase the resolution. Their frequencies are much higher than the switching frequency. Then, it is difficult to count the pulses. This method is disadvantageous for increasing the switching frequency.

As the other method using the VCO, the authors have already proposed a method detecting the frequency by giving a phase difference to the pulse signal from the VCO [49]–[52]. In the proposed method, the voltage loop is a general configuration of digital control using the ADC and the VCO is used for current detection. The peak current detection that ensures real-time performance is realized by detecting the frequency of the pulse signal from the VCO with a frequency detector composed of a simple digital circuit. The value of the frequency to be detected is controlled by the calculated value of the voltage loop. This calculated value is equivalent to the peak current instruction value, and therefore, the current value can be grasped by using it. It is possible to detect peak current without delay time with this procedure. The proposed method realizes a control system similar to the analog PCMC by digital control except for the delay time in the voltage loop. Furthermore, a method using phase difference, which is similar to the proposed method, realizes the PCMC in a high-frequency dc–dc converter in [53]. It is difficult to get the current value since the VCO is also used for output voltage detection and the pulse signal from the VCO is not converted to the digital value in this method. Due to this reason, it is not suitable for the implementation of management, monitoring, remote control, etc., which are the advantages of digital control, and its applications are limited. Therefore, it is desirable that the voltage loop is configured using the ADC as in the proposed method to take advantage of the features of digital control.

The review of six digital PCMC dc–dc converters using their block diagrams, which show the position of the proposed method clearly, is carried out in Appendix I to confirm the usefulness of the proposed method.

The proposed method has been limited to partial reports so far [49]–[52]. In particular, the design guidelines for the proposed method have not been clear. ADCs are generally utilized as sensors for the output voltage and reactor current so that the controller design can be considered the same as the general digital controller design method [20]–[22]. This configuration has no choice to avoid the delay time in the current loop. The proposed method has achieved the real-time sensing of the peak current in the digital controller using the VCO as the reactor current sensor and asynchronous digital logic circuit as the peak current detector [49]–[52]. However, designing parameters of the controller is difficult, and the design procedure is complex compared with the case of only using ADCs because the peak current is in inverse proportion to the current instruction value. This inverse proportional relationship influences the resolutions of the peak current and output voltage and the regulation characteristics. Due to this reason, it has not been possible to design the proposed PCMC switching power supply with performance that satisfies the required specifications for each application. In other words, the proposed method could not be widely applied.

This article presents the design guideline of the current–frequency conversion peak current mode dc–dc converter by organizing digital controller parameters and expressing their relationship by equations. They are derived by static characteristic analysis of the proposed method. Furthermore, the design chart is indicated based on the design guideline. Thus, this article promotes the wide spread of the PCMC in the digital control switching power supply.

First, the operation principle of the proposed method is reviewed, and static characteristic analysis is performed. Second,

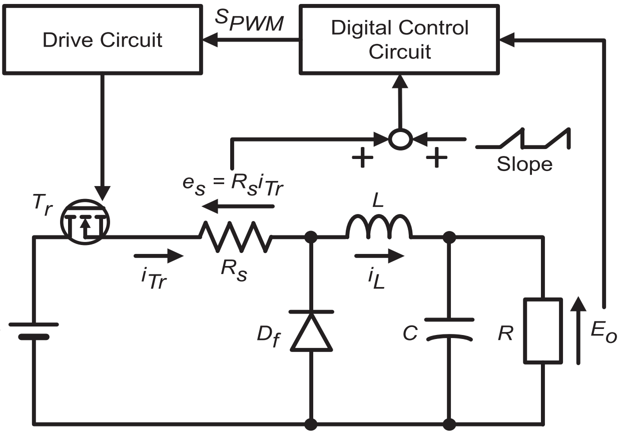


Fig. 1. Circuit configuration of the proposed digital PCMC dc–dc converter.

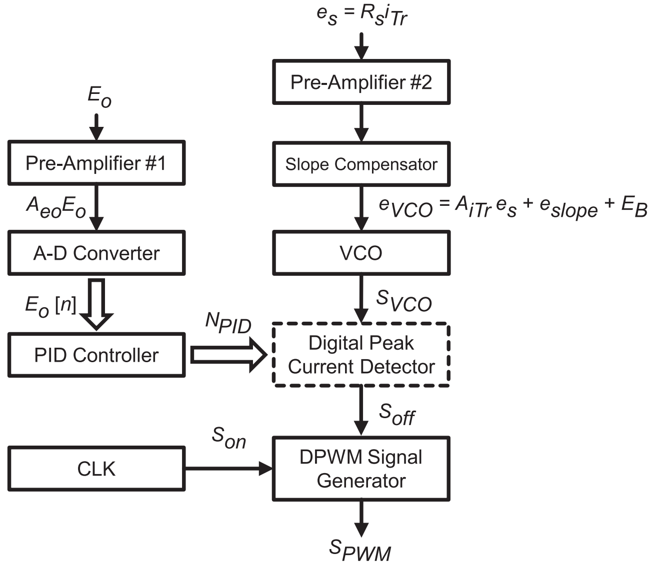


Fig. 2. Architecture of a digital control circuit.

theoretical clarification of the relationship between the peak current instruction value and the output voltage or peak current in consideration of perturbations is presented, and the resolutions of the peak current detection circuit and the output voltage are derived. Third, the design guideline is established, and the design chart is shown. Finally, the circuit that complies with the design guideline is prototyped. The result of static characteristic analysis is verified by this experimental circuit. The output voltage stabilization characteristics and transient characteristics obtained by the prototype are also discussed as they are associated with the current instruction value and resolutions of the peak current detection circuit and output voltage. Therefore, the proposed method can be designed clearly.

II. OPERATION PRINCIPLE AND STATIC ANALYSIS OF THE PROPOSED METHOD

The resolutions of the peak current and output voltage are simply derived because the reactor current and its digital value are proportional to each other in the conventional digital control method only using ADCs. However, the reactor current and its digital value are inverse proportional to each other in the proposed method because of the following reason: Reactor current is converted into the frequency by the VCO, and the peak current instruction value is set by the time. This relationship affects the resolutions of the peak current and output voltage. This difference between the conventional digital control method and the proposed method makes the design process of the proposed method complicated. This section aims to organize the digital controller parameters of the proposed method and express their relationships by equations, for clarifying the design guideline. To this end, the operation principle of the proposed method is reviewed, and the static characteristics of the proposed method are analyzed.

Fig. 1 shows the circuit configuration of the proposed digital PCMC dc–dc converter. T_r is the main switch, R_s is a sensing resistor to detect a switch current, D_f is a flywheel diode, L is an energy storage reactor, C is an output smoothing capacitor, and R is a load. Voltages and currents are denoted as follows: i_L is a reactor current, i_{T_r} is a switch current, e_s is a voltage across R_s, E_i is an input voltage, and E_o is an output voltage. e_s is equal to $R_s i_{T_r}$. i_{T_r} is detected instead of i_L because it is equivalent to i_L when T_r is ON. An ON-time $T_{\rm on}$ of T_r is controlled using E_o and i_{T_r}. e_s and E_o are inputted into the digital control circuit. As shown in this figure, the slope compensation is implemented in the analog circuit. The design of the slope signal presented in [10] is adopted here to take advantage of PCMC when the duty ratio D is less than 50%. Then, a pulsewidth modulation (PWM) signal $S_{\rm PWM}$ is generated according to the PCMC.

Fig. 2 illustrates the architecture of the digital control circuit. E_o is feedbacked through the preamplifier #1 and the ADC. The ADC outputs the digital value $E_o[n]$ of E_o. The relationship between E_o and $E_o[n]$ is given as follows:

$$E_o\,[n] = G_{\rm AD}\, A_{eo} E_o \tag{1}$$

where A_{eo} and G_{AD} are the gains of the preamplifier #1 and ADC, respectively. E_o[n] is processed in the digital PID controller. The calculation result $N_{\rm PID}$ of the digital PID controller is sent to the digital peak current detector to obtain the peak current instruction value. $N_{\rm PID}$ at nth switching period is generally expressed as follows:

$$\begin{aligned} N_{{\rm PID},n} = {} & K_{Pi}\ \left(N_r - E_o\,[n-1]\right) + K_{Ii} \sum_{j\,=\,0}^{n-1} \left(N_r - E_o\,[j]\right) \\ & + K_{Di}\left(E_o\,[n-2] - E_o\,[n-1]\right) \end{aligned} \tag{2}$$

where N_r is a digital value of a reference voltage E_r, the proportional, integral, and differential gains are K_{Pi}, K_{Ii}, and K_{Di}, respectively. i_{T_r} is acquired as the voltage e_s using R_s. e_s is expressed as follows:

$$e_s = R_s\, i_{Tr}. \tag{3}$$

e_s is amplified by the preamplifier #2. The slope signal e_{slope} generated by the slope compensator and bias voltage E_B to adjust the operating point of the VCO are added to the amplified e_s.

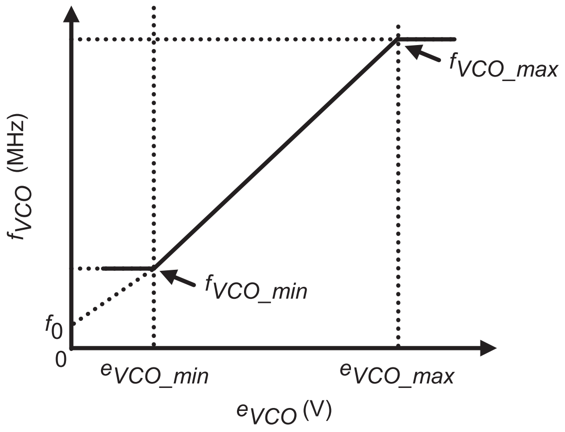


Fig. 3. Input–output characteristics of VCO.

Then, the input voltage e_{VCO} of the VCO is obtained as follows:

$$e_{\mathrm{VCO}} = A_{iTr}\, e_s + e_{\mathrm{slope}} + E_B. \tag{4}$$

The VCO outputs the frequency modulation (FM) pulse signal S_{VCO}, whose frequency f_{VCO} is proportional to the value of i_{T_r}. The VCO is utilized for peak current detection instead of a high resolution and high-speed ADC as mentioned in Section I. Assuming that the static characteristics are analyzed under the condition *D* is less than 50%, thus, e_{slope} is omitted below. The input–output characteristics of the VCO are illustrated in Fig. 3. Usually, the VCO is used in the range where f_{VCO} monotonically increases as e_{VCO} increases. The minimum and maximum values of f_{VCO} in this range are $f_{\mathrm{VCO\_min}}$ and $f_{\mathrm{VCO\_max}}$, respectively. f_{VCO} is given as

$$f_{\mathrm{VCO}} = A_{\mathrm{VCO}} e_{\mathrm{VCO}} + f_0 = A_{ICO}\, i_{Tr} + A_{\mathrm{VCO}} E_B + f_0 \tag{5}$$

where A_{VCO} is the gain of the VCO and f_0 is the intercept when the input–output characteristic of VCO is approximated linearly. A_{ICO} is the total current gain and is defined as

$$A_{ICO} = A_{\mathrm{VCO}} A_{iTr}\, R_s. \tag{6}$$

S_{VCO} is sent to the digital peak current detector. The turn-OFF signal S_{off} of T_r is outputted from the digital peak current detector when the peak current is detected. The turn-ON signal S_{on} of T_r is generated by the clock signal and sets a switching period T_s. The digital PWM (DPWM) signal generator generates S_{PWM} according to S_{on} and S_{off}.

The digital peak current detector, which is composed of the programmable delay line and a simple digital circuit, and a DPWM signal generator are shown in Fig. 4. The signal frequency detector consists of the SR latch and JK-FF as shown in this figure. S_{VCO} is sent to the programmable delay line and the signal frequency detector. $S_{\mathrm{VCO_d}}$ is the delayed signal of S_{VCO} and is generated by the programmable delay line. The multiplexer chooses a node of the delay line according to N_{PID} to control the delay of $S_{\mathrm{VCO_d}}$. The relationship between the delay time τ and N_{PID} is given as follows:

$$\tau = T_D N_{\mathrm{PID}} \tag{7}$$

where T_D is the resolution of the delay buffer in the delay line and is a conversion gain from the control signal to the peak current instruction value. As expressed in (7), τ is decided by the multiplication of N_{PID} and T_D. N_{PID} is converted into τ, which is equal to the peak current instruction value in the proposed method, using the delay line. N_{PID} is the dominant factor when τ is decided because T_D is designed as a fixed value. Although the output digital value of the PID controller to the time conversion is included, this procedure is equivalent to the analog PCMC. τ must be shorter than T_s due to the operation principle of the proposed method expressed later. $S_{\mathrm{VCO_d}}$ is sent to the signal frequency detector, which detects f_{VCO} using the phase difference between S_{VCO} and $S_{\mathrm{VCO_d}}$. The phase difference is equal to τ. S_{off} turns active when f_{VCO} is detected. The proposed method can easily correspond to the perturbation Δe_o of E_o because τ is controlled depending on e_o by the PID controller, where e_o represents $E_o + \Delta e_o$.

The timing chart of the digital peak current detector is shown in Fig. 5. This circuit consists of an asynchronous digital circuit. Ignore the rise time, fall time, and propagation delay time of elements, and assume the ideal operation in this figure. These delay times practically occur in the implemented circuit while their effects are naturally eliminated by the feedback control of E_o. Thus, the control law is not failed by tolerance of parameters, and this is an obvious difference between the proposed method and predictive current mode control. Q_1 is the output signal of the first SR latch. The active duration of Q_1 equals τ because rising edges of S_{VCO} and $S_{\mathrm{VCO_d}}$ are alternately inputted into the first SR latch. The period T_{VCO} of S_{VCO} gradually becomes short corresponding to linearly increasing i_{T_r}. S_{off} becomes active when T_{VCO} is equal to or shorter than τ. At this moment, the input terminal J of the JK-FF is high and S_{VCO} is inputted into the JK-FF as the clock signal. Thus, the digital peak current detector detects the peak value of i_{T_r} without the delay time. Note that f_{VCO} should be higher than f_s and the ratio f_{VCO}/f_s represents the sampling opportunity *M* in one switching period, as shown in Fig. 5.

Assuming that T_{VCO} is equal to τ at the detection timing, the following equation is true from (5) and (7)

$$T_{\mathrm{VCO}} = \frac{1}{f_{\mathrm{VCO}}} = \frac{1}{A_{ICO} i_{Tr}\,(T_{\mathrm{on}}) + A_{\mathrm{VCO}} E_B + f_0} = \tau \tag{8}$$

$i_{T_r}(T_{\mathrm{on}})$ in (8) is re-expressed using the following equations of the dc–dc converter, which is true in the continuous conduction mode (CCM):

$$E_o = \frac{T_{\mathrm{on}}}{T_s} \frac{E_i}{1 + \frac{r}{R}} \tag{9}$$

$$V_L = E_i - E_o = \left(1 - \frac{T_{\mathrm{on}}}{T_s} \frac{R}{R + r}\right) E_i \tag{10}$$

$$I_L = I_o = \frac{E_o}{R} = \frac{T_{\mathrm{on}}}{T_s} \frac{E_i}{R + r} \tag{11}$$

$$\begin{aligned} i_{Tr}\ (T_{\mathrm{on}}) = \frac{V_L}{2L} T_{\mathrm{on}} + I_L = & -\frac{E_i}{2L\left(1 + \frac{r}{R}\right)} \frac{{T_{\mathrm{on}}}^2}{T_s} \\ & + \frac{E_i}{r + R} \frac{T_{\mathrm{on}}}{T_s} + \frac{E_i}{2L} T_{\mathrm{on}} \end{aligned} \tag{12}$$

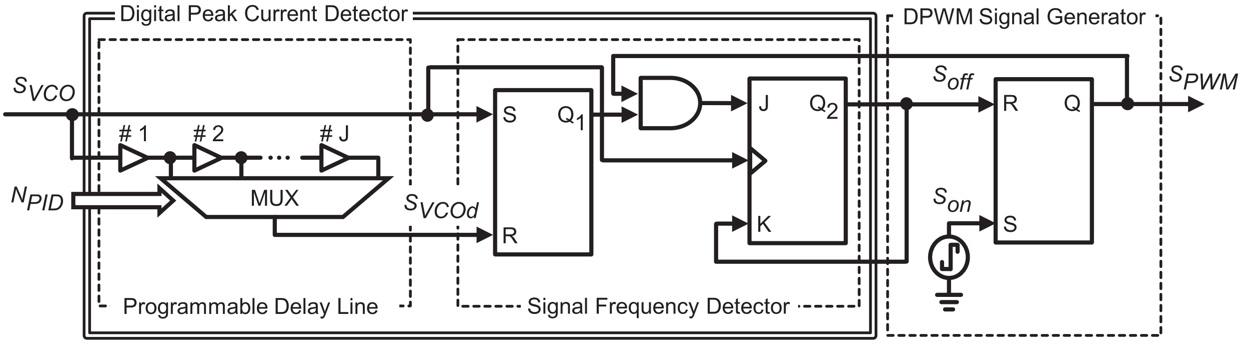
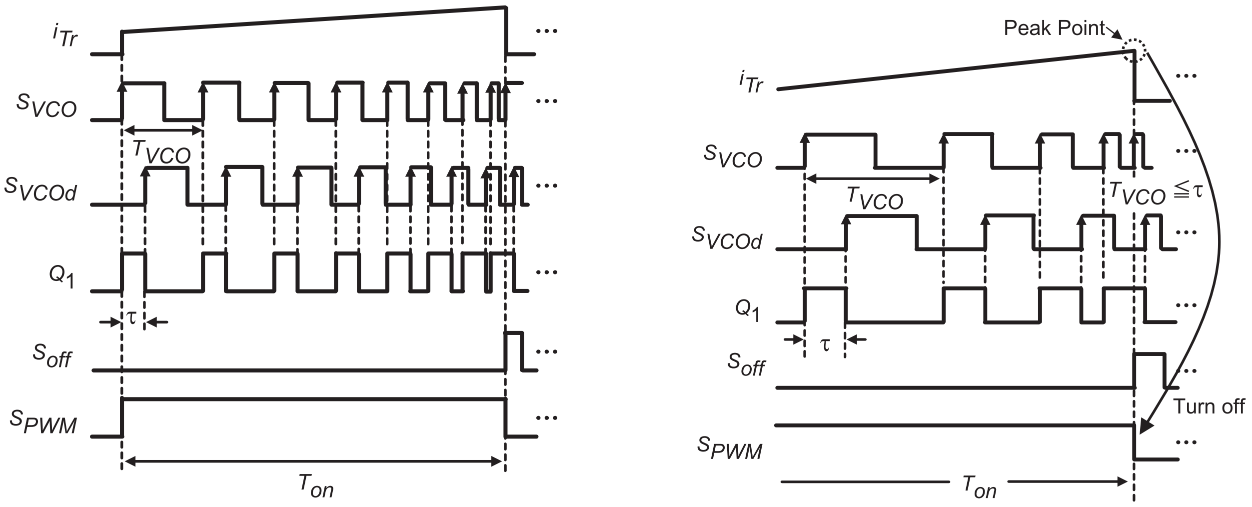


Fig. 4. Detail of a digital peak current detector and a DPWM signal generator.



(a) (b)

Fig. 5. Timing chart of a digital peak current detector. (a) Overview. (b) Detecting instant.

where r is the resistor that equivalently represents the loss of the circuit, I_L is the average current of i_L, and V_L is the voltage across L.

From (8) and (12), the following equation is derived:

$$\left(\frac{T_{\text{on}}}{T_s}\right)^2 - \frac{2L+(r+R)\,T_s}{T_sR}\frac{T_{\text{on}}}{T_s} + \frac{2L\left(1+\frac{r}{R}\right)}{T_sA_{iTr}R_sE_i} \left\{\frac{1}{A_{\text{VCO}}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\} = 0. \quad (13)$$

Therefore, T_{on}/T_s of the proposed method is expressed as

$$\frac{T_{\text{on}}}{T_s} = \frac{-b-\sqrt{b^2-4ac}}{2a} \quad \left(0 \leq \frac{T_{\text{on}}}{T_s} \leq 1\right) \quad (14)$$

where a, b, and c are given as follows:

$$a = 1 \quad (15)$$

$$b = -\frac{2L+(r+R)\,T_s}{T_sR} \quad (16)$$

$$c = \frac{2L\left(1+\frac{r}{R}\right)}{T_sA_{iTr}R_sE_i} \left\{\frac{1}{A_{\text{VCO}}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}. \quad (17)$$

See Appendix II about the existence range of solutions of (13).

When (14) is substituted into (9), an equation of the proposed method concerned with E_o is obtained as follows:

$$E_o = \frac{E_i}{1+\frac{r}{R}}\,\frac{-b-\sqrt{b^2-4ac}}{2a}. \quad (18)$$

From (7) and (8), the relationship between f_{VCO} and N_{PID} normalized by f_s is also derived as follows:

$$\frac{f_{\text{VCO}}}{f_s} = \frac{1}{\frac{T_D}{T_s}N_{\text{PID}}}\,. \quad (19)$$

f_{VCO} is inverse proportion to N_{PID} in the proposed method. This inverse proportional relationship is different from the conventional digital control [20]–[22], and this relationship make the resolutions of the proposed method complicated as will be derived later.

Perturbations are considered in (13) to derive the equations expressing the resolutions of the peak current and output voltage (20) shown at the bottom this page.

From (20), an equation concerned with perturbations is obtain as follows:

$$\begin{aligned}&\left(\frac{2T_{\text{on}}}{T_s}+b\right)\frac{\Delta T_{\text{on}}}{T_s}+\frac{2L\left(1+\frac{r}{R}\right)}{T_sA_{ICO}E_i\tau^2}\Delta\tau-\frac{1}{T_sR^2}\\&\left[\frac{T_{\text{on}}}{T_s}\left(2L+rT_s\right)+\frac{2rL}{A_{iTr}R_sE_i}\left\{\frac{1}{A_{\text{VCO}}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}\right]\\&\Delta R+\frac{c}{E_i}\Delta\, e_i=\ 0.\end{aligned}\tag{21}$$

Normalized $\Delta\tau$ by T_s is given by following equations from (7):

$$\frac{\tau+\Delta\tau}{T_s}=\frac{T_D}{T_s}\ \left(N_{\text{PID}}+\Delta N_{\text{PID}}\right)\tag{22}$$

$$\frac{\Delta\tau}{T_s}=\frac{T_D}{T_s}\ \Delta N_{\text{PID}}.\tag{23}$$

From (19), the relationship between Δf_{VCO} and ΔN_{PID} is obtained as follows:

$$\begin{aligned}\frac{f_{\text{VCO}}+\Delta f_{\text{VCO}}}{f_s}&=\frac{1}{\frac{T_D}{T_s}\left(N_{\text{PID}}-\Delta N_{\text{PID}}\right)}\\&=\frac{\left(N_{\text{PID}}+\Delta N_{\text{PID}}\right)}{\frac{T_D}{T_s}\left(N_{\text{PID}}-\Delta N_{\text{PID}}\right)\left(N_{\text{PID}}+\Delta N_{\text{PID}}\right)}\\&\approx\frac{N_{\text{PID}}+\Delta N_{\text{PID}}}{\frac{T_D}{T_s}{N_{\text{PID}}}^2}\end{aligned}\tag{24}$$

$$\frac{\Delta f_{\text{VCO}}/f_s}{\Delta N_{\text{PID}}}\approx\frac{1}{\frac{T_D}{T_s}{N_{\text{PID}}}^2}.\tag{25}$$

Equation (25) shows the resolution when the PID controller operates at the peak current. It is affected by the value of N_{PID} and is not constant. This relationship affects the resolution of E_o.

Here, the equations are further organized such as the case of the analog PCMC to indicate the relationship between the peak current and the current instruction value. From (5), (7), and (19), $(\Delta f_{\text{VCO}}/f_s)/\Delta i_{T_r}$ and $\Delta i_{T_r}/(\Delta\tau/T_s)$ are similarly given and shown through the following equations:

$$\begin{aligned}&\frac{f_{\text{VCO}}+\Delta f_{\text{VCO}}}{f_s}=\frac{A_{ICO}(i_{Tr}+\Delta i_{Tr})+A_{\text{VCO}}E_B+f_0}{f_s}\\&=\frac{1}{\frac{T_D}{T_s}(N_{\text{PID}}-\Delta N_{\text{PID}})}=\frac{1}{\frac{\tau-\Delta\tau}{T_s}}=\frac{\tau+\Delta\tau}{\frac{(\tau-\Delta\tau)(\tau+\Delta\tau)}{T_s}}\approx\frac{\tau+\Delta\tau}{\frac{\tau^2}{T_s}}\end{aligned}\tag{26}$$

$$\frac{\frac{\Delta f_{\text{VCO}}}{f_s}}{\Delta i_{Tr}}=\frac{A_{ICO}}{f_s}\tag{27}$$

$$\frac{\Delta i_{Tr}}{\frac{\Delta\tau}{T_s}}=\frac{1}{\frac{\tau^2}{T_s}A_{ICO}}\ .\tag{28}$$

Equation (27) is the relationship between i_{T_r} and its sensed value. Equation (28) is rearranged equation of (25) using (23) and (27) to yield the relationship between i_{T_r} and τ. This modification makes the design of the proposed method simpler. The input–output characteristics of the VCO and the resolution of the delay line affect this relationship. It is revealed that they are important parameters when the proposed method is designed. In addition, the resolution of i_{T_r} cannot be simply expressed by A_{ICO} unlike the conventional digital control and changes depending on the value of τ.

In order to derive the resolutions of E_o, the resolutions $(\Delta T_{\text{on}}/T_s)/(\Delta\tau/T_s)$, $(\Delta T_{\text{on}}/T_s)/\Delta R$, and $(\Delta T_{\text{on}}/T_s)/\Delta e_i$ are also derived from (21), respectively

$$\frac{\frac{\Delta T_{\text{on}}}{T_s}}{\frac{\Delta\tau}{T_s}}=-\frac{2L\left(1+\frac{r}{R}\right)}{\left(\frac{2T_{\text{on}}}{T_s}+b\right)A_{ICO}E_i\tau^2}\tag{29}$$

$$\begin{aligned}\frac{\frac{\Delta T_{\text{on}}}{T_s}}{\Delta R}&=\frac{1}{T_sR^2\left(\frac{2T_{\text{on}}}{T_s}+b\right)}\\&\left\{\frac{2rL}{A_{iTr}R_sE_i}\left\{\frac{1}{A_{\text{VCO}}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}\right.\\&\left.+\frac{T_{\text{on}}}{T_s}\left(2L+rT_s\right)\right\}\end{aligned}\tag{30}$$

$$\frac{\frac{\Delta T_{\text{on}}}{T_s}}{\Delta e_i}=-\frac{c}{E_i\left(\frac{2T_{\text{on}}}{T_s}+b\right)}.\tag{31}$$

Perturbations in (9) is expressed as

$$\Delta\, e_o=\frac{1}{1+\frac{r}{R}}\ \left(E_i\frac{\Delta T_{\text{on}}}{T_s}+\frac{T_{\text{on}}}{T_s}\Delta e_i+\frac{E_o}{R}\Delta R\right).\tag{32}$$

The resolutions $\Delta e_o/(\Delta\tau/T_s)$, $\Delta e_o/\Delta\ R$, and $\Delta e_o/\Delta e_i$ are also derived using (29)–(32)

Focusing on (33), the resolution of E_o is as complex as (28) because of τ on the right side.

From the above equations, i_{T_r} and τ are inversely proportional to each other as described in (8). From (28) and (33), the resolutions of i_{T_r} and E_o are influenced by the value of τ. These equations organize the controller parameters and make

$$\begin{aligned}&\left(\frac{T_{\text{on}}}{T_s}+\frac{\Delta T_{\text{on}}}{T_s}\right)^2-\frac{2L+\{r+(R+\Delta R)\}T_s}{T_s(R+\Delta R)}\left(\frac{T_{\text{on}}}{T_s}+\frac{\Delta T_{\text{on}}}{T_s}\right)+\frac{2L\left(1+\frac{r}{(R+\Delta R)}\right)}{T_sA_{iTr}R_s(E_i+\Delta e_i)}\left\{\frac{1}{A_{\text{VCO}}}\left(\frac{1}{\tau-\Delta\tau}-f_0\right)-E_B\right\}\\&=\left(\frac{T_{\text{on}}}{T_s}+\frac{\Delta T_{\text{on}}}{T_s}\right)^2-\frac{2L(R-\Delta R)+\{r+(R+\Delta R)\}(R-\Delta R)T_s}{T_s(R+\Delta R)(R-\Delta R)}\left(\frac{T_{\text{on}}}{T_s}+\frac{\Delta T_{\text{on}}}{T_s}\right)\\&+\frac{2L\left(1+\frac{r(R-\Delta R)}{(R+\Delta R)(R-\Delta R)}\right)}{T_sA_{iTr}R_s(E_i+\Delta e_i)(E_i-\Delta e_i)}\left\{\frac{1}{A_{\text{VCO}}}\left(\frac{\tau+\Delta\tau}{(\tau-\Delta\tau)(\tau+\Delta\tau)}-f_0\right)-E_B\right\}\\&\approx a\left(\frac{T_{\text{on}}}{T_s}\right)^2+b\frac{T_{\text{on}}}{T_s}+c+\left(\frac{2T_{\text{on}}}{T_s}+b\right)\frac{\Delta T_{\text{on}}}{T_s}+\frac{2L\left(1+\frac{r}{R}\right)}{T_sA_{ICO}E_i\tau^2}\\&\Delta\tau-\frac{1}{T_sR^2}\left[\frac{T_{\text{on}}}{T_s}\left(2L+rT_s\right)+\frac{2rL}{A_{iTr}R_sE_i}\left\{\frac{1}{A_{\text{VCO}}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}\right]\Delta R+\frac{c}{E_i}\Delta e_i=0\end{aligned}\tag{20}$$

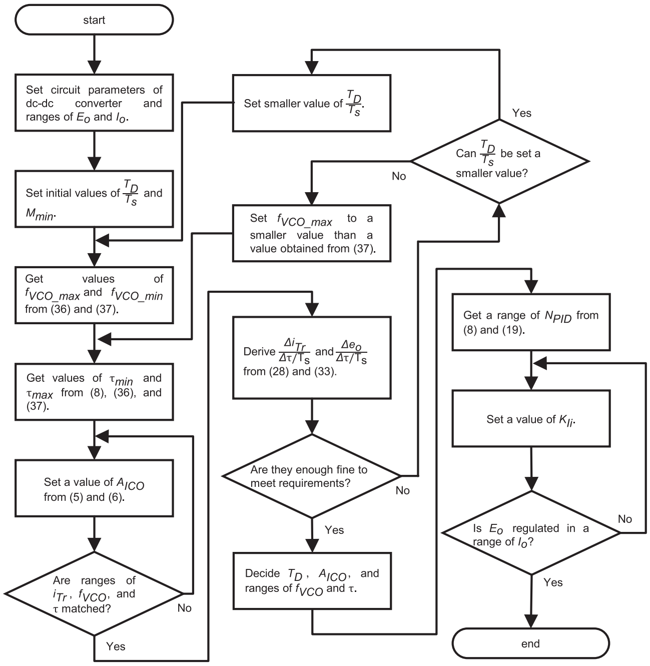


Fig. 6. Design chart of the proposed method.

their relationships clear. They are also very important in showing the design guidelines of the proposed method.

In Section III, the design guideline and design chart of the proposed method will be presented while considering the results focusing on τ.

III. DESIGN GUIDELINE AND DESIGN CHART OF THE PROPOSED METHOD

The proposed method was designed without the design guideline so far. Therefore, the design included controller parameters whose decision process was unclear. This section describes a design guideline using the design chart of the proposed method shown in Fig. 6 to deal with this issue. At the beginning of the design, set circuit parameters of the dc–dc converter and operation ranges of E_o and I_o as a fundamental specification. Initial values of T_D /T_s and $M_{\min}$ are set, where $M_{\min}$ is the minimum sampling opportunity when I_o is the lowest value in its operation range. From (28) and (33), finer resolution can be obtained when small values of T_D /T_s and $M_{\min}$ are chosen, while enough sampling opportunity should be secured. $M_{\min}$ cannot be an immoderately small value. According to these values, the values of $f_{\mathrm{VCO\_min}}$ and $f_{\mathrm{VCO\_max}}$ are obtained as follows:

$$f_{\mathrm{VCO\_min}} = M_{\min}\, f_s \tag{36}$$

$$f_{\mathrm{VCO\_max}} = \frac{1}{T_D}\,. \tag{37}$$

The range of f_{VCO} is limited by (36) and (37). Minimum and maximum values, i.e., $\tau_{\min}$ and $\tau_{\max}$, of τ is derived by (8), (36), and (37). The range of τ is also limited by these derived values. A value of A_{ICO}, which is expressed as the multiplication of R_s, $A_{i\,Tr}$, and A_{VCO}, is set using (5) and (6) so that ranges of i_{T_r}, f_{VCO}, and τ match within their minimum and maximum values. E_B may be applied to e_{VCO} for adjusting the operation range of f_{VCO}. When the range is mismatch, obtain and set a value for A_{ICO} again. After the setting of A_{ICO}, resolutions of the controller are derived from (28) and (33). Equation (28) is mainly influenced by the value of τ. On the other hand, (33) includes not only τ but also circuit parameters. Notice that values of R and E_i are involved.

When the resolutions cannot meet requirements, change the value of T_D /T_s to a smaller one and go back before getting $f_{\mathrm{VCO\_min}}$ and $f_{\mathrm{VCO\_max}}$. When T_D /T_s cannot be set to a smaller value, set $f_{\mathrm{VCO\_max}}$ to a value smaller than the value determined by (37). The value of T_D, ranges of f_{VCO} and τ, and A_{ICO} are decided when resolutions meet requirements. Then, get a range of N_{PID} from (8) and (19). K_{Ii} in the PID controller is tuned to cover the range of N_{PID} because the integral control is dominant in the steady state and influences the regulation of E_o. When E_o is not regulated over the range of I_o, change the value of K_{Ii} to a larger one. K_{Ii} is decided when E_o is regulated over the range of I_o, and then, the design chart ends.

In the actual design, the linear input–output characteristics of the VCO in a wide range are needed to cover a wider range of i_L. The value of T_D /T_s depends on the hardware performance of the delay line. This would limit the accuracy of the peak current and output voltage of the proposed method. When the proposed method is implemented into the switching power supply with a higher switching frequency, f_{VCO} should be higher to secure the value of $M_{\min}$. Accordingly, a smaller value of T_D/T_s is needed. Higher hardware performance of the delay line is required. Additionally, it should be considered that an extremely high operating frequency of VCO would lead to its unstable operation.

$$\frac{\Delta e_o}{\frac{\Delta\tau}{T_s}} = -\frac{2L}{\left(\frac{2T_{\mathrm{on}}}{T_s}+b\right) A_{ICO}\tau^2} \tag{33}$$

$$\frac{\Delta e_o}{\Delta R} = \frac{1}{1+\frac{r}{R}}\left[\frac{E_o}{R} + \frac{1}{T_s R^2\left(\frac{2T_{\mathrm{on}}}{T_s}+b\right)}\left\{\frac{2rL}{A_{iTr}R_sE_i}\left\{\frac{1}{A_{\mathrm{VCO}}}\left(\frac{1}{T_D N_{\mathrm{PID}}} - f_0\right) - E_B\right\} + \frac{2T_{\mathrm{on}}}{T_s}\left(2L + rT_s\right)\right\}\right] \tag{34}$$

$$\frac{\Delta e_o}{\Delta e_i} = -\frac{1}{1+\frac{r}{R}}\left(\frac{2L+rT_s}{T_sR} + \frac{c}{\frac{2T_{\mathrm{on}}}{T_s}+b}\right) \tag{35}$$

TABLE I
CIRCUIT PARAMETERS

E_i	20 V	R_s	0.05 Ω
$E_o{}^*$	5 V	A_{iTr}	23.5
$I_o{}^*$	1 A	A_{VCO}	2.75 MHz / V
f_s	100 kHz	A_{ICO}	3.23 MHz / A
T_s	10 µs	E_B	2.1 V
L	194 µH	f_0	-2.38 MHz
C	123 µF	T_D	1 ns
r	0.5 Ω	A_{eo}	0.25
R	5 Ω	G_{AD}	409.4 V^{-1}

From the above results, the design chart clarifies the design procedure of the proposed method. The decision of the controller parameters using the equations derived in Section II is described. Thus, the proposed method can be designed to meet the requirements for the switching power supply by following these design guideline and design chart.

IV. THEORETICAL AND EXPERIMENTAL RESULTS

In this section, the result of static characteristic analysis is confirmed using the prototype of the proposed method, which is designed based on the design chart mentioned above. The validity of the design guideline and design chart is similarly confirmed. After that, the output voltage stabilization characteristics and transient characteristics are demonstrated.

In the prototype, SPARTAN-3, which is a field programmable gate array (FPGA) from Xilinx and whose speed grade is -4, is utilized for the digital peak current detector. The PID control is executed by a digital signal processor (DSP) TMS320C6713 from TI. The ADC features the 11-b resolution and 1.2-μs sampling period. It can be configured with an inexpensive PWM-dedicated DSP or FPGA for the digital PID control, although this DSP is utilized in this prototype [21], [37].

The design of the prototype is explained along with the design chart. The operation and static characteristic analysis is confirmed in an experiment. Circuit parameters are summarized in Table I. They are used for deriving the theoretical value given below. $E_o{}^*$ is a target voltage of E_o. The rated current $I_o{}^*$ of I_o is set to 1 A to make the calculation process easier to understand in this article. By adjusting the parameters of the sensing resistor and the gain of the preamplifier, the equation and design chart in this article can be applied as they are even when the rated current increases. For instance, the sensing resistor should be changed from 0.05 to 0.01 Ω when the rated current becomes 5 A. The range of I_o is set from 0.1 to 1.5 A, and a ripple current of i_L is 0.1 A. In the experiment, I_o is in the range of 0.2–1.5 A to ensure that the dc–dc converter is operated in CCM. D is less than 50% in the steady state. A_{eo} is a gain of the preamplifier for detecting e_o. This preamplifier adjusts the range of e_o to the input voltage range of ADC, which is from 0 to 5 V. A_{eo} is set to 0.25 because the maximum value of e_o is 20 V. G_{AD} is the A–D conversion gain of the ADC and is calculated by its resolution and input voltage range; its calculated value is 409.4 V^{-1}.

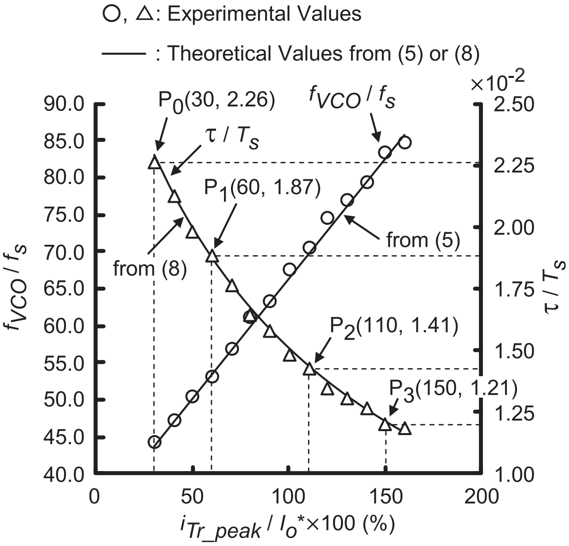


Fig. 7. Operation range of f_{VCO}/f_s and τ/T_s according to $i_{Tr\_\mathrm{peak}}/I_o{}^* \times 100$.

From the data sheet of SPARTAN-3 [54], the propagation time for data transition is 0.61 ns when the speed grade is -4. For this reason, T_D is set to 1 ns including the wire delay for easy calculation. The wiring is manually tuned to eliminate variations in each delay element in the delay line. Therefore, the initial value of T_D / T_s is 1×10^{-4}. From (37), $f_{\mathrm{VCO\_max}}$ is calculated as 1 GHz. The initial value of $M_{\min}$ is 40, in this article, so that the minimum value of T_{on} becomes 2.5% of T_s even when I_o becomes the lowest value. In this situation, f_{VCO} is equal to 4 MHz calculated using (36) and is higher than f_s. At this condition, A_{ICO} is designed to be 711 MHz/A. However, the resolution of the controller cannot meet the requirement in such a high frequency operation range of the VCO. Moreover, it is difficult for the VCO to operate stably. $f_{\mathrm{VCO\_max}}$ is redesigned and set to 8.5 MHz to make $\Delta i_{T_r}/(\Delta\tau / T_s)$ and $\Delta e_o/(\Delta\tau/T_s)$ 16 mA and 70 mV at $I_o{}^*$, respectively. In the prototype, 16 mA is 1.6% of $I_o{}^*$ and 70 mV is 1.4% of $E_o{}^*$. Then, A_{ICO} is redesigned to be 3.21 MHz/A. The operation ranges of f_{VCO}/f_s and τ / T_s corresponding to $i_{Tr\_\mathrm{peak}}/I_o{}^* \times 100$ are shown in Fig. 7. i_{Tr_peak} is the peak current of i_{T_r}. The theoretical values are obtained from (5) or (8). A_{ICO} obtained from this experimental result is 3.23 MHz/A, which matches the designed value well. In this article, f_0 is -2.38 MHz by linearly approximating the input–output characteristics of the VCO, as indicated in (4) and (5). In the same way, E_B is set to 2.1 V so that f_{VCO} becomes 4 MHz when I_o has the smallest value (0.1 A). The experimental values almost match the theoretical value. f_{VCO} is proportional to i_{Tr_peak} and there is a one-to-one correspondence among f_{VCO}, τ, and i_{Tr_peak}. It is revealed that ranges of f_{VCO} and τ correspond to i_{T_r}. It can be seen that f_{VCO} is in the range of 4.4–8.5 MHz and τ is in the range of 230–115 ns. f_{VCO} and τ are within their minimum and maximum values. Operating points P_0, P_1, P_2, and P_3 are shown, and their coordinates indicate $i_{Tr\_\mathrm{peak}}/I_o{}^* \times 100$ and τ/T_s. These correspond to P_0, P_1, P_2,

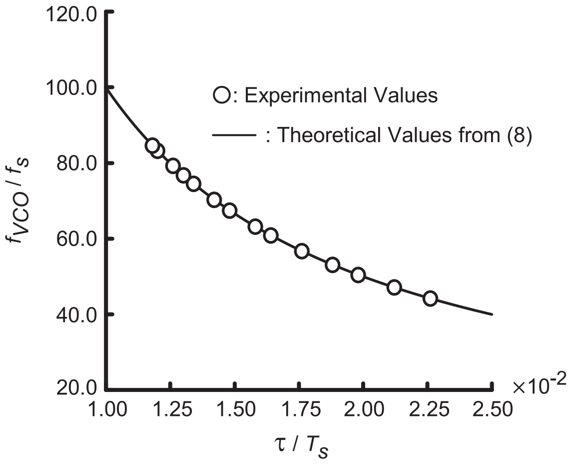
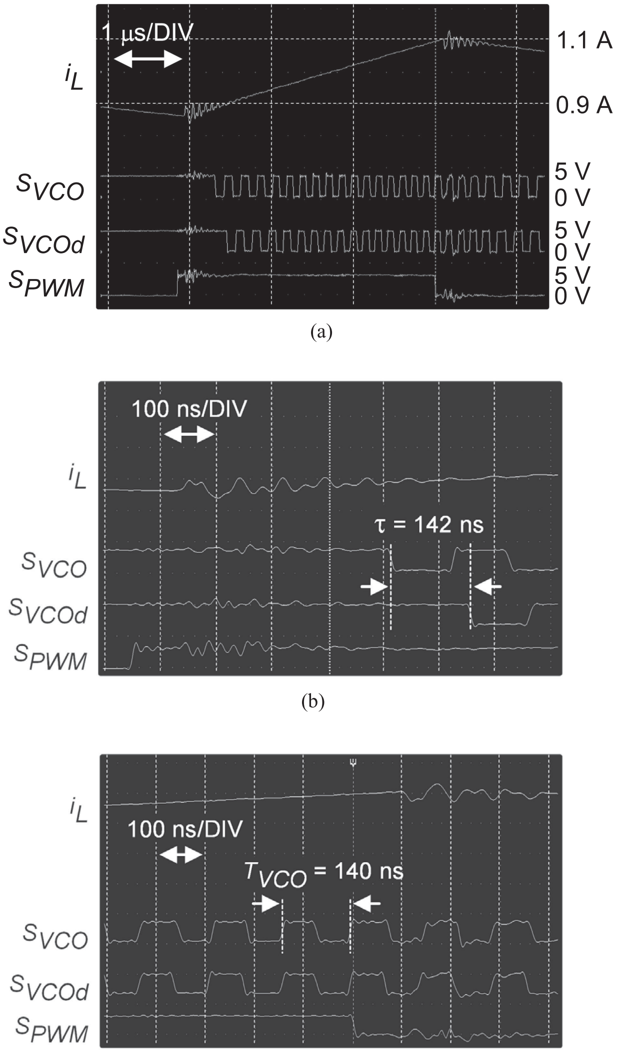


Fig. 8. Relationship between f_{VCO}/f_s and τ/T_s.



(a)

(b)

(c)

Fig. 9. Experimental waveforms of peak current detection. (a) Overview. (b) Enlarged view at start. (c) Enlarged view at peak point.

and P_3 in Fig. 13. Additionally, the relationship between f_{VCO}/f_s and τ/T_s is derived from (8) and shown in Fig. 8. This is an important relationship in the proposed method because f_{VCO} and τ are equivalent to i_{T_r} and the peak current instruction value, respectively. The experimental values validate this relationship, as shown in this figure. From the above data, the values of T_D and A_{ICO} are decided. Ranges of f_{VCO} and τ are also decided.

An experimental waveform of the peak current detection in the proposed method at $I_o{}^*$ is shown in Fig. 9. τ is set to 142 ns. The operating point is matched with the point P_2 shown in Fig. 7. When T_{VCO} is shorter than or equal to τ, S_{PWM} is turned OFF immediately. In this figure, S_{PWM} is turned OFF when T_{VCO} reaches 140 ns. Note that a photocoupler and a drive IC are implemented between the FPGA and T_r. There is a 100-ns delay time caused by propagation time, rising time, and falling time in these components. From Fig. 9, the proposed method works well in accordance with the principle and can realize real-time detection of a peak current.

Next, the resolutions of the controller are confirmed. Fig. 10 shows the relationship between $\Delta i_{T_r}/(\Delta\tau/T_s)$ and τ/T_s from (28). The theoretical value and experimental values have consistency. Thus, the static characteristic analysis has enough validity. In this article, $\Delta i_{T_r}/(\Delta\tau/T_s)$ is 14 mA at $I_o{}^*$, which is 1.4% of $I_o{}^*$. When τ (f_{VCO}) is set to a small (large) value, $\Delta i_{T_r}/(\Delta\tau/T_s)$ becomes large. This brings a high possibility of the occurrence of a limit cycle oscillation. For instance, $\Delta i_{T_r}/(\Delta\tau/T_s)$ becomes 53 mA at 1 A ($=I_o{}^*$) when only the operating point of $\Delta\tau/T_s$ at $I_o{}^*$ is changed from 1.41 $\times 10^{-2}$ (black circle) to 1.06×10^{-2} (black triangle). f_{VCO} turns out to be about 10 MHz at the black triangle point.

The relationship between $\Delta e_o/(\Delta\tau/T_s)$ and τ/T_s from (33) is described in Fig. 11. The theoretical value and experimental value are well matched. $\Delta e_o/(\Delta\tau/T_s)$ is, in this article, 64 mV at $I_o{}^*$, which is 1.28% of $I_o{}^*$. When τ (f_{VCO}) becomes a small (large) value, $\Delta e_o/(\Delta\tau/T_s)$ becomes large, as well as the discussion in Fig. 10 and the limit cycle oscillation would occur. $\Delta e_o/(\Delta\tau/T_s)$ becomes 261 mV at 5 V ($=E_o{}^*$) when the operating point of $\Delta\tau/T_s$ at $I_o{}^*$ is changed in the same way as shown in Fig. 10.

From Figs. 10 and 11, (28) and (33) are important to describe the performance of the proposed method and cannot be ignored in the design process of deciding the range of τ (f_{VCO}). By the static characteristic analysis, resolutions of i_{T_r} and E_o can be grasped. It makes the design process of the proposed method simpler.

After the decision of parameters, the relationship between ($E_o - E_o{}^*$)/$E_o{}^* \times 100$ and τ/T_s from (14) and (18) is confirmed and is shown in Fig. 12. This result shows that E_o can be set by τ in the vicinity of $I_o = I_o{}^*$. The experimental values exist along with the theoretical values. This result reveals the relationship between E_o and τ in the proposed method, which is derived in Section II. As shown in this figure, E_o is regulated into $E_o{}^*$ at P_2, and τ/T_s is 1.41×10^{-2}. It is the proper operation of the proposed method because this result is derived and measured in the condition $I_o = I_o{}^*$.

Fig. 13 is an experimental result of E_o versus I_o characteristics of the proposed method when K_{Ii} is set to 0.003 to verify a proper operation in the steady state. Coordinates of P_0, P_1, P_2, and P_3 indicate $I_o/I_o{}^* \times 100$ and ($E_o - E_o{}^*$)/$E_o{}^* \times 100$. K_{Ii} is tuned to

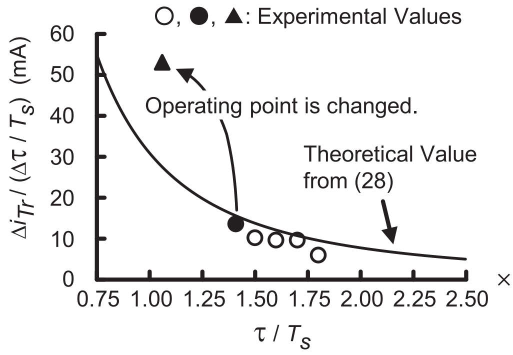


Fig. 10. Relationship between $\Delta i_{T_r}/(\Delta\tau/T_s)$ and τ/T_s.

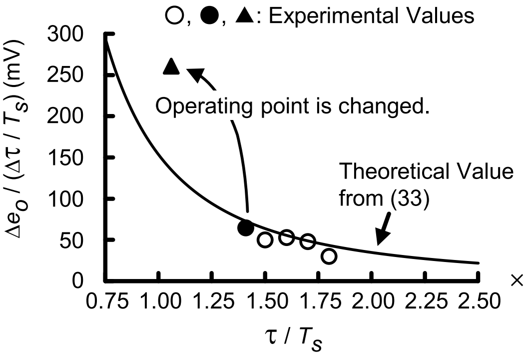


Fig. 11. Relationship between $\Delta e_o/(\Delta\tau/T_s)$ and τ/T_s.

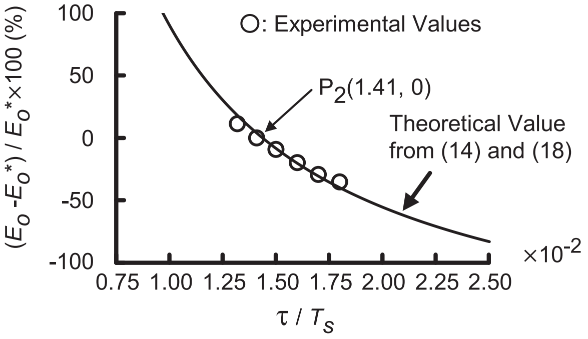


Fig. 12. Relationship between $(E_o - E_o{}^*) \times 100/E_o{}^*$ and τ/T_s.

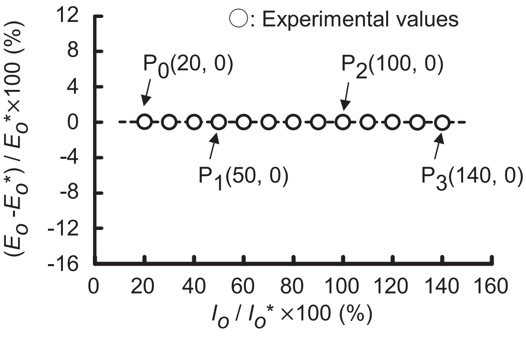


Fig. 13. Experimental result of E_o versus I_o characteristics of the proposed method.

TABLE II
MEASURED STATIC CHARACTERISTICS AT $E_O = E_O{}^*$

	I_o	τ / T_s	$\Delta i_{Tr} / (\Delta\tau / T_s)$	$\Delta e_o / (\Delta\tau / T_s)$
P$_0$	0.2 A	2.26×10^{-2}	4 mA (6 mA)	71 mV (116 mV)
P$_1$	0.5 A	1.87×10^{-2}	6 mA (9 mA)	51 mV (78 mV)
P$_2$	1.0 A (= I_o*)	1.41×10^{-2}	14 mA (16 mA)	64 mV (73 mV)
P$_3$	1.4 A	1.21×10^{-2}	17 mA (21 mA)	88 mV (72 mV)

regulate E_o over the range of I_o. A guideline for setting K_{Ii} in this prototype is briefly explained here. The operation amount of the integral control is calculated by the multiplication of K_{Ii} and the value N_I of the integral register in the digital PID controller. From the range of τ, the range of $N_{\rm PID}$ is derived by (8) and (19). It is considered from 100 to 250, including a margin. The range of N_I is set from $-32\,000$ to 32 000, which is about 16 b, in the prototype. When the bias value N_B of PID control is set to 175, which is the center of the range of $N_{\rm PID}$, the multiplication of K_{Ii} and N_I must be larger than or equal to 75. Therefore, K_{Ii} must be larger than or equal to 0.0023. Here, K_{Ii} is set to 0.003. As a result, E_o is well regulated from 20% to 140% of $I_o{}^*$.

At operating points from P$_0$ to P$_3$, I_o, τ/T_s, $\Delta i_{T_r}/(\Delta\tau/T_s)$, and $\Delta e_o/(\Delta\tau/T_s)$ are summarized in Table II. Here, E_o is regulated into 5 V ($= E_o{}^*$), as shown in Table I. Theoretical values are written in brackets. From Table II, experimental results are close to theoretical values, and their tendency is similar to the theoretical values. $\Delta i_{T_r}/(\Delta\tau/T_s)$ becomes finer as I_o (τ) becomes a small (large) value as mentioned above. $\Delta i_{T_r}/(\Delta\tau/T_s)$ at P$_3$ changes about four times in the experimental result compared with P$_0$. Although $\Delta e_o/(\Delta\tau/T_s)$ also becomes finer according to decreasing (increasing) I_o (τ), the value of R also affects $\Delta e_o/(\Delta\tau/T_s)$ as shown in (33). The influence of E_i is ignored since E_i is constant in this experiment. $\Delta e_o/(\Delta\tau/T_s)$ is almost the same value for the full load range by the influence of both τ and R, and it is from about 50 to about 90 mV. The proper operation of the proposed method in the steady state is verified. It is clear that $\Delta i_{T_r}/(\Delta\tau/T_s)$ and $\Delta e_o/(\Delta\tau/T_s)$ should be considered in the design process because they are affected by the operating point of I_o. The resolutions of i_{T_r} and E_o in the proposed method can be comprehended, and then, the proposed method can be completely designed for the first time, covering the full range of I_o. It is also found from the result that the resolutions of i_{T_r} and E_o have a close relation with τ.

The transient response of the proposed method in a simulation is indicated in Fig. 14. The load is changed suddenly from P$_1$ to P$_2$, which are shown in Figs. 7 and 13. K_{Pi} and K_{Di} are set to 2 and 1, respectively. K_{Ii} is set to 0.1. An undershoot $\delta e_{o\_\rm under}$ of e_o is 3.2%, where e_o represents a dynamic change of E_o. A convergence time $t_{\rm cv}$ until e_o converges within plus or minus 1% of $E_o{}^*$ is 317 μs. An overshoot of i_L is suppressed and almost zero. τ/T_s changes from 1.87×10^{-2} to 1.41×10^{-2} , although the limit cycle oscillation occurs. This result corresponds to P$_1$ and P$_2$ in Fig. 7. Similarly, e_o is regulated before and after the transient state. The transient response of the proposed method in the experiment corresponding to Fig. 14 is indicated

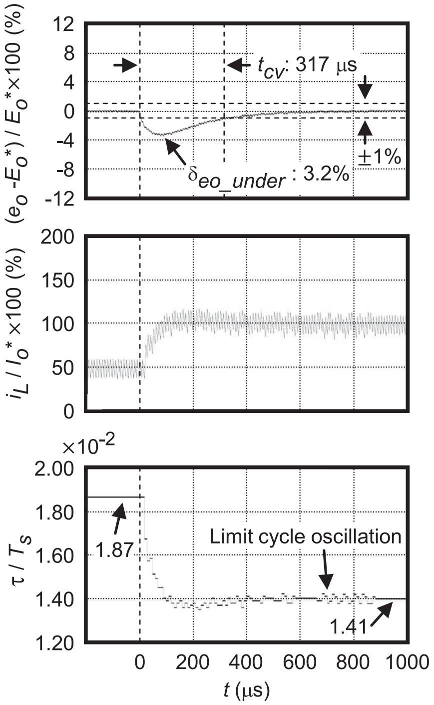


Fig. 14. Transient response of e_o, i_L, and τ of the proposed method in simulation.

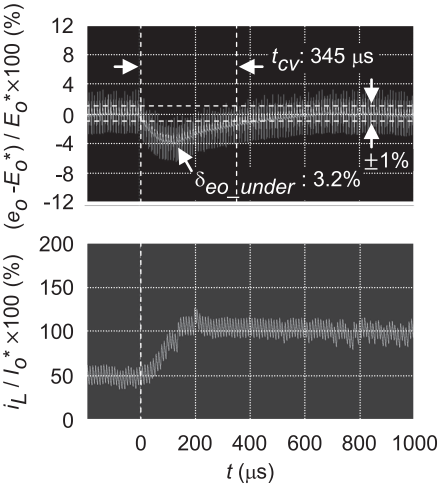


Fig. 15. Transient response of e_o and i_L of the proposed method in the experiment.

in Fig. 15. $\delta e_{o\_\mathrm{under}}$ and t_{cv} are 3.2% and 345 μs, respectively. An overshoot of i_L is suppressed, as well as the simulation. The simulation and experimental results are equivalent and reveal the proper operation of the proposed method in the transient state.

V. CONCLUSION

In this article, the static characteristic analysis of the digital peak current mode dc–dc converter using current–frequency conversion is presented to organize the relationship between controller parameters. Especially, the effect on the performance of the proposed method caused by the inverse proportional relationship between the peak current and the current instruction value is expressed by the equations. This analysis reveals that the peak current instruction value is related to the resolutions of the peak current detection circuit and output voltage, which are important to design. These relationships are also expressed by equations. Based on this result, the design guideline and design chart of the proposed method are established. The selection of the controller parameters is explained when the prototype is implemented following this guideline. By following this guideline, it is clarified that the VCO operating frequency and the resolutions of the delay line, reactor current, and output voltage can be smoothly designed according to requirements for the switching power supply. Thus, the unclear part in the design process of the proposed method is eliminated. The experimental result verifies the static characteristic analysis. In the prototype circuit, at the operating point 5 V - 1 A, the peak current resolution is 14 mA and the output voltage resolution is 64 mV, confirming that they are matched to theoretical values. The output voltage stabilization characteristics and transient characteristics obtained experimentally show the proper operation of the proposed method. Their association with the current instruction value and resolutions of peak current detection circuit and output voltage also becomes clear. This proves that the design guideline is valid.

It is obvious that the proposed method can be an optimal method when the digital PCMC is implemented into the switching power supply because the proposed method can capture the peak current in real time and improve the stability. In conclusion, the proposed method cannot be designed to suit the requirements of various applications without this analysis result, which provides the design guideline. This article can promote the development of the digital PCMC switching power supply.

APPENDIX I
OVERVIEW OF DIGITAL PCMC

A. Analog PCMC

The PCMC dc–dc converter using the analog control circuit is briefly explained. Figs. 16 and 17 show the circuit configuration of the PCMC dc–dc converter and its operation waveforms. The main circuit is the buck-type converter. ε is the peak current instruction value, which is generated based on an error signal between E_o and E_r. Toff is an OFF-time of T_r. A comparator compares ε and e_s. When e_s reaches ε, S_{off} becomes active and S_{PWM} is turned OFF. An unstable operation occurs when D exceeds 50% in the PCMC. A slope compensation is needed to avoid it [10], and a slope signal is added as shown in Fig. 16. e_s with or without the slope signal is shown in Fig. 17. A peak current of i_{T_r} is controlled according to this procedure. Thus, the PCMC can significantly improve the stability of the dc–dc converter by injecting i_{T_r} into the controller. This is an important fundamental concept of the PCMC.

The block diagram of the PCMC dc–dc converter using an analog controller [9]–[19] is shown in Fig. 18. $G_{deo}(s)$ is a transfer function from $\Delta D(s)$ to $\Delta e_o(s)$ of the dc–dc converter. $\Delta D(s)$ and $\Delta e_o(s)$ are Laplace transformed perturbations of D and E_o, respectively. $G_{diL}(s)$ is a transfer function from $\Delta D(s)$ to $\Delta i_L(s)$ of the dc–dc converter. $\Delta i_L(s)$ is a Laplace transformed

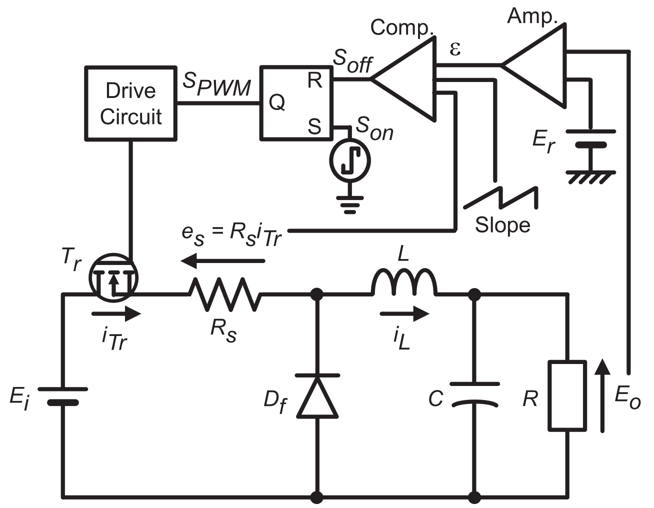


Fig. 16. PCMC dc–dc converter.

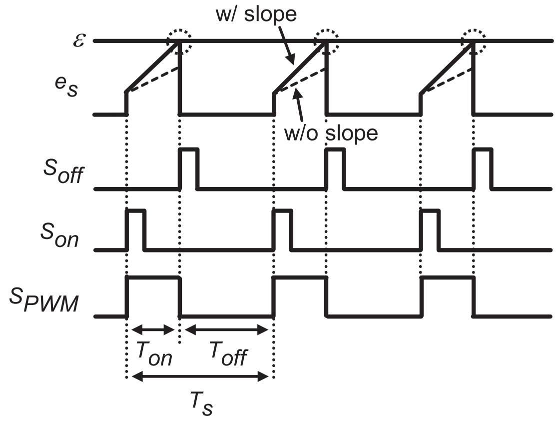


Fig. 17. Operation waveforms of a PCMC dc–dc converter.

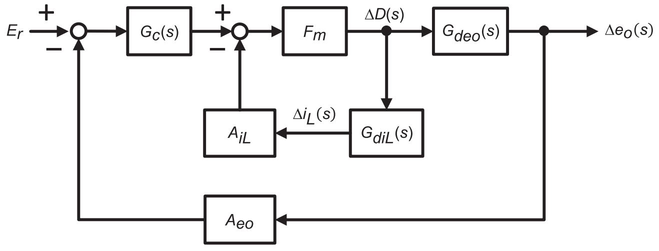


Fig. 18. Block diagram of a PCMC dc–dc converter using an analog controller.

perturbation of i_L. A_{eo} and A_{iL} are gains of preamplifiers for E_o and i_L, respectively. F_m is a transfer function of the PWM signal generator. $G_c(s)$ is a transfer function of a controller, such as a PID controller. This is a basic block diagram of the PCMC dc–dc converter.

The advantage of the PCMC is that the stability can be improved by adding the current loop having a real-time current detector. It is reasonable to suppose that the digital PCMC should also keep this advantage. From this point of view, the six digital methods are reviewed using their block diagrams and the usefulness of the proposed method is confirmed. The digital PCMC dc–dc converter has six methods mentioned in Section I. These methods are roughly divided into two methods: the voltage and current delayed type and voltage delayed type. Moreover, the voltage and current delayed type has two methods, and the voltage delayed type has four methods. Block diagrams of the digital PCMC dc–dc converter are shown in Fig. 19. Differences from Fig. 18 in Fig. 19(a)–(f) are surrounded by a dashed line.

B. Complete Digital PCMC Using an ADC

Fig. 19(a) illustrates a block diagram of the digital PCMC using the ADC [20]–[22]. $G_{eo\mathrm{AD}}$ and $G_{iL\mathrm{AD}}$ are gains of ADCs for e_o and i_L, respectively. $e^{-s\tau_{eo}}$ and $e^{-s\tau_{iL}}$ are delay times for e_o and i_L, respectively, due to the ADC and a processing time. There are delay times in the voltage and current loop. $e^{-s\tau_{eo}}$ and $e^{-s\tau_{iL}}$ spoil the stability. $e^{-s\tau_{iL}}$ still exists even when a very high-speed ADC is utilized to detect the reactor current in real time. Therefore, real-time property of the current detection is not achieved.

C. Complete Digital Peak Current Prediction Method

Fig. 19(b) describes a block diagram of the peak current prediction method [23]–[33]. K_{iL} and K_{Er} are gains to reconvert digital values of i_L and E_r into their analog values. K_{iD} is a gain to convert a current value to *D*. This method also has delay times in the voltage and current loop. In addition, a value of *D* from one switching period ago is used to calculate a value of *D* for the next switching period. As can be seen, the system configuration of this method is obviously different from Fig. 18.

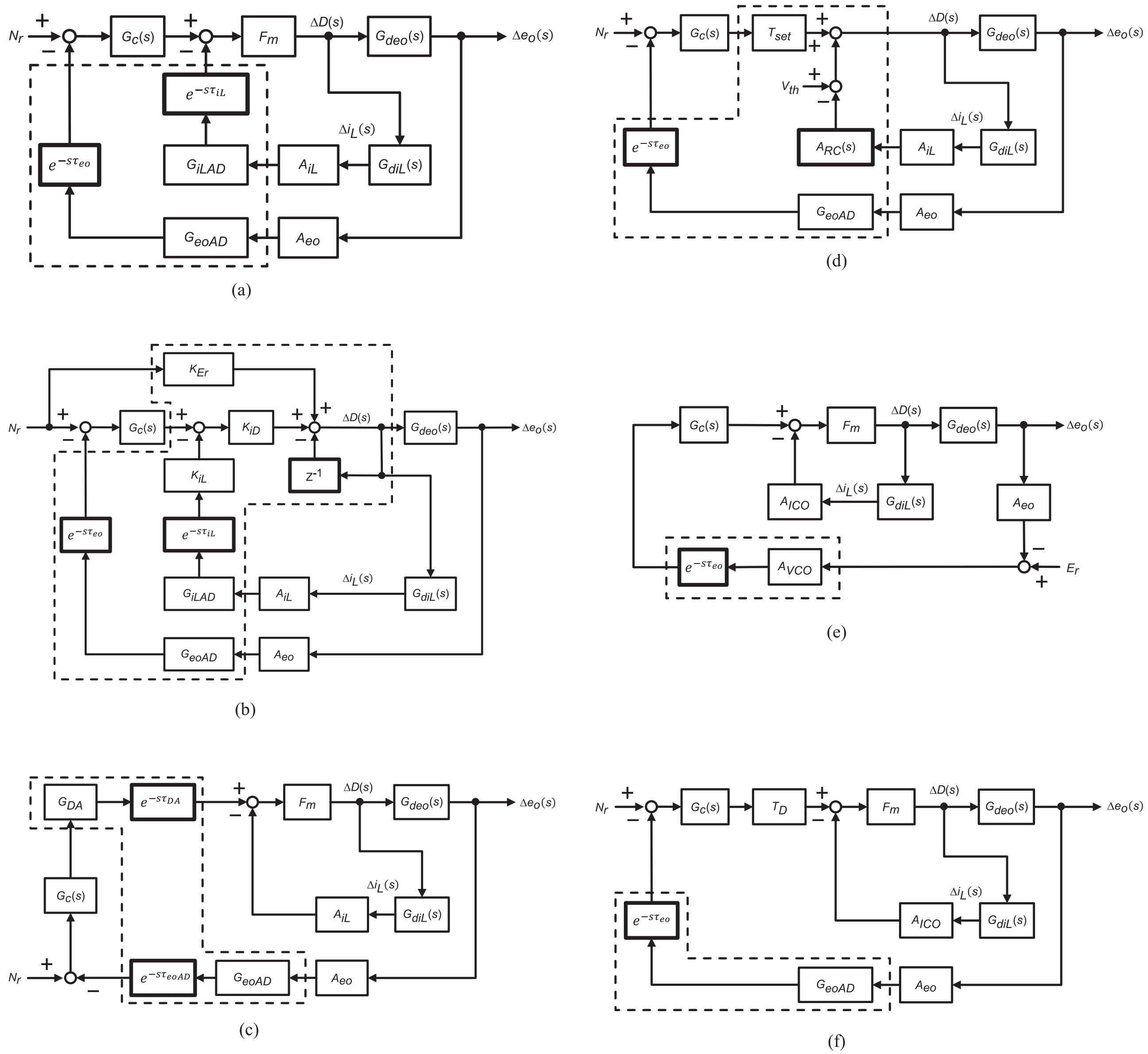
The two methods shown in Fig. 19(a) and (b) have the complete digital configuration and aims to capture accurately. They cannot realize real-time peak current detection, and it does not fit the concept of PCMC already described.

D. Hybrid Analog-Digital PCMC Using a DAC

A block diagram of the method using the DAC [34]–[44] is shown in Fig. 19(c). G_{DA} is a gain of the DAC. $e^{-s\tau_{eo\mathrm{AD}}}$ and $e^{-s\tau_{\mathrm{DA}}}$ are delay times caused by the A–D conversion and D–A conversion in the voltage loop. The current instruction value converted by DAC is compared in the analog domain with detected i_L. This configuration can realize real-time current detection as the analog control can. A disadvantage of this method is that the delay time in the voltage loop tends to be longer than the general digital controller because this method needs the DAC in addition to the ADC.

E. Hybrid Analog–Digital PCMC Using an RC Integrator Circuit

Fig. 19(d) shows the block diagram of the method using the *RC* integrator circuit [45]. T_{set} is a gain when a control signal is converted into a preset time of T_{on} at every switching period. *V*th is a threshold voltage. $A_{RC}(s)$ is a transfer function of the *RC* integrator circuit, which has a very small time constant and is used for i_L detection in this method. This *RC* integrator



(a) (b) (c) (d) (e) (f)

Fig. 19. Block diagrams of a digital PCMC dc–dc converter. (a) Digital PCMC using ADCs. (b) Digital PCMC with peak current prediction. (c) Digital PCMC using DAC. (d) Digital PCMC using CR integrator circuit. (e) Digital PCMC using VCO. (f) Proposed digital PCMC using VCO.

circuit can be replaced by the multivibrator. The voltage loop has $e^{-s\tau_{eo}}$ as the general digital controller has. The influence of the time constant of A_{RC}(s) is less than the influence of $e^{-s\tau_{iL}}$ in Fig. 19(a) and (b). However, it affects the stability. Additionally, the configuration of the system is different from Fig. 18.

F. Hybrid Analog–Digital PCMC Using VCO

Fig. 19(e) shows the block diagram of the method counting the pulse signal from the VCO [46]–[48]. A_{VCO} and A_{ICO} are gains of e_o and i_L detection using VCOs. There is no delay in the current detection, whereas the voltage loop has $e^{-s\tau_{eo}}$ because of the A–D conversion and processing by the controller. The real-time property of the current detection is secured in this method. The issue with this method is that it is difficult for this method to increase the resolution of the controller since the high-frequency VCO and high clock frequency for counting are needed.

G. Proposed Hybrid Analog–Digital PCMC Using a VCO

Finally, a block diagram of the proposed method is illustrated in Fig. 19(f). The real-time current detection can be achieved using a phase difference of the pulse signal from the VCO. Hence, there is no delay time in the current loop. Moreover, the proposed method does not count the pulse signal from the VCO so that an improvement in the resolution is easier than the method presented in Fig. 19(e). The voltage loop is composed by the general configuration of the digital controller, and $e^{-s\tau_{eo}}$ exists as the other methods have.

TABLE III
COMPARISON OF DIGITAL PCMC

References	Configuration	Response		Sensors		Features
		Voltage Loop	Current Loop	Voltage Loop	Current Loop	
[20]-[22]	Complete digital control	Delayed	Delayed	ADC	ADC	Using a high-speed ADC for current loop
[23]-[33]	Complete digital control	Delayed	N/A	ADC	N/A	Predicting peak current
[34]-[44]	Hybrid analog-digital control	Delayed	No delay	ADC	Analog comparator	Generating current instruction value using DAC
[45]	Hybrid analog-digital control	Delayed	No delay	ADC	RC circuit or multivibrator	Sensing a reactor current for very short time
[46]-[48]	Hybrid analog-digital control	No delay	No delay	VCO	VCO	Counting a pulse signal from VCO
Proposed method [49]-[52]	Hybrid analog-digital control	Delayed	No delay	ADC	VCO	Detecting a frequency of pulse signal from VCO

From the above discussion, methods shown in Fig. 19(e) and (f) are the closest configuration to Fig. 18 except for $e^{-s\tau_{eo}}$. They can improve the stability since they follow the important concept of the PCMC, which says i_L is injected in real time. In addition, the proposed method is advantageous compared to the method shown in Fig. 19(e) considering the resolution at an implementation. Therefore, it is clear that the proposed method is suitable for implementing the digital PCMC. The comparison of these digital PCMCs is summarized in Table III.

APPENDIX II
EXISTENCE RANGE OF SOLUTIONS OF THE DUTY RATIO IN THE PROPOSED METHOD

Here, the existence of the solution of (13) is discussed. Equation (13) is the quadratic equation and has two solutions. The function is defined as follows:

$$f\left(\frac{T_{\rm on}}{T_s}\right)=\left(\frac{T_{\rm on}}{T_s}\right)^2-\frac{2L+(r+R)\,T_s}{T_sR}\frac{T_{\rm on}}{T_s}+\frac{2L\left(1+\frac{r}{R}\right)}{T_sA_{iTr}R_sE_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}. \tag{A1}$$

In order to ensure that only one solution exists in the range from $T_{\rm on}/T_s=0$ to $T_{\rm on}/T_s=1$ and also to verify which solution is suitable for the proposed method, the sign of $f(0)$, $f(1)$, and $f(0)f(1)$ is examined. The sign of $f(0)$ and $f(1)$ must be different, and $f(0)f(1)$ must be negative to meet this condition.

At first, $f(0)$ is examined and is expressed by the following equation:

$$f\ (0)=\frac{2L\left(1+\frac{r}{R}\right)}{T_sA_{iTr}R_sE_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}. \tag{A2}$$

(i) When $f(0)>0$, the following inequality is obtained:

$$\frac{2L\left(1+\frac{r}{R}\right)}{T_sA_{iTr}R_sE_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}>0 \tag{A3}$$

$$\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau}-f_0\right)-E_B>0. \tag{A4}$$

Substituting (5) into(A4) because $1/\tau$ is equal to $f_{\rm VCO}$

$$A_{ICO}i_{Tr}>0. \tag{A5}$$

This inequality is true.

(ii) When $f(0)=0$, the following equation is obtained in the same way as (i):

$$A_{ICO}i_{Tr}=0. \tag{A6}$$

This equation is impossible because the PCMC dc–dc converter is generally operated in CCM.

(iii) When $f(0)<0$, the following equation is obtained in the same way as (i):

$$A_{ICO}i_{Tr}<0. \tag{A7}$$

This inequality is impossible because the left side cannot be negative. Therefore, $f(0)$ is larger than zero.

Next, an examination for $f(1)$ is done

$$f\ (1)=-\frac{2L+rT_s}{T_sR}+\frac{2L\,(R+r)}{T_sRA_{iTr}R_sE_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}. \tag{A8}$$

(iv) When $f(1)>0$, the following inequality is obtained:

$$-\frac{2L+rT_s}{T_sR}+\frac{2L\,(R+r)}{T_sRA_{iTr}R_sE_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}>0 \tag{A9}$$

$$\frac{2L\,(R+r)}{T_sRA_{iTr}R_sE_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}>\frac{2L+rT_s}{T_sR} \tag{A10}$$

$$\frac{2L\,(R+r)}{A_{iTr}R_sE_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau}-f_0\right)-E_B\right\}>2L+rT_s. \tag{A11}$$

Substitute (5) into (A11) in the same way as above

$$\frac{2L\,(R+r)\,i_{Tr}}{E_i}>2L+rT_s \tag{A12}$$

$$\frac{2L\,(R+r)\,i_{Tr}}{2L+rT_s}>E_i. \tag{A13}$$

When *r* is ignored in this inequality, the following inequality is obtained:

$$Ri_{Tr} \approx E_o > E_i. \tag{A14}$$

This is not true because the left side of (A14) is considered to be almost E_o and the main circuit is a buck-type dc–dc converter.

(v) When $f(1) = 0$, the following equation is obtained in the same way as (iv):

$$E_o = E_i\ . \tag{A15}$$

This equation is true.

(vi) When $f(1) < 0$, the following equation is obtained in the same way as (iv):

$$E_o < E_i. \tag{A16}$$

This equation is also true. Therefore, $f(1)$ is less than or equal to zero.

Finally, a sign of $f(0)f(1)$ must be negative because there is only one solution in the range from $T_{\rm on}/T_s = 0$ to $T_{\rm on}/T_s = 1$. $f(0)f(1)$ is given by the following equation:

$$f\,(0)\,f\,(1) = X\,(X - \alpha) \tag{A17}$$

where *X* and α are expressed as follows:

$$X = \frac{2L\left(1+\frac{r}{R}\right)}{T_s A_{iTr} R_s E_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau} - f_0\right) - E_B\right\} \tag{A18}$$

$$\alpha = \frac{2L + rT_s}{T_s R}. \tag{A19}$$

From (A17), *X* must be in the following range when $f(0)f(1)$ is negative:

$$0 < X < \alpha. \tag{A20}$$

(vii) When $0 < X$, the inequality is derived as follows:

$$0 < \frac{2L\left(1+\frac{r}{R}\right)}{T_s A_{iTr} R_s E_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau} - f_0\right) - E_B\right\}. \tag{A21}$$

This inequality is the same as (i). In the same way as (i), it is true.

(viii) When $X < \alpha$, the following inequality is obtained:

$$\frac{2L\left(1+\frac{r}{R}\right)}{T_s A_{iTr} R_s E_i}\left\{\frac{1}{A_{\rm VCO}}\left(\frac{1}{\tau} - f_0\right) - E_B\right\} < \frac{2L + rT_s}{T_s R}. \tag{A22}$$

This inequality is the same as (vi). In the same way as (vi), it is also true. Thus, $f(0)f(1)$ is negative.

From (i)–(viii), following inequalities are true:

$$f\,(0) > 0 \tag{A23}$$

$$f\,(1) \le 0 \tag{A24}$$

$$f\,(0)\,f\,(1) < 0. \tag{A25}$$

Consequently, the smaller one of two solutions is proper except for the condition $f(1) = 0$.

REFERENCES

[1] D. Maksimovic, R. Zane, and R. Erickson, "Impact of digital control in power electronics," in *Proc. IEEE Int. Symp. Power Semicond. Devices ICs*, 2004, pp. 13–22.

[2] P. T. Krein, "Digital control generations—Digital controls for power electronics through the third generation," in *Proc. Int. Conf. Power Electron. Drive Syst.*, Nov. 2007, pp. 1–5.

[3] Y. Liu, E. Meyer, and X. Liu, "Recent developments in digital control strategies for DC/DC switching power converters," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2567–2577, Nov. 2009.

[4] L. Corradini, D. Maksimovic, P. Mattavelli, and R. Zane, *Digital Control of High-Frequency Switched-Mode Power Converters*. Hoboken, NJ, USA: Wiley, 2015.

[5] S. Buso and P. Mattavelli, *Digital Control in Power Electronics*, 2nd ed. San Rafael, CA, USA: Morgan & Claypool, 2015.

[6] F. Kurokawa, R. Yoshida, and Y. Furukawa, "Digital fast p slow ID control dc-dc converter using A–D converters in different resolutions," *IEEE Trans. Ind. Appl.*, vol. 51, no. 1, pp. 353–361, Jan./Feb. 2015.

[7] H. Maruta, D. Mitsutake, and F. Kurokawa, "A neural network based reference modified PID control with simple duration design for digitally controlled DC–DC converters," *Int. J. Renewable Energy Res.*, vol. 6, no. 2, pp. 550–559, 2016.

[8] K. Kajiwara, H. Tajima, H. Maruta, F. Kurokawa, and I. Colak, "Dynamic characteristics of integral gain changeable digital control DC–DC converter for suppression of output capacitance," *Int. J. Renewable Energy Res.*, vol. 6, no. 1, pp. 237–244, 2016.

[9] A. Capel, G. Ferrante, D. O'Sullivan, and A. Weinberg, "Application of the injected current model for the dynamic analysis of switching regulators with the new concept of LC3 modulator," in *Proc. IEEE Power Electron. Spec. Conf.*, 1978, pp. 135–147.

[10] C. W. Deisch, "Simple switching control method changes power converter into a current source," in *Proc. IEEE Power Electron. Spec. Conf.*, 1978, pp. 300–306.

[11] S.-P. Hsu, A. Brown, L. Rensink, and R. D. Middlebrook, "Modelling and analysis of switching DC-to-DC converters in constant-frequency current-programmed mode," in *Proc. IEEE Power Electron. Spec. Conf.*, 1979, pp. 284–301.

[12] R. Redl and I. Novak, "Instability in current-mode controlled switching voltage regulators," in *Proc. IEEE Power Electron. Spec. Conf.*, 1981, pp. 17–28.

[13] R. Redl and I. Novak, "Stability analysis of constant-frequency current-mode controlled switching regulators operating above 50% duty ratio," in *Proc. IEEE Power Electron. Spec. Conf.*, 1982, pp. 213–223.

[14] R. D. Middlebrook, "Topics in multiple-loop regulators and current-mode programming," *IEEE Trans. Power Electron.*, vol. PE-2, no. 2, pp. 109–124, Apr. 1987.

[15] R. D. Middlebrook, "Modeling current-programmed buck and boost regulators," *IEEE Trans. Power Electron.*, vol. 4, no. 1, pp. 36–52, Jan. 1989.

[16] R. B. Ridley, "A new, continuous-time model for current-mode control," *IEEE Trans. Power Electron.*, vol. 6, no. 2, pp. 271–280, Apr. 1991.

[17] W. Tang, F. C. Lee, and R. B. Ridley, "Small-signal modeling of average current-mode control," *IEEE Trans. Power Electron.*, vol. 8, no. 2, pp. 112–119, Apr. 1993.

[18] J. Li and F. C. Lee, "New modeling approach and equivalent circuit representation for current-mode control," *IEEE Trans. Power Electron.*, vol. 25, no. 5, pp. 1218–1230, May 2010.

[19] Y. Yan, F. C. Lee, and P. Mattavelli, "Comparison of small signal characteristics in current mode control schemes for point-of-load buck converter applications," *IEEE Trans. Power Electron.*, vol. 28, no. 7, pp. 3405–3414, Jul. 2013.

[20] S. Kapat, "Selectively sampled subharmonic-free digital current mode control using direct duty control," *IEEE Trans. Circuits Syst.-II, Express Briefs*, vol. 62, no. 3, pp. 311–315, Mar. 2015.

[21] A. K. Singha, S. Kapat, S. Banerjee, and J. Pal, "Nonlinear analysis of discretization effects in a digital current mode controlled boost converter," *IEEE J. Emerg. Sel. Topics Circuits Syst.*, vol. 5, no. 3, pp. 336–344, Sep. 2015.

[22] Y. Chen, F. Xie, B. Zhang, D. Qiu, and M. Xu, "Analysis of digital PCM-controlled boost converter with trailing-edge modulation based on z-domain and describing-function model," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 3250–3259, Dec. 2020.

[23] J. Chen, A. Prodic, R. W. Erickson, and D. Maksimovic, "Predictive digital current programmed control," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 411–419, Jan. 2003.

[24] S. Chattopadhyay and S. Das, "A digital current-mode control technique for DC–DC converters," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1718–1726, Nov. 2006.

[25] O. Trescases, A. Parayandeh, A. Prodic, and W. T. Ng, "Sensorless digital peak current controller for low-power DC–DC SMPS based on a bi-directional delay line," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 1670–1676.

[26] Y. S. Lai and C. A. Yeh, "Predictive digital-controlled converter with peak current-mode control and leading-edge modulation," *IEEE Trans. Ind. Electron.*, vol. 56, no. 6, pp. 1854–1863, Jun. 2009.

[27] Y. T. Chang and Y. S. Lai, "Parameter turning method for digital power converter with predictive current-mode control," *IEEE Trans. Power Electron.*, vol. 24, no. 12, pp. 2910–2919, Dec. 2009.

[28] Q. Tong, Q. Zhang, R. Min, X. Zou, Z. Liu, and Z. Chen, "Sensorless predictive peak current control for boost converter using comprehensive compensation strategy," *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2754–2766, Jun. 2014.

[29] W. Fang, X. Liu, S. Liu, and Y. Liu, "A digital parallel current-mode control algorithm for DC–DC converters," *IEEE Trans. Ind. Informat.*, vol. 10, no. 4, pp. 2146–2153, Nov. 2014.

[30] Q. Zhang, R. Min, Q. Tong, X. Zou, Z. Liu, and A. Shen, "Sensorless predictive current controlled DC–DC converter with a self-correction differential current observer," *IEEE Trans. Ind. Electron.*, vol. 61, no. 12, pp. 6747–6757, Dec. 2014.

[31] S. Dutta, S. Hazra, and S. Bhattacharya, "A digital predictive current-mode controller for a single-phase high-frequency transformer-isolated dual-active bridge DC-to-DC converter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 9, pp. 5943–5952, Sep. 2016.

[32] X. Zhang, R. Min, D. Lyu, D. Zhang, Y. Wang, and Y. Gu, "Current tracking delay effect minimization for digital peak current mode control of DC–DC boost converter," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12384–12395, Dec. 2019.

[33] G. Bonanno and L. Corradini, "Digital predictive current-mode control of three-level flying capacitor buck converters," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 4697–4710, Apr. 2021.

[34] S. Saggini, M. Ghioni, and A. Geraci, "An innovative digital control architecture for low-voltage, high-current DC–DC converters with tight voltage regulation," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 210–218, Jan. 2004.

[35] O. Trescases, A. Prodic, and W. T. Ng, "Digitally controlled current-mode DC–DC converter IC," *IEEE Trans. Circuits Syst.-I, Reg. Papers*, vol. 58, no. 1, pp. 219–231, Jan. 2011.

[36] J. Wang and J. Xu, "Peak current mode bifrequency control technique for switching DC–DC converters in DCM with fast transient response and low EMI," *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1876–1884, Apr. 2012.

[37] M. Hallworth and S. A. Shirsavar, "Microcontroller–based peak current mode control using digital slope compensation," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3340–3351, Jul. 2012.

[38] S. Pan and P. K. Jain, "A low-complexity dual-voltage-loop digital control architecture with dynamically varying voltage and current references," *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 2049–2060, Apr. 2014.

[39] A. K. Singha and S. Kapat, "A unified framework for analysis and design of a digitally current-mode controlled buck converter," *IEEE Trans. Circuits Syst.-I, Reg. Papers*, vol. 63, no. 11, pp. 2098–2107, Nov. 2016.

[40] V. I. Kumar and S. Kapat, "Unified digital current mode control tuning with near optimal recovery in a CCM buck converter," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8461–8470, Dec. 2016.

[41] Y. Wen, M. Rose, R. Fernandes, R. V. Otten, H. J. Bergveld, and O. Trescases, "A dual-mode driver IC with monolithic negative drive-voltage capability and digital current-mode controller for depletion-mode GaN HEMT," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 423–432, Jan. 2017.

[42] C. Wang, S. Xu, S. Lu, and W. Sun, "A low-cost constant current control method for DCM and CCM in digitally controlled primary-side regulation flyback converter," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, no. 3, pp. 1483–1494, Sep. 2018.

[43] A. K. Singha, S. Banerjee, and S. Kapat, "Enhanced stability caused by a one-cycle delay in a digital current-mode controlled buck converter," *IEEE Trans. Circuits Syst.-II, Express Briefs*, vol. 65, no. 12, pp. 1979–1983, Dec. 2018.

[44] R. Roy and S. Kapat, "Discrete-time framework for analysis and design of digitally current-mode-controlled intermediate bus architectures for fast transient and stability," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 4, pp. 3237–3249, Dec. 2020.

[45] K. Kajiwara, T. Ueki, Y. Shibata, H. Maruta, and F. Kurokawa, "Overcurrent limitation for digital peak current mode DC–DC converter," *Int. J. Renewable Energy Res.*, vol. 6, no. 1, pp. 90–98, 2016.

[46] H. Matsuo, F. Kurokawa, and M. Asano, "Overcurrent limiting characteristics of the DC–DC converter with a new digital current-injected control circuit," *IEEE Trans. Power Electron.*, vol. 13, no. 4, pp. 645–650, Jul. 1998.

[47] M. Truntic and M. Milanovic, "Voltage and current-mode control for a buck-converter based on measured integral values of voltage and current implemented in FPGA," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6686–6699, Dec. 2014.

[48] H. Matsuo, F. Kurokawa, M. Ikehara, and T. Takeda, "Regulation characteristics of the digitally controlled DC–DC converter with a function of the temperature compensation," in *Proc. Int. Power Electron. Conf.*, Apr. 1990, pp. 1152–1156.

[49] F. Kurokawa and Y. Komichi, "A new peak-current injected digital control circuit for DC–DC converter," in *Proc. IEEE Eur. Conf. Power Electron. Appl.*, Aug. 2011, pp. 1–7.

[50] F. Kurokawa, H. Tamenaga, Y. Shibata, and Y. Yamabe, "Regulation characteristics of fast response digitally peak current controlled DC–DC converter," in *Proc. IEEE Power Electron. Drive Syst.*, Apr. 2013, pp. 1114–1118.

[51] F. Kurokawa, S. Maeda, and Y. Furukawa, "Analysis of digital peak current control DC–DC converter," in *Proc. Int. Conf. Renewable Energy Res. Appl.*, Oct. 2014, pp. 737–742.

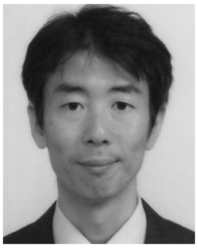
[52] Y. Furukawa, S. Maeda, F. Kurokawa, and I. Colak, "Performance characteristic of digital peak current mode control switching power supply," in *Proc. IEEE Eur. Conf. Power Electron. Appl.*, Sep. 2015, pp. 1–10.

[53] J. Kang, J. Park, M. Jeong, and C. Yoo, "A time-domain-controlled current-mode buck converter with wide output voltage range," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 865–873, Mar. 2019.

[54] Spartan-3 FPGA Family Data Sheet, Dec. 2009.

Yudai Furukawa (Member, IEEE) received the B.S., M.S., and Ph.D. degrees from Nagasaki University, Nagasaki, Japan, in 2013, 2015, and 2018, respectively.

Since 2018, he has been an Assistant Professor with Fukuoka University, Fukuoka, Japan. His current research interests include switching power converters, digital control, degradation diagnosis, and artificial intelligence application to switching power converters.



Yuichiro Shibata (Member, IEEE) received the B.E. degree in electrical engineering and the M.E. and Ph.D. degrees in computer science from Keio University, Tokyo, Japan, in 1996, 1998, and 2001, respectively.

He is currently a Professor with the School of Information and Data Sciences, Nagasaki University, Nagasaki, Japan. He was a Visiting Scholar with the University of South Carolina in 2006. His research interests include reconfigurable computing and field-programmable gate array application systems.

Dr. Shibata was the recipient of the Best Paper Award of IEICE in 2004 and the Best Paper Award of IEEE ICRERA in 2017.

Haruhi Eto (Member, IEEE) received the B.E. degree from Kyushu University, Fukuoka, Japan, in 1980, and the Dr. Eng. degree from Nagasaki University, Nagasaki, Japan, in 2004.

During 1980–2013, he was with Nissan Group Company and MHI Group Company. During 2013–2019, he was with Nagasaki University. He is currently with the Nagasaki Institute of Applied Science, Nagasaki, Japan.

Ilhami Colak (Senior Member, IEEE) was born in 1962 in Turkey. He received the diploma degree in electrical engineering from Gazi University, Ankara, Turkey, in 1985, the M.Sc. degree in electrical engineering in the field of speed control of wound rotor induction machines using semiconductor devices from Gazi University, in 1991, the M.Phil. degree from Birmingham University, Birmingham, U.K., in 1991, by preparing a thesis on high-frequency resonant dc-link inverters, and the Ph.D. degree from Aston University, Birmingham, U.K., in 1994, with a focus on mixed-frequency testing of induction machines using inverters.

He became an Assistant Professor, an Associate Professor, and a Full Professor in 1995, 1999, and 2005, respectively. He was the Head of Department, Dean, and Vice Rector of Gazi University, Istanbul Gelisim University, and Nisantasi University, Istanbul, Turkey. He is currently a Full Professor with Nisantasi University. He has authored or coauthored more than 120 journal papers, 235 conference papers, and 7 books in different subjects, including electrical machines, drive systems, machine learning, reactive power compensation, inverter, converter, artificial neural networks, distance learning automation, and alternating energy sources. More than 207 of his papers have been cited in Science Citation Index. His papers have received more than 2161 citations by 1900 papers. His Thomson Reuters H-index is 24 and average citation per paper is 10.72. In SCOPUS, H-index is 30. His 264 papers have received 3439 citations from 2955 documents. He supervised 23 M.Sc. students and 14 Ph.D. students. He also spent around three years at the European Commission Research Centre in The Netherlands. He achieved a great success of 10% by being included in the list of “2% World’s Most Influential Scientists,” which was created by USA Stanford University considering the “Works of the Year 2020.” He has organized more than 100 international IEEE supported workshops, special sessions, and conferences. In the last 20 years, he has concentrated his studies on renewable energy and smart grids by publishing papers, journals (www.ijrer.org; www.ijSmartGrid.org) and organizing international IEEE sponsored conferences (www.icrera.org; icSmartGrid.org).

Dr. Colak is a member of IES, IAS, PELS, and PES.

Fujio Kurokawa (Fellow, IEEE) was born in Yamaguchi, Japan, in 1952. He received the B.S. degree in electronic engineering from the Fukuoka Institute of Technology, Fukuoka, Japan, in 1976, and the Dr. Eng. degree from Osaka Prefecture University, Sakai, Japan, in 1988.

Since 2017, he has been with the Nagasaki Institute of Applied Science, Nagasaki, Japan. He is currently a Professor with the Institute for Innovative Science and Technology. His research and teaching interests include the area of dc–dc converters, ac–dc converters, inverters and their digital control, renewable energy technologies, power electronics technologies in aerospace and automobile, switching power supply for lighting systems, and so on.

Dr. Kurokawa was the General Chair of the 1st International Conference on Renewable Energy Research and Applications (ICRERA 2012), the General Chair of the 2013 IEEE International Conference on Power Electronics and Drive Systems, the General Co-Chair of the 2013 IEEE International Conference on Power Engineering, Energy and Electrical Drives, the General Co-Chair of 2014 International Power Electronics and Motion Control Conference and Exposition, the Organizing Committee Chair of 2015 IEEE International Telecommunications Energy Conference, and the General Co-Chair of ICRERA 2013–2021. He is a Fellow of the Illuminating Engineering Institute of Japan, a Fellow Member of the Institute of Electronics, Information and Communication Engineers of Japan, and a Senior Member of the Institute of Electrical Engineers of Japan.