Nonlinear Capacitance Model of SiC MOSFET Considering Envelope of Switching Trajectory

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***Abstract*—The nonlinear capacitance model is important to predict the dynamic characteristics of SiC MOSFETs. Different from the conventional modeling method extracting the parameters from the full data, this article proposes a modeling method based on the envelope of the switching trajectory, which greatly reduces the complexity of the model and avoids divergence during the simulation. The proposed modeling method clarifies the value range of gate–source voltage $v_{\rm gs}$ and drain–source voltage $v_{\rm ds}$ in each interterminal capacitance operation period, and only necessary data will be taken into consideration, whereas the unnecessary data out of switching trajectory will be discarded. In order to verify the correctness and accuracy of the proposed model, the SiC MOSFET C2M0080120D (1200 V/36 A) with the nonlinear capacitances is modeled in the Pspice environment and compared with the measured results of the double-pulse experiment. The proposed model is also simulated in a full-bridge inverter. The results show that the proposed model has enough accuracy and efficiency in dynamic behavior prediction of SiC MOSFETs, which would be potential for the more complex system-level simulation.**

***Index Terms*—Device model, dynamic characteristic, nonlinear capacitance, SiC MOSFET.**

I. Introduction

DUE to the excellent material characteristics of the silicon carbide (SiC), the SiC MOSFETs have great advantages in improving the efficiency and power density of the converter systems [1]–[4]. In order to evaluate the performance of the power converters with wide-bandgap semiconductor devices, the modeling method should be elaborately addressed [5]–[8]. However, the modeling of SiC MOSFETs and prediction of the dynamic characteristics are quite complex, which are needed to calculate the responses of the drain–source voltage and the channel current accurately during the switching transients.

The switching trajectory has been researched recently and could be used to predict complex switching behaviors of the SiC MOSFETs, such as the dead-time effects [9], crosstalk phenomenon [10], switching losses [11], [12], electrical stresses [13], and electromagnetic interferences [14], [15]. As the interterminal capacitances $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ of the SiC MOSFET determine the switching speed directly, the modeling of the interterminal capacitances of the SiC MOSFET is the key work in the research of the switching trajectory. However, the interterminal capacitances have strong nonlinear features and vary according to the change of terminal voltage, which makes them difficult to be described and modeled. Many modeling methods have been put forward in the literature, such as equivalent integration [16], *C*–*v* function fitting [17]–[20], extraction from results of measurement [21], or numerical simulation with lookup table (LUT) [22]. The equivalent integration method is the simplest, but the accuracy is poor in a wide voltage range. The function fitting method has the advantage of easy convergence, but the accuracy of the nonlinear function fitting method depends on the type and order of the function. The measurement- or numerical-simulation-based LUT is the closest one to the actual physical characteristics of the power devices among all modeling methods, which is widely adopted in recent years. However, this method requires a complicated parameter extraction process, and the accurate model needs the LUT with an extremely large size, which makes the simulation of some complex converter systems, such as the modular multilevel converter, impractical.

In order to achieve the simulation in high efficiency, a compromise between the complexity and accuracy of the nonlinear capacitance model should be considered. In this article, a modeling method based on the envelope of the switching trajectory to construct the nonlinear capacitance is proposed. A concise LUT is set up by considering the switching trajectory only in specific voltage periods, where the interterminal capacitance in the SiC MOSFET depends only on the drain–source voltage and gate–source voltage and neglecting the actions of current and certain small voltage periods in the switching trajectory is reasonable. Then, the proposed nonlinear capacitance model has sufficient accuracy and a highly efficient simulation for the performance evaluation.

The rest of this article is organized as follows. In Section II, the characteristics of the voltage-dependent capacitance inside the SiC MOSFET are discussed and analyzed in detail. In Section III, the nonlinear capacitances between different terminal poles are modeled based on the switching trajectory. In Section IV, the simulation and experiment validations are carried out. Finally, Section V conlcudes this article.

II. Capacitance Characteristics

A. Interterminal Capacitance

The interterminal capacitance includes the parasitic capacitances inside the SiC MOSFET, as shown in Fig. 1. Taking a

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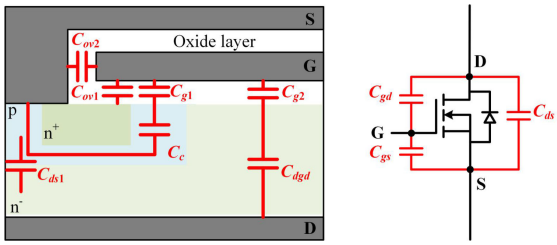

Fig. 1. Distribution of parasitic capacitances inside SiC MOSFET.

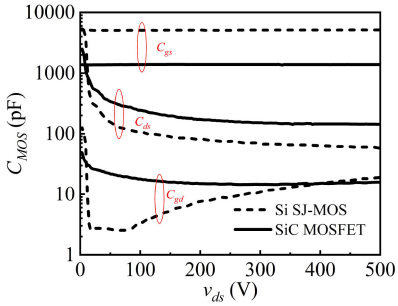

Fig. 2. Comparison of capacitances in Si SJ-MOS (IPW65R041CFD7, 650 V/50 A) and SiC MOSFET (IMZA65R039M1H, 650 V/50 A).

typical VDMOSFET structure as an example, there are multiple capacitances connected in serial or parallel according to the terminal poles of the power device. The value of the gate–source capacitance $C_{\rm gs}$ can be expressed as follows:

$$C_{\rm gs} = C_{ov1} + C_{ov2} + \frac{1}{\frac{1}{C_{g1}} + \underbrace{\frac{1}{C_c}}_{\text{Nonlinear}}} \tag{1}$$

where C_{ov1}, C_{ov2}, and C_{g1} are the linear capacitances of the gate and n+ doped region, gate and source, and gate and channel, respectively. All of these linear capacitances are only related to the dielectric constant of the material and the geometric arrangement of the device. C_c is the voltage-dependent semiconductor capacitance of the p-base layer, which leads to the nonlinear characteristics of $C_{\rm gs}$.

The gate–drain capacitance $C_{\rm gd}$ consists of two serial basic capacitances and can be expressed as follows:

$$C_{\rm gd} = \frac{1}{\frac{1}{C_{g2}} + \underbrace{\frac{1}{C_{gdg}}}_{\text{Nonlinear}}} \tag{2}$$

where C_{g2} is the linear capacitance between the gate and the n−drift layer, and C_{gdg} is the nonlinear semiconductor capacitance of the n−drift layer. The drain–source capacitance $C_{\rm ds}$ can be simplified as the nonlinear PN junction capacitance $C_{\rm ds1}$ between the p-base and n−drift layer and is given as follows:

$$C_{\rm ds} = \underbrace{C_{\rm ds1}}_{\text{Nonlinear}}. \tag{3}$$

It should be noted that the input capacitance C_{iss}, the transfer capacitance C_{rss}, and the output capacitance C_{oss} are normally given by the manufacturer in the datasheet. Then, the interterminal capacitance can be calculated as follows:

$$\begin{cases} C_{\rm gs} = C_{iss} - C_{rss} \\ C_{\rm gd} = C_{rss} \\ C_{\rm ds} = C_{oss} - C_{rss}. \end{cases} \tag{4}$$

The nonlinear capacitances $C_{\rm gs}$, $C_{\rm gd}$, and $C_{\rm ds}$ are dependent on the drain–source voltage $v_{\rm ds}$, and such relationships could be shown in C–v curves of the manufacturer's datasheet under different voltages $v_{\rm ds}$ [23], [24]. Due to the high breakdown field of the SiC material, the drift region of the SiC MOSFET is thinner than that of Si devices, and the chip volume can be reduced by increasing the doping concentration [1]. Therefore, in the traditional concept, the parasitic capacitances can be reduced by applying the SiC material. This is also correct in the comparisons of SiC MOSFETs and Si insulated-gate bipolar transistor (IGBTs). However, it is not always correct when comparing SiC MOSFETs with Si superjunction MOSFETs (SJ-MOS). Fig. 2 shows the comparison of the capacitances in Si SJ-MOS and SiC MOSFET, where the special vertical junction structure makes the values of $C_{\rm ds}$ and $C_{\rm gd}$ in the Si SJ-MOS lower than those in the SiC MOSFET in some voltage range. Therefore, the device structure would influence the interterminal capacitances. Actually, the C–v curves given in the datasheet have reflected the device structures and in the practical implications the treatment of such C–v curves is extremely important during the capacitance modeling.

The capacitance varies a lot among SiC MOSFETs with different power levels. In terms of continuous current, the increasing of the current capacity means the reduction of the ON-state resistance $R_{\rm ds\cdot on}$ and the larger doping concentration or the cross-sectional area is required [1]. Therefore, the increase in the current capacity will result in larger capacitance values, which reduce the switching speed of the SiC MOSFETs in turn. The large difference in capacitance between SiC MOSFETs calls for the acquisition of detailed and targeted models. At the same time, the influence of the gate–source voltage $v_{\rm gs}$ should be considered in the capacitance model too.

B. Switching Trajectory

The switching trajectory exhibits the dynamic performance of the SiC MOSFET from the cutoff region to the ohmic region, which is expressed by the voltages $v_{\rm gs}$ and $v_{\rm ds}$ and the drain current i_d in the time domain. The switching trajectory can be obtained with the help of the double-pulse test (DPT). Fig. 3 shows the platform of the DPT, where $V_{\rm dc}$ is the bus voltage, $C_{\rm dc}$ is the bus capacitance, $L_{\rm loop}$ is the parasitic inductance in the loop, I_L is the load current, D_f is the freewheeling diode, C_f is the junction capacitance of the freewheeling diode, $i_{\rm ch}(v_{\rm gs})$ is the voltage-controlled channel current, R_g is the total gate loop resistance, V_{GG} is the positive driving voltage, V_{EE} is the negative driving voltage, and S_H and S_L are the driving transistors.

The relationship of nonlinear capacitances with the switching trajectory of the SiC MOSFET is shown in Fig. 4. There are five periods in the switching transients of the SiC MOSFET, namely, period 1, delay; period 2, *di/dt*; period 3, *du/dt*; period 4, overshoot; period 5, stable state with ON-state or OFF-state.

TABLE I
RELATIONSHIP BETWEEN SWITCHING TRANSIENTS AND NONLINEAR CAPACITANCES

	Period	Time	Main capacitance	Voltage range
Turn-on transients	delay	$t_1-t_0=R_gC_{iss}(v_{gs},v_{ds})\ln(\frac{V_{GG}-V_{EE}}{V_{GG}-V_{TH}})$	$C_{gs}(v_{gs},v_{ds})$	$v_{gs}\in(V_{EE},V_{TH})$ $v_{ds}=V_{dc}$
	di/dt	$t_2-t_1=R_gC_{iss}(v_{gs},v_{ds})\ln(\frac{V_{GG}-V_{TH}}{V_{GG}-V_{mil1}})$	$C_{gs}(v_{gs},v_{ds})$	$v_{gs}\in(V_{TH},V_{mil1})$ $v_{ds}=V_{dc}$-$L_{loop}\lvert di/dt\rvert$
	du/dt+overshoot	$t_3-t_2=\frac{Q_{gd}R_g}{V_{GG}-\frac{V_{mil1}+V_{mil2}}{2}}$	$C_{gd}(v_{gs},v_{ds})\&C_{ds}(v_{gs},v_{ds})$	$v_{gs}\in(V_{mil1},V_{mil2})$ $v_{ds}\in(I_LR_{ds\_on},V_{dc})$
	on-state	$t_4-t_3=R_gC_{gs}(v_{gs},v_{ds})\ln[\frac{10(V_{GG}-V_{mil2})}{V_{GG}}]$	$C_{gs}(v_{gs},v_{ds})$	$v_{gs}\in(V_{mil2},V_{GG})$ $v_{ds}\in(0,I_LR_{ds\_on})$
Turn-off transients	delay	$t_6-t_5=R_gC_{gs}(v_{gs},v_{ds})\ln(\frac{V_{EE}-V_{GG}}{V_{EE}-V_{mil2}})$	$C_{gs}(v_{gs},v_{ds})$	$v_{gs}\in(V_{mil2},V_{GG})$ $v_{ds}\in(0,I_LR_{ds\_on})$
	du/dt	$t_7-t_6=\frac{Q_{gd}R_g}{\frac{V_{mil1}+V_{mil2}}{2}-V_{EE}}$	$C_{gd}(v_{gs},v_{ds})\&C_{ds}(v_{gs},v_{ds})$	$v_{gs}\in(V_{mil1},V_{mil2})$ $v_{ds}\in(I_LR_{ds\_on},V_{dc})$
	di/dt+overshoot	$t_8-t_7=R_gC_{gs}(v_{gs},v_{ds})\ln(\frac{V_{EE}-V_{mil1}}{V_{EE}-V_{TH}})$	$C_{gs}(v_{gs},v_{ds})$	$v_{gs}\in(V_{TH},V_{mil1})$ $v_{ds}=V_{dc}$+$L_{loop}\lvert di/dt\rvert$
	off-state	$t_9-t_8=R_gC_{gs}(v_{gs},v_{ds})\ln[\frac{10(V_{EE}-V_{TH})}{V_{EE}}]$	$C_{gs}(v_{gs},v_{ds})$	$v_{gs}\in(V_{EE},V_{TH})$ $v_{ds}=V_{dc}$

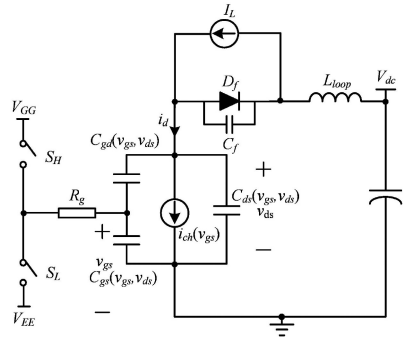

Fig. 3. DPT for dynamic characteristics of SiC MOSFETs.

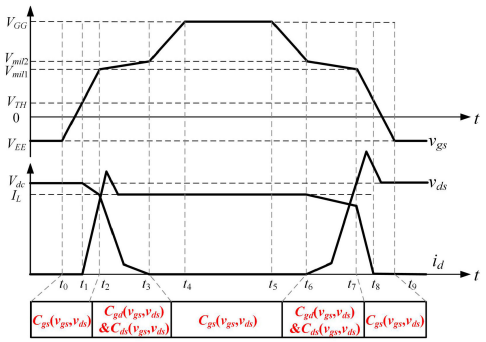

Fig. 4. Relationship of nonlinear capacitances with switching trajectory.

Table I presents the relationship between switching transients and nonlinear capacitances, where the expressions of switching time are given. The switching time is determined by the charging and discharging speed of the capacitances, which dominates the switching speed of the power devices. It is obvious that each switching transient corresponds to a relatively certain voltage range, in which the voltage-dependent capacitances operate nonlinearly.

Different from the Si MOSFET, the SiC MOSFET has a more significant drain-induced barrier lowering (DIBL), which is caused by the short-channel effect [26], [28]. When the length of the channel reduces to a certain value, the proportion of the depletion between the p-base and n−drift region will increase evidently. Therefore, the threshold voltage $V_{\rm TH}$ will be reduced as there is no need to attract as many charges as before to form the channel. The expression of the voltage-controlled channel current $i_{\rm ch}(v_{\rm gs})$ is shown in (5). It is obvious that the reduction of $V_{\rm TH}$ will cause an increase in $v_{\rm gs}$, when the load current conducted by the channel is constant

$$i_{\rm ch}(v_{\rm gs})=g_{fs}(v_{\rm gs}-V_{\rm TH}) \tag{5}$$

where g_{fs} is the transconductance of the SiC MOSFET. This phenomenon can be described as "Miller ramp" instead of "Miller plateau," where $v_{\rm gs}$ should be increased from $V_{\rm mil1}$ to $V_{\rm mil2}$. Therefore, the assumption that voltage v_{gs} remains constant during the *du/dt* period in the conventional model is inaccurate, to which special attention should be paid in the modeling of nonlinear capacitance based on the switching trajectory. The change in the gate–source voltage can be expressed as follows:

$$\begin{cases} V_{\rm mil1}=\frac{I_L}{g_{fs}}+V_{\rm TH} \\ V_{\rm mil2}=V_{\rm mil1}+\Delta V_{\rm TH} \end{cases} \tag{6}$$

where $\Delta V_{\rm TH}$ is the threshold reduction caused by DIBL.

III. CAPACITANCE MODEL

As the interterminal capacitance of the SiC MOSFET is nonlinear and voltage dependent, the capacitances with two independent voltage variables $v_{\rm gs}$ and $v_{\rm ds}$ are studied in [22], where the SiC MOSFET (C2M0080120D, 1200 V/36 A) is simulated under the technology computer aided design (TCAD) tool. The

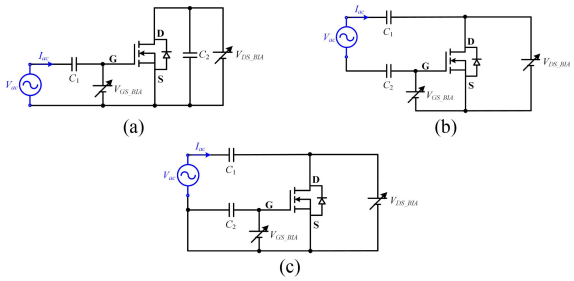

Fig. 5. Parameter extraction methodology. (a) C_{iss}. (b) C_{rss}. (c) C_{oss}.

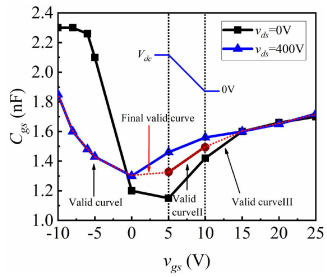

Fig. 6. C–v characteristics of gate–source capacitance.

parameters $C_{iss}(v_{\rm gs},v_{\rm ds})$, $C_{rss}(v_{\rm gs},v_{\rm ds})$, and $C_{oss}(v_{\rm gs},v_{\rm ds})$ can be extracted by adopting a numerical model of semiconductor devices based on the finite-element method [22], [30], [31]. The dc bias voltage and ac small testing signal are applied to obtain the value of nonlinear capacitance at different voltages, as shown in Fig. 5. In Fig. 5(a), an ac small signal $V_{\rm ac}$ is applied to gate terminal through an ac coupling capacitor C_1. In the meantime, two dc bias voltages, $V_{\rm GS\_BIA}$ between the gate and the source and $V_{\rm DS\_BIA}$ between the drain and the source, are adopted. The value of C_{iss} can be extracted by the response current $i_{\rm ac}$ under the excitation $V_{\rm ac}$. The curve of $C_{iss}(v_{\rm gs},v_{\rm ds})$ could be obtained by adjusting the two dc bias voltages $V_{\rm GS\_BIA}$ and $V_{\rm DS\_BIA}$. $C_{rss}(v_{\rm gs},v_{\rm ds})$ and $C_{oss}(v_{\rm gs},v_{\rm ds})$ can be extracted in a similar way according to Fig. 5(b) and (c), where ac excitation signal $V_{\rm ac}$ exerts to the gate and drain terminals with coupling capacitors C_1 and C_2. Finally, the nonlinear capacitances $C_{\rm gs}(v_{\rm gs},v_{\rm ds})$, $C_{\rm gd}(v_{\rm gs},v_{\rm ds})$, and $C_{\rm ds}(v_{\rm gs},v_{\rm ds})$ can be calculated according to (4), and then, a 3-D LUT is adopted to exhibit the comprehensive nonlinear characteristics of the SiC MOSFET. However, it is inefficient to extract parameters from a large amount of data and even leads to divergence. In fact, when the SiC MOSFET switches at a high speed, $v_{\rm ds}$ and $v_{\rm gs}$ only go through part of the region on the C–v curved surface, and therefore, it is not necessary to extract all the data under different biased voltages. As the three nonlinear capacitances have the discrepancy in the voltage-dependence characteristics under different switching transients, the LUT can be simplified by eliminating one of the variables, such as $v_{\rm gs}$ or $v_{\rm ds}$, in specific periods of the curved surface. Therefore, it is necessary to set up the nonlinear capacitance model considering the switching trajectory of the SiC MOSFET.

Generally, the range of the gate–source voltage in the gate drivers of the SiC MOSFET is selected as $v_{\rm gs}\in(-5\ {\rm V},\ 20\ {\rm V})$. Taking the bus voltage $V_{\rm dc}=400$ V as an example, the modeling method based on the switching trajectory will be discussed as follows.

A. $C_{gs}(v_{gs},v_{ds})$

The value of $C_{\rm gs}(v_{\rm gs},v_{\rm ds})$ dominates switching periods (t_0,t_2), (t_3,t_4), (t_5,t_6), and (t_7,t_9). According to the formation mechanism of the MOS capacitors, $C_{\rm gs}$ depends on $v_{\rm gs}$ strongly. When $v_{\rm gs}$ is negative, holes accumulate on the top of p-base and the ac measuring signal will respond to the majority carrier, so that it has $C_{\rm gs}\approx C_{ov1}+C_{ov2}+C_{g1}$. When $v_{\rm gs}$ increases, holes are repelled by the electric force while the remaining electrons form a weak inversion layer. In this condition, the thickness of the depleted region enhances with the increase in $v_{\rm gs}$, so the value of C_c will decrease, which leads to the reduction of $C_{\rm gs}$. Once $v_{\rm gs}>V_{\rm TH}$ is achieved, the establishment of the strong inversion layer makes the channel begin to conduct current. Since the source region provides a large number of carriers, C_c can be considered to disappear and the value $C_{\rm gs}$ will increase. It is worthy to note that the increase in the speed of $C_{\rm gs}$ is slow and insignificant, which is abrupt in the Si MOSFET applications [28].

As shown in Fig. 6, it is obvious that $C_{\rm gs}(v_{\rm gs})$ presents a significant concave shape near $v_{\rm gs}\approx 0$ V, so the influence of the gate–source voltage must be incorporated into the model. Since $C_{\rm gs}$ only affects switching transients other than the *du/dt* period, there is no need to take all $v_{\rm ds}$ operation points into consideration. Therefore, two nonlinear curves at $v_{\rm ds}=V_{\rm dc}$ and $v_{\rm ds}=0$ V points are obtained. When $v_{\rm ds}$ changes sharply, taking the average of two curves will not increase the modeling error for the *du/dt* period significantly. In order to avoid discontinuity at dividing points, such as the points at $v_{\rm gs}=5$ V and $v_{\rm gs}=10$ V shown in Fig. 6, the interpolation algorithm is applied to fill the gaps between two discrete data in LUT. Actually, the red-dashed curve in Fig. 6 is the final valid curve of $C_{\rm gs}$, which keeps a smooth transition between the different curves. Then, the modeling of $C_{\rm gs}(v_{\rm gs},v_{\rm ds})$ can be derived as (7), which is marked as Valid curveI, Valid curveII, and Valid curveIII in Fig. 6

$$C_{\rm gs}(v_{\rm gs},v_{\rm ds}) = \begin{cases} C_{\rm gs}(v_{\rm gs})\big|_{v_{\rm ds}=V_{\rm dc}} & v_{\rm ds}>0.9V_{\rm dc} \\ \dfrac{C_{\rm gs}(v_{\rm gs})|_{v_{\rm ds}=V_{\rm dc}}+C_{\rm gs}(v_{gs})\big|_{v_{\rm ds}=0\rm V}}{2} & 0.1V_{\rm dc}<v_{\rm ds}<0.9V_{\rm dc} \\ C_{\rm gs}(v_{\rm gs})\big|_{v_{\rm ds}=0\rm V} & v_{\rm ds}<0.1V_{\rm dc}. \end{cases} \tag{7}$$

B. $C_{gd}(v_{gs},v_{ds})$

The value of $C_{\rm gd}(v_{\rm gs},v_{\rm ds})$ dominates switching periods (t_2,t_3) and (t_6,t_7). $C_{\rm gd}(v_{\rm gs},v_{\rm ds})$ has the most significant nonlinear characteristics among the three interterminal capacitances. On the one hand, $C_{\rm gd}$ is connected between the gate and the source, so that $v_{\rm gs}$ and $v_{\rm ds}$ will influence it strongly. On the other hand, $C_{\rm gd}$ is closely related to the slew rate of $v_{\rm ds}$ as shown in (8) and (9). In the *du/dt* period, $v_{\rm ds}$ changes sharply and $v_{\rm gs}$ is not a constant value due to the DIBL. Therefore, more data and a more detailed regional division of the LUT should be applied to the modeling of $C_{\rm gd}(v_{\rm gs},v_{\rm ds})$

$$\left.\frac{du_{\rm ds}}{dt}\right|_{\rm turn-on} = -\frac{V_{GG}-\frac{V_{\rm mil1}+V_{\rm mil2}}{2}}{R_g C_{\rm gd}(v_{\rm gs},v_{\rm ds})} \tag{8}$$

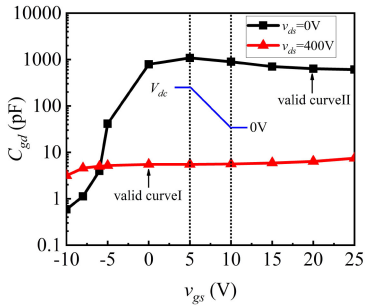

Fig. 7. *C–v* characteristics of gate–drain capacitance during periods when $v_{\rm ds}$ does not change a lot.

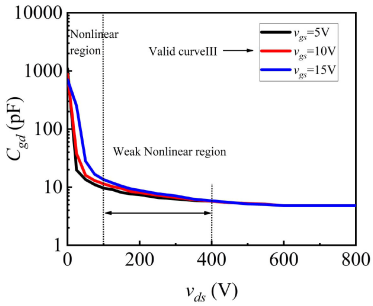

Fig. 8. *C–v* characteristics of gate–drain capacitance during *du/dt* periods with $v_{\rm ds} = 0$–800 V.

$$\left.\frac{du_{\rm ds}}{dt}\right|_{\rm turn-off} = \frac{V_{EE} - \frac{V_{\rm mil1}+V_{\rm mil2}}{2}}{R_g C_{\rm gd}(v_{\rm gs}, v_{\rm ds})}. \tag{9}$$

When the SiC MOSFET is in the OFF-state, the depletion layer inside the n−drift region is established because $v_{\rm gd} < 0$ V. As the value of $v_{\rm gs}$ increases, the voltage across $C_{\rm gd}$ decreases and the thinner depletion layer induces the larger C_{gdg}, so the value of $C_{\rm gd}$ will increase according to (2). Once $v_{\rm gs} > V_{\rm TH}$, the channel is formed, which causes the value of C_{gdg} to increase to the maximum and then start to decrease. However, the value of $C_{\rm gd}$ changes at a very slow speed due to the higher doping concentration of the n−drift layer compared to the Si MOSFET application [28]. It is obvious that the influence of $v_{\rm gs}$ is the dominant factor of $C_{\rm gd}(v_{\rm gs},v_{\rm ds})$ during the periods where $v_{\rm ds}$ does not change a lot. Two curves under the conditions of $v_{\rm ds} = V_{\rm dc}$ and $v_{\rm ds} = 0$ V can be selected to describe this phenomenon, as shown in Fig. 7.

When considering the *du/dt* period, the effects of $v_{\rm gs}$ and $v_{\rm ds}$ should be integrated. Since the range of voltage of this period is about $v_{\rm gs}\in$(5 V,15 V) and $v_{\rm ds}\in(0,V_{\rm dc})$, taking $C_{\rm gd}(v_{\rm ds})$ curves at $v_{\rm gs} = 5$ V, 10 V, 15 V is reasonable for observing the dual voltage-dependence characteristics. As shown in Fig. 8, the trend of $C_{\rm gd}(v_{\rm gs},v_{\rm ds})$ can be divided into the weak nonlinear region and the nonlinear region. When $v_{\rm ds} > 25\% V_{\rm dc}$, where $v_{\rm ds}$ far exceeds the value of $v_{\rm gs}$, and v_{gs} has little effect on $C_{\rm gd}$, the $C_{\rm gd}(v_{\rm ds})$ curve under the $v_{\rm gs} = 10$ V condition is suitable to express this phenomenon. If $v_{\rm ds}$ continues to drop to a lower value compared to $v_{\rm gs}$, the impact of $v_{\rm gs}$ cannot be ignored anymore. The detailed 3-D curved surface expression should be applied to describe the dual voltage dependence of $C_{\rm gd}$, as shown in Fig. 9(b). It should be noted that the data in the LUT are discrete and limited at $v_{\rm gs} = 5$ V, 10 V, and 15 V points and the cubic

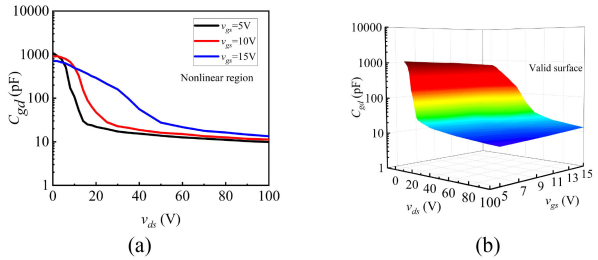

Fig. 9. *C–v* characteristics of gate–drain capacitance during *du/dt* periods with $v_{\rm ds} = 0$–100 V. (a) Two-dimensional curves. (b) Three-dimensional curved surface.

spline interpolation is used to fill the gap between the curves for achieving better accuracy, convergence, and smoothness at the interpolation points. By conversing 2-D curves to the 3-D curved surface, the data of $C_{\rm gd}(v_{\rm ds})$ other than $v_{\rm gs} = 5$ V, 10 V, and 15 V points can be estimated. The modeling of $C_{\rm gd}(v_{\rm gs},v_{\rm ds})$ can be written as (10), which can be found as the Valid curveI and Valid curveII in Fig. 7, Valid curveIII in Fig. 8, and Valid surface in Fig. 9(b)

$$C_{\rm gd}(v_{\rm gs}, v_{\rm ds}) = \begin{cases} C_{\rm gd}(v_{\rm gs})|_{v_{\rm ds}=V_{\rm dc}} & v_{\rm ds} > 0.9V_{\rm dc} \\ C_{\rm gd}(v_{\rm ds})|_{v_{\rm gs}=10\rm V} & 0.25V_{\rm dc} < v_{\rm ds} < 0.9V_{\rm dc} \\ C_{\rm gd}(v_{\rm ds})|_{v_{\rm gs}\in(5\rm V,15\rm V)} & 0.1V_{\rm dc} < v_{\rm ds} < 0.25V_{\rm dc} \\ C_{\rm gd}(v_{\rm gs})|_{v_{\rm ds}=0} & v_{\rm ds} < 0.1V_{\rm dc}. \end{cases} \tag{10}$$

C. $C_{ds}(v_{gs},v_{ds})$

Since the drain–source capacitance $C_{\rm ds}$ does not exist in the gate loop, its influence on the delay period and the *di/dt* period is trivial. The influence of $C_{\rm ds}$ on the switching transients is mainly reflected in the following three aspects, which emphasize the importance of accurate modeling for $C_{\rm ds}(v_{\rm gs},v_{\rm ds})$.

1) In the turn-ON transients, the drain current i_d is the combination of the channel current $i_{\rm ch}$ and the output capacitance discharge current i_{oss}. The simulation error of i_{oss} will cause the inaccuracy in turn-ON losses. The actual channel current of the SiC MOSFET during the turn-ON *du/dt* period can be solved as follows:

$$i_{\rm ch}(t) = i_d(t) - \underbrace{C_{oss}(v_{\rm gs}, v_{\rm ds})\frac{dv_{\rm ds}(t)}{dt}}_{i_{oss}}. \tag{11}$$

2) The value of $C_{\rm ds}$ will affect the discharge speed of the output capacitance, which influences the value of *du/dt* in turn. It has been confirmed that $C_{\rm ds}$ participates in the *du/dt* period as a secondary factor, which can be expressed as [25, eq. (26)].
3) When the switching transients enter the OFF-state, the SiC MOSFET is equivalent to a single capacitance connected in series in the resonant loop. The value of $C_{\rm ds}$ dominates the resonant frequency because the value of $C_{\rm ds}$ is much larger than the value of $C_{\rm gd}$ in the high drain–source voltage range.

When the SiC MOSFET is in the cut-off region, it is reasonable to use the $C_{ds}(v_{ds})$ curve at $v_{\rm gs} = 0$ V to characterize the value

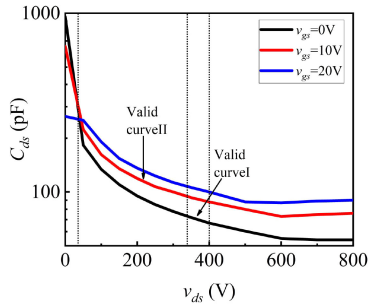

Fig. 10. *C–v* characteristics of drain–source capacitance with $v_{\mathrm{d}s} = 0$–800 V.

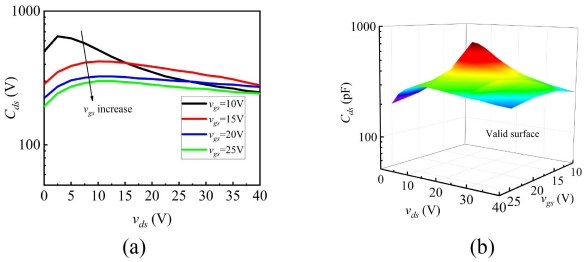

Fig. 11. *C–v* characteristics of drain–source capacitance with $v_{\mathrm{ds}} = 0$–40 V. (a) Two-dimensional curves. (b) Three-dimensional curved surface.

of the drain–source capacitance. As the channel is turned ON, there is a certain change in the value of v_{gs}, and therefore, the $C_{\mathrm{ds}}(v_{\mathrm{ds}})$ curve at $v_{\mathrm{gs}} = 10$ V can be applied when v_{ds} changes in the range of $10\%V_{\mathrm{dc}}$ to $90\%V_{\mathrm{dc}}$, as shown in Fig. 10.

However, the influence of v_{gs} on C_{ds} should not be ignored in the condition when v_{ds} drops to a low value. The reason can be explained as the rise of v_{gs} causes a large number of electrons to gather at the top of the n−drift region, and these carriers communicate with n+ region through the channel. Therefore, the equivalent area of the drain body junction and the carrier concentration at the bottom of the n−drift region will decrease significantly, which means the value of C_{ds} will also decrease. In addition, Fig. 9(a) confirms that the value of C_{gd} will increase obviously in the low drain–source voltage condition, and therefore, the relationship between C_{ds} and *du/dt* becomes nonnegligible when the value difference between C_{ds} and C_{gd} is small. As a solution, a more detailed LUT considering both v_{gs} and v_{ds} should be established in the low drain–source voltage range, as shown in Fig. 11(b). The modeling of $C_{\mathrm{ds}}(v_{\mathrm{gs}},v_{\mathrm{ds}})$ can be expressed as (12), which is shown as the Valid curveI and Valid curveII in Fig. 10 and Valid curved surface in Fig. 11(b)

$$C_{\mathrm{ds}}(v_{\mathrm{gs}}, v_{\mathrm{ds}}) = \begin{cases} C_{\mathrm{ds}}(v_{\mathrm{ds}})|_{v_{\mathrm{gs}}=0} & v_{\mathrm{ds}} > 0.9V_{\mathrm{dc}} \\ C_{\mathrm{ds}}(v_{\mathrm{ds}})|_{v_{\mathrm{gs}}=10\,\mathrm{V}} & 0.1V_{\mathrm{dc}} < v_{\mathrm{ds}} < 0.9V_{\mathrm{dc}} \\ C_{\mathrm{ds}}(v_{\mathrm{ds}})|_{v_{\mathrm{gs}}\in(10\,\mathrm{V},20\,\mathrm{V})} & v_{\mathrm{ds}} < 0.1V_{\mathrm{dc}}. \end{cases} \quad (12)$$

In summary, the nonlinear capacitance model based on the switching trajectory of the SiC MOSFET is shown in Fig. 12. All the data on valid curves and valid curved surfaces about the nonlinear capacitance will be included in the switching trajectory calculation of the SiC MOSFET. For example, when the

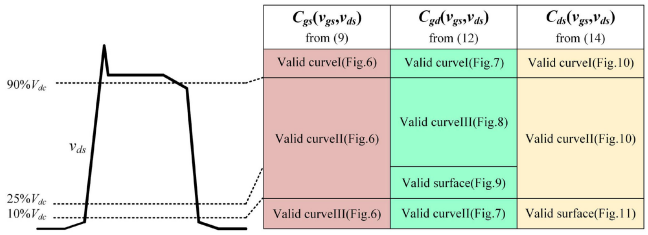

Fig. 12. Nonlinear capacitance model based on switching trajectory of SiC MOSFET.

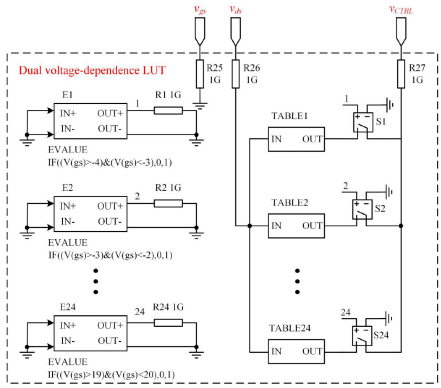

Fig. 13. Implement of dual voltage-dependence LUT in Pspice.

SiC MOSFET is in the turn-ON delay period of (t_0-t_1) in Fig. 4, the voltage trajectory has $v_{\mathrm{gs}}\in(V_{EE},V_{\mathrm{TH}})$ and $v_{\mathrm{ds}} = V_{\mathrm{dc}}$, and therefore, the nonlinear characteristic of $C_{\mathrm{gs}}(v_{\mathrm{gs}},v_{\mathrm{ds}})$ could be represented by the Valid curveI in Fig. 6. Once v_{ds} starts to fall in the *du/dt* period, the data of Valid curveII and curveIII in Fig. 6 will be applied in turn. When the resolution of the parameter's extraction is the same as given in [22], the number of capacitance values required by the proposed modeling method is only 30% of that presented in [22]. It is evident that the proposed modeling method divides the LUT into different data areas reasonably by considering the different voltage dependence in different switching transients. The avoidance of unnecessary data, which is out of the switching trajectory, can reduce the complexity of the model, and the simulation efficiency can be optimized. At the same time, more detailed data during the *du/dt* period are included in the LUT, which ensures the accuracy of the model under the fast switching condition.

IV. Validations

A. Simulation

The Pspice has plentiful specific device models and is used to construct the proposed nonlinear capacitance models of the SiC MOSFET. As the Pspice does not support dual-input single-output table module, the establishment of the dual voltage-dependence LUT is carried out. As shown in Fig. 13, the LUT can be divided into the single-input single-output tables in parallel by applying voltage-controlled switches.

The voltage-controlled capacitance is applied to imitate the nonlinear behavior of the interterminal capacitances inside the SiC MOSFET, as shown in Fig. 14. The description method based

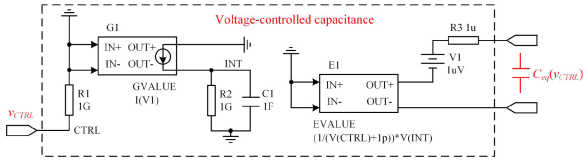

Fig. 14. Implement of voltage-controlled capacitance in Pspice.

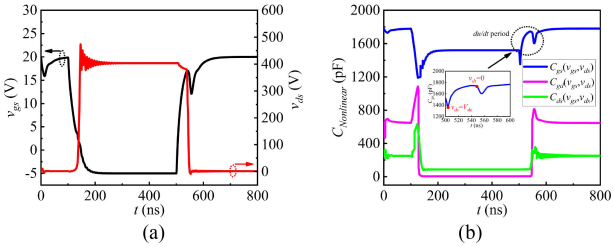

Fig. 15. (a) Switching trajectory. (b) Dynamic output of nonlinear capacitance model.

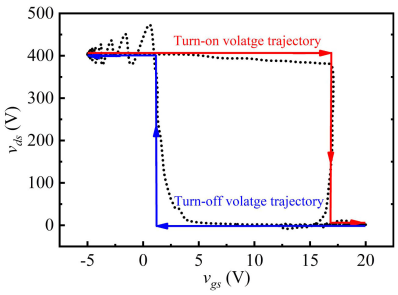

Fig. 16. Voltage trajectory in whole switching period.

on the linear capacitance C_1, the controlled current source G_1, and the controlled voltage source E_1 has good convergence, because no additional differential or integral expressions are required in this method. The equivalent capacitance $C_{\rm eq}$ is completely controlled by the input voltage $v_{\rm CTRL}$, and $v_{\rm CTRL}$ is the output value of the extracted LUT in Fig. 13. It should be noted that dynamic behaviors of the SiC MOSFET is also influenced by the transconductance g_{fs}. The transconductance model in this article is the Shichman–Hodges model, which is widely used by the manufacturers [27].

During the simulations of the DPT, the parameters $R_g = 10\,\Omega$, $L_{\rm loop} = 20$ nH, $I_L = 20$ A, and $V_{\rm dc} = 400$ V and the SiC MOSFET C2M0080120D are selected. The switching trajectories of $v_{\rm gs}$ and $v_{\rm ds}$ are shown in Fig. 15(a). Fig. 15(b) shows the dynamic output of the nonlinear capacitance model based on the switching trajectory of the SiC MOSFET, and it is shown from Fig. 15 that the value of nonlinear capacitances can reflect the dual voltage-dependence dynamically. The zoomed output of $C_{\rm gs}(v_{\rm gs},v_{\rm ds})$ in Fig. 15(b) shows the capacitance $C_{\rm gs}$ keeping smooth at the transition of $v_{\rm ds} = 0$ V to $v_{\rm ds} = V_{\rm dc}$.

The trajectories of $v_{\rm gs}$ and $v_{\rm ds}$ in the whole switching period can be described in Fig. 16, where the voltage trajectory of the ideal switching period (solid line) and the practical switching period (dashed line) forms a closed envelope. Based on the relationship of the voltage trajectory and nonlinear capacitance, only the data around the envelope of the voltage trajectory are

TABLE II
DPT SETTING

Name	Information
V_{dc}	400V
I_L	5~20A
R_g	5~20Ω
V_{GG}/V_{EE}	20V/-4V
C_{dc}	450V/1000μF (2 in series)
L_{loop}	94nH
SiC MOSFET	C2M0080120D (1200V/36A, TO-247)
Voltage probe	SI-9002
Current probe	TCP305A
Oscilloscope	TPS2024B
Temperature	25°C

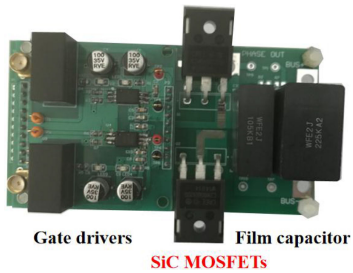

Fig. 17. DPT platform.

considered in the proposed model. Therefore, compared with the model presented in [22], which includes the full data of the whole switching period, the proposed model in this article will have the characteristics of compact size and high accuracy at the same time.

B. Experiment

The DPT is implemented to compare the measured results and the simulated results of the nonlinear capacitance models. The configuration of the DPT is shown in Table II. The body diode of the SiC MOSFET is the freewheeling diode, and the loop parasitic inductance is extracted by ANSYS Q3D. It should be noted that two film capacitors (1 μF/630 V and 2.2 μF/630 V) are connected in parallel on the bus to prevent excessive voltage overshoot induced by the parasitic inductance. Fig. 17 shows the DPT platform.

It is necessary to ensure the measurement error is reduced to an acceptable level when obtaining the switching trajectory of the SiC MOSFET. In order to fulfill this aim, three measures are adopted during the experiment. First, the voltage probes are placed at the root of the device pin as close as possible, as the error caused by the parasitic inductance could be reduced. Second, short and thick jumper wires should be selected in the current measurement, which can reduce the additional parasitic inductance. Third, further alignment of i_d and $u_{\rm ds}$ is implemented because the probe delay would affect the measured results of switching losses. All the errors between the tested switching trajectory and the modeled switching trajectory will be expressed as the relative errors $\Delta\%$

$$\Delta\% = \frac{|x_{\rm test} - x_{\rm model}|}{x_{\rm test}} \times 100\% \tag{13}$$

TABLE III
SWITCHING TRAJECTORY CHARACTERISTICS WITH DIFFERENT R_g ($I_L = 20$ A)

		Turn-on trajectory					Turn-off trajectory				
		Delay	*di/dt*	I_{peak}	*du/dt*	E_{on}	Delay	*du/dt*	V_{peak}	*di/dt*	E_{off}
5Ω	Tested value	83ns	0.77A/ns	25.4A	6.62V/ns	96μJ	85ns	13.81V/ns	442V	0.57A/ns	135μJ
	Modeled value	72ns	0.54A/ns	24.1A	6.06V/ns	85μJ	89ns	10.32V/ns	426V	0.49A/ns	146μJ
	Δ%	13.3%	29.9%	5.1%	8.5%	11.5%	4.7%	25.3%	3.6%	14%	8.1%
10Ω	Tested value	89ns	0.74A/ns	24.8A	6.56V/ns	134μJ	95ns	12.10V/ns	452V	0.5A/ns	148μJ
	Modeled value	81ns	0.59A/ns	23.7A	6.03V/ns	120μJ	99ns	10.00V/ns	468V	0.45A/ns	142μJ
	Δ%	9.0%	20.3%	4.4%	8.1%	10.4%	4.2%	17.4%	3.5%	10%	4.1%
15Ω	Tested value	91ns	0.71A/ns	24.8A	5.26V/ns	135μJ	102ns	12.9V/ns	450V	0.47A/ns	160μJ
	Modeled value	84ns	0.63A/ns	25.1A	5.33V/ns	143μJ	93ns	10.5V/ns	471V	0.43A/ns	154μJ
	Δ%	7.7%	11.3%	1.2%	1.3%	5.9%	8.8%	18.6%	4.7%	8.5%	3.8%

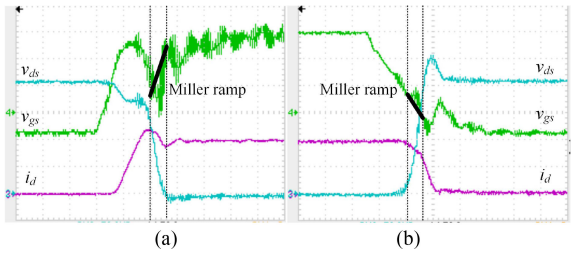

Fig. 18. Experimental results of switching trajectory of SiC MOSFET with $R_g = 20\ \Omega$ and $I_L = 20$ A. (a) Turn-ON. (b)Turn-OFF. $v_{\rm gs}$ (5 V/div), $v_{\rm ds}$ (100 V/div), i_d (10 A/div), time (50 ns/div).

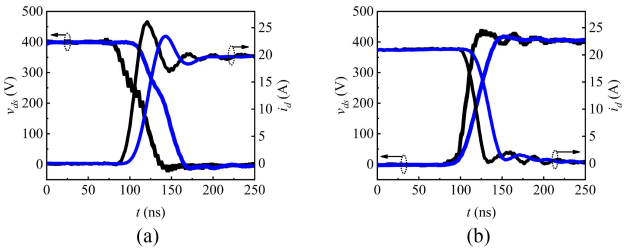

Fig. 19. Comparison of experimental and simulation waveforms when applying the CREE model ($R_g = 5\ \Omega$ and $I_L = 20$ A). (a) Turn-ON. (b) Turn-OFF.

where $x_{\rm test}$ is the measured value and $x_{\rm model}$ is the modeled value.

The switching trajectory of the tested SiC MOSFET with $R_g = 20\ \Omega$ and $I_L = 20$ A is shown in Fig. 18. It is obvious that $v_{\rm gs}$ has a "Miller ramp" rather than a constant value. As discussed in Section III-B and -C, the nonlinear capacitance models considering both $v_{\rm gs}$ and $v_{\rm ds}$ should be established during the *du/dt* periods.

In the official model of C2M0080120D provided by the CREE, $C_{\rm gs}$ and $C_{\rm ds}$ both taken as constant values, and the value of $C_{\rm gd}$ is expressed as the hyperbolic tangent function of $v_{\rm gd}$. As shown in Fig. 19, the switching trajectories of the SiC MOSFET for the CREE model show considerable errors compared with the measured results because the modeling of nonlinear capacitances is incomplete. When the switching losses are taken as the comparison objects, the measured turn-ON loss is 96 μJ, whereas the turn-ON loss for the CREE model is 147 μJ, which means a large relative error reaching 53.1%. The turn-OFF loss in the experiment is 135 μJ, whereas 160 μJ is calculated for the CREE model, which means $\Delta\%$ is 15.6%.

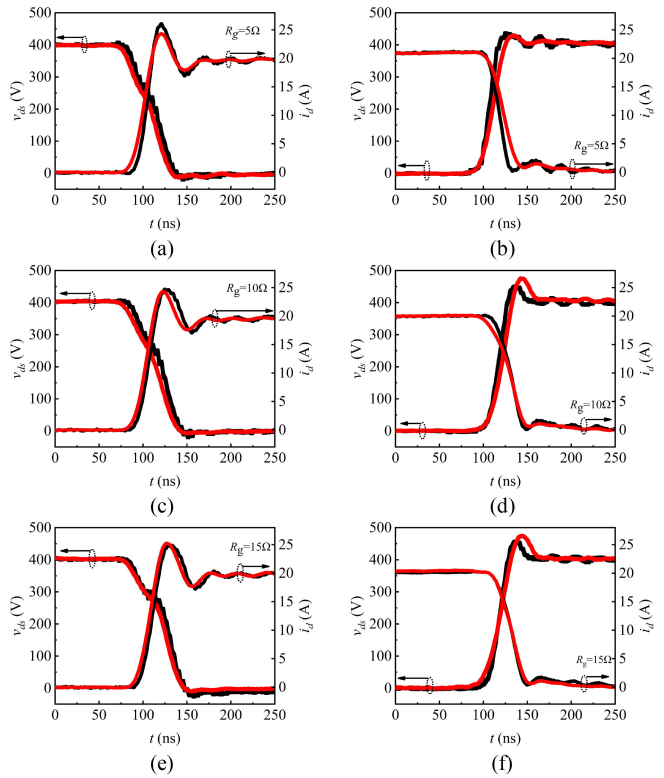

Fig. 20. Comparisons of experiment and simulation waveforms when applying the proposed model ($I_L = 20$ A). (a) Turn-ON with $R_g = 5\ \Omega$. (b) Turn-OFF with $R_g = 5\ \Omega$. (c) Turn-ON with $R_g = 10\ \Omega$. (d) Turn-OFF with $R_g = 10\ \Omega$. (e) Turn-ON with $R_g = 15\ \Omega$. (f) Turn-OFF with $R_g = 15\ \Omega$.

The nonlinear capacitance model considering the switching trajectory of the SiC MOSFETs can make the simulation waveforms closer to the measured results. Fig. 20 shows the comparisons between the experimental results and the simulation results of the switching trajectories. Since a more comprehensive LUT is applied to the model, the delay time, slew rate, and overshoot of the switching trajectories correspond very well with the experiment. The switching trajectory characteristics of the SiC MOSFET with different R_g values are listed in Table III when the load current is 20 A. It is not difficult to find that when $R_g = 5\ \Omega$ is selected, the relative error of the turn-ON loss is only 11.5%, whereas the relative error of the turn-OFF loss is 8.1%, which is far better than the CREE model. As shown in Fig. 21, the proposed model presents good accuracy of switching losses in a

TABLE IV
SWITCHING TRAJECTORY CHARACTERISTICS WITH DIFFERENT I_{L} ($R_{\mathrm{G}} = 5\ \Omega$)

		Turn-on trajectory					Turn-off trajectory				
		Delay	di/dt	I_{peak}	du/dt	E_{on}	Delay	du/dt	V_{peak}	di/dt	E_{off}
10A	Tested value	88ns	0.67A/ns	16.5A	9.09V/ns	42μJ	95ns	11.81V/ns	427V	0.28A/ns	35.4μJ
	Modeled value	79ns	0.53A/ns	14.8A	6.15V/ns	38μJ	84ns	8.89V/ns	414V	0.22A/ns	39.4μJ
	Δ%	10.3%	20.9%	10.3%	32.3%	9.5%	11.6%	24.7%	3.0%	21.4%	11.3%
15A	Tested value	88ns	0.67A/ns	16.5A	7.41V/ns	58μJ	95ns	11.76V/ns	430V	0.58A/ns	87.8μJ
	Modeled value	80ns	0.65A/ns	14.8A	6.25V/ns	67μJ	84ns	9.76V/ns	418V	0.54A/ns	77.2μJ
	Δ%	9.1%	3.0%	10.3%	15.7%	15.5%	11.6%	17%	2.8%	6.9%	12.1%

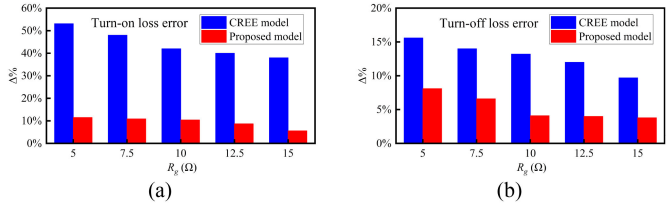

Fig. 21. Comparisons of switching losses errors between the CREE model and the proposed model with different R_g ($I_L = 20$A). (a) Turn-ON. (b) Turn-OFF.

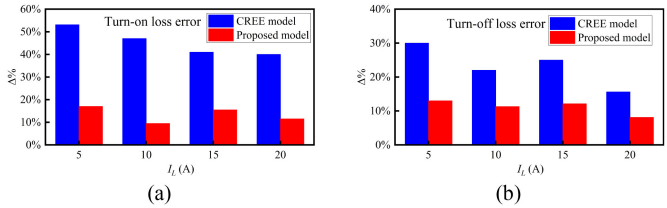

Fig. 23. Comparisons of switching losses errors between the CREE model and the proposed model with different I_L ($R_g = 5\ \Omega$). (a) Turn-ON. (b) Turn-OFF.

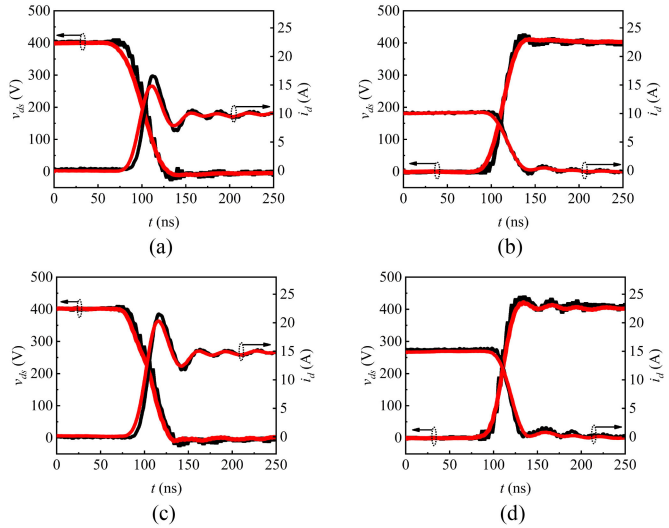

Fig. 22. Comparison of experimental and simulation waveforms when applying the proposed model ($R_g = 5\ \Omega$). (a) Turn-ON with $I_L = 10$ A. (b) Turn-OFF with $I_L = 10$ A. (c) Turn-ON with $I_L = 15$ A. (d) Turn-OFF with $I_L = 15$ A. .

wide range of the switching speed, and the advantage becomes more significant while R_g is relatively high.

Comparisons of experimental and simulation waveforms when applying the proposed model at different load currents are shown in Fig. 22. It can be seen that the proposed model has good performance in predicting the dynamic characteristics of the SiC MOSFET. Table IV gives the detailed data of the experiment and the simulation results, and Fig. 23 shows the relative errors in different load currents when $R_g = 5\ \Omega$ is selected. It is obvious that the accuracy of the model is high in a wide load current range, which makes up for the shortcomings of the CREE model.

The complexity, accuracy, and simulation speed are three key criteria for evaluating the device model, as shown in Table V. It should be noted that the computer configuration used for the comparison is the Intel Core i5-7th Gen, and Pspice 16.6 is the software version where the maximum step size is selected as 0.1 ns. In terms of the complexity of the model, the size of the CREE model is 5 kB, the size of the model presented in [22] is 37 kB, and the size of the model proposed in this article is 10.5 kB. The smaller size benefits from the simplified LUT and the compact form of the voltage-controlled capacitance. In terms of the accuracy of the model, the relative error of the proposed model is only 3.1% lower than that presented in [22] (turn-ON loss with $R_g = 5\ \Omega$, $I_L = 20$ A) because the critical data of the interterminal capacitances are taken into consideration. The comparison of the simulation speed is carried out with the running time of 1 μs of DPT. In Pspice, the local convergence speed of the Newton–Raphson iterative solution is related to the simulation speed directly. Only 9.4 s are required in the DPT simulation applying the proposed model, which is only 47% of the time cost in [22].

TABLE V
PERFORMANCE OF DIFFERENT MODELS

Model type	Size	Error (Δ%)	Simulation time
CREE Model	5KB	53.1%	2.9s
Model in [22]	37KB	8.4%	19.8s
Proposed model	10.5KB	11.5%	9.4s

Different from the official model, the authors in [17]–[21] modeled the nonlinear capacitance with the fitting functions. To verify the performance of the proposed model, comparisons between the different models are carried out.

Fig. 24 shows the comparisons of the nonlinear capacitance model, where the capacitance models of C_{gs} and C_{gd} in [18] and C_{ds} in [20] are adopted due to the relatively high accuracy compared with other methods with fitting function. In [18], a hyperbolic-tangent-based function describes the impact of v_{gs} on C_{gs}, then the dynamic switching period could be modeled. However, the v_{gs} and v_{ds} change sharply during the switching

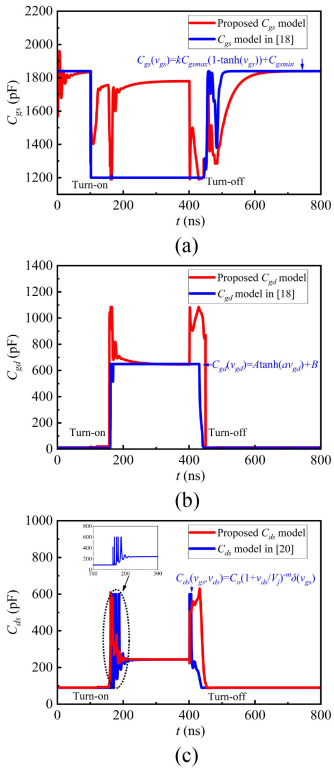

Fig. 24. Comparisons of nonlinear capacitance model (a) $C_{\rm gs}$. (b) $C_{\rm gd}$. (c) $C_{\rm ds}$.

period. It can be seen in Fig. 24(a) that the proposed model performs more dynamically than the model presented in [18] during the turn-ON and the turn-OFF transitions. Fig. 24(b) shows that the proposed $C_{\rm gd}$ model has larger dynamic responses at the switching period than the model presented in [18], and so better accuracy can be realized for the simulation models. The exponential function with a correction factor is used in [20] for the $C_{\rm ds}$ model, where the $v_{\rm ds}$ and $v_{\rm gs}$ are taken as variables for the exponential function and the correction factor, respectively. In this case, the output in [20] and the proposed model is similar, as shown in Fig. 24(c). However, obvious oscillations occurred in the model [20] during the turn-ON period, which would cause the divergence. As mentioned in [22], the accuracy of the capacitance model is directly related to the amount of valid data. Since the proposed model based on the numerical simulated LUT may include more valid data than the models based on the fitting function, the improved accuracy for the nonlinear capacitance model would be realized in this article.

The switching losses are calculated and compared between a composite model ($C_{\rm gs}$ and $C_{\rm gd}$ in [18] and $C_{\rm ds}$ in [20]) and the proposed model with different R_g, as shown in Fig. 25. It can be seen that the proposed model has better accuracy than the composite model in predicting switching losses for the SiC MOSFETs. When $R_g = 10\ \Omega$ and $I_L = 20$ A are selected, the proposed model has only 10.4% relative error in turn-ON loss and 4.1% relative error in turn-OFF loss, while the relative errors are 12.2% and 9.7% in the composite model, respectively.

The simulation speed is evaluated with the DPT circuit ($R_g = 10\,\Omega, I_L = 20$ A) for the different models under the same

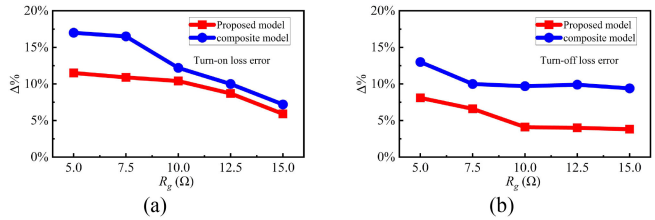

Fig. 25. Comparisons of switching losses between the composite model and the proposed model with different R_g ($I_L = 20$A). (a) Turn-ON. (b) Turn-OFF.

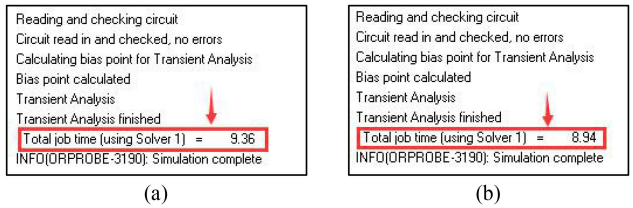

Fig. 26. Comparison of simulation speed (DPT circuit, $R_g = 10\,\Omega, I_L = 20$ A). (a) Proposed model. (b) Composite model.

TABLE VI
FULL-BRIDGE INVERTER TEST SETTING

Name	Information
V_{dc}	200 V
L_{load}	5 mH
R_{load}	10 Ω
R_g	10 Ω
Modulation Ratio	0.8
Switching frequency	10 kHz
Output frequency	50 Hz

solver configurations applied in Table V (maximum step size, 0.1 ns; running time, 1 μs). As shown in Fig. 26, the composite model takes 8.94 s, whereas the proposed model takes 9.36 s. Obviously, the advantage of simulation speed for the model with a fitting function is trivial as the complex nonlinear function is used. Therefore, considering the accuracy and simulation speed, the proposed model is superior to the models presented in [17]–[21].

C. System-Level Validation

In order to verify the performance of the proposed model, the system-level simulation and experiment are carried out based on a single-phase full-bridge inverter with *RL* load. Table VI presents the parameters of the single-phase full-bridge inverter. The unipolar sinusoidal pulsewidth modulation (SPWM) and the bipolar SPWM are applied to the full-bridge inverter for evaluating the model more comprehensively, as shown in Fig. 27. The experimental prototype is implemented by adopting two half-bridge circuits shown in Fig. 17.

Fig. 28 shows the experimental results of the full-bridge inverter with the unipolar SPWM and bipolar SPWM. Fig. 29 shows the simulation results with the proposed model. It can be seen that there is no obvious distortion in the waveforms of $v_{\rm AB}$ and $i_{\rm load}$, and no significant errors occur between the measured results and simulated results.

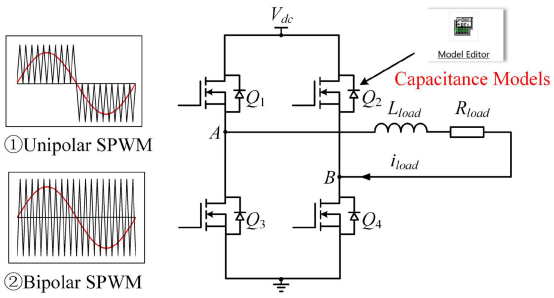

Fig. 27. Single-phase full-bridge inverter.

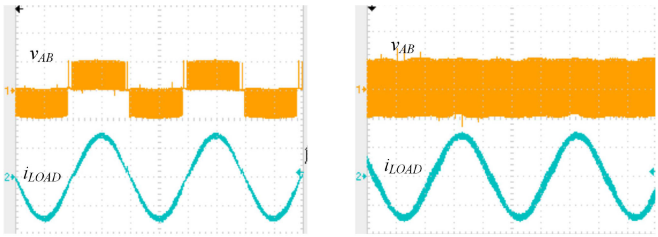

Fig. 28. Experimental results of the full-bridge inverter. (a) Unipolar SPWM. (b) Bipolar SPWM. $V_{\rm AB}$ (200 V/div), $i_{\rm load}$ (10 A/div), time (2.5 ms/div).

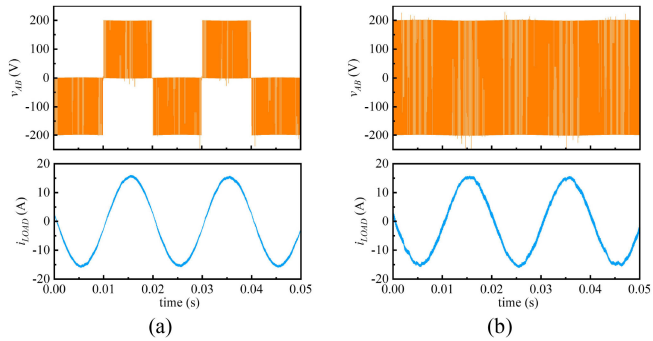

Fig. 29. Simulation results of the full-bridge inverter with the proposed model (maximum step size, 10 ns). (a) Unipolar SPWM. (b) Bipolar SPWM.

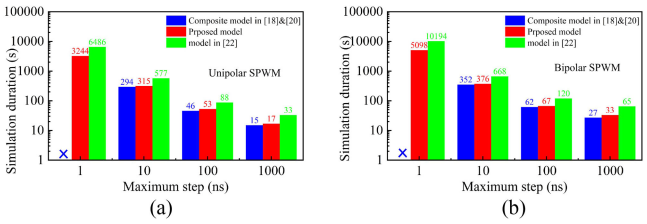

Fig. 30. Comparisons of simulation speed of the full bridge inverter with different models (running time, 20 ms). (a) Unipolar SPWM. (b) Bipolar SPWM.

It is known that with the decreasing of the maximum simulation step size, the simulation accuracy and time cost will increase [29]. Fig. 30 compares the simulation speed of the full-bridge inverter with different models in varied maximum step sizes, where the same solver as the one presented in Section IV-B is used. It can be seen that the bipolar SPWM takes more time than the unipolar SPWM because two switches of the unipolar SPWM work at a low frequency (50 Hz). Fig. 30 shows the proposed

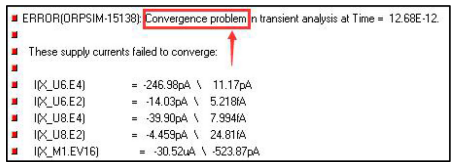

Fig. 31. Divergence of composite model.

model has obviously higher simulation speed compared to the model presented in [22], where the simulation speed of the proposed model is close to that of the composite model in [18] and [20]. It should be mentioned that the system-level simulation with the composite model has the divergency problem at the maximum step size of 1 ns, as shown in Fig. 31. Therefore, good convergence performance for the proposed model has been validated in the system-level simulation.

V. Conclusion

A nonlinear capacitance model based on the envelope of switching trajectory of the SiC MOSFET was proposed in this article, which can predict the dynamic characteristics of the SiC MOSFET efficiently. On one hand, the proposed model could obtain higher accuracy than the conventional model since the dual voltage-dependence of the interterminal capacitances was considered and the accurate LUT was applied. On the other hand, the proposed model has the advantages of simplified expression and high simulation speed, as the unnecessary data of the nonlinear capacitances out of the switching trajectory were neglected. The implementation method of the proposed model in Pspice was described in detail, whereas the correctness of the model was verified well in the DPT with different gate resistances and different load currents, and in the full-bridge inverter with different modulations.

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