Fast Discharging (N+1) Switch Converter With Regenerative Flyback Operation for N-Phase SRM Drives

Ashwani Kumar Rana, *Student Member, IEEE*, and A. V. Ravi Teja, *Member, IEEE*

***Abstract*—This article proposes a converter topology that can provide fast discharging for any N-phase switched reluctance motor (SRM) drive. The proposed converter achieves fast discharging with only (N+1) switches for an N-phase SRM drive. The discharging can also be varied and made faster as per requirement. The proposed converter achieves fast discharging by dumping the winding energy to a capacitor and feeding it back to the source through a flyback transformer. The proposed converter uses fewer switches, is easy to control, and has variable discharging voltage which can be made much greater than the supply voltage. The proposed converter has been implemented with a four-phase SRM drive using MATLAB/Simulink software and the results are presented. A hardware prototype of the proposed converter is developed in the laboratory and tested on a four-phase SRM. The corresponding experimental results are presented at different operating conditions. The proposed converter is also compared with other existing SRM converters with respect to different performance metrics and a detailed comparison table is presented. Using the proposed converter, a minimum discharge time of 0.32 ms has been achieved at 3 A reference current.**

***Index Terms*—Capacitance minimization, flyback, modular converter, switched reluctance motor (SRM) converter, torque ripple.**

I. Introduction

SWITCHED reluctance motor (SRM) offers numerous advantages like fault tolerance, robust operation, comprehensive speed range capability, low cost, and high-reliability. However, SRM is a highly nonlinear motor and has some issues like torque ripple, acoustic noise, and vibrations [1]–[3]. Recent developments in control algorithms and advanced converters have made it easier to overcome these issues. Advance control algorithms such as torque sharing functions (TSF) [2], [4]–[10], direct torque control [11], [12], sliding mode control (SMC) [13], [14], model predictive control (MPC) [15], [16], and fuzzy logic-based techniques [17], [18] improve the performance of SRM. However, these are not fully able to reduce the limitations. Hence, power converter has a crucial role in SRM drive operation [19]. Various converters are being used for the SRM drives, such as conventional asymmetrical converter [20], C-dump converter [21], [22], and high demagnetizing converter [23]. SRM being a multiphase machine requires more number of switches with increasing number of phases. A higher number of switches increases the cost of the converter and makes it bulky. Therefore, the development of the power converters with low cost (lesser switches) and giving less torque ripple is desirable for SRM drive development [24], [25]. For achieving minimum torque ripple, fast demagnetization must be done by the converter. In a conventional asymmetrical converter, same dc voltage is used for charging and discharging the SRM windings. Hence, the dc bus voltage has to be increased to increase the charging or discharging times [20]. Conventional C -dump converter requires a high capacitance with voltage rating equal to double the demagnetizing voltage. Also, this converter does not fully transfer the energy back to source [21]. Improved C-dump converter is presented in [22], but it does not provide a detailed analysis of the capacitor design and requires a high-value of capacitor for effective demagnetization. A variable voltage converter is proposed in [23]. It has a lower number of switches but lacks phase independence in multiphase SRM machines. The integrated multiport converter is also becoming popular in SRM for reduction of capacitance requirement in dc bus [26]. For fast magnetizing and demagnetizing, a three-phase asymmetrical converter is proposed in [27] but this converter requires an extra switch along with two switches per phase. It also requires a high value of capacitor and lacks phase independence. Recently, some converters are developed to extend the fault-tolerant capability [28]–[34] but they require a large number of switches and relays. A converter with extended speed capabilities is presented in [35] but this converter is bulky due to extra windings. A converter with voltage boost features is presented in [36]. This converter is designed for fast excitation of SRM at higher speeds. For higher efficiency, a low-cost converter is proposed in [37], but it is bulky in size.

In this article, a converter requiring minimum switches is proposed which is suitable for any N-phase SRM drive. The proposed converter requires a smaller value of capacitor, across which desired demagnetizing voltage is maintained. This voltage is used to discharge the SRM windings quickly. A flyback converter is integrated with this capacitor for regenerative action.

Manuscript received December 23, 2021; accepted February 5, 2022. Date of publication February 10, 2022; date of current version March 24, 2022. This work was supported by the Department of Science and Technology (SERB), Govt. of India, under Grant SRG/2019/001356. Recommended for publication by Associate Editor E. Armando. *(Corresponding author: A. V. Ravi Teja.)*

The authors are with the Department of Electrical Engineering, Indian Institute of Technology Ropar, Rupnagar 140001, India (e-mail: 2017eez0002@iitrpr.ac.in; rabiteza@gmail.com).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3150229.

Digital Object Identifier 10.1109/TPEL.2022.3150229

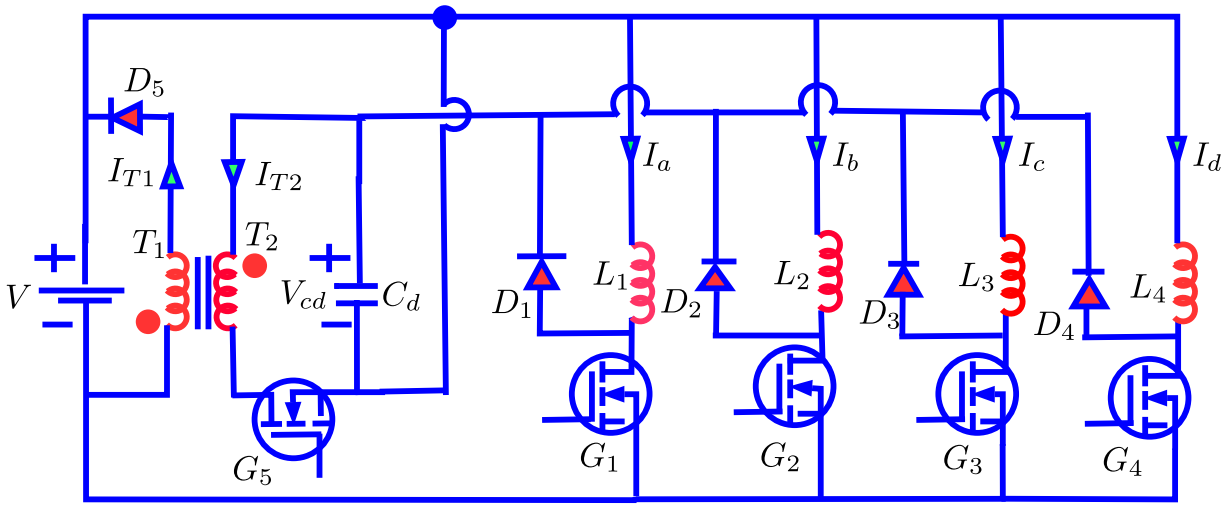

Fig. 1. Circuit diagram of the proposed converter.

The flyback operation is performed using a high frequency switch in order to reduce the size of the core and hence the converter. The proposed converter can be extended for more number of phases with minimum number of changes. The unique features offered by the proposed converter are outlined as follows.

1) The proposed converter has almost half the number of switches when compared with the conventional asymmetrical converter.
2) It has a variable voltage discharging capability with minimum voltage stress on the capacitor unlike conventional C-dump converter.
3) The capacitor requirement is small as compared to other existing converters.
4) The integrated flyback converter facilitates regenerative action to the source.
5) The proposed converter can be extended to a higher number of phases with only one extra switch per phase.

The rest of this article is organized as follows. Section II presents the proposed SRM converter topology and its modes of control. The control of SRM drive employing the proposed converter is explained in Section III. Capacitance calculation and design of flyback transformer are explained in Sections IV and V, respectively. Simulation study is presented in Section VI. Experimental prototype description and hardware results are presented and explained in Section VII. Comparative analysis is presented in Section VIII. Finally, Section IX concludes this article.

II. Proposed Converter and Its Modes of Control

The proposed converter is shown in Fig. 1. The proposed converter is used to drive the four phase 8/6 SRM drive. This converter is suitable for four phase SRM drive but can be extended to more number of phases by adding one switch per phase. The converter is divided into two parts. The first part has four switches and used to excite the phase windings independently while the second part consists of switch G_5, capacitor C_d and flyback inductor. The switch G_5 is used additionally to modulate the discharging voltage V_{cd} and send the energy back to the source through flyback operation. The capacitor C_d is employed for freewheeling and discharging operation of the phase winding.

The modes of operation of proposed converter are shown in Fig. 2. It has four modes of operation which are defined as follows:

Mode 1: Excitation mode [see Fig. 2(a)].
Mode 2: Discharging mode [see Fig. 2(b)].
Mode 3: Flyback mode-a [see Fig. 2(c)].
Mode 4: Flyback mode-b [see Fig. 2(d)].

A. Excitation Mode

In Mode 1 or the excitation mode, the winding is excited with source voltage by turning ON the switch G_1 for phase-a. Similarly, switch G_2 is turned ON for exciting phase-b and so on. In this mode, the dc source is directly connected to the phase winding and the winding charges in the path as shown in Fig. 2(a) for phase-a.

B. Discharging Mode

In Mode 2 or the discharging mode, the winding is discharged through capacitor C_d with voltage $-V_{cd}$ when the switch G_1 (for phase-a) is turned OFF. In this mode, the current completes its path through L_1, D_1, and C_d (for phase-a) as shown in Fig. 2(b). Discharging of the other phase windings is similarly achieved by turning OFF their respective series connected switches (G_2–G_4 for phase-b to phase-d).

C. Flyback Mode-A and Flyback Mode-B

Flyback mode-a (Mode 3) and flyback mode-b (Mode 4) are used whenever we need to discharge the capacitor C_d and give this energy back to the dc source.

In Mode 3 or the flyback mode-a, the switch G_5 is turned ON and the capacitor's energy is transferred to the T_2 coil of the

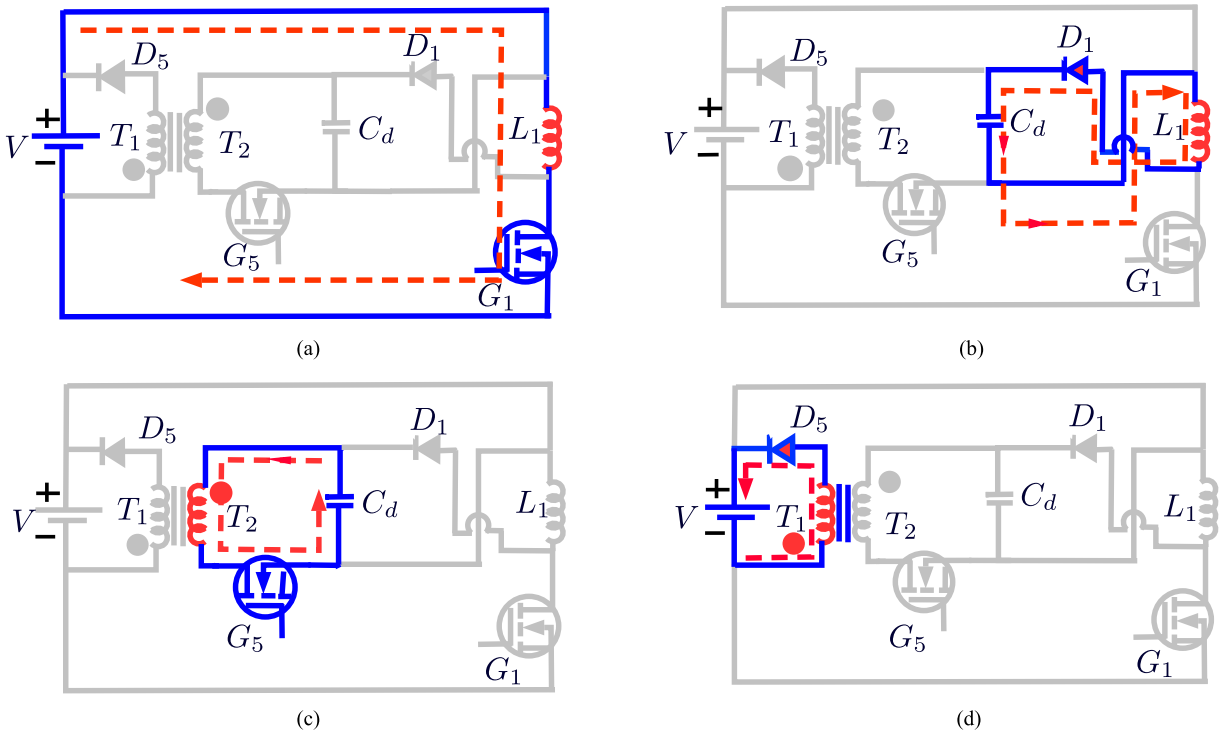

Fig. 2. Modes of operation of the proposed converter. (a) Mode 1: Excitation mode. (b) Mode 2: Discharging mode. (c) Mode 3: Flyback mode-a. (d) Mode 4: Flyback mode-b.

flyback transformer. In this mode, the current path completes through C_d, G_5, and T_2 of flyback as shown in Fig. 2(c).

In Mode 4 or the flyback mode-b, the switch G_5 is turned OFF. The energy in the T_2 coil discharges to the dc source through T_1 coil and diode D_5 as shown in Fig. 2(d).

III. Control of SRM Drive Using the Proposed Converter

To understand the control, the mathematical modeling [1] of 4-phase 8/6 SRM is given as follows:

$$V = R_s i + \frac{d\psi(\theta, i)}{dt} \tag{1}$$

where R_s, $\psi(\theta, i)$, V, i, are the per phase winding resistance, flux linkage per-phase voltage, and current, respectively, of the stator winding and θ is the rotor position.

$\psi(\theta, i)$ is given by

$$\psi(\theta, i) = L(\theta, i) * i \tag{2}$$

where $L(\theta, i)$ is the inductance per phase.

SRM is a nonlinear motor and the torque per phase is given by

$$T_e = \frac{\partial(\int L(\theta, i) i di)}{\partial\theta}. \tag{3}$$

When SRM is operating in the linear operating region ($\frac{dL(\theta,i)}{d\theta}$ is constant), the per phase torque can be calculated as

$$T_e = \frac{dL(\theta, i)}{d\theta} * \frac{i^2}{2}. \tag{4}$$

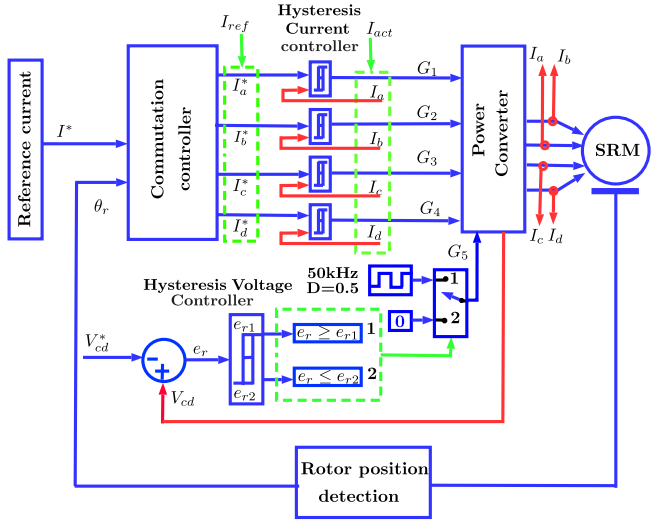

Fig. 3. Block diagram of SRM drive using the proposed converter.

The control block diagram is given in Fig. 3 and explained as follows.

1) *Reference current (I^*):* Reference current is selected based on the torque requirement of the drive.
2) Rotor position, current, and voltage detection
   a) Rotor position is detected using speed encoder and fed back to the controller.
   b) All the four phase currents of SRM (I_a, I_b, I_c, and I_d) are sensed using current sensors and fed back to the controller through ADC.

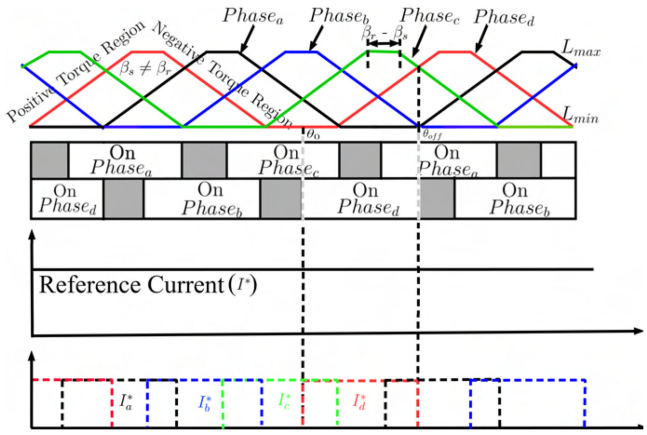

Fig. 4. Four-phase inductance profile with phase reference currents generated by the commutation controller.

c) Capacitor voltage V_{cd} is also sensed using a voltage sensor and fed back to the controller through ADC.

3) *Commutation controller:* This generates the individual phase current references (I_a^*, I_b^*, I_c^*, and I_d^*) from the reference current based on rotor position as follows.
Typical inductance profile of a four-phase SRM plotted with respect to rotor position (θ) is given in Fig. 4. Any SRM phase provides positive torque for a phase current in positive slope region of inductance, zero torque in zero slope region of inductance, and negative torque in negative slope region of inductance. Therefore, for running the motor in positive direction, we need to switch the phases and provide current in their respective positive slope regions only. Therefore, the commutation controller receives rotor position feedback from the encoder connected to the SRM and generates phase current references only during the turn-ON and turn-OFF periods of the respective phases. Other than this period, the phase currents references are made zero. This ensures that the phase current is present only during θ_{ON} to θ_{OFF} period, thus giving a continuous positive torque on the motor.
4) *Hysteresis current controller:* The hysteresis current controller gives gate pulses according to the error between the reference and actual currents of a phase. A hysteresis band is selected with suitable upper and lower limits. If the current error exceeds the upper limit, the respective switch is turned OFF (mode 2). Similarly, if the current error falls below the lower limit of the hysteresis band, the switch is turned ON (mode 1). Four such hysteresis controllers are employed for controlling the four phase currents. The corresponding gate pulses are given to the four switches G_1–G_4, respectively.
5) *Hysteresis V_{cd} voltage controller:* This decides the operation of flyback converter. First, the desired demagnetizing voltage to be applied on the SRM windings is selected as the reference V_{cd}^*. The error e_r between the actual V_{cd} (from voltage sensor) and V_{cd}^* is given to a hysteresis controller with a desirable band. If the error $e_r \geq e_{r1}$ (e_{r1} is the upper limit of the hysteresis band), then a 50 kHz gate pulse with 0.5 duty ratio (mode 3 and mode 4) is given to the flyback converter switch G_5. This feeds back the excess energy at the capacitor C_d to the source and hence the voltage V_{cd} decreases until e_r goes below e_{r2}. In the case when the error $e_r \leq e_{r2}$ (e_{r2} is the lower limit of the hysteresis band), then the flyback converter is laid to rest by giving a zero gate pulse to switch G_5. Since the flyback is not operating, power is not fed back to the source. In this period, whenever a phase is demagnetizing, the voltage V_{cd} increases until e_r goes beyond e_{r1}.
6) *Control of the proposed power converter:* The control of SRM currents and V_{cd} voltage using different modes of the proposed converter is shown in Fig. 5. When a reference current I_a^* is given, mode 1 is applied to increase the phase current from zero. When the reference current is reached, mode 1 and 2 are alternately applied based on hysteresis current controller and the phase current is maintained. After this, when the reference current becomes zero, mode 2 is applied permanently (until again the reference is given). V_{cd} control is done by the voltage hysteresis controller using modes 3 and 4.

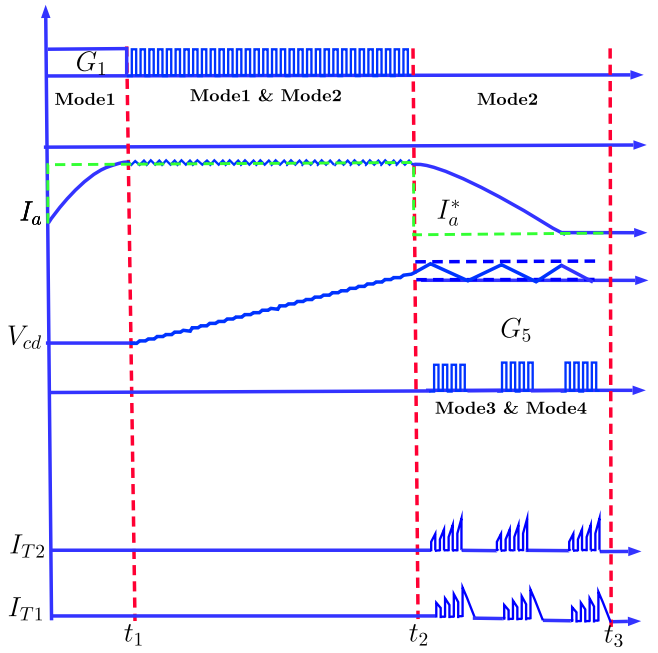

Fig. 5. Sample waveforms of the SRM drive control using the modes of proposed converter.

IV. Capacitance Calculation

The capacitance requirements can be calculated from the amount of energy to be stored. The voltage V_{cd} of the capacitor C_d (see Fig. 1) is used to discharge the phase winding. Let E_m be the energy stored in the winding which needs to be discharged to the capacitor C_d

$$E_m = \int_{\theta_u}^{\theta_a} i(\psi, \theta)\, d\psi. \tag{5}$$

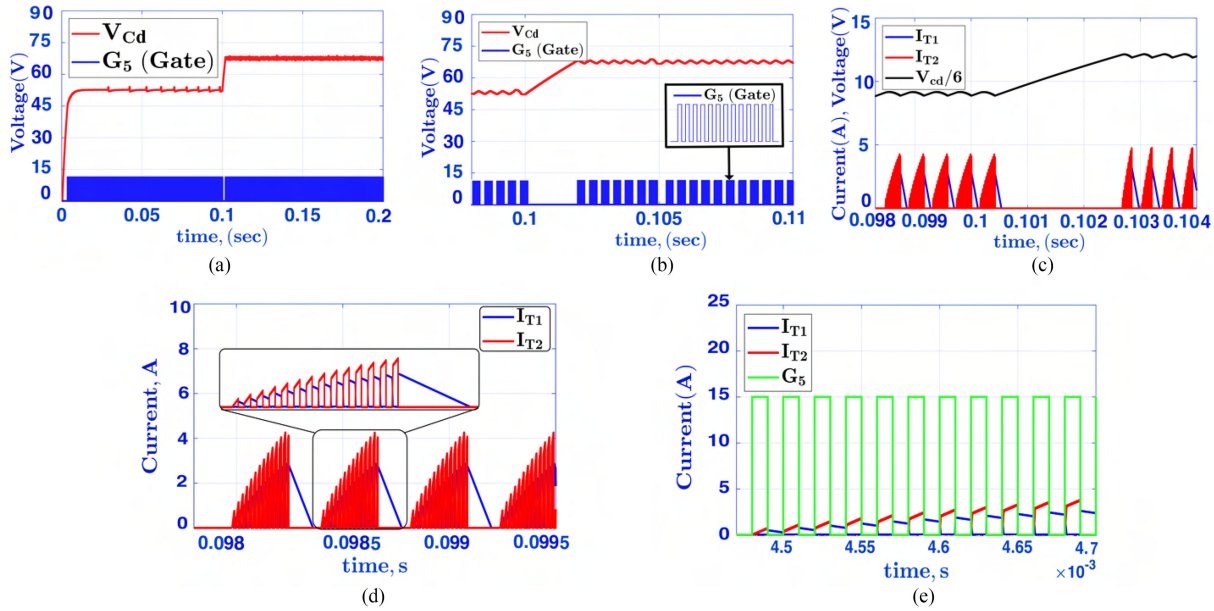

Fig. 6. Simulation results of flyback operation to control V_{cd} in proposed converter. (a) V_{cd} and G_5 gate pulses during a change in V^*_{cd} from 48 to 72 V. (b) Magnified view of V_{cd} and G_5 gate pulses during a change in V^*_{cd} from 48 to 72 V. (c) V_{cd}, I_{T1}, and I_{T2} during a change in V^*_{cd} from 48 to 72 V. (d) Magnified view of I_{T1} and I_{T2}. (e) Magnified view of I_{T1} and I_{T2} along with G_5 gate pulse.

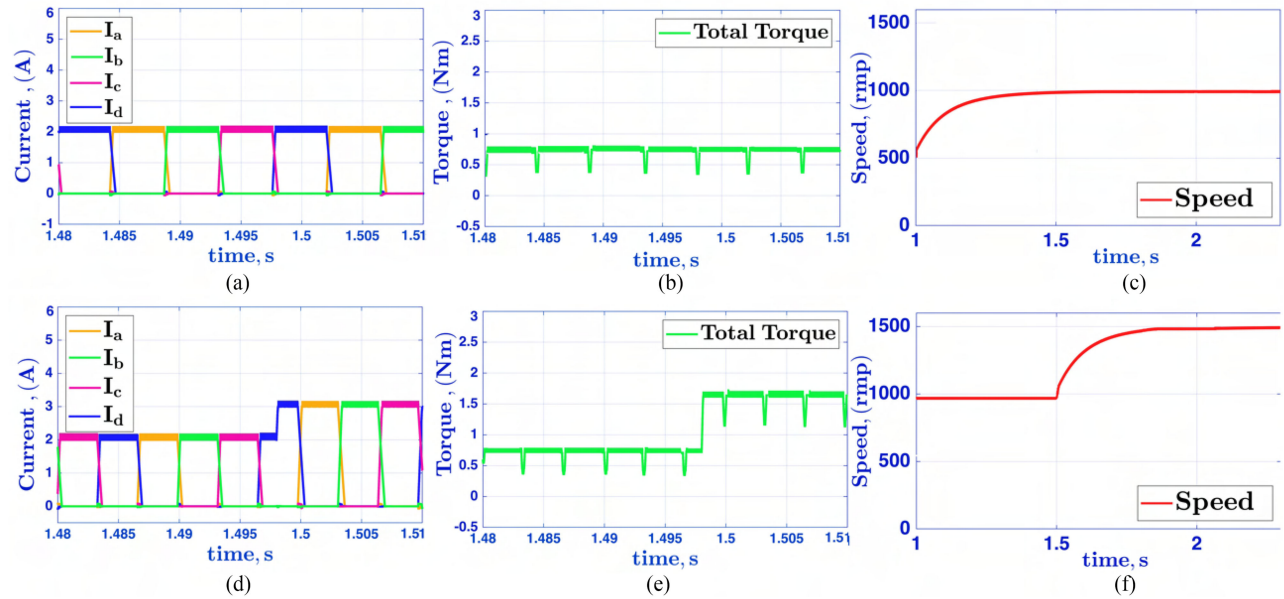

Fig. 7. Simulation results of current control of SRM drive. (a) Four phase currents of SRM drive. (b) Total torque. (c) Speed at 2 A reference current. (d) Current dynamics of SRM drive when I^* is changed from 2 to 3 A. (e) Change in total torque due to current dynamics. (f) Speed dynamics of SRM.

When the motor operated in the linear mode, it can be further simplified as

$$E_m = \int_{\theta_u}^{\theta_a} i(\psi,\theta)\, d\psi = \frac{1}{2}\frac{\partial \psi}{\partial i} i^2 = \frac{1}{2} L i^2 \tag{6}$$

where θ_u and θ_a are the angles at unaligned and aligned position of rotor. Let E_c be the kinetic energy stored in capacitor C_d due to the voltage difference V_{cmax} to V_{cmin}

$$\int E_c = \frac{1}{2} C V_{cmax}^2 - \frac{1}{2} C V_{cmin}^2 \tag{7}$$

$$\Delta V_c = V_{cmax} - V_{cmin}. \tag{8}$$

From (6) and (8), we get

$$C_{\min} = \frac{2E_m}{2V_{cmin}\Delta V_c + \Delta V_c^2}. \tag{9}$$

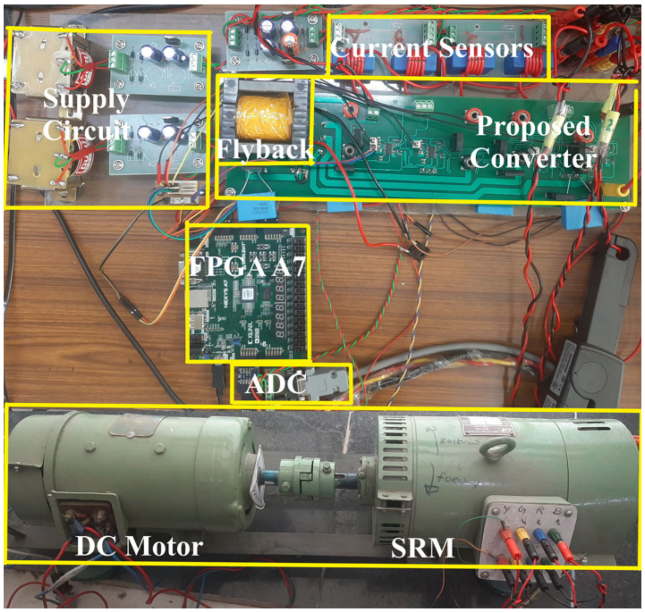

Fig. 8. Experimental setup of the SRM drive using proposed converter.

For the worst case scenario, inductance is considered as maximum ($L_{\max}$). Generally, in practical situation voltage ripple is considered about 5% of the dc link voltage so capacitance can be calculated as

$$C_{\min} = \frac{L_{\max} i^2}{0.1 V_{cmin}^2}. \tag{10}$$

From (10), it can be observed that, the capacitance value can be reduced by increasing the voltage ripple. As the value of voltage ripple will decrease, capacitance value will increase. In the proposed converter, the capacitor is not connected to the dc bus directly, it is used to discharge the winding energy and then through flyback inductor it transfer its complete energy to the source. In the proposed converter capacitor, value depends on the current rating of the machine and maximum value of voltage that the capacitor can handle.

V. Design of Flyback Inductor

The design of the inductor should follow some standard norms, which requires the following steps.

1) Calculate the size of wire to be used for the electric circuit to carry the rated current safely.
2) Calculate the size and shape of the magnetic core to be used such that core should not saturate.
3) Calculate the size of the core to accommodate the conductor safely.
4) Calculate the desired inductance based on the switching frequency and number of turns.

The voltages for both the winding is given by

$$V_1 = 4 f B_m A_c T_1 \tag{11}$$

$$V_2 = 4 f B_m A_c T_2 \tag{12}$$

where, V_1, V_2, T_1, and T_2 are the primary voltage, secondary voltage, number of primary, and secondary turns, respectively.

TABLE I
SRM Parameters

Power	0.6 hp
Number of stator/rotor poles	8/6
Stator outer diameter	163 mm
Rotor inner diameter	80.5 mm
Number of turns per pole, Air gap length	130 , 0.5 mm
Stator and Rotor pole arc	22° & 23°
Maximum and Minimum phase inductances	21 mH & 72 mH

TABLE II
Proposed Converter Parameters

DC bus voltage & current	200V & 10A
C_d, C_{in}	100 μF
Sampling frequency	30 kHz
Switching Frequency	15 kHz max
Mosfet Switch	IRFP260M
Flyback inductance (L_1 & L_2)	2mH & 500 μH
Flyback inductor switching Frequency	50 kHz

B_m, A_c, and f are the flux density, core area, and switching frequency of the flyback inductor.

Both the windings are accommodated in window of the flyback

$$k_w A_w = \frac{T_1 I_1}{J_1} + \frac{T_2 I_2}{J_2} \tag{13}$$

where A_w is the window area of the core and K_w is the winding factor.

From the above (11)–(13), following equations are derived:

$$V_1 I_1 + V_2 I_2 = 4 k_w f J B_m A_c A_w \tag{14}$$

$$VA = 2 f B_m A_c A_w J K_W \tag{15}$$

$$A_c A_w = \frac{VA}{2 f B_m J K_w}. \tag{16}$$

In (16), A_c and Aw represent the area product of the core to handle the VA rating of flyback.

Wire size for secondary and primary are calculated as follows:

$$a_{w1} = \frac{I_1}{J}, a_{w2} = \frac{I_2}{J} \tag{17}$$

where a_w is the cross sectional area of wire and J is the current density.

VI. Simulation Study

The simulation study is conducted on four phase 8/6 SRM drive. The parameters of the SRM and proposed converter are given in Tables I and II, respectively. The proposed converter is tested under different operating conditions in MATLAB/Simulink software. To test the efficacy of proposed converter, it is tested under dynamic conditions and results are analyzed and shown in Figs. 6 and 7.

A. Analysis of the Proposed Converter

The simulation results of the proposed converter are shown in Fig. 6. The gate pulses of switch G_5 along with capacitor voltage (V_{cd}) is shown in the Fig. 6(a). The capacitor voltage is given a

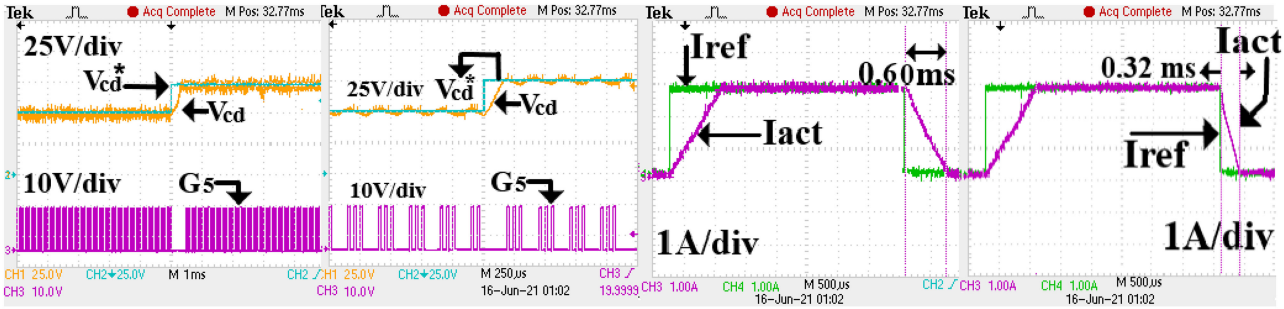

Fig. 9. Experimental results of SRM drive. (a) V_{cd} and gate pulse of G_5 switch. (b) Magnified view of V_{cd} and gate pulse of G_5 switch. (c) Reference and actual phase currents at the discharging voltage (V_{cd}) of 48 V. (d) Reference and actual phase currents at the discharging voltage (V_{cd}) of 72 V.

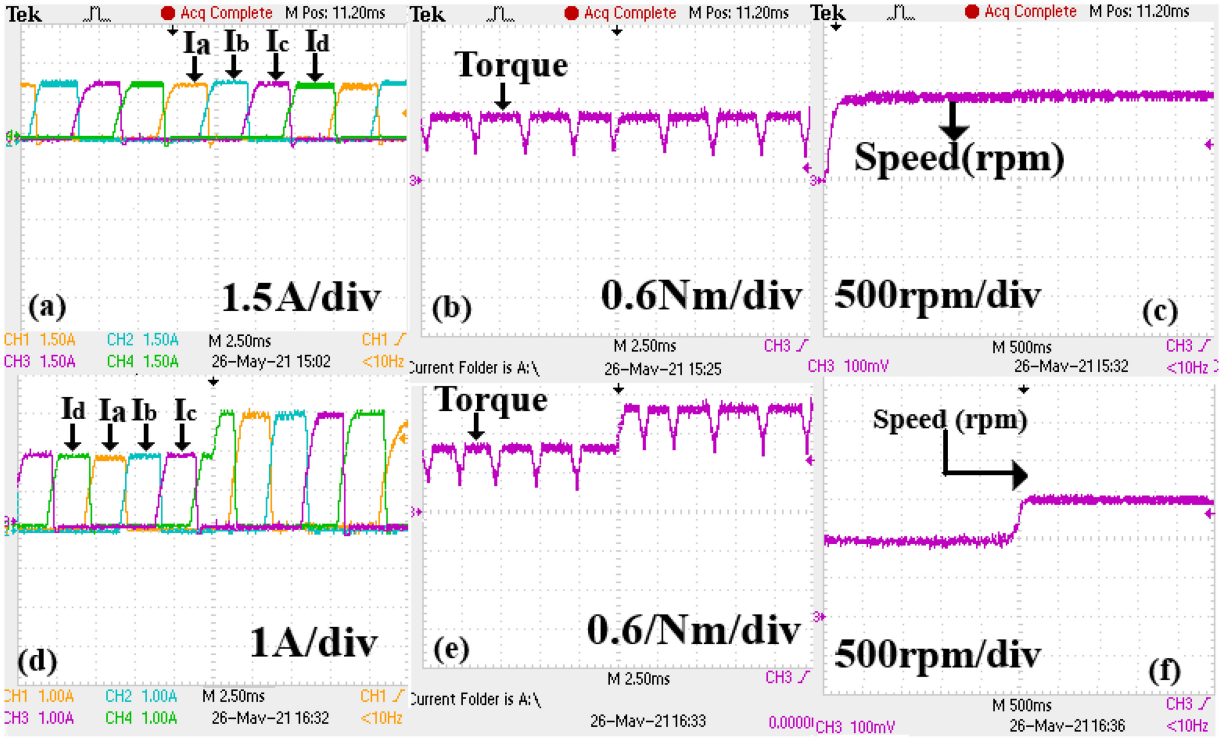

Fig. 10. Experimental results of current control of SRM drive. (a) Four phase currents. (b) Total torque. (c) Speed at 2 A reference current. (d) Current dynamics of SRM drive when reference is changes from 2 to 3 A. (e) Change in total torque due to current dynamics (f) Speed dynamics of SRM.

reference (V_{cd}^*) of 48 V till 0.1 s and then it is changed to 72 V. The magnified view of the V_{cd} voltage along with gate pulse of switch G_5 is illustrated in Fig. 6(b). V_{cd} voltage with respect to the flyback transformer currents (I_{T1} and I_{T2}) is shown in Fig. 6(c). The magnified view of I_{T1} and I_{T2} and the same waveforms with respect to gate pulse G_5 are provided in Fig. 6(d) and (e), respectively.

B. Simulation Results of SRM Drive Using the Proposed Converter

The simulations results of closed loop current control for 4 phase 8/6 SRM drives are shown in Fig. 7. The four phase currents of SRM are shown in Fig. 7(a). The total torque and speed at 2 A is shown in the Fig. 7(b) and (c). The dynamic result of four-phase currents is shown in Fig 7(d). The current reference is changed from 2 to 3 A at 1.498 s and the current dynamics are presented in Fig. 7(d). The torque and speed dynamics are presented in Fig. 7(e) and (f).

VII. Experimental Setup

The experimental setup of the proposed converter is shown in Fig. 8. The experimental verification is done on 0.6 hp four-phase 8/6 SRM. The control algorithm is implemented using Nexys A7 FPGA digital controller. A 1024 ppr encoder is integrated to the shaft for rotor position. The feedback is taken using LA-55p current sensors and fed to FPGA controller using ADC. A 4 channel DAC is interfaced to obtain the results in digital oscilloscope.

TABLE III
COMPARATIVE ANALYSIS OF CONVERTERS FOR 8/6 SRM DRIVE

Converters	Asymmetrical [20]	C-dump [21]	Variable voltage [23]	Four level [27]	Proposed
Number of Switches	8	5	6	9	5
Number of Diodes	8	5	5	9	5
Number of Capacitors	1	1	2	2	1
Magnetization voltage	Fixed (V)	Fixed (V)	Variable (up to $2V$) with extra switch	Fixed ($2V$)	Fixed (V)
Demagnetization voltage	Fixed ($-V$)	Fixed ($-V$)	Variable (up to $-2V$) with extra switch	Fixed ($-2V$)	(Any V_{cd} Voltage)
Phase Independence	Full	Full	No	No	Full
Freewheeling	No	No	Yes	Yes	No
VA Rating	$8VI_{dc}$	$10VI_{dc}$	$4.25VI_{dc} + 5U_{aux}I_{dc}$	$13VI_{dc}$	$(4 + \frac{T_2}{T_1})VI_{dc} + 5V_{cd}I_{dc}$
VA Rating(for -2V demagnetizing)	–	$14VI_{dc}$	$14.25VI_{dc}$	$13VI_{dc}$	$14.25VI_{dc}$
MOSFET Switching losses (p.u.)	8	10	9.25	13	9.25
Diode conduction losses (p.u.)	8	5	6	9	6

A. Hardware Results

For experimental results, the parameters of the SRM and the converter are taken to be same used as in simulation which are given in Tables I and II, respectively. Fig. 9 presents the voltage control of capacitor voltage and phenomena of variable discharging. The capacitor voltage along with control pulses of switch G_5 is shown in Fig. 9(a). The magnified view of V_{cd} is shown in Fig. 9(b). It is observed that V_{cd} is maintained for a reference voltage satisfactorily. Fig. 9(c) shows the phase current at $V_{cd} = 48\ V$. It takes 0.60 ms to discharge the winding from the 3 A reference. In similar fashion when the discharging voltage is increased to 75 V the discharging time is reduced to 0.32 ms as shown in the Fig. 9(d). In Fig. 10, experimental results of proposed converter with SRM drive are shown. The four phase currents are shown in Fig. 10(a). The SRM is operated at 2 A current. The total torque and the speed characteristics of the SRM corresponding to 2 A current are shown in Fig. 10(b) and (c). The current dynamics of the SRM drive is shown in Fig. 10(d). The current reference is changed from 2 A to rated current 3 A and corresponding change in total torque is observed in Fig. 10(e). The speed dynamics is given in Fig. 10(f). It can be observed that the experimental results are in good match with the simulation results.

VIII. COMPARATIVE ANALYSIS

Table III presents the comparative analysis of the proposed converter with other existing converter topologies. The dc input has been kept constant at V for all the converters. Converters in [23] and [27] are proposed for a three-phase SRM. These are extended for four-phase SRM and presented in Table III for fair comparison. The following can be inferred from Table III.

1) There is no phase independence in [23] and [27] since magnetizing and demagnetizing cannot happen simultaneously. One phase can magnetize only after other phase has completely demagnetized.
2) Among all the converters, converter in [21] and the proposed converter require minimum number of switches. However, for a demagnetizing voltage of $-V$, capacitor voltage rating in [21] is $2\,V$, whereas it is V in the proposed converter.

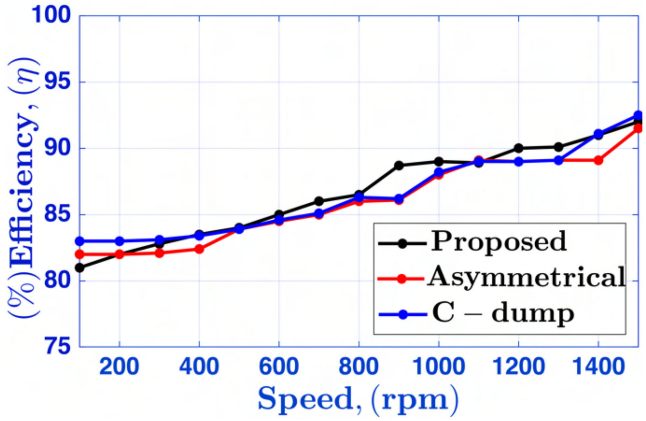

Fig. 11. Efficiency comparison of proposed converter with C-dump and asymmetrical converters.

3) The VA rating of all the converters is calculated as per the method given in [38] and compared in Table III. The VA rating of the proposed converter is comparable with the existing converter topologies. The VA rating is calculated using dc-bus voltage V and current I_{dc}. The normalized diode conduction and MOSFET switching losses are also calculated and given in Table III.
4) The proposed converter offers flexible demagnetizing voltage of any magnitude. The maximum demagnetizing voltage, $V_{cd_{\max}}$, depends on how fast the winding needs to be demagnetized and this decides the voltage rating of the capacitor.
5) The normalized losses of the proposed converter along with other topologies are shown in Table III. It is observed show that the proposed converter offers good efficiency as shown in Fig. 11.

IX. CONCLUSION

This article has proposed a novel converter topology with fewer switches and variable demagnetizing voltage capability. The unique feature of the proposed converter topology is that it can be easily extended to any higher number of phases by adding just one switch per phase. This converter also offers a feature of modulating the demagnetizing voltage V_{cd} to any

desired value. Also, it feeds back the demagnetizing energy to the source through a flyback transformer. Further, the capacitor requirement in the proposed converter is confined to the demagnetizing voltage required. Also, the capacitor can be allowed to have more ripple since it is not charging the dc bus directly. Using the switch G_5 used in the flyback circuit, the voltage V_{cd} is modulated, and the energy is sent back to the source whenever the reference value of V_{cd} is exceeded. This converter offers independent operation for all phases, and hence any number of phases can be magnetized/demagnetized simultaneously as per control requirement. The proposed converter has been implemented with a four phase 8/6 SRM using MATLAB/Simulink software. The results are also experimentally validated on an FPGA-based hardware setup developed in the laboratory. From the results, it can be observed that the converter is able to work as expected and control all the phases independently while maintaining the desired demagnetizing voltages (48 and 75 V) that are set. The discharging time for these two demagnetizing voltages are found to be 0.6 and 0.32 ms, respectively. The proposed converter is also compared with other existing topologies. The proposed converter shows the advantages in terms of requiring minimum number of switches, one capacitor, offers full flexibility in demagnetizing voltage, good efficiency, and provides complete phase independence making it suitable for any N phase SRM drive.

REFERENCES

[1] R. Krishnan, *Switched Reluctance Motor Drives-Modeling: Simulation, Analysis, Design, and Applications*. Boca Raton, FL, USA: CRC Press, 2001.

[2] Y. Wei, M. Qishuang, Z. Poming, and G. Yangyang, "Torque ripple reduction in switched reluctance motor using a novel torque sharing function," in *Proc. IEEE Int. Conf. Aircr. Utility Syst.*, 2016, pp. 177–182.

[3] I. Husain, "Minimization of torque ripple in SRM drives," *IEEE Trans. Ind. Appl.*, vol. 49, no. 1, pp. 28–39, Feb. 2002.

[4] A. K. Rana and A. V. R. Teja, "A mathematical torque ripple minimization technique based on a nonlinear modulating factor for switched reluctance motor drives," *IEEE Trans. Ind. Electron.*, vol. 69, no. 2, pp. 1356–1366, Feb. 2022.

[5] C. Gan, J. Wu, Q. Sun, W. Kong, H. Li, and Y. Hu, "A review on machine topologies and control techniques for low-noise switched reluctance motors in electric vehicle applications," *IEEE Access*, vol. 6, pp. 31430–31443, 2018.

[6] G. K. Sah, S. Jagwani, and L. Venkatesha, "A new simplified control strategy for switched reluctance motor," in *Proc. Recent Develop. Control, Automat. Power Eng.*, 2017, pp. 241–244.

[7] J. Ye, B. Bilgin, and A. Emadi, "An offline torque sharing function for torque ripple reduction in switched reluctance motor drives," *IEEE Trans. Energy Convers.*, vol. 30, no. 2, pp. 726–735, Jun. 2015.

[8] M. Dowlatshahi, S. M. S. Nejad, and J. Ahn, "Torque ripple minimization of switched reluctance motor using modified torque sharing function," in *Proc. 21st Iranian Conf. Elect. Eng.*, 2013, pp. 1–6.

[9] H. Li, B. Bilgin, and A. Emadi, "An improved torque sharing function for torque ripple reduction in switched reluctance machines," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1635–1644, Feb. 2019.

[10] N. C. Sahoo, J. X. Xu, and S. K. Panda, "Low torque ripple control of switched reluctance motors using iterative learning," *IEEE Trans. Energy Convers.*, vol. 16, no. 4, pp. 318–326, Dec. 2001.

[11] P. K. Reddy, D. Ronanki, and P. Parthiban, "Direct torque and flux control of switched reluctance motor with enhanced torque per ampere ratio and torque ripple reduction," *Electron. Lett.*, vol. 55, no. 8, pp. 477–478, 2019.

[12] A. Xu, W. Zhang, and P. Ren, "Comparison of torque ripple reduction for switched reluctance motor based on DTC and DITC," in *Proc. 13th IEEE Conf. Ind. Electron. Appl.*, 2018, pp. 1727–1732.

[13] D. Kim, H. Jeong, and K. Lee, "Torque ripple minimization of switched reluctance motors based on fuzzy logic and sliding mode control," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2013, pp. 1–6.

[14] S. Li, S. Zhang, C. Jiang, J. R. Mayor, T. G. Habetler, and R. G. Harley, "A fast control-integrated and multiphysics-based multi-objective design optimization of switched reluctance machines," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2017, pp. 730–737.

[15] S. Mehta, M. A. Kabir, and I. Husain, "Speed current profiling algorithm for low torque ripple SRM using model predictive control," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2018, pp. 4558–4563.

[16] S. D. F. Valencia, R. Tarvirdilu-Asl, C. Garcia, J. Rodriguez, and A. Emadi, "Vision, challenges, and future trends of model predictive control in switched reluctance motor drives," *IEEE Access*, vol. 9, pp. 69926–69937, 2021.

[17] M. Divandari, R. Brazamini, A. Dadpour, and M. Jazaeri, "A novel dynamic observer and torque ripple minimization via fuzzy logic for SRM drives," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2009, pp. 847–852.

[18] M. Divandari, A. Koochaki, A. Maghsoodloo, H. Rastegar, and J. Noparast, "High performance SRM drive with hybrid observer and fuzzy logic torque ripple minimization," in *Proc. IEEE Int. Symp. Ind. Electron.*, 2007, pp. 1230–1235.

[19] O. Ellabban and H. Abu-Rub, "Switched reluctance motor converter topologies: A review," in *Proc. IEEE Int. Conf. Ind. Technol.*, 2014, pp. 840–846.

[20] A. P. Khedkar and P. S. Swami, "Comparative study of asymmetric bridge and split AC supply converter for switched reluctance motor," in *Proc. Int. Conf. Comput. Power, Energy Inf. Commun.*, 2017, pp. 522–526.

[21] S. Mir, I. Husain, and M. E. Elbuluk, "Energy-efficient c-dump converters for switched reluctance motors," *IEEE Trans. Power Electron.*, vol. 12, no. 5, pp. 912–921, Sep. 1997.

[22] K. Tomczewski and K. Wrobel, "Improved C-dump converter for switched reluctance motor drives," *IET Power Electron.*, vol. 7, no. 10, pp. 2628–2635, 2014.

[23] C. Zhang, K. Wang, S. Zhang, X. Zhu, and L. Quan, "Analysis of variable voltage gain power converter for switched reluctance motor," *IEEE Trans. Appl. Supercond.*, vol. 26, no. 7, Oct. 2016, Art. no. 0610905.

[24] Y. Kim, Y. Yoon, B. Lee, J. Hur, and C. Won, "A new cost effective SRM drive using commercial 6-switch IGBT modules," in *Proc. IEEE Power Electron. Specialists Conf.*, 2006, pp. 1–7.

[25] X. D. Xue, K. W. E. Cheng, and Y. J. Bao, "Control and integrated half bridge to winding circuit development for switched reluctance motors," *IEEE Trans. Ind. Informat.*, vol. 10, no. 1, pp. 109–116, Feb. 2014.

[26] W. Cai and F. Yi, "An integrated multiport power converter with small capacitance requirement for switched reluctance motor drive," *IEEE Trans. Power Electron.*, vol. 31, no. 4, pp. 3016–3026, Apr. 2016.

[27] D. Lee and J. Ahn, "A novel four-level converter and instantaneous switching angle detector for high speed SRM drive," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 2034–2041, Sep. 2007.

[28] B. Ji, V. Pickert, W. Cao, and B. Zahawi, "In situ diagnostics and prognostics of wire bonding faults in IGBT modules for electric vehicle drives," *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5568–5577, Dec. 2013.

[29] Q. Sun, J. Wu, C. Gan, and J. Guo, "Modular full-bridge converter for three-phase switched reluctance motors with integrated fault-tolerance capability," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2622–2634, Mar. 2019.

[30] N. S. Gameiro and A. J. Marques Cardoso, "Fault tolerant power converter for switched reluctance drives," in *Proc. 18th Int. Conf. Elect. Mach.*, 2008, pp. 1–6.

[31] Q. Chen, D. Xu, L. Xu, J. Wang, Z. Lin, and X. Zhu, "Fault-tolerant operation of a novel dual-channel switched reluctance motor using two 3-phase standard inverters," *IEEE Trans. Appl. Supercond.*, vol. 28, no. 3, Apr. 2018, Art. no. 5204205.

[32] W. Ding, Y. Hu, and L. Wu, "Investigation and experimental test of fault-tolerant operation of a mutually coupled dual three-phase SRM drive under faulty conditions," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 6857–6872, Dec. 2015.

[33] A. Cordeiro, V. F. Pires, A. J. Pires, J. F. Martins, and H. Chen, "Fault-tolerant voltage-source-inverters for switched reluctance motor drives," in *Proc. IEEE 13th Int. Conf. Compat., Power Electron. Power Eng.*, Sonderborg, Denmark, 2019, pp. 1–6.

[34] Y. Hu, C. Gan, W. Cao, J. Zhang, W. Li, and S. J. Finney, "Flexible fault-tolerant topology for switched reluctance motor drives," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4654–4668, Jun. 2016.

[35] M. Abd Elmutalab, A. Elrayyah, T. Husain, and Y. Sozer, "Extending the speed range of a switched reluctance motor using a fast demagnetizing technique," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3294–3304, Jul./Aug. 2018.
[36] J. D. Navamani, A. Lavanya, and K. Vijayakumar, "Modified SEPIC converter with high boosting capability," *Electron. Lett.*, vol. 55, no. 13, pp. 759–761, Jun. 2019.
[37] K. Ha, C. Lee, J. Kim, R. Krishnan, and S. Oh, "Design and development of low-cost and high-efficiency variable-speed drive system with switched reluctance motor," *IEEE Trans. Ind. Appl.*, vol. 43, no. 3, pp. 703–713, May/Jun. 2007.
[38] Ye and A. Emadi, "Power electronic converters for 12/8 switched reluctance motor drives: A comparative analysis," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, 2014, pp. 1–6.

Ashwani Kumar Rana (Student Member, IEEE) received the B.E. degree in electrical engineering from the University of Mumbai, Mumbai, India, in 2012, and the M.Tech. degree in power electronics and power system (PEPS) from Nagpur University, Nagpur, India, in 2015. He is currently working toward the Ph.D. degree in electrical engineering with the Indian Institute of technology Ropar, Rupnagar, India.

His research interests include drives and control for electric vehicles, control of switched reluctance motor drives, inverter design, sensor less control, and robust control.

A. V. Ravi Teja (Member, IEEE) received the B.E. degree in electrical and electronics engineering from Osmania University, Hyderabad, India, in 2008, and the M.Tech. degree in machine drives and power electronics from the Indian Institute of Technology Kharagpur (IIT Kharagpur), Kharagpur, India, in 2010, and the Ph.D. degree from the Department of Electrical Engineering, IIT Kharagpur, Kharagpur, India, in 2016.

He is currently working as an Assistant Professor with Electrical Engineering Department, IIT Ropar, Rupnagar, India. Prior to joining IIT Ropar, he worked with the Department of Electronics and Electrical Engineering, BITS Pilani, Hyderabad, India. His current research interests include electric vehicles and renewable energy integration.