Cu Clip-Bonding Method With Optimized Source Inductance for Current Balancing in Multichip SiC MOSFET Power Module

Laili Wang, *Senior Member, IEEE*, Tongyu Zhang, Fengtao Yang, *Student Member, IEEE*, Dingkun Ma, Cheng Zhao, *Student Member, IEEE*, Yunqing Pei, *Member, IEEE*, and Yongmei Gan, *Member, IEEE*

***Abstract*—Cu clip-bonding is a promising packaging method for lower resistance, lower inductance, and higher reliability than wire-bonding. Previous studies only simply replace bond wires with Cu clips on an individual die. However, current sharing and thermal coupling issues among multichip modules are still big challenges in the clip-bonded silicon carbide (SiC) MOSFET power module. In this article, a novel source inductance optimization method is proposed. Extra modification paths (MPs) on Cu clips are used in this method. A clip-bonded half-bridge multichip SiC power module is designed and fabricated to verify the superiority of the method. In a simple straight layout, the distance between adjacent dies is large enough to avoid heat concentration and junction temperature differences resulting from the thermal coupling effect. The MPs structure on the Cu clip is designed to optimize the power source inductances. Parasitic circuit model and mathematical analysis are derived to demonstrate the features of proposed MPs. Simulations and experiments workbench are conducted to analyze drain current sharing performance. Derivation and simulation show the highest branch's inductance is reduced. Test results show the current imbalance and loss imbalance are relatively mitigated, which proves that the effect of power inductances imbalance is suppressed by the proposed optimization method.**

***Index Terms*—Cu clip-bonding, current sharing, parasitic inductance, power module, silicon carbide (SiC) MOSFET.**

I. Introduction

POWER electronic applications have been used in a broad range, such as electric vehicles, naval vessels, aircraft, and well drilling. Power semiconductor devices for electric energy conversion are used in the form of power modules in high power occasions. In recent years, wide bandgap semiconductor power devices with superior performance in switching speed and loss have attracted much attention [1]. Silicon carbide (SiC) is one of the most potential candidates to replace silicon-based power devices in medium/high power level converters. However, the achievement of SiC-based converters in high power applications is still limited by the traditional packaging method, especially wire-bonding [2]–[5]. The structure of a conventional wire-bonded power module is shown in Fig. 1(a). Al wire-bonding is widely used for the upper surface connection since it is of low cost, high maturity, and high flexibility. However, Al wires introduce excessive parasitic inductance and therefore lead to voltage spike and switching loss increment, especially in SiC applications [2], [6], [7]. What is more, expanded operating temperature increases the thermal-mechanical stress, which is likely to cause bond wires' lift-off and fracture [8]–[11].

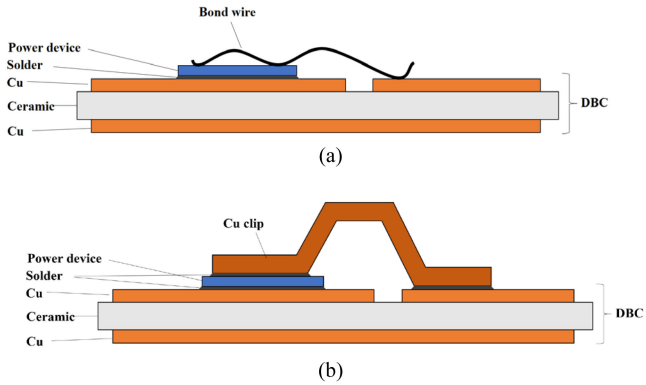

Fig. 1. Structure diagram of (a) wire-bonded power module and (b) Cu clip-bonded power module.

To tackle the problems, researchers have developed several methods for upper surface connection in recent years. Cu wire and Cu-Al wire possess better electrical and thermal performance than Al wire [12], [13]. However, the number of wires is limited by SiC die's smaller surface area in large current applications. Moreover, the higher required bond power is more likely to break the die [11], [14]. Al ribbon achieves bigger cross-sectional but discards the horizontal layout flexibility [15], [16]. In [17], planar SKiN technology enables a high integration, while the parasitic inductance and resistance do not alleviate too much. In [18] and [19], the metal posts interconnected parallel plate structure obtain a double-sided structure by using metal posts on the upper face connection. However, the metal posts cause high thermal–mechanical stress at solder. Cu clip-bonding,

Manuscript received August 17, 2021; revised November 18, 2021; accepted January 1, 2022. Date of publication January 7, 2022; date of current version March 24, 2022. This work was supported by the National Key Research and Development Program of China under Grant 2019YFE0122800. Recommended for publication by Associate Editor H. Li. *(Corresponding author: Laili Wang.)*

The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, Xi'an 710049, China (e-mail: llwang@mail.xjtu.edu.cn; zty598979175@stu.xjtu.edu.cn; yangfengtao@stu.xjtu.edu.cn; mdk1014@stu.xjtu.edu.cn; zhaocheng3117@stu.xjtu.edu.cn; peiyq@mail.xjtu.edu.cn; ymgan@mail.xjtu.edu.cn).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3141373.

Digital Object Identifier 10.1109/TPEL.2022.3141373

as shown in Fig. 1(b), is a remarkable method for SiC applications. Clip-bonding uses flat copper clips with a large cross section and soldering area for connection. Since copper has extremely high electrical conductivity, the Cu clip can obtain relatively low resistance. The high thermal conductivity of Cu provides an extra heat dissipation path, which can improve heat dissipation capability and power cycling reliability of power modules [14], [20]–[23].

Although Cu clip-bonding has a bright prospect on SiC power devices' interconnection, only a few modules with IGBTs or single SiC MOSFET are reported. Therefore, a Cu clip-bonded multichip SiC module is fabricated in this article. Due to the current rating of commercial SiC MOSFET is still limited to a lower level than Si IGBTs, paralleling dies is the most popular solution to enhance current handling capability [2], [24]. In parallel operation, the current imbalance is likely to make devices out of the safe operating area. Therefore current sharing plays an essential role in paralleled dies. Under high-frequency conditions, the dynamic loss is a big part of the total loss of dies, thus dynamic current sharing is necessary for multichip power modules. As the statement in [25], dynamic current sharing is closely related to power source inductances. Therefore, the source inductances of paralleled MOSFETs need to be adjusted to be identical. Some symmetric layouts are designed to get uniform inductances on paralleled branches in [26] and [27], whereas the design steps are hard to be expanded. To avoid complicated symmetric layout design, some researchers establish equivalent circuit models to describe dynamic current sharing behavior and mitigate current imbalance. In [28] and [29], lengths and directions of Al wires are optimized to adjust the inductances. However, the adjustment range (i.e., the length of wires) is also limited by DBC's space and bonding process. It is worth noting that the current paths of Cu clips are above the power dies and the arrangement of inductances on Cu clips does not occupy space on the DBC substrate. Moreover, the inductance on the clip is relatively easy to control by changing the shape. Owing to the above reasons, it is possible to modify parasitic inductances distribution by adding and shaping new paths on Cu clips.

In this article, a novel source inductances optimization method for current balancing by adding modification paths (MPs) in the Cu clip is proposed. To illustrate the optimization method, a Cu clip-bonded half-bridge SiC multichip power module is designed and fabricated. In the designed module, three SiC MOSFETs are paralleled with a straight DBC layout design. The distance of dies is determined under the consideration of thermal decoupling. The conventional wire-bonding for upper surface connection is replaced by Cu clip-bonding. MPs on Cu clips are proposed and designed to reduce and adjust power source branches' inductances. Kelvin-source connection is employed to eliminate the effect of common source inductance [30].

The rest of this article is organized as follows. Section II shows the designed clip-bonded module and proposed optimization method by shaping the MPs. Section III introduces the fabrication of the prototype. Section IV presents the experimental results of the module. Finally, Section V concludes this article.

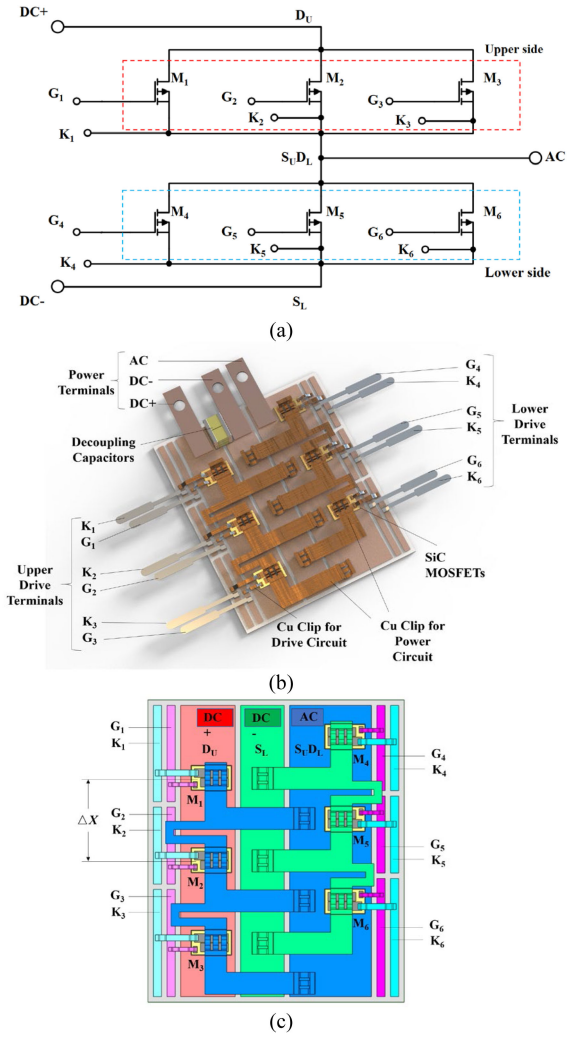

Fig. 2. (a) Schematic diagram of half-bridge module with three parallel MOSFETs. (b) Overview and components of designed clip bonded module. (c) Layout top view of module.

II. Module Design and Analysis

A. Clip-Bonded Module Overview

The overview of the designed SiC module is shown in Fig. 2. Fig. 2(a) is the schematic diagram of the proposed module. The half-bridge circuit is divided into the upper side and the lower side. Three paralleled SiC MOSFETs are paralleled at each side, that is, M_1–M_3 on the upper side and M_4–M_6 on the lower side. As reported in [31], the body diode of SiC MOSFET has already possessed quite close performance with SiC Schottky barrier diode. In addition, with the use of synchronous modulation, the body diode could be conducted only in relatively short dead time in periods. As a consequence, the performance of body diodes will not affect the module much. There is no external anti-parallel diode in the designed module to reduce the cost of the module and the complexity of the Cu clip's structure. The gate drive signals are given respectively by gate drive terminals G_1–G_6. To eliminate the effect of common source inductance, the Kelvin source connection is utilized by extra auxiliary source terminals K_1–K_6.

The overall appearance of the designed clip-bonded module is shown in Fig. 2(b). Location of MOSFETs at different sides are staggered arranged to ensure that Cu clips for power circuit do not contact. Power dies' upper surface electrical connection is realized by Cu clip bonding. The width of the main current path on power Cu clips is 4 mm. Decoupling capacitors are integrated between input power terminals dc+ and dc- to improve dynamic performance. The size of the DBC substrate is 55 mm × 47 mm × 1.6 mm. The materials of DBC layers are Cu/Al_2O_3/Cu with a thickness of 0.3 mm/1 mm/0.3 mm. The type of SiC MOSFETs is QPM3-1200-0013D from CREE with a small die size of 4.36 mm × 7.26 mm × 0.18 mm. The rated voltage, current, and ON-state resistance of MOSFETs are 1200 V, 149 A, and 13 mΩ, respectively. Metallization on the electrode surface is Ni/Pd/Au with a thickness of 2 μm/0.2 μm/0.05 μm. The special metallization on the electrodes of dies makes it suitable for soldering. Dies with soldering-suitable metallization on both sides are available from manufacturers.

Fig. 2(c) shows the module's layout design. Different colors represent different electric circuit nodes in the schematic. The power circuit layout of DBC is designed as simple straight parallel routings. The middle three wider paths, D_U, S_UD_L, and S_L, belong to the power circuit where the main current goes through. For purpose of easily integrating decoupling capacitors, D_U and S_L are arranged closely. The other paths belong to the gate drive circuits, which are gate signals G_i and corresponding Kelvin source signals K_i ($i = 1, 2, \ldots, 6$). The distance between two dies ΔX affects the thermal coupling, which leads to the heat concentration and uneven temperature distribution. Different junction temperatures change the electrical characteristics of dies and then lead to further current imbalance and loss imbalance. The shorter the distance ΔX, the more serious the thermal decoupling is. In [32] and [33], the relationship of distance ΔX and thermal coupling is discussed. To clarify the relationship between the thermal coupling effect and the distance ΔX, a thermal simulation with three dies (M_1, M_2, and M_3) is built in COMSOL Multiphysics. The losses of dies are set as 70 W. The heat transfer coefficient is set as 3000 W/(m^2·K). Fig. 4(a) shows the highest temperature on the middle die M_2 versus ΔX. The rate of temperature decline decreases with the increase of ΔX. Fig. 4(b) shows the drifting of the peak temperature point. The peak temperature points of M_1 and M_3 move from the edge to the center of the dies. This means the thermal coupling effect is gradually eliminated with the distance's increase. Consider to almost eliminate thermal coupling effect, the distance is reserved high enough as $\Delta X = 15$ mm. According to the simulation data in [32], the thermal coupling degree at $\Delta X = 15$ mm is lower than 2%. Unfortunately, long-distance brings extremely high and unbalanced parasitic inductances. Therefore, Cu clips are shaped to adjust power source inductances. Details will be discussed later.

Views of Cu clips are shown in Fig. 3. Fig. 3(a) shows the structure of power clips for power source connection. Every power clip is combined by several units. The number of clip units is the same as paralleled dies. The separate unit realizes the connection between power MOSFET source metallization and copper path on DBC substrate by two kinds of joints, that

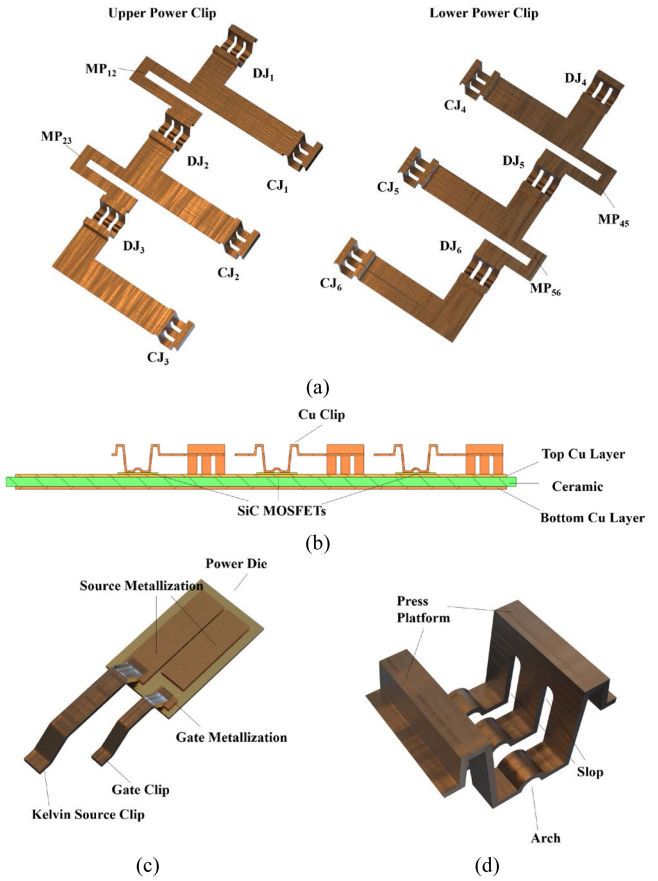

Fig. 3. (a) Structure of power clips. (b) Cross-sectional side view of upper power Cu clip. (c) Structure of gate clip and auxiliary source clip. (d) Structure of die joint.

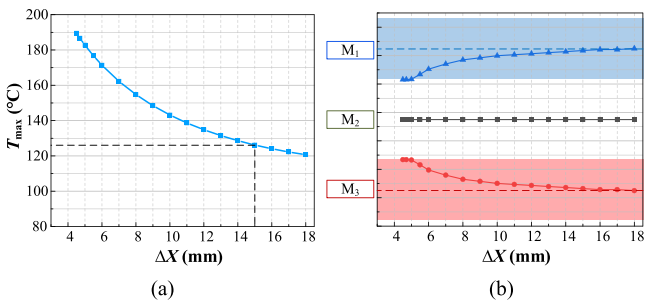

Fig. 4. Thermal coupling effect simulation results. (a) Peak temperature on the middle die M_2 versus distance ΔX. (b) Drifting of peak temperature points on dies.

is, die joint (DJ) and copper joint (CJ). To adjust the source inductances, separate units are connected by MPs. Since the power clips have similar and almost symmetrical structures, the cross-sectional side view in Fig. 3(b) only shows the upper power clip. The current path of the power clip is 2 mm higher than DBC. In Fig. 3(c), small gate clips and auxiliary source clips are designed for gate connection and Kelvin source connection. The widths of the gate clip and auxiliary clip are 0.7 and 1.1 mm. All of the clips have a thickness of 0.2 mm. The structure for the attached area is specially designed. As an illustration, a DJ

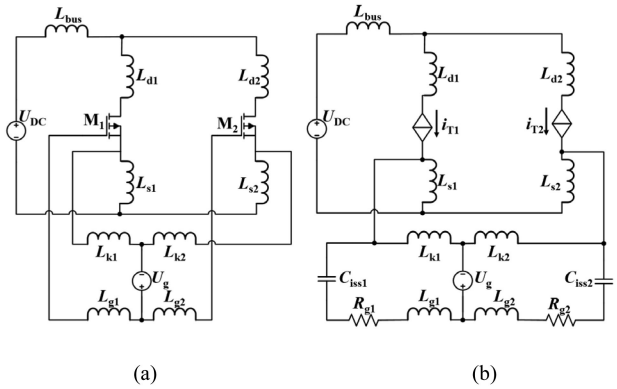

Fig. 5. (a) Parasitic circuit model of two parallel MOSFETs. (b) Equivalent dynamic circuit model of two parallel MOSFETs.

TABLE I
PARAMETERS IN CIRCUIT MODEL OF TWO PARALLEL MOSFETS

Symbols	Parameters description
$U_{\rm DC}$	DC bus voltage
$U_{\rm g}$	Gate drive voltage
$L_{\rm bus}$	DC bus parasitic inductance
$L_{\rm d1}$, $L_{\rm d2}$	Drain parasitic inductance
$L_{\rm s1}$, $L_{\rm s2}$	Power source parasitic inductance
$L_{\rm g1}$, $L_{\rm g2}$	Gate parasitic inductance
$L_{\rm k1}$, $L_{\rm k2}$	Kelvin source parasitic inductance
$R_{\rm g1}$, $R_{\rm g2}$	Gate resistance
$C_{\rm iss1}$, $C_{\rm iss2}$	Input capacitance
$i_{\rm T1}$, $i_{\rm T2}$	Current flowing through the controlled current source

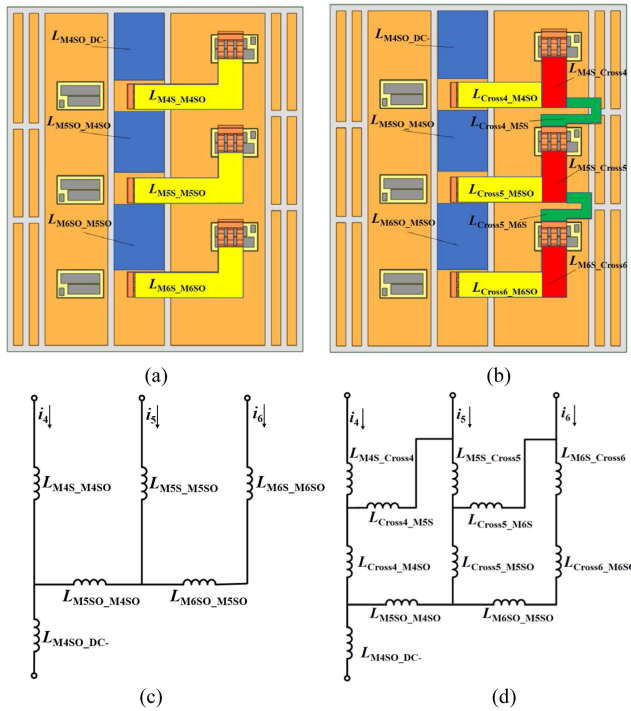

Fig. 6. (a) Parasitic source inductances distribution of lower side without MPs. (b) Parasitic source inductances distribution of lower side with MPs. (c) Distributed power source parasitic circuit model of lower side without MP inductances. (d) Distributed power source parasitic circuit model of lower side with MP inductances.

for connection between power clip and power die is shown in Fig. 3(d). An arch structure on the DJ is designed since the source metallization of the die is divided into two parts. Slops are hollowed out to reduce thermal–mechanical stress. Taking into account some connection technologies need pressure, press platforms on joints are designed to get better contact between clips and power dies or DBC.

B. Modification Paths Design

The switching performance of power devices is notably affected by parasitic inductances, so is the current sharing performance. The dynamic current sharing behavior could be described by the circuit model in Fig. 5. Considering the condition of two parallel MOSFETs, the parasitic circuit model is shown in Fig. 5(a). To describe the switching behavior, MOSFETs in the dynamic model are replaced by controlled current sources in Fig. 5(b). Parameters in the circuit model are listed in Table I. The current flowing through the controlled source at ON-state could be described as

$$i_{\rm T} = g(V_{\rm gs} - V_{\rm th})^2 \tag{1}$$

where i_T is the current go through the controlled current source, g is coefficient, V_{gs} is the voltage between gate and source, and $V_{\rm th}$ is the threshold voltage of MOSFETs.

Several factors can give rise to the current imbalance. The current difference between two MOSFETs could be described as

$$\Delta i_T = G_{Tg}\Delta L_g + G_{Tk}\Delta L_k + G_{Ts}\Delta L_s + G_{\rm TV}\Delta V_{\rm th} \tag{2}$$

where Δi_T is the current difference of two paralleled MOSFETs, ΔL_g, ΔL_k, ΔL_s are the difference of gate parasitic inductances, Kelvin source parasitic inductances, and source inductances respectively. G_{Tg}, G_{Tk}, $G_{\rm Ts}$, and G_{TV} are the coefficients affected by circuit parameters and MOSFETs' characteristics.

Equation (2) shows that all of ΔL_g, ΔL_k, ΔL_s, and $\Delta V_{\rm th}$ could lead to dynamic current imbalance. Corresponding coefficients G_{Tg}, G_{Tk}, G_{Ts}, and G_{TV} indicate the effect of inductance difference on current imbalance. According to the derivation in [25], the effect of $\Delta L_{\rm s}$ is dominant in dynamic current sharing. As above-mentioned, the designed module has extremely asymmetric power source parasitic inductances before optimization. Since it is easy to adjust inductances by changing the shape of Cu clips, the inductances distribution is changed by introducing extra MPs on power Cu clips. Power source copper paths of the lower half-bridge side without and with MPs are separated as Fig. 6(a) and (b), which are expressed in different colors. Two MPs are used to adjust the parasitic inductances in the forms of $L_{\rm Cross4\_M5S}$ and $L_{\rm Cross5\_M6S}$. The values of parasitic inductances are extracted by Ansys Q3D Extractor and given in Table II except for MPs. To describe the effect of MPs, parasitic models without and with added paths are shown in Fig. 6(c) and (d), respectively. It should be pointed out that some inductances in Fig. 6(d) are combined in Fig. 6(c)

$$\begin{cases} L_{\rm M4S\_M4SO} = L_{\rm M4S\_Cross4} + L_{\rm Cross4\_M4SO} \\ L_{\rm M5S\_M5SO} = L_{\rm M5S\_Cross5} + L_{\rm Cross5\_M5SO} \\ L_{\rm M6S\_M6SO} = L_{\rm M6S\_Cross6} + L_{\rm Cross6\_M6SO}. \end{cases} \tag{3}$$

TABLE II
INDUCTANCES VALUES OF DISTRIBUTED POWER SOURCE PARASITIC CIRCUIT MODEL FOR LOWER SIDE

Symbols	Inductance value (nH)
$L_{\mathrm{M4S\_Cross4}}$	1.31
$L_{\mathrm{M5S\_Cross5}}$	1.36
$L_{\mathrm{M6S\_Cross6}}$	1.38
$L_{\mathrm{Cross4\_M4SO}}$	3.87
$L_{\mathrm{Cross5\_M5SO}}$	3.89
$L_{\mathrm{Cross6\_M6SO}}$	3.98
$L_{\mathrm{M6SO\_M5SO}}$	1.31
$L_{\mathrm{M5SO\_M4SO}}$	1.17

The distributed parasitic inductance circuit model is built by separating the copper paths into segments as Fig. 6. However, the model could not show the paralleled power source inductances clearly. Thus, further approximation and transformations are necessary. According to (1), the current distribution on paralleled dies is affected by V_{gs}. Different voltage drops on power source inductances lead to a difference of V_{gs}. By using the superposition theorem, the source voltage drops in the circuit without MPs in Fig. 6(c) could be calculated as (4) (the detailed derivation and expression can be found in Appendix A)

$$v_{LS} = (L_S + L_{\mathrm{M4SO\_DC-}}) \cdot \frac{d}{dt} i \tag{4}$$

where $v_{\mathrm{LS}} = [\, v_{LS4}\ v_{LS5}\ v_{LS6}\,]^T$, $i = [\, i_4\ i_5\ i_6\,]^T$, and $L_S = \mathrm{diag}(L_{S4}, L_{S5}, L_{S6})$.

The equivalent source inductances are

$$\begin{cases} L_{\mathrm{S4}} = L_{\mathrm{M4S\_M4SO}} \\ L_{\mathrm{S5}} = L_{\mathrm{M5S\_M5SO}} + 2L_{\mathrm{M5SO\_M4SO}} \\ L_{\mathrm{S6}} = L_{\mathrm{M6S\_M6SO}} + L_{\mathrm{M6SO\_M5SO}} + 2L_{\mathrm{M5SO\_M4SO}}. \end{cases} \tag{5}$$

From equations (4) and (5), the imbalance of equivalent source inductances is caused by the parasitic inductances between branches, that is, $L_{\mathrm{M6SO\_M5SO}}$ and $L_{\mathrm{M5SO\_M4SO}}$. In the same way, the superposition theorem is used for the circuit with MPs in Fig. 6(d) to illustrate the effect of new paths $L_{\mathrm{Cross4\_M5S}}$ and $L_{\mathrm{Cross5\_M6S}}$. The result is shown in (6) and (7). Detailed derivation and expression are listed in Appendix B

$$v_{LS}{}' = (L_S{}' + L_{\mathrm{M4SO\_DC-}}) \cdot \frac{d}{dt} i \tag{6}$$

where $v_{LS}{}' = [\, v_{LS4}{}'\ v_{LS5}{}'\ v_{LS6}{}'\,]^T$, $i = [\, i_4\ i_5\ i_6\,]^T$, and $L_{\mathrm{S}}{}' = \mathrm{diag}(L_{\mathrm{S4}}{}', L_{\mathrm{S5}}{}', L_{\mathrm{S6}}{}')$.

The equivalent source inductances are

$$\begin{cases} L_{S4}{}' = L_{41} + L_{42} + L_{43} \\ L_{S5}{}' = L_{51} + L_{52} + L_{53} \\ L_{S6}{}' = L_{61} + L_{62} + L_{63}. \end{cases} \tag{7}$$

To illustrate the effect of MPs, the surface diagrams of $L_{S4}{}'$, $L_{S5}{}'$, $L_{S6}{}'$ and inductance imbalance ΔL versus $L_{\mathrm{Cross4\_M5S}}$ and $L_{\mathrm{Cross5\_M6S}}$ are shown in Fig. 7. The inductance imbalance ΔL is the difference value between maximum inductance and minimum inductance ($\max\{L_{S4}{}', L_{S5}{}', L_{S6}{}'\}$–$\min\{L_{S4}{}', L_{S5}{}', L_{S6}{}'\}$). In Fig. 7(a)–(c), it is shown that the equivalent power source inductances $L_{S4}{}', L_{S5}{}', L_{S6}{}'$ are calculated as 7.2, 6.0, and 5.4 nH when MPs inductances are only 0.1 nH. As $L_{\mathrm{Cross4\_M5S}}$ and $L_{\mathrm{Cross5\_M6S}}$ increase, $L_{S4}{}'$ decreases and $L_{S6}{}'$ increases, while the change of $L_{S5}{}'$ is irregular and the range is not large. It means, there is a balance point for this design. At this point, the paralleled branches have almost uniform equivalent power source inductances. Before reaching the balance point, as the MPs' inductances increase the source inductances become more even. To find the balance point, inductance imbalance ΔL versus $L_{\mathrm{Cross4\_M5S}}$ and $L_{\mathrm{Cross5\_M6S}}$ is plotted in Fig. 7(d). There is a balance point getting the minimum inductance imbalance near 0 nH. Inductances of MPs are selected around the balance point as $L_{\mathrm{Cross4\_M5S}} = 3.7$ nH and $L_{\mathrm{Cross5\_M6S}} = 2.9$ nH. Equivalent power source inductances of paralleled branches are listed in Table III. According to the results in Table III, the maximum source branch inductance is reduced by 27.4%. Moreover, the inductances of paralleled branches are adjusted to uniform, which could improve dynamic current sharing performance.

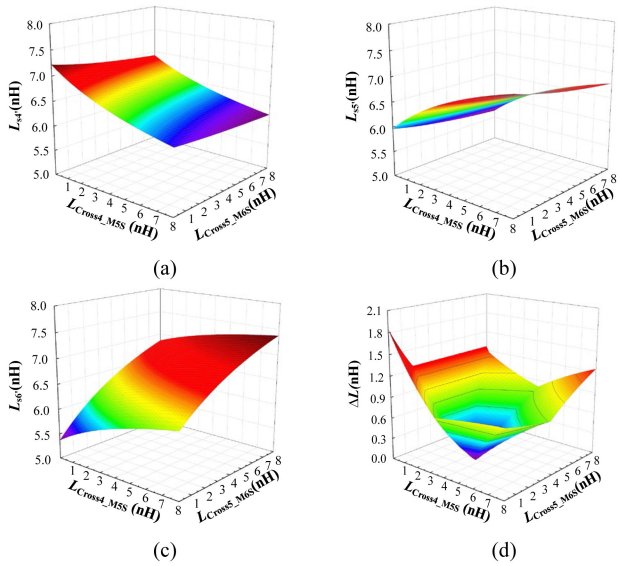

Fig. 7. (a) Surface diagram of $L_{S4}{}'$ versus $L_{\mathrm{Cross4\_M5S}}$ and $L_{\mathrm{Cross5\_M6S}}$. (b) Surface diagram of $L_{S5}{}'$ versus $L_{\mathrm{Cross4\_M5S}}$ and $L_{\mathrm{Cross5\_M6S}}$. (c) Surface diagram of $L_{S6}{}'$ versus $L_{\mathrm{Cross4\_M5S}}$ and $L_{\mathrm{Cross5\_M6S}}$. (d) Surface diagram of ΔL versus $L_{\mathrm{Cross4\_M5S}}$ and $L_{\mathrm{Cross5\_M6S}}$.

TABLE III
EQUIVALENT POWER SOURCE INDUCTANCES VALUE OF SIMPLIFIED MODEL FOR LOWER SIDE

Condition	Symbols	Inductance value (nH)
Without modification paths	L_{S4}	5.18
	L_{S5}	7.59
	L_{S6}	9.01
With modification paths	$L_{\mathrm{S4}}{}'$	6.54
	$L_{\mathrm{S5}}{}'$	6.53
	$L_{\mathrm{S6}}{}'$	6.54

C. Circuit Simulation

To certify the advantage of modification paths, the distributed parasitic circuit models with and without modification paths are

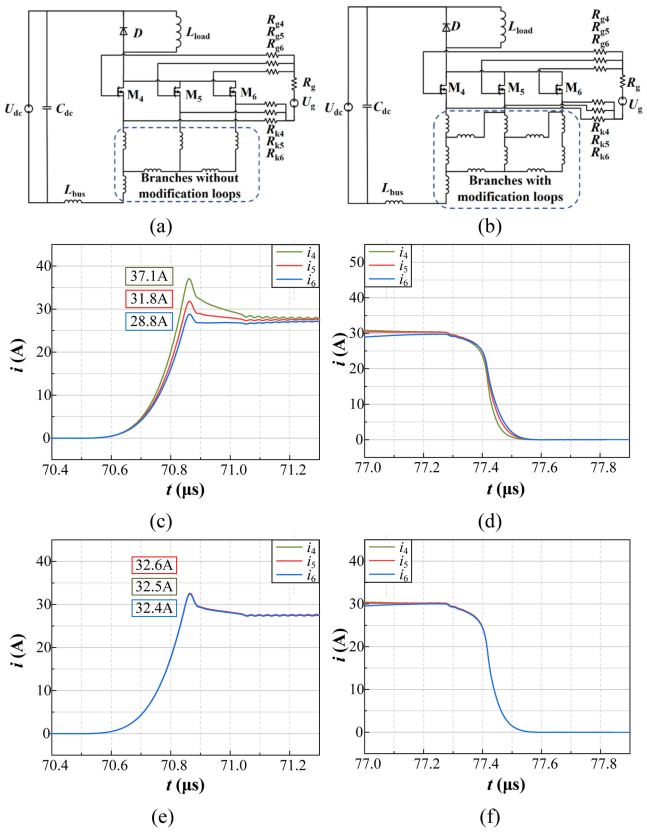

Fig. 8. (a) Simulation model of DPT without modification paths. (b) Simulation model of DPT with modification paths. (c) Current waveform without modification paths at turn-ON. (d) Current waveform without modification paths at turn-OFF. (e) Current waveform with modification paths at turn-ON. (f) Current waveform with modification paths at turn-OFF.

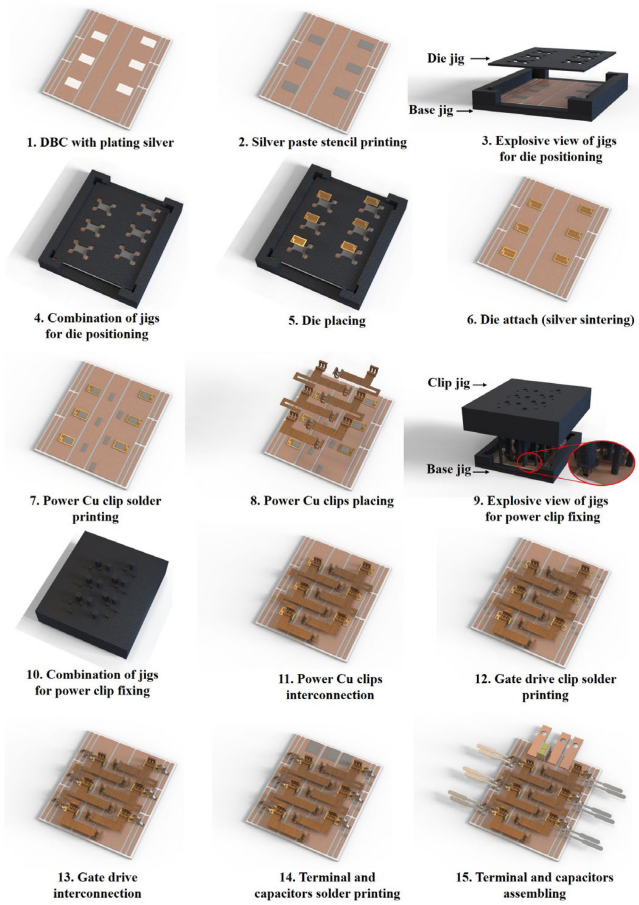

Fig. 9. Fabrication procedure of designed Cu clip-bonded SiC module prototype.

simulated in LTspice. The device model used in the simulation is CPM3-1200-0013A from the manufacturer, which has the same parameters as the used die. The current imbalance degree δ is used to describe the imbalanced parallel currents. The current imbalance degree δ is expressed as

$$\delta = \frac{\Delta i}{\bar{i}} \times 100\% \tag{8}$$

where Δi is the difference between the maximum and minimum branch currents, and $\bar{i}$ is the average value of currents through paralleled dies.

Two double pulse test (DPT) circuits without and with modification paths are built and simulated as Fig. 8(a) and (b). In the simulation setting, the dc bus voltage $V_{\rm dc}$ is 400 V. Decoupling capacitance $C_{\rm bus}$ is 600 nF. The external gate resistor is set as 10 Ω. Load inductance is set as 300 μH. The first pulse is 60 μs. The current on the load inductor at the second pulse is over 80 A. The simulation current waveforms are shown in Fig. 8(c)–(f). Fig. 8(c) and (d) are waveforms at turn-ON and turn-OFF without modification paths. Fig. 8(e) and (f) are waveforms with modification paths. In Fig. 8(c), because of the large source inductance difference, the maximum peak current difference Δi is 8.3 A with a high imbalance degree of 25.5%. After adding modification paths, the peak current of turn-ON in Fig. 8(e) only has a difference of 0.2 A (δ<1%). Similarly, the current difference at turn-OFF also decreases. Although some factors are neglected in simulation, it is still certified that specially modified paths exceedingly improve the current sharing performance of paralleled SiC power dies.

TABLE IV
MATERIAL LIST IN FABRICATION PROCESS

Component/Step	Material
DBC Substrate	Cu/ Al_2O_3/ Cu
Power die	SiC MOSFET(QPM3-1200-0013D)
Clips and power terminals	Copper
Gate drive terminals	Copper (silver plated)
Die attach	Nanosilver paste
Power interconnection	$Sn_{96.5}Ag_3Cu_{0.5}$
Drive, terminals and decoupling capacitors assembling	$Sn_{42}Bi_{57.6}Ag_{0.4}$
Jigs	Graphite

III. MODULE FABRICATION

A prototype of the designed Cu clip-bonded SiC multichip power module is fabricated. The fabrication procedure is shown in Fig. 9 and materials are given in Table IV. Fabrication of the designed module could be divided into four main connections,

which are die-attach, power interconnection, gate drive interconnection, and assembling of terminals and decoupling capacitors. To prevent the later process from affecting the former process, the former process's melting point is higher. Specifically, silver sintering is used for die-attach. Solder $Sn_{96.5}Ag_3Cu_{0.5}$ is used for power interconnection. Solder $Sn_{42}Bi_{57.6}Ag_{0.4}$ is used for gate drive interconnection and later assembling of terminal and capacitors. On account of the requirements for positioning accuracy, extra jigs for positioning and fixing are required. A set of customized graphite jigs are used due to graphite's heat transfer capacity, high temperature bearing capacity, solder incompatibility, and easy processing. The set of jigs includes three parts, which are the base jig, the die jig, and the clip jig. The base jig and the die jig are used in combination at die-attach. The combination of the base jig and the clip jig is used in power interconnection.

Locations of six power dies are indicated by thin plated silver on DBC. The silver coating also makes it more suitable for nanosilver sintering. At the beginning of the die-attach, nanosilver paste is printed through a customized stencil with a thickness of 80 μm. Then, the base jig and the die jig are used in combination for die positioning and placement. Six power dies with a size of 4.36 mm $\times$ 7.26 mm $\times$ 0.018 mm are placed on DBC through the holes of the die jig. Afterward, die-attach is achieved by pressure-less nanosilver sintering at over 200 °C for 30 min. After die-attach, solder $Sn_{96.5}Ag_3Cu_{0.5}$ is printed on the solder area at the upper surface of power devices and DBC. The combination of the base jig and the clip jig is used for fixing power Cu clips. There are screw holes ($\Phi = 4$ mm) and vias ($\Phi = 2$ mm) on the clip jig. Graphite screw bolts are used to fix power Cu clips by gently pressing the press platforms. Graphite bars go through the vias to prevent the Cu clips from drifting. Gate drive interconnection is achieved without graphite jig. After printing solder $Sn_{42}Bi_{57.6}Ag_{0.4}$, the gate drive clips are placed and soldered. Finally, the terminals and decoupling capacitors are assembled. The decoupling capacitance value is 600 nF, combined by six 100 nF ceramic capacitors. No baseplate is connected below the module so that no extra thermal resistance is introduced. The heat dissipation is accomplished by the lower surface of DBC. Also, no encapsulation is used for the convenience experimental measurement.

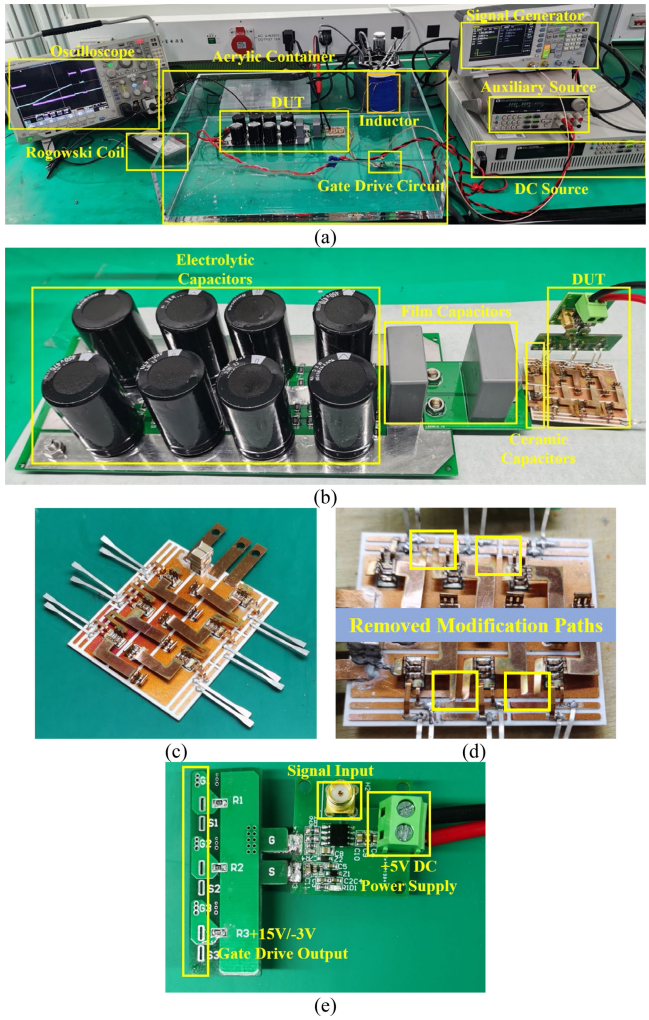

Fig. 10. Experimental setup of DPT platform. (a) Overall test platform. (b) Capacitor pack. (c) Prototype with modification paths. (d) Prototype without modification paths. (e) Gate drive circuit.

IV. Experimental Verification

A. Experimental Setup

The experimental DPT platform is fabricated as Fig. 10. The schematic diagram is the same as Fig. 8(a) and (b). The lower side MOSFETs are tested as devices under test (DUTs). The upper side dies are used as diodes. For comparison, the modification paths on the prototype are subsequently removed and measured. The Rogowski coil (120 A, 30 MHz) is employed to detect the currents going through the power MOSFETs. According to the discussion in [34], the measurement error of the Rogowski coil is low enough. The fabricated module is tested under 400 V for safety consideration. Since the output capacitance almost does not change after 400 V, the test under 400 V is enough to show the performance of the die under higher voltage conditions. The voltage of DUTs is measured by the high voltage differential probe (600 V/ 6000 V, 200 MHz). Waveforms are observed by oscilloscope Tektronix MDO4104C (1 GHz, 5 Gs/s). To get certain insulation, DUTs are immersed in 45# transformer oil in an acrylic container with a size of 650 mm $\times$ 450 mm $\times$ 200 mm. DC bus voltage $V_{\rm dc}$ and gate drive voltage $V_{\rm g}$ are provided by high voltage dc source and auxiliary source respectively. The double pulse signal is generated by a signal generator. The first pulse time and the second pulse time are 60 and 5 μs, respectively. The bus capacitance $C_{\rm bus}$ achieves 940 μF, which includes two in series and four in parallel electrolytic capacitors (470 μF/450 V). The decoupling capacitance $C_{\rm dc}$ is divided into two parts for different frequencies, that is, two film capacitors (2 $\times$ 12 μF/1000 V) and six ceramic capacitors (6 $\times$ 100 nF/1000 V). The film capacitors are assembled on an external PCB, while the ceramic capacitors are integrated into the module. Load inductor $L_{\rm load}$ is an air-core inductor with an inductance of 300 μH. The gate resistance R_g is 9.1 Ω. There are also individual small gate resistors and source resistors with

TABLE V
DPT TEST CONDITION

Parameter	Value
V_{dc}	400 V
V_g	+15 V/ -3V
R_g	9.1 Ω
C_{bus}	940 μF
C_{dc}	24 μF
L_{load}	300 μH

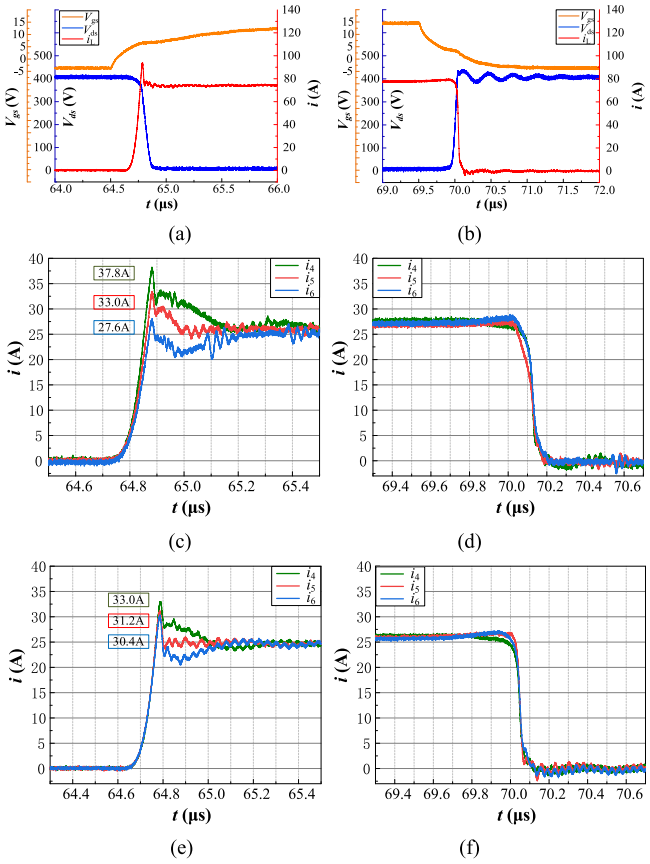

Fig. 11. Experimental waveforms of prototype test. (a) Drain–source voltage, gate–source voltage, and total current of prototype at turn-ON. (b) Drain–source voltage, gate–source voltage, and total current of prototype at turn-OFF. (c) Current of paralleled dies at turn-ON before optimization. (d) Current of paralleled dies at turn-OFF before optimization. (e) Current of paralleled dies at turn-ON after optimization. (f) Current of paralleled dies at turn-OFF after optimization.

a resistance of 1Ω for every die. In the test, +15 V/ −3 V gate drive voltage is given to the lower side by the gate drive circuit. The upper side's gate terminal and Kelvin source terminal are directly connected to turn MOSFETs OFF. Test conditions are given in Table V.

B. Result Analysis

DPT was conducted to evaluate the proposed optimization method on the designed module. Fig. 11 shows the experimental waveforms. The total waveform of the fabricated prototype at the second pulse time is shown in Fig. 11(a) and (b). Drain–source voltage, gate–source voltage, and total current of three MOSFETs are displayed. At turn-ON, the drain–source voltage starts to fall after gate–source voltage rises over the threshold voltage V_{th}. The total current of three MOSFETs quickly rises to about 75 A with an overshoot current of 93.9 A. High frequency resonant (27.01 MHz) could be detected on total current. This frequency is caused by the MOSFET output capacitance C_{oss} and the inner parasitic inductance of the module. The resonant frequency could be expressed by

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{9}$$

where f is the resonance frequency, L and C are the inductance and capacitance participating in the resonance.

Drain–source voltage goes down to 0 V subsequently at turn-ON. Voltage fall time at turn-ON is 79.6 ns. The highest *dv/dt* is 17.14 V/ns and the highest *di/dt* is 1.87 A/ns. At turn-OFF, the drain–source voltage rises to 400 V with an overshoot of 28 V (7.0%). A low frequency resonant (2.86 MHz) after voltage rising is detected. This resonant frequency could also be described by (9). It is caused by the resonant of decoupling capacitance and bus parasitic inductance. The total current falls to 0 A and remains a small oscillating trailing current. Voltage rise time at turn-OFF is 66.4 ns. The highest *dv/dt* is 14.29 V/ns and the highest *di/dt* is 2.89 A/ns. The parasitic inductance of the module could be calculated as 9.7 nH from waveform in Fig. 11(b)

$$\Delta V = L\frac{di}{dt} \tag{10}$$

where ΔV is the drain–source voltage overshoot caused by parasitic inductance and L is the total parasitic inductance of the module.

To confirm the result of current sharing, the drain current waveforms of three paralleled MOSFETs before and after optimization are shown in Fig. 11. In Fig. 11(c) and (d), the waveforms of the prototype with removed modification paths (before optimization) are displayed. The peak currents at turn-ON are 37.8, 33.0, and 27.6A. The imbalance degree of current is relatively high at 31.1%. While after optimization, the peak currents of three MOSFETs in Fig. 11(e) are 33.0, 31.2, and 30.4 A. The current difference Δi is 2.6 A with an imbalance degree low at 8.3%. It is detected that the currents are not balanced at a short time after the peak at turn-ON. This could be attributed to the differences in gate–source voltages of paralleled dies after the drain–source voltage drops to 0 V, which is likely caused by uneven internal gate resistances (external gate resistances have been controlled to be the same in the experiment). After the Miller plateau, the drain–source voltages drop to 0 V, while the gate–source voltages continue to rise and still not reach the maximum value. The dies could be considered as resistors at this time and the resistances are stilled related to gate–source voltage. Imbalance gate–source voltages at this time could cause different drain–source ON-state resistances and therefore lead to current imbalance in a short time as Fig. 11(e) until gate–source voltages reach +15 V. Even so, this imbalance does not make a

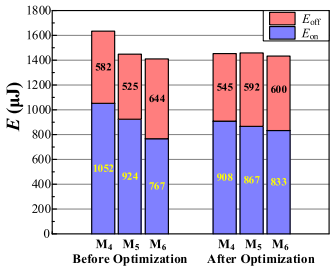

Fig. 12. Experimental total switching losses before optimization (without modification paths) and after optimization (with modification paths).

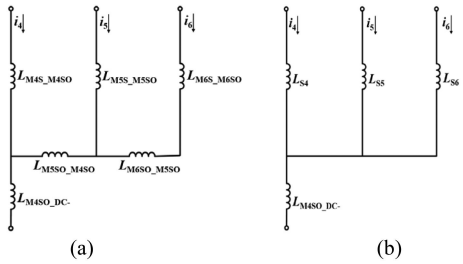

Fig. 13. Transformation of parasitic circuits without modification paths. (a) Parasitic circuit before transformation. (b) Parasitic circuit after transformation.

TABLE VI
SWITCHING CURRENT AND LOSSES SUMMARIZATION

Parameter	M_4	M_5	M_6	Imbalance degree
Peak current at turn-ON before optimization (A)	37.8	33.0	27.6	31.1%
Total switching losses before optimization(μJ)	1636.2	1448.5	1414.2	14.8%
Peak current at turn-on after optimization (A)	33.0	31.2	30.4	8.3%
Total switching losses after optimization(μJ)	1452.9	1458.2	1433.5	1.7%

TABLE VII
EXPRESSIONS OF INTERMEDIATE PARAMETERS

Symbols	Expression
L_{k1}	$L_{Cross4\_M5S} + L_{M5S\_Cross5} + \left[L_{Cross5\_M5SO} // (L_{k2})\right] + L_{M5SO\_M4SO}$
L_{k2}	$L_{Cross5\_M6S} + L_{M6S\_Cross6} + L_{Cross6\_M6SO} + L_{M6SO\_M5SO}$
L_{k3}	$L_{M5S\_Cross5} + \left[L_{Cross5\_M5SO} // (L_{k2})\right] + L_{M5SO\_M4SO}$
L_{k4}	$L_{M6S\_Cross6} + L_{Cross6\_M6SO} + L_{M6SO\_M5SO}$
L_{k5}	$L_{M5S\_Cross5} + L_{Cross4\_M5S} + L_{Cross4\_M4SO}$
L_{k6}	$\frac{L_{k5} \cdot L_{Cross5\_M5SO}}{L_{k5} + L_{Cross5\_M5SO} + L_{M5SO\_M4SO}}$
L_{k7}	$\frac{L_{Cross5\_M5SO} \cdot L_{M5SO\_M4SO}}{L_{k5} + L_{Cross5\_M5SO} + L_{M5SO\_M4SO}}$
L_{k8}	$\frac{L_{k5} \cdot L_{M5SO\_M4SO}}{L_{k5} + L_{Cross5\_M5SO} + L_{M5SO\_M4SO}}$
L_{k9}	$\frac{L_{k4} \cdot L_{Cross5\_M6S}}{L_{k4} + L_{Cross5\_M5SO} + L_{Cross5\_M6S}}$
L_{k10}	$\frac{L_{Cross5\_M5SO} \cdot L_{Cross5\_M6S}}{L_{k4} + L_{Cross5\_M5SO} + L_{Cross5\_M6S}}$
L_{k11}	$\frac{L_{k4} \cdot L_{M5SO\_M4SO}}{L_{k4} + L_{Cross5\_M5SO} + L_{Cross5\_M6S}}$

big difference in losses since the drain–source voltage is almost 0 V at this time. The total switching losses before and after optimization is shown in Fig. 12. The imbalance degree of peak current at turn ON and total switching losses are given in Table VI. Losses rely on the peak currents in switching time therefore the optimization for peak current sharing is of great significance. After using the proposed optimization method, the paralleled dies' loss imbalance degree decreases much from 14.8% to 1.7%. The designed module used the proposed optimization method the have balanced currents and switching losses, which helps to increase the capacity of the SiC converter.

V. CONCLUSION

This article presents a novel power source inductance optimization method using modification paths in a clip-bonded SiC multichip power module with the capability of current and loss sharing, thermal decoupling, and extensibility. In the designed module, the interconnection of the upper surface of dies is accomplished by Cu clip-bonding. The source inductances of branches are optimized by introducing extra paths on Cu clips. The simulation indicates that the specially modified paths get the same equivalent source inductances and reduce inductance by 27.4%. The test results of the prototype demonstrate that the designed module with modification paths has a balanced switching current with a maximum imbalance degree of 8.3% at turn-ON (compared with 31.1% without modification paths) and balanced loss with an imbalance degree of 1.7% (compared with 14.8% without modification paths) at a switching period. It means the power source inductances and losses of paralleled dies are balanced well by proposed modification paths. The proposed clip-bonded multichip module and optimization method is a promising solution to improve both electrical and thermal performances. Due to the simple routing design and optimization method, this Cu clip-bonded module and optimization method could be expanded to cases that more paralleled devices are needed.

APPENDIX

A. Equivalent Source Inductances Without Modification Paths

The parasitic circuit without modification paths before transformation is shown in Fig. 13(a). Define v_{LS4}, v_{LS5}, and v_{i6} as the voltage drops on parasitic source inductances of the corresponding branches. The voltage drops on three power source branches could be derived as (A1). Writing (A1) in matrix form as (A2). Making an approximation $i_4 = i_5 = i_6$, which means the current flowing through every branch is the same. Then, the matrix in (A2) could be simplified as (A3). The equivalent source inductances in (A3) are listed

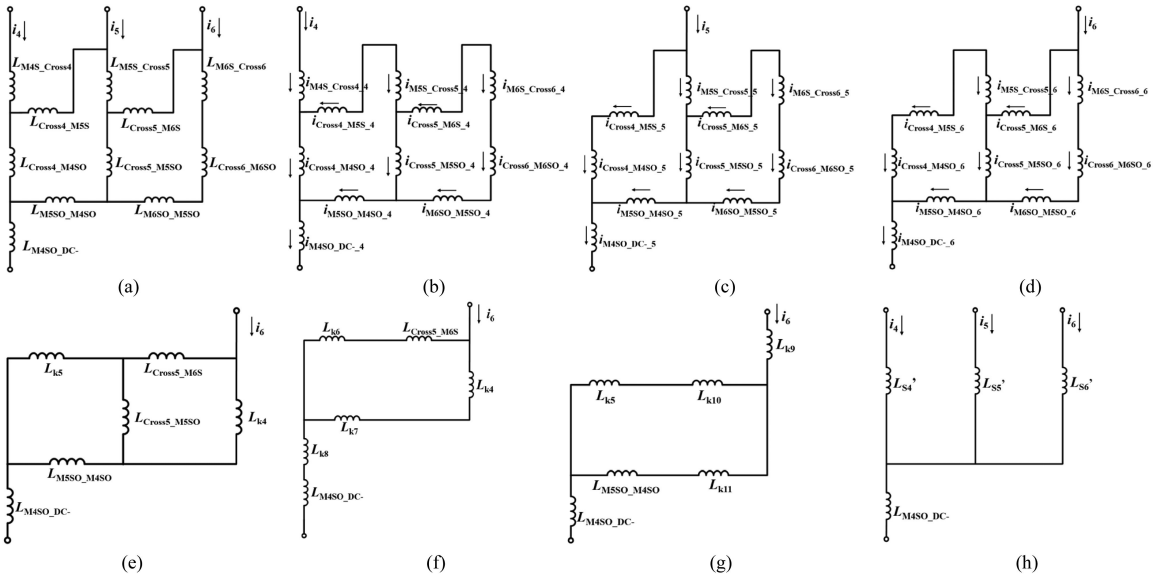

Fig. 14. Transformation of parasitic circuits with modification paths. (a) Parasitic circuit before transformation. (b) Subcircuit of *M*4. (c) Subcircuit of *M*5. (d) Subcircuit of *M*6. (e) Inductances combination of (d). (f)$\Delta - Y$ transformation of (e). (g) $Y - \Delta$ transformation of (f). (h) Simplified circuit model with MPs.

in (A4) where

$$v_{\mathrm{LS}} = (L_S + L_{\mathrm{M4SO\_DC-}}) \cdot \frac{d}{dt} i \tag{A2}$$

where $v_{LS} = [\, v_{LS4}\ v_{LS5}\ v_{LS6}\,]^T$, $i = [\, i_4\ i_5\ i_6\,]^T$

B. Equivalent Source Inductances With Modification Paths

The parasitic circuit with modification paths before transformation is shown in Fig. 14(a). Three MOSFETs are considered as current sources. Subcircuits with individual current sources are shown in Fig. 14(b)–(d). The currents flowing through the circuit in subcircuit with M_4 (Fig. 14(b)) are derived according to the series and parallel relationship in (B1). Currents flowing through subcircuits in Fig. 14(c) and (d) could be derived in the same way. Therefore similar formulas are omitted. Additionally, Δ-*Y* and *Y*-Δ transformations are needed in the derivation of Fig. 14(d). The inductances combination, Δ-*Y* transformation, and *Y*-Δ transformation are shown in Fig. 14(e)–(g). After calculation of currents on three subcircuits, the voltage drops on source inductances could be expressed by adding currents of subcircuits as (B3). The parameters in the matrix of (B3) are shown in (B6). The intermediate parameters L_{k1}-L_{k11}, are given in Table VII. Using the same approximation $i_4 = i_5 = i_6$, (B3) could be simplified as (B4). The equivalent source inductances in (B4) are listed in (B5) where

$$\begin{cases} v_{LS4} = L_{\mathrm{M4S\_M4SO}} \cdot \frac{di_4}{dt} + L_{\mathrm{M4SO\_DC-}} \cdot \frac{d(i_4+i_5+i_6)}{dt} \\ v_{LS5} = L_{\mathrm{M5S\_M5SO}} \cdot \frac{di_5}{dt} + L_{\mathrm{M5SO\_M4SO}} \cdot \frac{d(i_5+i_6)}{dt} + L_{\mathrm{M4SO\_DC-}} \cdot \frac{d(i_4+i_5+i_6)}{dt} \\ v_{LS6} = L_{\mathrm{M6S\_M6SO}} \cdot \frac{di_6}{dt} + L_{\mathrm{M6SO\_M5SO}} \cdot \frac{di_6}{dt} + L_{\mathrm{M5SO\_M4SO}} \cdot \frac{d(i_5+i_6)}{dt} \\ + L_{\mathrm{M4SO\_DC-}} \cdot \frac{d(i_4+i_5+i_6)}{dt} \end{cases} \tag{A1}$$

$$L_S = \begin{bmatrix} L_{\mathrm{M4S\_M4SO}} & 0 & 0 \\ 0 & L_{\mathrm{M5S\_M5SO}} + L_{\mathrm{M5SO\_M4SO}} & L_{\mathrm{M5SO\_M4SO}} \\ 0 & L_{\mathrm{M5SO\_M4SO}} & L_{\mathrm{M6S\_M6SO}} + L_{\mathrm{M6SO\_M5SO}} + L_{\mathrm{M5SO\_M4SO}} \end{bmatrix}$$

$$v_{LS} = \mathrm{diag}\,(L_{S4}{+}3L_{\mathrm{M4SO\_DC-}}, L_{S5}{+}3L_{\mathrm{M4SO\_DC-}}, L_{\mathrm{S6}}{+}3L_{\mathrm{M4SO\_DC-}}) \cdot \frac{d}{dt} i \tag{A3}$$

$$\begin{cases} L_{S4} = L_{\mathrm{M4S\_M4SO}} \\ L_{S5} = L_{\mathrm{M5S\_M5SO}} + 2L_{\mathrm{M5SO\_M4SO}} \\ L_{S6} = L_{\mathrm{M6S\_M6SO}} + L_{\mathrm{M6SO\_M5SO}}{+}2L_{\mathrm{M5SO\_M4SO}} \end{cases} \tag{A4}$$

$$\begin{cases} i_{\mathrm{M4S\_Cross4\_4}} = i_4, i_{\mathrm{Cross4\_M4SO\_4}} = \frac{L_{k1}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot i_4 \\ i_{\mathrm{Cross4\_M5S\_4}} = -\frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot i_4, i_{\mathrm{M5S\_Cross5\_4}} = \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot i_4 \\ i_{\mathrm{Cross5\_M5SO\_4}} = \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot \frac{L_{\mathrm{k2}}}{L_{\mathrm{Cross5\_M5SO}}+L_{\mathrm{k2}}} \cdot i_4 \\ i_{\mathrm{Cross5\_M6S\_4}} = -\frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot \frac{L_{\mathrm{Cross5\_M5SO}}}{L_{\mathrm{Cross5\_M5SO}}+L_{\mathrm{k2}}} \cdot i_4 \\ i_{\mathrm{M6S\_Cross6\_4}} = \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot \frac{L_{\mathrm{Cross5\_M5SO}}}{L_{\mathrm{Cross5\_M5SO}}+L_{\mathrm{k2}}} \cdot i_4 \\ i_{\mathrm{Cross6\_M6SO\_4}} = \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot \frac{L_{\mathrm{Cross5\_M5SO}}}{L_{\mathrm{Cross5\_M5SO}}+L_{\mathrm{k2}}} \cdot i_4 \\ i_{\mathrm{M6SO\_M5SO\_4}} = \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot \frac{L_{\mathrm{Cross5\_M5SO}}}{L_{\mathrm{Cross5\_M5SO}}+L_{\mathrm{k2}}} \cdot i_4 \\ i_{\mathrm{M5SO\_M4SO\_4}} = \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot i_4, i_{\mathrm{M4SO\_DC-\_4}} = i_4 \end{cases} \tag{B1}$$

$$\begin{cases} L_{k1} = L_{\mathrm{Cross4\_M5S}} + L_{\mathrm{M5S\_Cross5}} + [L_{\mathrm{Cross5\_M5SO}} // (L_{k2})] + L_{\mathrm{M5SO\_M4SO}} \\ L_{k2} = L_{\mathrm{Cross5\_M6S}} + L_{\mathrm{M6S\_Cross6}} + L_{\mathrm{Cross6\_M6SO}} + L_{\mathrm{M6SO\_M5SO}} \end{cases} \tag{B2}$$

$$\begin{bmatrix} v_{LS4}{}' \\ v_{LS5}{}' \\ v_{LS6}{}' \end{bmatrix} = \left(\begin{bmatrix} L_{41} & L_{42} & L_{43} \\ L_{51} & L_{52} & L_{53} \\ L_{61} & L_{62} & L_{63} \end{bmatrix} + L_{\mathrm{M4SO\_DC-}} \right) \cdot \frac{d}{dt} \begin{bmatrix} i_4 \\ i_5 \\ i_6 \end{bmatrix} \tag{B3}$$

$$v_{LS}{}' = \mathrm{diag}\left(L_{S4}{}' + 3L_{\mathrm{M4SO\_DC-}}, L_{S5}{}' + 3L_{\mathrm{M4SO\_DC-}}, L_{S6}{}' + 3L_{\mathrm{M4SO\_DC-}}\right) \cdot \frac{d}{dt} i \tag{B4}$$

$$\begin{cases} L_{S4}{}' = L_{41} + L_{42} + L_{43} \\ L_{S5}{}' = L_{51} + L_{52} + L_{53} \\ L_{S6}{}' = L_{61} + L_{62} + L_{63} \end{cases} \tag{B5}$$

$$\begin{cases} L_{41} = L_{\mathrm{M4S\_Cross4}} + \frac{L_{k1}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot L_{\mathrm{Cross4\_M4SO}} \\ L_{42} = \frac{L_{\mathrm{k3}}}{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}+L_{k3}} \cdot L_{\mathrm{Cross4\_M4SO}} \\ L_{43} = \frac{L_{k11}+L_{\mathrm{M5SO\_M4SO}}}{L_{k5}+L_{k10}+L_{k11}+L_{\mathrm{M5SO\_M4SO}}} \cdot L_{\mathrm{Cross4\_M4SO}} \\ L_{51} = \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot L_{\mathrm{M5S\_Cross5}} + \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot \frac{L_{\mathrm{k2}}}{L_{\mathrm{Cross5\_M5SO}}+L_{k2}} \cdot L_{\mathrm{Cross5\_M5SO}} \\ + \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot L_{\mathrm{M5SO\_M4SO}} \\ L_{52} = \frac{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}}{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}+L_{k3}} \cdot L_{\mathrm{M5S\_Cross5}} + \frac{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}}{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}+L_{k3}} \cdot \frac{L_{k2}}{L_{\mathrm{Cross5\_M5SO}}+L_{k2}} \cdot L_{\mathrm{Cross5\_M5SO}} \\ + \frac{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}}{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}+L_{k3}} \cdot L_{\mathrm{M5SO\_M4SO}} \\ L_{53} = -\frac{L_{k11}+L_{\mathrm{M5SO\_M4SO}}}{L_{k5}+L_{k10}+L_{k11}+L_{\mathrm{M5SO\_M4SO}}} \cdot L_{\mathrm{M5S\_Cross5}} + \left(\frac{L_{k5}+L_{k10}}{L_{k5}+L_{k10}+L_{k11}+L_{\mathrm{M5SO\_M4SO}}} - \frac{L_{k6}+L_{\mathrm{Cross5\_M6S}}}{L_{k4}+L_{k7}+L_{k6}+L_{\mathrm{Cross5\_M6S}}} \right) \\ \cdot L_{\mathrm{Cross5\_M5SO}} \\ + \frac{L_{k5}+L_{k10}}{L_{k5}+L_{k10}+L_{k11}+L_{\mathrm{M5SO\_M4SO}}} \cdot L_{\mathrm{M5SO\_M4SO}} \\ L_{61} = \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot \frac{L_{\mathrm{Cross5\_M5SO}}}{L_{\mathrm{Cross5\_M5SO}}+L_{k2}} \cdot (L_{\mathrm{M6S\_Cross6}} + L_{\mathrm{Cross6\_M6SO}} + L_{\mathrm{M6SO\_M5SO}}) \\ + \frac{L_{\mathrm{Cross4\_M4SO}}}{L_{\mathrm{Cross4\_M4SO}}+L_{k1}} \cdot L_{\mathrm{M5SO\_M4SO}} \\ L_{62} = \frac{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}}{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}+L_{k3}} \cdot \frac{L_{\mathrm{Cross5\_M5SO}}}{L_{\mathrm{Cross5\_M5SO}}+L_{k2}} \cdot (L_{\mathrm{M6S\_Cross6}} + L_{\mathrm{Cross6\_M6SO}} + L_{\mathrm{M6SO\_M5SO}}) \\ + \frac{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}}{L_{\mathrm{Cross4\_M4SO}}+L_{\mathrm{Cross4\_M5S}}+L_{k3}} \cdot L_{\mathrm{M5SO\_M4SO}} \\ L_{63} = \frac{L_{\mathrm{k6}}+L_{\mathrm{Cross5\_M6S}}}{L_{k4}+L_{k7}+L_{k6}+L_{\mathrm{Cross5\_M6S}}} \cdot (L_{\mathrm{M6S\_Cross6}} + L_{\mathrm{Cross6\_M6SO}} + L_{\mathrm{M6SO\_M5SO}}) \\ + \frac{L_{k5}+L_{k10}}{L_{k5}+L_{k10}+L_{k11}+L_{\mathrm{M5SO\_M4SO}}} \cdot L_{\mathrm{M5SO\_M4SO}} \end{cases} \tag{B6}$$

REFERENCES

[1] W. J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[2] M. Wang, F. Luo, and L. Xu, "A double-end sourced multi-chip improved wire-bonded SiC MOSFET power module design," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Mar. 2016, pp. 709–714.

[3] F. L. Chen and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 170–186, Sep. 2017.

[4] H. Lee, V. Smet, and R. Tummala, "A review of SiC power module packaging technologies: Challenges, advances, and emerging issues," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 239–255, Mar. 2020.

[5] F. Hou *et al.*, "Review of packaging schemes for power module," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 223–238, Mar. 2020.

[6] R. Bayerer and D. Domes, "Power circuit design for clean switching," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, 2010, pp. 1–6.

[7] G. Miller, "New semiconductor technologies challenge package and system setups," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, 2010, pp. 1–6.

[8] C. Durand, M. Klingler, D. Coutellier, and H. Naceur, "Power cycling reliability of power module: A survey," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 1, pp. 80–97, Mar. 2016.

[9] M. Ciappa and P. Malberti, "Plastic-strain of aluminium interconnections during pulsed operation of IGBT multichip modules," *Qual. Rel. Eng. Int.*, vol. 12, no. 4, pp. 297–303, 1996.

[10] K. B. Pedersen and K. Pedersen, "Bond wire lift-off in IGBT modules due to thermomechanical induced stress," in *Proc. 3rd IEEE Int. Symp. Power Electron. Distrib. Gener. Syst.*, Jun. 2012, pp. 519–526.
[11] J. Goehre, M. Schneider-Ramelow, U. Geißler, and K. Lang, "Interface degradation of A1 heavy wire bonds on power semiconductors during active power cycling measured by the shear test," in *Proc. 6th Int. Conf. Integr. Power Electron. Syst.*, 2010, pp. 1–6.
[12] J. Ling, T. Xu, and C. Luechinger, "Large Cu wire wedge bonding process for power devices," in *Proc. IEEE 13th Electron. Packag. Technol. Conf.*, Dec. 2011, pp. 1–5.
[13] R. Schmidt, C. König, and P. Prenosil, "Novel wire bond material for advanced power module packages," *Microelectron. Rel.*, vol. 52, no. 9, pp. 2283–2288, 2012.
[14] W. Chi, H. Chen, and H. Liao, "High reliability wire-less power module structure," in *Proc. 13th Int. Microsyst. Packag., Assem. Circuits Technol. Conf.*, 2018, pp. 71–74.
[15] L. Fy, L. Wo, L. Cc, and B. Rizal, "Process characterization of aluminum ribbon bond," in *Proc. Int. Conf. Electron. Mater. Packag.*, 2007, pp. 1–5.
[16] N. Marenco, M. Kontek, W. Reinert, J. Lingner, and M. Poech, "Copper ribbon bonding for power electronics applications," in *Proc. Eur. Microelectron. Packag. Conf.*, 2013, pp. 1–4.
[17] U. Scheuermann, "Reliability of planar SKiN interconnect technology," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst.*, 2012, pp. 1–8,.
[18] S. Haque *et al.*, "An innovative technique for packaging power electronic building blocks using metal posts interconnected parallel plate structures," *IEEE Trans. Adv. Packag.*, vol. 22, no. 2, pp. 136–144, May 1999.
[19] F. Yang *et al.*, "Interleaved planar packaging method of multichip SiC power module for thermal and electrical performance improvement," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1615–1629, Feb. 2022.
[20] H. Chang, J. Bu, G. Kong, and R. Labayen, "300A 650V 70 um thin IGBTs with double-sided cooling," in *Proc. IEEE 23rd Int. Symp. Power Semicond. Devices ICs*, May 2011, pp. 320–323.
[21] T. Abdoulahad, S. Emmanuel, S. William, R. Frédéric, and D. Maël, "3D-FE electro-thermo-magnetic modeling of automotive power electronic modules - wire-bonding and copper clip technologies comparison," in *Proc. IEEE Int. Workshop Integr. Power Packag.*, Apr. 2019, pp. 78–82,.
[22] Q. Zhu, A. Forsyth, R. Todd, and L. Mills, "Thermal characterisation of a copper-clip-bonded IGBT module with double-sided cooling," in *Proc. 23rd Int. Workshop Thermal Investig. ICs Syst.*, 2017, pp. 1–6.
[23] Y. Zhu, H. Chen, K. Xue, M. Li, and J. Wu, "Thermal and reliability analysis of clip bonding package using high thermal conductivity adhesive," in *Proc. IEEE 15th Electron. Packag. Technol. Conf.*, Dec. 2013, pp. 259–263.
[24] O. Sivkov, M. Novak, and J. Novak, "Comparison between Si IGBT and SiC MOSFET inverters for AC motor drive," in *Proc. 18th Int. Conf. Mechatronics Mechatronika*, 2018, pp. 1–5.
[25] C. Zhao, L. Wang, and F. Zhang, "Effect of asymmetric layout and unequal junction temperature on current sharing of paralleled SiC MOSFETs with kelvin-source connection," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 7392–7404, Jul. 2020.
[26] H. Li, S. Munk-Nielsen, S. Bęczkowski, and X. Wang, "A novel DBC layout for current imbalance mitigation in SiC MOSFET multichip power modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8042–8045, Dec. 2016.
[27] B. Zhang and S. Wang, "Parasitic inductance modeling and reduction for wire-bonded half-bridge SiC multichip power modules," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5892–5903, May 2021.
[28] S. Bęczkowski, A. B. Jørgensen, H. Li, C. Uhrenfeldt, X. Dai, and S. Munk-Nielsen, "Switching current imbalance mitigation in power modules with parallel connected SiC MOSFETs," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, 2017, pp. P.1–P.8.
[29] C. Zhao, L. Wang, F. Zhang, and F. Yang, "A method to balance dynamic current of paralleled SiC MOSFETs with kelvin connection based on response surface model and nonlinear optimization," *IEEE Trans. Power Electron.*, vol. 36, no. 2, pp. 2068–2079, Feb. 2021.
[30] Z. Zeng, X. Zhang, and X. Li, "Layout-dominated dynamic current imbalance in multichip power module: Mechanism modeling and comparative evaluation," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11199–11214, Nov. 2019.
[31] X. Jiang *et al.*, "Comparison study of surge current capability of body diode of SiC MOSFET and SiC Schottky diode," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2018, pp. 845–849.
[32] F. Yang *et al.*, "The study on thermal coupling effect for SiC power module design guidelines," in *Proc. IEEE Workshop Wide Bandgap Power Devices Appl. Asia*, Sep. 2020, pp. 1–7.
[33] W. Mu *et al.*, "Direct integration of optimized phase-change heat spreaders into SiC power module for thermal performance improvements under high heat flux," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5398–5410, May 2022, doi: 10.1109/TPEL.2021.3125329.
[34] Z. Zeng, J. Wang, L. Wang, Y. Yu, and K. Ou, "Inaccurate switching loss measurement of SiC MOSFET caused by probes: Modelization, characterization, and validation," *IEEE Trans. Instrum. Meas.*, vol. 70, Sep. 2021, Art. no. 1002014.

Laili Wang (Senior Member, IEEE) received the B.S., M.S., and Ph.D. degrees from the School of Electrical Engineering, Xi'an Jiaotong University, Xi'an, China, in 2004, 2007, and 2011, respectively.

Since 2011, he has been a Postdoctoral Research Fellow with the Department of Electrical Engineering, Queen's University, Kingston, ON, Canada. From 2014 to 2017, he was an Electrical Engineer with Sumida, Kingston, ON, Canada. In 2017, he was a Full Professor with Xi'an Jiaotong University. His research interests include wide bandgap power devices, package and integration, high density power conversion, wireless power transfer, and energy harvesting.

Dr. Wang is the recipient of Outstanding Young Scholar Award from China Power Supply Society, China Electric Power Excellent Young Technological Talent Award from Chinese Society of Electrical Engineering. He is currently an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS and IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN POWER ELECTRONICS. He is the Co-Chair of System Integration and Application in International Technology Roadmap for Wide Band-Gap Power Semiconductor, and the Chair of CPSS and IEEE PELS Joint Chapter in Xi'an, China.

Tongyu Zhang was born in Shaanxi, China, in 1997. He received the B.S. degree in electrical engineering in 2019 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in electronic and electrical engineering.

His research interests include the packaging and connection method of SiC power semiconductor devices and modules.

Fengtao Yang (Student Member, IEEE) was born in Shandong, China, in 1994. He received the B.S. degree in electronic and electrical engineering from the China University of Mining and Technology, Xuzhou, China, in 2016. He is currently working toward the Ph.D. degree in electronic and electrical engineering with Xi'an Jiaotong University, Xi'an, China.,

His current interests include advancement in electrical performance, thermal management, operation temperature, power density and integration of power modules, especially applied in wide-bandgap semiconductor device-based, high-current, high-temperature, and high-frequency power conversion systems.

Dingkun Ma was born in Shaanxi, China, in 1996. He received the B.S. degree in electrical engineering in 2018 from Xi'an Jiaotong University, Xi'an, China, where he is currently working toward the Ph.D. degree in electronic and electrical engineering.

His research interests include packaging and reliability of power semiconductor modules.

Cheng Zhao (Student Member, IEEE) was born in Shanxi, China, in 1996. He received the B.S. degree in electrical engineering from Jilin University, Changchun, China, in 2017. He is currently working toward the Ph.D. degree in electronic and electrical engineering with Xi'an Jiaotong University, Xi'an, China.

His research interests include packaging and applications of power semiconductor devices and parallel operation of SiC MOSFETs.

Yunqing Pei (Member, IEEE) was born in 1969. He received the B.S. and M.S. degrees in electrical engineering and the Ph.D. degree in power electronics from Xi'an Jiaotong University, Xi'an, China, in 1991,1994, and 1999, respectively.

He was a Faculty Member with Xi'an Jiaotong University, where he is currently a Professor. From February 2006 to February 2007, he was a Visiting Scholar of the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University. His research interests include high-power inverters, switch mode power supply, and converters in distributed generation systems.

Yongmei Gan (Member, IEEE) was born in 1971. She received the B.S. and M.S. degrees in control engineering from the Xi'an University of Technology, Xi'an, China, in 1993 and 1996, respectively, and the Ph.D. degree in control theory and control engineering from Northwestern Polytechnical University, Xi'an, China, in 1999.

Since 2000, she has been with the School of Electrical Engineering, Xi'an Jiaotong University, where she is currently an Associate Professor. From February 2008 to February 2009, she was a Visiting Scholar of Electrical and Computer Engineering, University of Toronto. Her research interests include package and integration, energy harvesting, and supervisory control of discrete-event systems.