Bayesian Optimization of PCB-Integrated Field Grading for a High-Density 10 kV SiC Power Module Interface

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***Abstract*—An automated numerical optimization workflow using Bayesian optimization and a novel weighted point-of-interest (POI) cost function is proposed and demonstrated for PCB-integrated electric field grading structures. The traditional manual design techniques for high-density insulation systems involve simulating the electric field performance and manually assessing the performance characteristics, iterating until an acceptable design is achieved. The proposed technique improves on this by allowing for a fully automated workflow, based on a scalable, computationally efficient cost function that is readily implemented in commercial software and finite element method (FEM) packages. The workflow is demonstrated on PCB-integrated field grading structures, which are employed to alleviate field crowding, and improve field uniformity around the terminals of a high-density 10 kV SiC MOSFET power module. The integrated field grading, in conjunction with the module housing, enables a power terminal spacing of 6 mm, while ensuring partial discharge (PD) free operation of the module. The proposed workflow accelerates design time by a factor of three when compared with a competing descent-based technique, and by a factor of 100 when compared with manual design techniques, with seven times lower convergence error. In addition, the optimized system performed 38% better than the previous manually designed version, experimentally demonstrating a PD inception voltage of 11.6 kV rms (16.4 kV peak). The proposed workflow is scalable to larger systems, making it applicable to a broad range of high-density, high-voltage insulation design problems.**

***Index Terms*—Bayesian, field grading, numerical techniques, optimization, partial discharge (PD), silicon carbide, triple-point.**

I. Introduction

MULTICHIP, wide bandgap power modules have the potential to dramatically improve the density and efficiency of medium voltage power conversion systems, due in part to their reduced ON-state losses, improved stability at temperature, and higher blocking voltages [1]–[4]. Innovative medium-voltage SiC power modules are quickly outpacing their Si counterparts, employing new materials, processes, and topologies to translate the advantages of SiC to the converter and system level. Initially reported in [5], the power module shown in Fig. 1, uses 10 kV 4H-SiC MOSFETs, large area silver sintering, and high-density spring-pin terminations to enable a power loop inductance of 4 nH/device and switching speeds >150 V/ns [6], in a footprint of only 83 × 68 × 16 mm^3 [7].

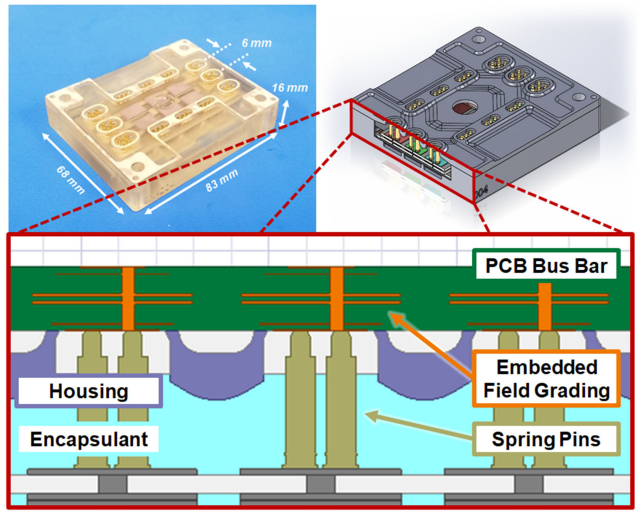

Fig. 1. Cross-section of the 10 kV, 80 A SiC MOSFET power module showing the fully enclosed power terminals sealed beneath the housing by the encapsulant and above the housing by the PCB busbar.

As voltage ratings increase, further improvements in power density and reduction of parasitic inductance become more difficult to achieve, as creepage and clearance distances ultimately dictate the required spacing between the terminals. The UL840 standard for insulation coordination of electrical equipment requires a minimum creepage distance of 40 mm for 10 kV systems at sea level and as much as three times higher as altitude increases [8].

The power module in Fig. 1 voids this requirement, reducing the terminal spacing to 6 mm, by removing the in-air path between the terminals. Fig. 1 shows how each terminal is fully enclosed, sealed beneath the housing by the encapsulant, and above the housing by a printed circuit board (PCB) busbar. While this technique voids the creepage requirement, the close

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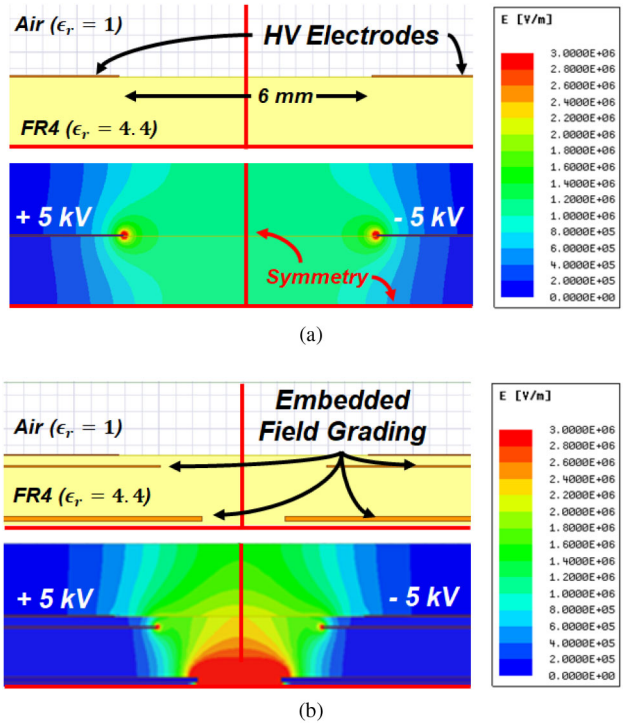


Fig. 2. a) Two high-voltage traces on a PCB dielectric surface with no integrated field grading show intense field crowding. b) With the addition of integrated field grading geometry, the crowding is alleviated. Note the lines of symmetry that can be used to further reduce the complexity of the domain when simulating the geometry.

proximity of the terminals creates intense field crowding, and high electric field magnitude that can lead to partial discharge (PD) or destructive breakdown of the system.

Initially proposed in [5], the PCB busbar design utilizes an integrated field grading structure (see Fig. 2), which makes use of the internal copper traces to draw the high intensity electric field inside the PCB dielectric, where the higher breakdown strength of the material can support the field without significant PD. In this way, the system takes advantage of insulation materials already present in the interface and does not require additional encapsulants, sealants, or gaskets to insulate the terminals.

The design of field grading structures is nontrivial. The complicated geometry makes analytical field solutions challenging and time consuming, unless the geometry can be dramatically simplified. This approach can result in coarse approximations of behavior and is limited to simple structures of one or two geometric parameters [9]. The traditional manual design techniques involving iterative simulation and modification by the designer quickly become suboptimal as the geometric complexity increases. High dimensionality prevents graphical analysis of performance trends and requires either significant geometric simplification, or a piecewise design approach, where regions are optimized independently from one another [10]. The result is a design approach that is both time consuming and may yield suboptimal, single-point designs that are not readily transferred or applied to other design problems [11], [12].

This article proposes an automated numerical optimization workflow using finite element analysis (FEA), Bayesian optimization, and a weighted point-of-interest (POI) cost function, which improves on the state-of-the-art by providing a computationally efficient, highly scalable, design framework that can be readily implemented with off-the-shelf software tools. This article will provide background on the state-of-the-art design techniques for insulation systems, specifically those with highly nonuniform electric fields and the associated challenges. This will be followed by a description of the cost function and Bayesian optimization as a means of addressing the shortcomings in the state-of-the-art. The proposed optimization workflow will then be used to 1) efficiently characterize the field reduction performance of integrated field grading geometry; and 2) streamline the design and optimization of the 10 kV SiC power module busbar and interface. This article will conclude with experimental verification of the design in the form of PD testing.

PD testing is carried out to verify the insulation performance of the system in an operational environment and assist in quantifying insulation performance improvements that are achieved as a result of the proposed optimization technique. This article will conclude with a tabulated summary of the benefits and drawbacks of the proposed numerical optimization scheme as compared with the conventional, manual design techniques.

II. Background

Electric field grading structures are most commonly found on a macroscopic scale in high voltage insulation systems, such as transmission cable terminations [13]–[15], and on a microscopic scale, such as edge terminations on high voltage semiconductor devices [16]–[18]. Field grading is achieved by one or more of three key mechanisms: 1) resistive field grading, where the field is graded by varying conductivity of the material; 2) permittivity grading, where permittivity of the material is varied, and 3) capacitive grading, where geometry is varied to manipulate where the electric field lines terminate [19]. The simplified model of the field grading structure, shown in Fig. 2, is an example of capacitive grading, where the geometry is used to redirect the electric field lines into the FR4 dielectric, where they can be supported without PD. Note that the color scale in Fig. 2 is limited to displaying values $\leq$ 3 kV/mm. This is because 3 kV/mm is the approximate breakdown strength of air and thus any in-air region exceeding 3 kV/mm is unacceptable and must be mitigated via field grading [20]. In contrast, the FR4 can contain significantly higher electric field strengths (up to 20 kV/mm [21]) and thus is allowed to support fields greater than 3 kV/mm.

Typically, field grading structures, and nonuniform fields in general, are designed using a manual technique, where design variables are swept independently and their impact is assessed graphically [14], [22]–[25]. When the geometric complexity of system is high, and the design variables cannot be visualized in a few dimensions, numerical optimization techniques have been employed. Historically, when the problem is nonconvex (i.e., multiple local minimums exist in the domain), neural networks have been used [26]–[29] and more recently, genetic [30] and particle swarm algorithms [31]–[33]; however, the usefulness is

often limited by long simulation times, large training sets, and marginal insulation performance improvements.

Descent-based algorithms have been used sparingly and are intended to improve computational efficiency but have achieved varied success [34]–[37]. When used in conjunction with an FEM solver, descent-based techniques can exhibit poor convergence due to nonphysical shallow minimums and finite difference derivative errors stemming from singularities in the domain [9], [38].

To improve the convergence of descent-based techniques, and smooth the domain of more sophisticated algorithms, field integration cost functions have been used [39]. This class of cost functions works by calculating the energy W contained in the electric field by means of Gauss's law

$$W = \frac{\epsilon}{2}\left(\int_{\mathcal{V}} E^2 d\tau + \oint_{\mathcal{S}} V\boldsymbol{E}\cdot d\boldsymbol{a}\right) \tag{1}$$

where ϵ is the permittivity, $\boldsymbol{E}$ and V are the electric field and scalar potential field, respectively, $\int_{\mathcal{V}}$ is the volume integral over the domain, and $\oint_{\mathcal{S}}$ is the surface integral around the domain [40]. The integration of the field requires a finely resolved mesh over the entire domain, which significantly increases the computational load of the FEM, as well as the integration.

Another approach to improve convergence is to use a solver that is more conducive to singularities, such as a boundary element solver (BEM) [41], [42]. A BEM technique can accurately resolve singularities by only discretizing and solving the boundaries; however, they typically require material properties that are not readily available from manufacturers [43]. In addition, BEM solvers are not readily available in commercial software packages such as ANSYS Electronics Desktop® and MATLAB®.

III. Numerical Optimization

A. Weighted POI Cost Function

To improve computational efficiency and scalability, a weighted POI cost function is proposed that relies on a least-squares-style sum of the peak electric field strength at a set of critical locations, or POIs. The POIs are placed only at the location of field crowding, near the crowding mechanism, such as a triple-point or singularity. In this way, the optimization relies only on those points, which limit the performance of the system.

To determine appropriate locations for the POIs, the electric field in the entire domain should be simulated to inform the designer of the limiting regions of the system, similar to what is done in conventional manual insulation design. Care must be taken to accurately identify the limiting regions as successful convergence of the result depends on effective POI selection.

A buffer term ε is employed, as proposed in [44], to help minimize the mesh dependent error of the FEA solution around singularities [45], [46], as shown in Fig. 3. A field intensity factor η is defined as the ratio between the electric field intensity at a given POI $E(\text{POI})$ and the dielectric breakdown strength of the

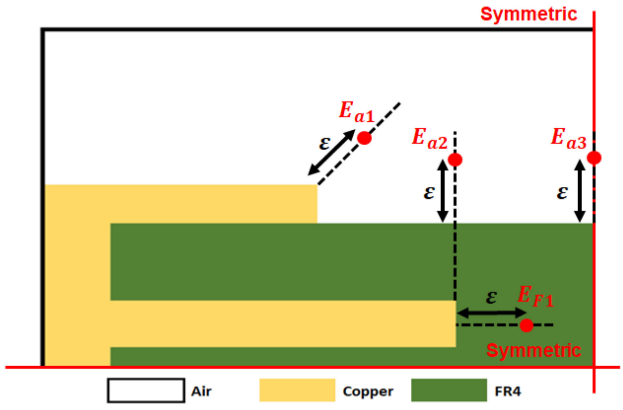


Fig. 3. Four-layer symmetric field structure with four POIs located a distance ε from the singularities.

containing medium E_{BD}

$$\eta = \frac{||\boldsymbol{E}(\text{POI})||}{E_{\text{BD}}}. \tag{2}$$

The intensity factor rescales the solution, ensuring the cost function is on the order of 1, as opposed to the order of the electric field strength (commonly 10^6 or higher for high-voltage, high-density systems). In addition, the intensity factor provides a weighting effect, scaling the intensity at each POI to be proportional to the breakdown strength of the containing medium. The η at each POI can then be summed as shown in (3), where M is the number of POIs in the system, FOS is a factor of safety which can vary for each medium or POI, and p is a penalty term which is selected such that $p > 1$

$$f(\vec{x}) = \sum_{i=1}^{M} (\text{FOS}_i \times \eta_i)^p \,. \tag{3}$$

In this formulation, the field strength at each POI is proportionally weighted by the dielectric breakdown strength of the containing medium. The penalty term p serves to penalize POIs with an intensity factor significantly larger than 1, indicating $||\boldsymbol{E}|| > E_{\text{BD}}$. When the intensity factor is less than one, meaning $||\boldsymbol{E}|| < E_{\text{BD}}$, the penalty term reduces the contribution of the POI to the cost function so that emphasis is maintained on those POIs with $\eta > 1$. This behavior can be visualized as shown in Fig. 4(a). In this article, a penalty term of $p = 2$ was selected as it provided sufficient decay of the POI. In general, the choice of p may be different for different geometries. In problems with disparity in the sensitivities of the POIs (i.e., where certain POIs are more sensitive to geometry changes than others), a lower penalty term such as 1.25 or 1.5 may be preferred to ensure more sensitive POIs to not dominate the cost function. To that end, it is important to run preliminary simulations to understand the variability in the POIs before selecting the value of the penalty term.

A factor of safety FOS term is introduced as an additional weighting term for materials that require further electric field reduction. For instance, the dielectric strength of standard 370 HR FR-4 is 20 kV/mm; however, the dielectric strength decreases significantly with thermal cycling as the interface between the

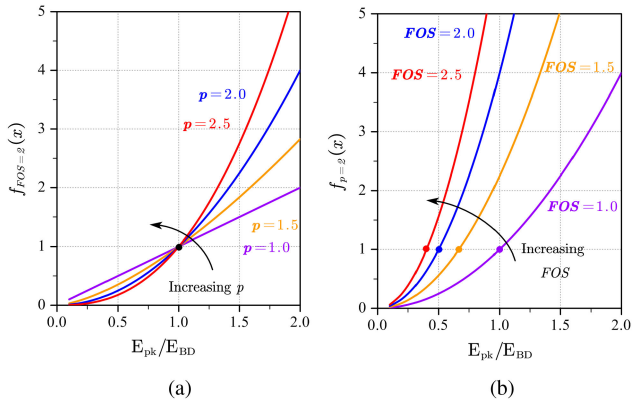


Fig. 4. (a) Effect of varying the penalty term p on the cost function $f(x)$ while holding the FOS term constant at FOS $= 2$. (b) Effect of varying the FOS term on the cost function while holding the penalty term p constant at $p = 2$.

copper traces and the dielectric degrades [21]. Therefore, an FOS of 2 or higher is preferred for this material. The weighting behavior of the FOS can be visualized as shown in Fig. 4(b), where as the FOS term increases, the point at which the contribution of the POI begins to diminish (the 1-crossing) moves closer to the origin. Note that one of the consequences of this behavior is that as the FOS increases, so does the rate at which the POI degrades. As a result, for systems that require a higher FOS, a lower penalty term may be used, such as $p = 1.5$ or $p = 1.25$.

The proposed cost function significantly reduces computational time when compared with field integration techniques in two key ways. First, the cost function is computationally trivial when compared to expensive 2-D and 3-D quadrature routines that are required to calculate field energy. Second, weighted POI only requires accurate FEM field solutions at the designated POIs, allowing the mesh in the rest of the domain to be very coarse. This contrasts with field integration techniques that require heavily resolved meshes across the entire domain for accurate integration, increasing both memory requirements, and computation times, while penalizing scalability. In this way, even though both the weighted-POI and the field integration technique solve for the entire domain, the weighted-POI can take advantage of a coarser mesh, which enables the speed improvement.

B. Bayesian Optimization Algorithm

While the proposed cost function decreases computation time, it comes at the cost of additional noise in the cost function as a result of the mesh dependent FEA error around singularities [44]. While the effect of the noise is reduced with the use of the buffer term ε, some degree of corruption is always present in the cost function, allowing shallow, false minimums, and sharp discontinuities to corrupt an otherwise smooth domain [47].

Rather than using complicated and expensive heuristic techniques, such as neural networks and genetic algorithms, the proposed workflow utilizes Bayesian optimization, which employs an efficient mechanism to combat the noise and corruption in the cost function. In this way, the algorithm directly addresses the corruption issue by providing noise immunity, allowing for the efficient optimization of an otherwise smooth domain. Heuristic algorithms, in contrast, address the symptom of the issue, employing expensive, nonlinear, and nonconvex solvers to navigate a corrupted domain.

The buffer term in conjunction with the Bayesian algorithm, addresses the FEA noise caused by the singularity, but not the inaccuracy of the solution. In this article, the inaccuracy is acceptable as the goal is to establish relative performance rather than absolute performance [44]. Determining the best design in a class of design variants only requires evaluation of performance relative to the other design variants in the class. Predicting absolute performance, e.g., predicting the PDIV of a given design, would require not only improved computational accuracy, but also improved geometric modeling, with the inclusion of surface quality, defects, and manufacturing tolerance, along with specific material and environmental properties, which are outside the scope of this article.

Bayesian optimization provides noise immunity by fitting a Gaussian process ($\mathcal{GP}$) model to the cost function and optimizing the model as opposed to optimizing the cost function directly. As a result, the algorithm does not require any derivative information and, because it is inherently a probabilistic model, allows for a degree of Gaussian distributed noise in the cost function. Bayesian optimization techniques are suitable for problems where

1) no analytical or numerical derivative information is available for the cost function;
2) cost function evaluation is expensive or relies on experimental data;
3) the cost function is only observable with some amount of Gaussian distributed error $f_{\text{obs}}(\vec{x}) = f(\vec{x}) + e$.

A $\mathcal{GP}$ is a multivariate analog to a Gaussian distribution, where the process is defined in terms of a mean function $m(\vec{x})$ and a covariance function $\boldsymbol{K}(\vec{x})$, as opposed to a Gaussian distribution, which is defined by a scalar mean μ and scalar variance σ^2

$$\begin{aligned} x &\in \mathbb{R}^1 \sim \mathcal{N}(\mu, \sigma^2) \\ \vec{x} &\in \mathbb{R}^N \sim \mathcal{GP}(m(\vec{x}), \boldsymbol{K}(\vec{x})). \end{aligned} \tag{4}$$

Fitting a $\mathcal{GP}$ to a dataset $(y_i, \vec{x}_i)$ as in (5) is called Gaussian process regression (GPR) and provides a means of determining an estimate value $y*$ and error bound $\sigma*$ for a query point $\vec{x}^*$ the same way a Gaussian distribution allows estimates and error bounds to be determined for future samples

$$\begin{aligned} \vec{y} &= \{y_1, y_2, \ldots, y_M\} \quad \text{for} \quad y_i \in \mathbb{R}^1 \\ \boldsymbol{x} &= \{\vec{x}_1, \vec{x}_2, \ldots, \vec{x}_M\} \quad \text{for} \quad \vec{x}_i \in \mathbb{R}^N \\ \text{where } y_i &= f(\vec{x}_i) \quad \text{for} \quad f : \mathbb{R}^N \to \mathbb{R}^1. \end{aligned} \tag{5}$$

These techniques are used extensively in machine learning and nonlinear curve fitting problems, where a $\mathcal{GP}$ is "trained" using a GPR on a training set (5) and then used to infer the properties of a query set $\boldsymbol{x}^* = \{\vec{x}_1^*, \vec{x}_2^*, \ldots, \vec{x}_M^*\}$ [48]. In an optimization problem, the cost function can be evaluated for a random set of 4 or 5 design variants, and the resulting data can

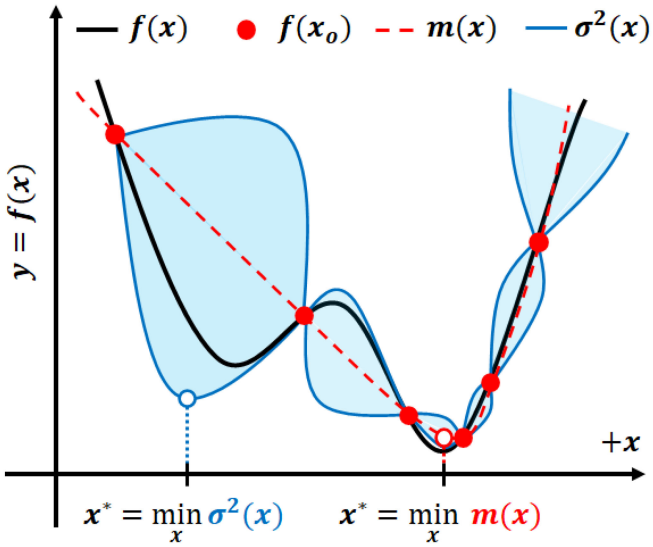


Fig. 5. Example of a 1-D optimization problem using GPR shows how minimizing the variance function (blue) and minimize the mean function (red dash) can yield different minimum estimates.

be use to fit a $\mathcal{GP}$. The $\mathcal{GP}$ can then be optimized resulting in an optimization process, which is immune to the mesh dependent noise in the same way that a Gaussian distribution is immune to noise.

The ability of the GP to model the system depends on selection of the covariance function $\boldsymbol{K}(\vec{x})$. In this article, the automatic relevance determination (ARD) Matérn 5/2 covariance kernel function is selected as described in [49]. This is a modified version of the more common ARD squared exponential function, which is widely regarded as the default standard in GPR problem [49] and has the advantage of being implemented in the MATLAB® Optimization Toolbox.

Optimizing the $\mathcal{GP}$ is completed without any gradient information by means of an acquisition function $a(\vec{x})$, which predicts the probability that the minimum objective function $f_{\min}$ will exist at a given location $\vec{x}$. The acquisition function works by balancing exploration, (exploring regions with high variance) and exploitation (exploiting regions with low mean).

Fig. 5 shows the domain of a 1-D optimization problem, where the objective function $f(x)$ is sampled on the points $\vec{x}_0 = \{x_1, x_2, \ldots, x_6\}$. With GPR, mean, and variance functions $m(x)$ and $\sigma^2(x)$ are fit to the sample data. The $\mathcal{GP}$ can be optimized by selecting the point with the lowest minimum or the point with the highest variance. The purpose of the acquisition function is to balance these two objectives, exploring new regions with high variance, and exploiting known regions for better minimums.

There are three main classes of acquisition functions: potential improvement (PI) [50], expected improvement (EI) [51], and upper/lower confidence bound (UCB/LCB) [52]. The EI acquisition function is the most popular and will be discussed here, while details for the remaining techniques can be found in the literature. The EI technique starts with the construction of the improvement matrix $\boldsymbol{I}$ as in (6), where $f_{\min}$ is the lowest objective function value observed thus far

$$f^*(\vec{x}) = m(\vec{x}) + \sigma^2(\vec{x})$$
$$\boldsymbol{I}(\vec{x}) = \begin{cases} f_{\min} - f^*(\vec{x}) & f^*(\vec{x}) < f_{\min} \\ 0 & \text{otherwise.} \end{cases} \tag{6}$$

The acquisition function is then calculated as the expectation of the improvement matrix

$$a(\vec{x}) = \mathbb{E}(\boldsymbol{I}(\vec{x}))$$
$$a(\vec{x}) = -\frac{\sigma(\vec{x})}{\sqrt{2\pi}}\exp\left(-\frac{(f_{\min} - m(\vec{x}))^2}{2\sigma^2(\vec{x})}\right) + (f_{\min} - m(\vec{x}))\Phi\left(\frac{f_{\min} - m(\vec{x})}{\sigma(\vec{x})}\right) \tag{7}$$

where $\Phi(\cdot)$ is the cumulative normal density function. From a physical interpretation standpoint, the EI acquisition function is the sum of two terms (7), where the leftmost term is weighted by the variance function, and the rightmost term is weighted by the mean function. In this way, the function balances the need for exploration with the need for exploitation. The $\vec{x}^*$ with the best probability of improving on the observed minimum $f_{\min}$ can now be calculated as follows:

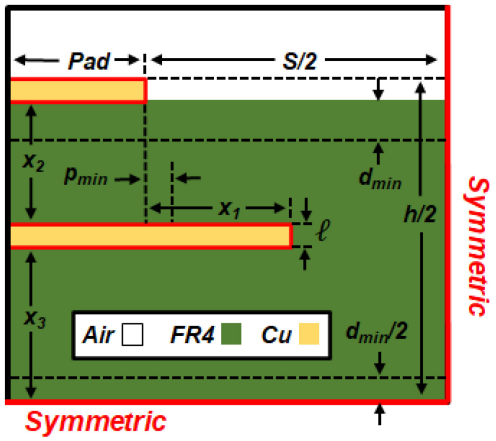
$$\vec{x}^* = \min_{\vec{x}} a(\vec{x}). \tag{8}$$

Given a means of assessing relative design performance (3), modeling the system without noise (4), and optimizing the model (8), a novel framework now exists to efficiently optimize insulation systems with highly nonuniform fields with commercially available FEM software packages.

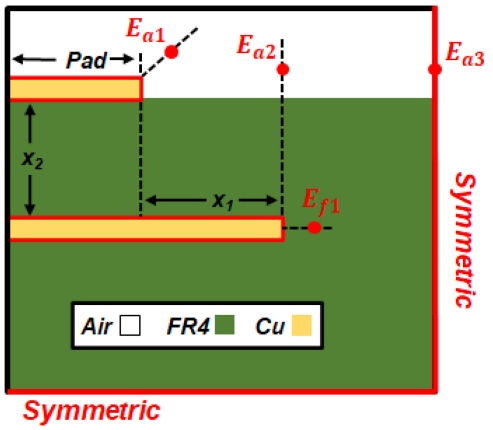
The Bayesian optimization algorithm can now be implemented as shown:

Generate random seed points $\boldsymbol{X}_0$ and $\boldsymbol{f}_0 = f(\boldsymbol{X}_0)$
while $i < K$ **do**
  Build GPR from training set $(\boldsymbol{f}_i, \boldsymbol{X}_i)$
  Locate minimum $\vec{x}_{i+1} = \min a(\vec{x})$
  $f_{i+1} = f(\vec{x}_{i+1})$
  $(\boldsymbol{f}_{i+1}, \boldsymbol{X}_{i+1}) \rightarrow (\boldsymbol{f}_i \cup f_{i+1}, \boldsymbol{X}_i \cup \vec{x}_{i+1})$
  Index $i \rightarrow i + 1$
end while.

The weighted POI cost function in conjunction, the Bayesian optimization algorithm, and the commercial FEA solver represent the proposed pipeline for high-voltage, high-density insulation system design. The FEA solver is used to enable ease of adoption, allowing the workflow to be implemented on a wide range of commercial software packages. Weighted POI is proposed as a means of improving efficiency and scalability, relying only on the field solution at those locations, which ultimately dictate system performance. Finally, Bayesian optimization and the underlying GP model is employed as a means to directly address the problem of noise in the cost function, allowing the efficient optimization of the underlying smooth domain, without the need for complicated heuristic techniques. The Bayesian algorithm is easily implemented in MATLAB®



(a)



(b)

Fig. 6. (a) Parameterized symmetric four-layer field grading structure with constraints and fixed design variables. (b) POI used for cost function formulation placed a distance ε from the singularity location.

with built-in routines and functions, further simplifying adoption and implementation.

IV. Optimization Results

A. Convergence Performance

The Bayesian optimization algorithm with weighted POI is benchmarked against a state-of-the-art descent-based interior-point algorithm for nonlinear systems [53]. Both algorithms will use a weighted POI cost function to optimize the four-layer symmetric field grading structure as parameterized in Fig. 6(a) with POIs located as shown in Fig. 6(b). The parameters used in the convergence performance study are given in Table I.

The optimization problem is constrained as shown in

$$\begin{aligned} \min_{\vec{x}} \ & \sum_{i=1}^{4} (\text{FOS}_i \times \eta_i)^p \\ p_{\text{min}} \leq \ & x_1 \leq S/2 \\ d_{\text{min}} \leq \ & x_2 \leq h/2 - 2\ell - d_{\text{min}}/2 \end{aligned} \tag{9}$$

TABLE I
Optimization, Simulation, and Material Parameters

Name	Parameter	Value
PCB Thickness	h	80 mil
Terminal Spacing	S	200 mil
Terminal Voltage	V_{dc}	10 kV
Trace Thickness	ℓ	1.4 mil (1 oz.)
Relative Permittivity of Air	ϵ_{ra}	1.0
Relative Permittivity of FR-4	ϵ_{rf}	4.4
Dielectric Strength of Air	E_{bd-a}	3 kV/mm
Dielectric Strength of FR-4	E_{bd-f}	20 kV/mm
Factor of Safety	FOS	2
Penalty Term	p	2
Buffer Term	ε	15 μm
Minimum Mesh Size	h_{min}	5 μm

TABLE II
Relative Error of Interior-Point Versus Bayesian Algorithm

	Interior-Point (Weighted POI)	Bayesian (Weighted POI)
Case 1	13.49 mils	0.29 mils
Case 2	3.33 mils	2.18 mils
Case 3	7.24 mils	0.86 mils
Average	8.02 mils	1.11 mils

where the plate length x_1 is constrained by the minimum effective plate length p_{min} and the axis of symmetry located a distance $S/2$ from the pad edge. The dielectric thickness x_3 can be removed from the optimization problem by fixing the PCB finish height h and copper trace thickness ℓ. The remaining dielectric height x_2 is bounded by a minimum manufacturable dielectric thickness d_{min} and the fixed height of the PCB. With only two optimizable variables, the convergence results can be visualized in a 3-D plot.

To evaluate convergence performance, the solution domain of the optimization problem, as defined by bounds in Fig. 9, is evaluated on a 1-mil grid and the minimum is found manually as shown in Fig. 7. The Bayesian optimization is run three times using five randomly selected seed points to build the initial GPR. The interior-point algorithm is run three times starting from three different reasonable initial design cases. The initial design points as well as the converged minimums are plotted in Fig. 7.

Despite the use of three different initial design points, all contained within the convex region of the domain, the interior-point is unable to converge to a repeatable minimum. The FEA electrostatic simulation of each initial point and the corresponding descent path is shown in Fig. 8. Each descent path illustrates the largely convex nature of the domain, which is corrupted with shallow minimums and sharp discontinuities stemming from the mesh dependent solution of the singularity. In contrast, the Bayesian algorithm is immune to the noise and reliably converges. A summary of the relative error, defined as the difference between the converged minimum and the known minimum, is shown in Table II. Compared with the interior-point algorithm, the Bayesian technique with weighted POI achieves seven times

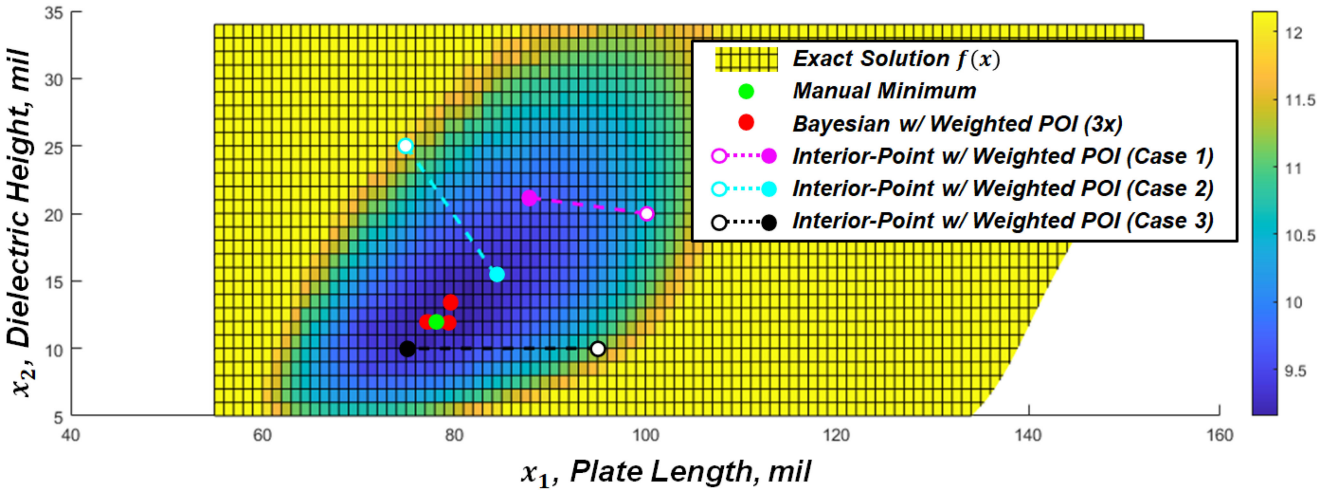


Fig. 7. Converged minimums of three independent Bayesian routines (red) and three interior-point routines (magenta, cyan, and black) both with weighted POI plotted against the known minimum (green). The Bayesian algorithm repeatedly converges to within 1 mil of the known minimum, while the interior point is unable to converge to a consistent minimum.

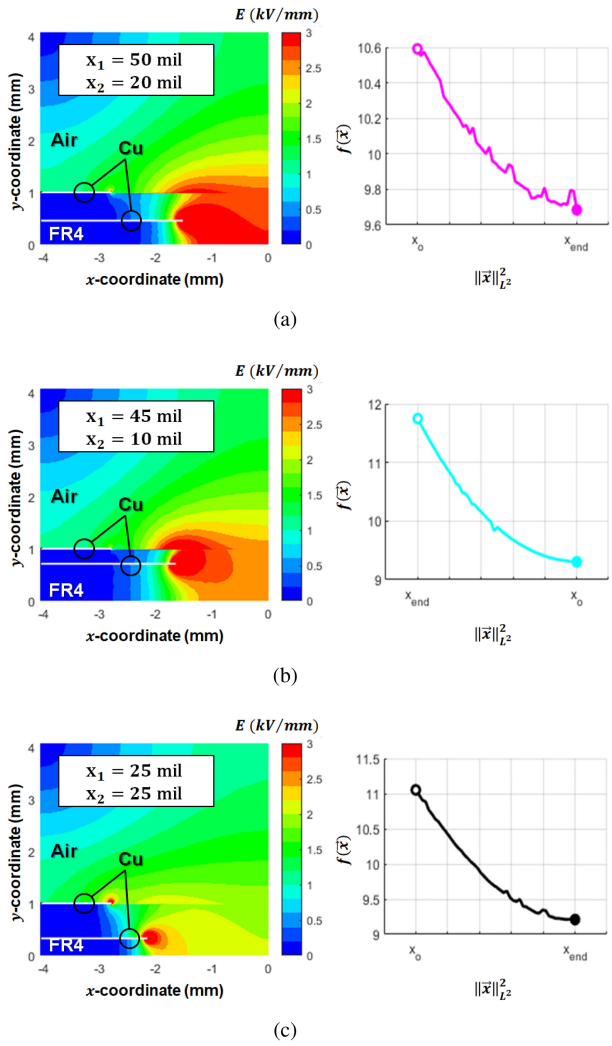


Fig. 8. Simulated electric field intensity of each of the three initial design points for the interior-point algorithm along with the corresponding descent path taken by the algorithm. (a) Case 1. (b) Case 2. (c) Case 3.

TABLE III
OBJECTIVE FUNCTION EVALUATIONS

		Cost Function Evaluations	Average Speed Increase of Bayesian
Interior-Point (Weighted POI)	Case 1	149	3x
	Case 2	78	
	Case 3	79	
Bayesian (Weighted POI)		30	1x
Manual Optimization (Weighted POI)		2940	100x

lower error, repeatably converging to within 1.1 mil of the known minimum.

B. Computation Time Comparison

With regard to simulation time, the run times of each algorithm can be compared in terms of the number of required cost function evaluations. Since the dimensionality of the problem is low (only two optimizable variables), the simulation time can be taken to be proportional to the number of required FEA simulations (1 per cost function evaluation), since the FEA simulation time is the dominating factor. Table III presents the number of FEA iterations used by each algorithm. Note that the number of FEA iterations is not necessarily equivalent to number of algorithm iterations. In the case of Bayesian optimization, the number of FEA iterations is equivalent to the number of optimization iterations as each objective function evaluation is used to refine the $\mathcal{GP}$ regardless of value. However, the interior-point routine may evaluate the objective function, and thus compute an FEA solution, many times in a given iteration in order to evaluate finite difference derivatives and determine effective step sizes.

The above study shows how the Bayesian optimization algorithm with weighted POI can quickly outpace a state-of-the-art descent-based algorithm in terms of simulation time and convergence error. Given the 2-D constrained optimization problem defined in (9), the proposed technique repeatably converges to

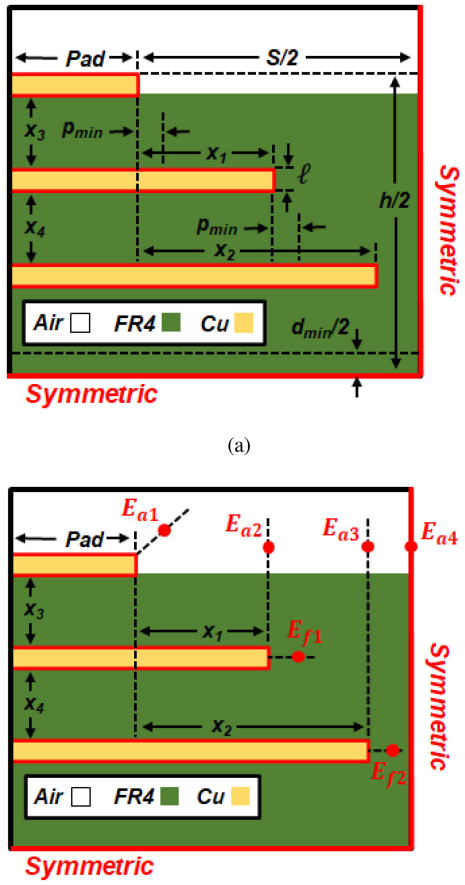


Fig. 9. (a) Parameterized symmetric six-layer field grading structure with constraints and fixed design variables. (b) POI used for cost function formulation placed a distance ε from the singularity location.

within 1.1 mil of the known minimum, resulting in seven times lower error than the competing technique. Due to the reduced number of FEA iterations required, the Bayesian technique arrives at the minimum in only 30 iterations, making it three times faster than interior-point, and 100 times faster than manually sweeping the domain for the minimum. As the dimension of the problem increases, the speed improvement of the Bayesian technique continues to increase.

V. Field Grading System Characterization

Bayesian optimization is used to fully characterize the performance of the symmetric four-layer field grading structure from Fig. 6 as well as the symmetric six-layer system shown in Fig. 9. The constraints for the six layer systems are built out in a similar fashion as the four-layer system, using the minimum effective plate length and minimum feasible dielectric $p_{\min}$ and $d_{\min}$ as shown in the following:

$$\min_{\vec{x}} \sum_{i=1}^{6} (\text{FOS}_i \times \eta_i)^p$$

$$p_{\min} \leq x_1 \leq S/2$$

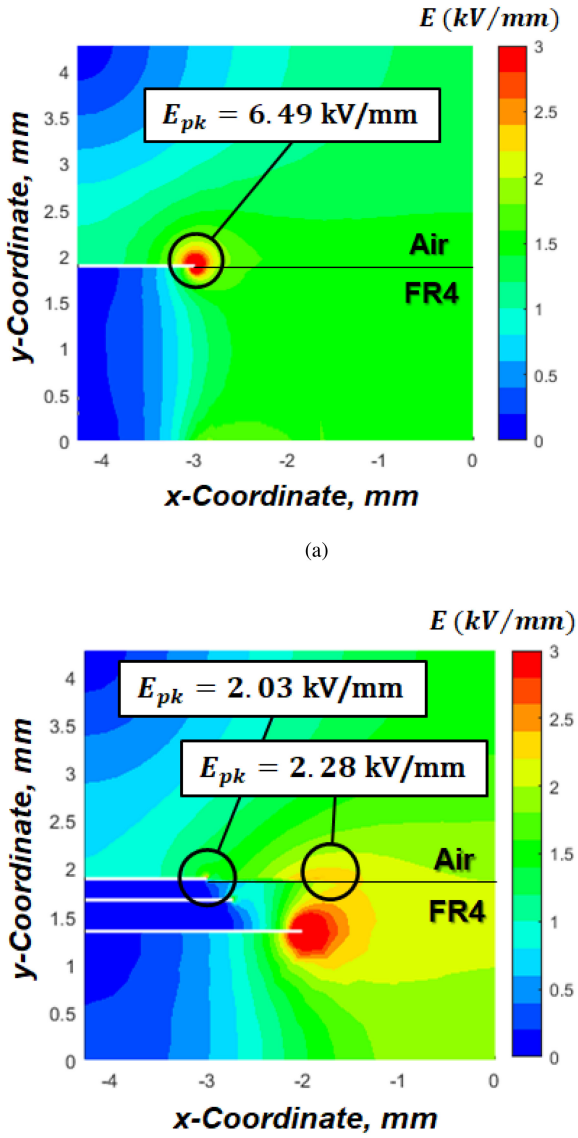


Fig. 10. (a) Electrostatic FEA simulation of baseline cross-section with no field grading shows a peak electric field intensity of 6.49 kV/mm. (b) Simulation of optimized field grading geometry shows the peak electric field intensity in air reduced to 2.28 kV/mm, a factor of $1 - \lambda$.

$$x_1 + p_{\min} \leq x_2 \leq S/2$$
$$d_{\min} \leq x_3 \leq h/2 - 3\ell - d_{\min}/2 - x_4$$
$$d_{\min} \leq x_4 \leq h/2 - 3\ell - d_{\min}/2 - x_3. \quad (10)$$

To compare relative performance between design variants, a performance metric λ is defined, called the field grading coefficient. The coefficient is defined as the ratio between the peak electric field intensity with optimal field grading $E_{pk-\text{Grading}}$ versus the electric field intensity with no field grading $E_{pk-No-\text{Grading}}$ as shown in (11). To evaluate the electric field strength without field grading plates $E_{pk-No-\text{Grading}}$ a baseline simulation is used as shown in Fig. 10(a). The baseline simulation has an identical geometry to the field grading structure in Fig. 10(b) (same dielectric size, pad size, trace spacing, etc.)

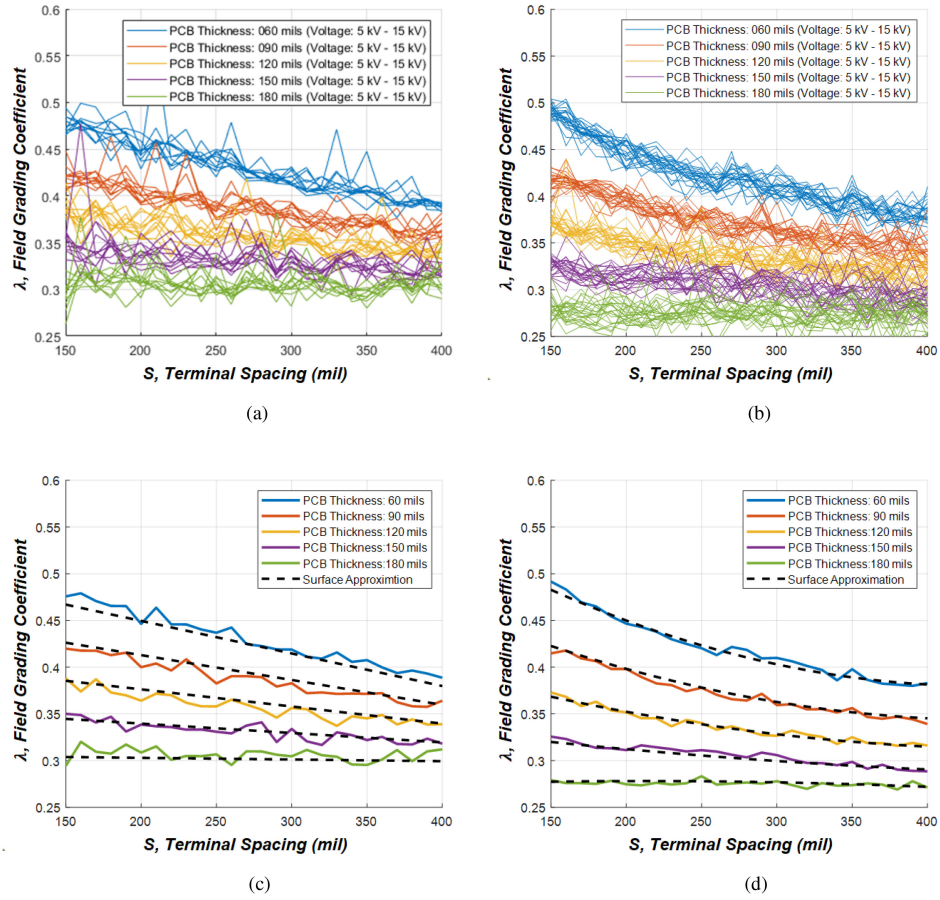


Fig. 11. (a) and (b) Field grading coefficient λ plotted over all design variants from Table IV for the four-layer and six-layer structure, respectively. (c) and (d) Averaged data from all voltage curves plotted along with a low order polynomial surface fit (dashed line).

TABLE IV
DESIGN PARAMETER SWEEP FOR CHARACTERIZATION

Parameter	Min.	Incr.	Max.	Variants
Terminal Voltage	5 kV	1 kV	15 kV	11
Terminal Spacing	150 mil	10 mil	400 mil	26
PCB Thickness	60 mil	30 mil	180 mil	5
			Total Design Variants:	1430

except that all of the field grading plates have been removed. The field grading coefficient is especially useful as it normalizes the effect of varying terminal voltage V_{dc}, reducing the number of fixed design variables to two: the terminal spacing S and the PCB finish height h.

$$\lambda = \frac{E_{pk-\text{Grading}}}{E_{pk-No-\text{Grading}}}. \tag{11}$$

To characterize the system, both of the fixed design variables S and h will be swept across a reasonable range as shown in Table IV for both the four-layer and six-layer structure. The field grading coefficient λ will be calculated for each case and compared. In addition to S and h, the terminal voltage V_{dc} will be swept from 5 to 15 kV to demonstrate the independence of voltage.

Due to the lightweight mesh required for weighted POI, the electrostatic field FEA is quickly computed on a modern workstation with MATLAB®. Each Bayesian routine iterates 30 times before terminating and takes approximately 2 min in total to run. When parallelized across eight cores on a 4 GHz desktop processor, the optimization of all 1430 design cases takes 6 h.

Fig. 11 shows the relative performance for the four-layer and six-layer symmetric structures. Fig. 11(a) and (b) shows the field grading coefficients for all the simulated design cases, and how the performance, as measured by λ, is independent of the terminal voltage. Any dependence that does exist is below the convergence tolerance of the algorithm.

Fig. 11(c) and (d) shows the performance when averaged across the different terminal voltages. A low order polynomial surface regression is fit to the data to provide a means of quickly estimating system performance. The polynomial surface fits are shown in Table V, where λ_4 and λ_6 are the field grading coefficients for the four-layer and six-layer structures, respectively. Each curve fit has a 3σ tolerance of 0.022 and 0.012, respectively.

VI. HIGH-DENSITY INTERFACE DESIGN

The layout of the wirebond-less 10 kV SiC MOSFET package from Fig. 1 is shown in Fig. 12 along with relevant potentials and dimensions. Critical design regions, as indicated by the bold red line in Fig. 12, are identified as having the highest potential

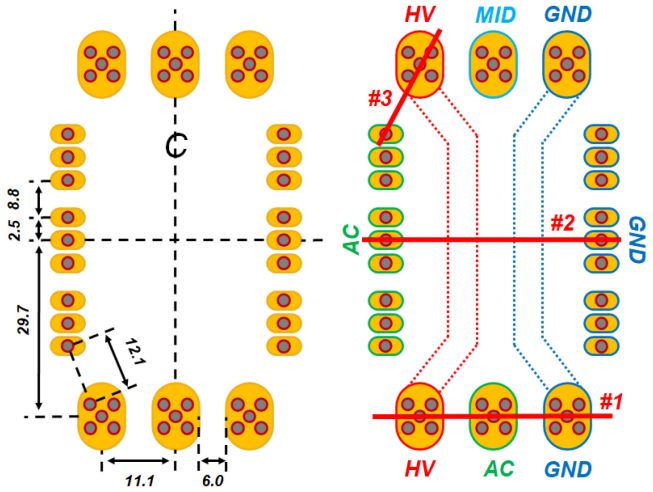


Fig. 12. PCB footprint of 80 A. 10 kV SiC MOSFET power module with relevant dimensions (left) and critical design regions (right) shown by the solid red line and numbered 1–3. All dimensions are in mm. Internal traces are shown with a fine dashed line.

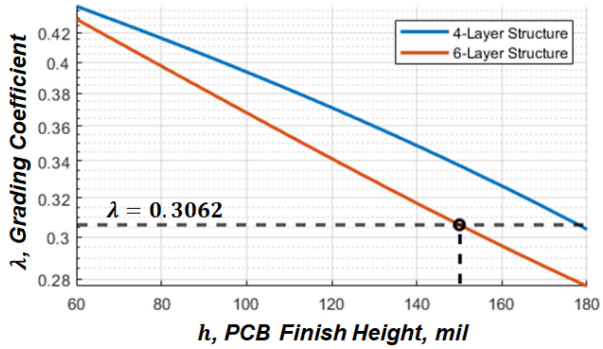


Fig. 13. Polynomial surface approximations from Table V use to determine the structure (layer count) and PCB height of a critical design region.

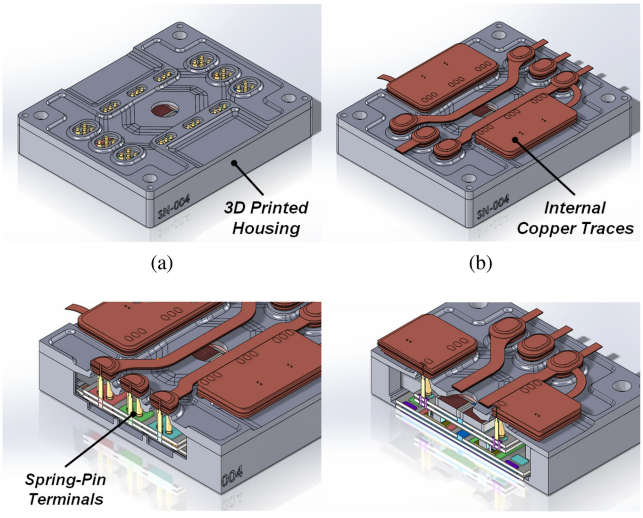


Fig. 14. Optimized (a) housing, (b) housing and PCB busbar, (c) critical region 1, and (d) critical region 2.

TABLE V
λ POLYNOMIAL SURFACE APPROXIMATIONS

	units	$\lambda_4(h,S)$	$\lambda_6(h,S)$
1	mil	0.626	0.829
h	mil	-1.77e-3	-3.69e-3
S	mil	-0.51e-3	-1.69e-3
hS	mil^2	2.75e-6	9.79e-6
h^2	mil^2	-	3.24e-6
S^2	mil^2	-	1.98e-6
hS^2	mil^3	-	-12e-9
3σ $Tol.$		$\pm$ 0.022	$\pm$ 0.012

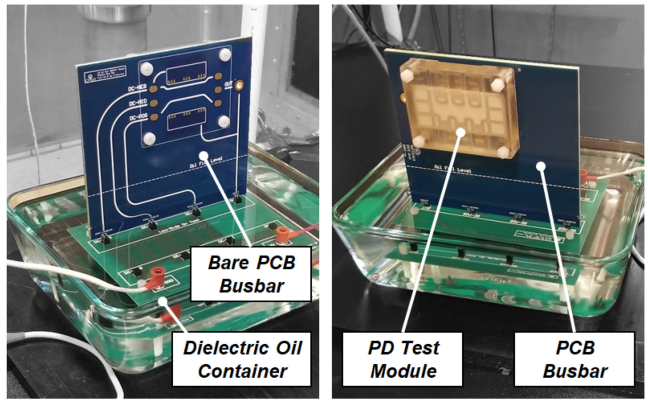


Fig. 15. PD test setup showing the PCB busbar mounted to the base board with the high-voltage interconnects submerged in oil, (a) bare PCB, and (b) PCB mated to the PD test module.

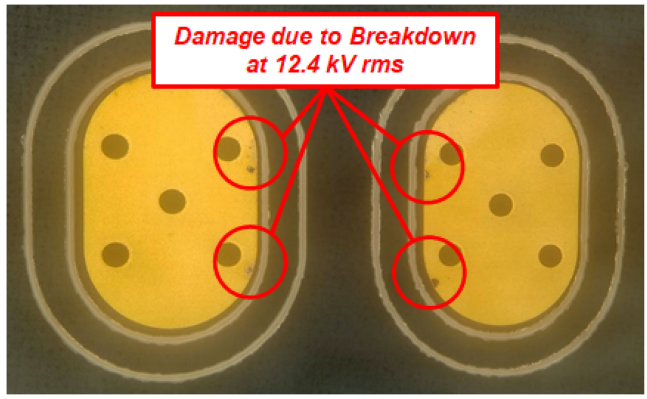
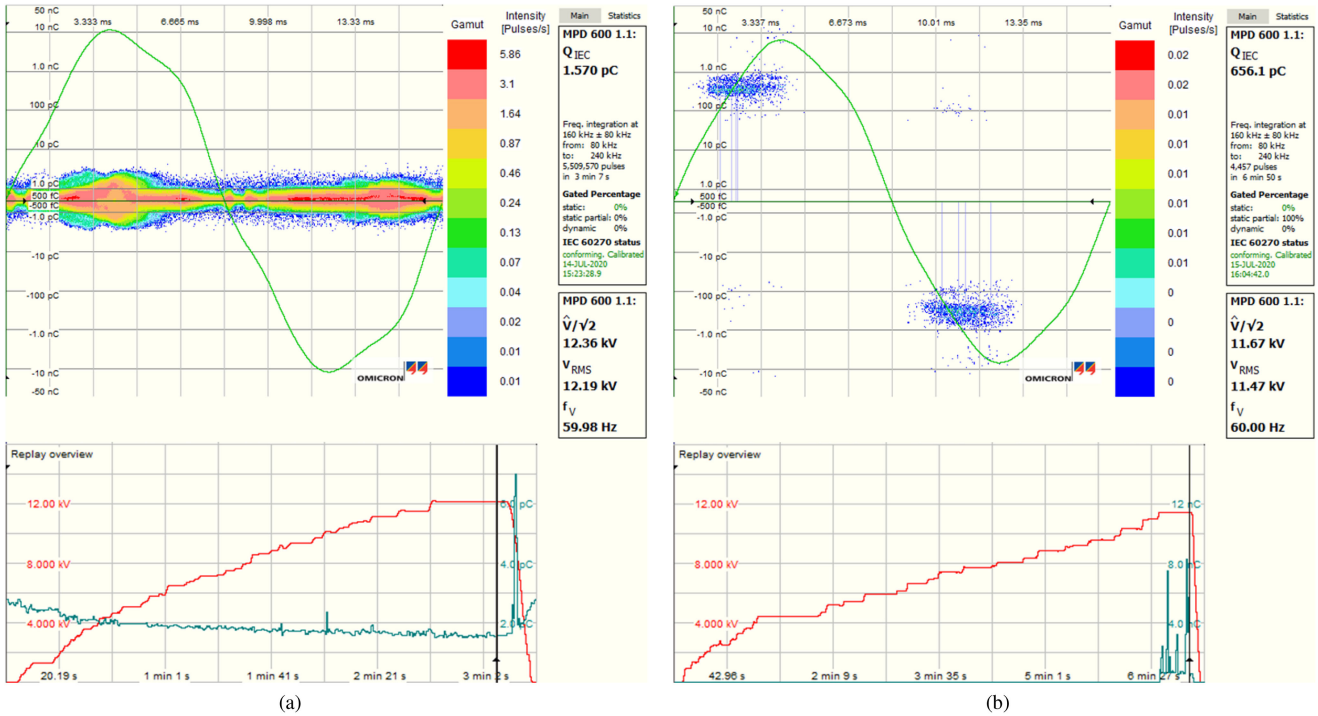


Fig. 16. Destructive breakdown occurring on the surface of the PCB when PD tested without the PD test module attached. Breakdown occurred between the $+V_{\text{dc}}$ and $\pm V_{\text{dc}}$ pads of the busbar along critical cross section 1.

across the smallest terminal spacings. Each of these three critical regions require the design of integrated field grading geometry. Once designed, the geometry can be mirrored to the rest of the package footprint.

Since the terminal spacing is determined by the footprint, and field grading performance as defined by λ is independent of voltage, the only design parameters that must be established for optimization are the PCB finish height h, and the number of layers in the structure. The polynomial surface approximations from Table V can be used to quickly evaluate the relative performance of different PCB heights and layer counts for each critical region in Fig. 12.



(a) (b)

Fig. 17. PRPD and corresponding Q_{IEC} versus time plot for (a) low-side-on configuration without the PD test module and (b) low-side-on configuration with PD test module.

Fig. 13 shows the polynomial surface approximations of the field grading coefficients for a four-layer and six-layer field grading structure at the first critical region. From the polynomial regression, it is seen that a six-layer structure provides significantly more field reduction than a four-layer structure with the same terminal spacing of 236 mil (6 mm). In addition to providing improved field reduction, a six-layer structure will allow for additional design flexibility when the housing is designed and mated to the busbar, as shown in Fig 1. A PCB finish height of 150 mil is selected, which yields an estimated electric field reduction of $1-\lambda$ or approximately 70%. The resulting geometry is optimized and shown in Fig. 10. The remaining critical regions and the housing are parameterized and optimized in the same manner as above. The completed busbar and housing designs are shown in Fig. 14.

VII. Experimental Verification

PD testing is used to verify the performance of both the manually designed and numerically design PCB busbars, and to demonstrate the viability of the module/busbar interface. Both versions of the busbar (manually and numerically optimized) are tested with and without a PD test module as will be discussed in the following sections.

A. PD Test Setup

The PD test setup uses a variable output 100 kV 60 Hz ac supply with a 1 nF, 100 kV coupling capacitor and an Omicron MPD® 600 PD measurement and analysis system. The system is calibrated per the IEC 60270 standard with a 10 pC charge injection. During testing, the high-voltage interconnects from the power supply are submerged in Shell Diala® S4 ZX-I ($V_{BD} = 60$ kV/mm) dielectric oil to ensure PD only occurs in the desired test region. The test setup is shown in Fig. 15.

The PCB busbar is tested both as a bare PCB, to verify the field grading design, and mated to the module, to verify the module interface. The interface is tested using a PD test module as opposed to a functional package. The module is constructed to be electrostatically equivalent to a functional package but contains no functional devices. The busbar is benchmarked against a previous version of the busbar and module interface that was designed exclusively using an iterative manual design technique.

B. Experimental Results

Ten PCBs in total were tested starting with the bare PCB (no PD test module). Of the ten PCBs, four failed during test due to destructive breakdown across the test region at 12.4 kV rms before PD was observed. The damage on the PCB pads after breakdown is shown in Fig. 16. The occurrence of breakdown before PD indicates a highly uniform electric field in the test region and thus serves as a preliminary verification that the field grading structures successfully alleviated the nonuniform field crowding. The damage on the pads shows symmetric discharge occurring evenly over the width of the pad, further suggesting a highly uniform electric field [54].

Of the six remaining PCBs, the median PDIV was 12.2 kV rms. The phase resolved PD (PRPD) plot and corresponding charge Q_{IEC} (as defined in IEC 60664) versus time plot are shown in Fig. 17(a). The plot shows no PD >10 pC in magnitude up to 12.2 kV rms. The approximately 2 pC Q_{IEC} visible for the duration of the test is the noise threshold of the test setup and

TABLE VI
SUMMARY OF KEY METRICS

	Manual Design Technique	Weighted-POI Bayesian
FEA Iterations	2940	30
Measured PDIV	8.4 kV rms	11.6 kV rms
Convergence Error	0	1.11 mils
Extracted Design Trends	No	Yes
Requires Hyperparameters	No	Yes

is not representative of PD occurring in the system. The test was stopped before significant PD occurred to avoid potential breakdown.

After testing the bare PCBs, the PD test module was mated to the busbar, and the same tests were run again. The median PDIV of the tests was 11.6 kV rms. The PRPD plot and corresponding Q_{IEC} plot are shown in Fig. 17(b). In this test, significant sustained PD occurred at ll.7 kV rms.

The PD distribution from the PRPD plot in Fig. 17(b) indicates PD is occurring within a void as opposed to corona discharge in air [55]. While the void could be present in the FR-4 of the PCB, the previous tests of the bare PCB did not indicate this behavior, and thus it can be concluded that the void is present in the PD test module, contained either in the silicone encapsulant, or perhaps within the contained AlN substrate. This test result indicates that the PCB busbar and the housing/busbar interface are not the limiting factors of the design and instead, the insulation performance of the system is limited by the fabrication techniques of the 10 kV power module.

This contrasts with the performance of the manually optimized variant, where the performance is limited by the interface. The manual variant was tested in a similar manner, with individual tests performed for the low-side-on and high-side-on configurations, both with and without a PD test module. With the PD dummy module attached, the manually designed variant experienced destructive breakdown at 8.4 kV rms, 38% lower than the 11.6 kV rms PDIV of the numerically optimized version.

From the experimental results, several key conclusions are drawn. First, the embedded field grading geometry successfully alleviates the highly nonuniform electric field crowding around the terminals as indicated by destructive breakdown occurring before the observation of any significant PD. Second, the embedded field grading successfully mitigated the PD risk of the 6 mm terminal spacing in air, resulting the module being the limiting factor of the design. This is indicated by the PRPD plot in Fig. 17(b), which shows discharge occurring in a void contained in the PD test module. Third, the Bayesian design technique with weighted-POI directly enables a significant performance increase by allowing for the evaluation of a broader design range, and streamlined identification of optimal design cases, as indicated by the 38% performance increase when compared to a manually designed variant.

VIII. CONCLUSION

This article presents a computationally efficient, scalable, numerical optimization workflow using commercial FEA software, a novel, weighted POI cost function, and Bayesian optimization. The technique is specifically designed to enable the optimization of high-density, high-voltage insulation systems, with nonuniform electric fields and intense field crowding. The weighted POI cost function is defined to be computationally trivial, and rely only on the electric field strength in the regions that ultimately limit the electrostatic performance, allowing for coarse FEA meshes, faster simulation times, and a high degree of scalability.

Bayesian optimization is selected specifically to address the FEA solution error around the singularity. The Gaussian process model provides noise immunity, allowing for the efficient optimization of the underlying system dynamics. The result is a workflow that demonstrates three times faster convergences, and seven times lower convergence error when compared to a competing descent-based algorithm. When compared with the conventional manual design techniques, the proposed workflow was 100 times faster and fully automated. Table VI summarizes the key metrics of the proposed Weighted-POI + Bayesian optimization technique as compared with the conventional manual design techniques. The weighted-POI + interior-point algorithm is not included in this table as the technique does not converge reliably.

The optimization workflow was applied to the design of a high-density, high-voltage PCB busbar with integrated field grading structures for a 10 kV SiC MOSFET power module. The technique allowed for efficient characterization of the field grading structure, yielding useful insights into the performance limitations. The insights were quantified in a series of low-order models that can be used to easily predict and evaluate system performance. The data obtained from the structure characterization were used in conjunction with the optimization routine to streamline the design of the field grading structures and module interface.

PD testing was used to validate that a successful design was achieved by the proposed optimization technique. The measured PDIV for the manually optimized design was 8.4 kV rms (11.9 kV peak), while the measured PDIV for the numerically optimized design was 11.6 kV rms (16.4 kV peak). The numerical optimization thus provided a design with 38% higher PDIV than the manually optimized design while also reducing the number of required FEA iterations by a factor of 100. This demonstrates the viability of both the optimization technique and the high-density module/busbar interface.

The weighted POI cost function in conjunction with Bayesian optimization allows for streamlined design and optimization of high-density, high-voltage insulation systems. The computational efficiency, scalability, and ease of integration make the proposed workflow applicable to a broad range of insulation design problems such as high- and medium-voltage power modules, laminate busbars, high density magnetic components, and high-voltage cable assemblies. Opportunities for future work include exploring the possibility of a hybrid optimization technique that would utilize both the field integration and the POI to enable a reduction in computational time while reducing the noise content in the cost function.

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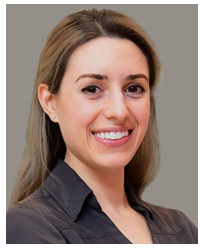

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