An Integrated Power Converter-Based Brushless DC Motor Drive System

Jun Cai, *Senior Member, IEEE*, Xin Zhang, *Senior Member, IEEE*, Wan Zhang, and Yu Zeng

***Abstract*—In this article, an integrated power converter with dc bus voltage boosting capability is proposed for driving the brushless dc motors. In the topology, a bidirectional buck/boost dc–dc (BBD) converter can be integrated with the three-phase voltage-source inverter (TVSI) through a common three-switch leg. As compared with the traditional TVSI with a front-end BBD converter (TVSI-BBD), one power switch and its associate driving circuits in the BBD converter part can be saved. Thus, the integrated power converter has the benefits of reducing the converter size, lowering system costs, and enhancing power density. To decouple the dc bus voltage boosting control and the speed closed-loop control, a field-oriented control algorithm with space vector pulsewidth modulation technique is also proposed. The feasibility of the driving system is evaluated through systematic analysis and validated experimentally on a developed motor drive system prototype.**

***Index Terms*—Brushless dc motor (BLDCM), dc bus voltage boost, field-oriented control (FOC), integrated power converter.**

I. Introduction

DUE to the advantages of high efficiency, high power density, flexible control strategies, and wide range of speed regulation, the brushless dc motors (BLDCM) are widely used in many applications, such as precision servo, electrical tools, aerospace, and electric vehicles (EV) [1].

Power converters play a key role in the BLDCM drive systems, which can make connections of the power source and the BLDCM with matched voltage amplitudes and power flow. Thus, optimal design of the power converter topologies and control algorithms is quite necessary for improving the overall performance of the BLDCM drive systems. Traditionally, the BLDCM can be driven by a conventional three-phase voltage-source inverter (TVSI) with the dc-link cascade connected with the dc source. Generally, the dc source can be an ac–dc rectifier, a solar photovoltaic, or a battery bank. Many power converter topologies have been developed for the BLDCM drives in the past literature [2]–[25].

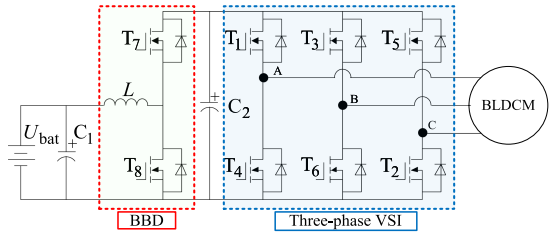

Fig. 1. Front-end BBD converter-based BLDCM drive power converter.

For ac grid powered BLDCM drives, several rectifier topologies are developed for generating the dc-link voltage. Traditionally, the front-end diode bridge rectifier and the large dc-link capacitor are widely used [2], [3]. However, this converter may lead to very low power factor and high total harmonic distortion in the ac-source current. To improve the power quality of the ac mains, many converter topologies with power factor correction (PFC) function are developed in [2]–[7], such as the boost-PFC converter based [2], Cuk converter based [3], Zata converter based [4], bridgeless Cuk and Luo converter based [5], [6], and bridgeless canonical switching cell converter [7].

For solar photovoltaic powered BLDCM drives, the frond-end dc–dc converters [8]–[12], such as buck, boost, buck/boost, Cuk, SEPIC, Zeta, and Luo converters, can be utilized for maximum power point tracking control. To replace the dc–dc converter, the Z-source-based VSI [13], [14] can also be utilized.

For battery powered BLDCM drives, the front-end buck converter [15]–[17] and buck–boost converter [18]–[21] are widely used. In the front-end buck converter-based system, the torque or speed control can be achieved by regulating the dc-link voltage of the VSI, which can improve current/torque performance and reduce copper/iron loss. Thus, this converter structure is more suitable for high-speed BLDCM applications. As shown in Fig. 1, in the traditional TVSI with a front-end bidirectional buck/boost dc–dc (BBD) converter (TVSI-BBD), the dc bus voltage of the TVSI can be boosted, and the bidirectional power flow between the battery and motor drive can be controlled. In this system, the series number of the battery bank can be reduced, and the effects of the battery balance problem can also be alleviated by using the front-end BBD converter. Thus, this system is suitable for battery powered EV applications. However, to construct the additional BBD converter, two more power switches

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and auxiliary drive circuit should be added, which may increase the overall system costs, volume, and complexity. One possible solution is to develop an integrated power converter topology with shared power switches and synthetic control algorithms. In the traditional integrated converter topologies, the three switches can be series connected to construct one three-switch leg. Three three-switch legs can be parallel connected to form a nine-switch converter, which can ensure dual outputs by using the shared middle switch in each three-switch bridge leg. This is a compact and low-cost structure for dual three-phase load systems [22]. In [23] and [24], the compact nine-switch inverters are employed to control a dual-motor drive or dual-stator windings based motor drive. As discussed in [25] and [26], the three-switch leg can also be used for interfacing the dc sources. In [27], a simplified single-phase split-source inverter is proposed with a three-switch leg. This inverter can ensure reduced power switch count, enhanced voltage boost gain, reduced output power filter requirement, and enhanced power efficiency as compared with the traditional topologies. A family of multi-input converters based on the three-switch leg is also developed in [28] and [29], which are capable of applying in renewable energy storage systems. However, no attention has been paid to construct an integrated converter for BLDCM drives.

The main contribution of this article is to develop a compact integrated power converter topology with dc bus voltage boosting capability and its control strategy for a battery powered BLDCM drive. In the proposed converter, a three-switch leg is utilized as a common bridge leg to integrate the BBD converter with the TVSI. As compared with the traditional TVSI-BBD converter, 50% power switches and drive circuits for the dc–dc converter part can be saved. To ensure reliable voltage boosting and speed closed-loop control, the operation of the dc–dc converter part and the three-phase inverter part is decoupled with a novel field-oriented control (FOC) algorithm. To verify the validity of the proposed power converter topology and its control strategy, a rated 60-W BLDCM prototype-based testbed is developed. Detailed principle analysis and experimental results discussion are provided in the following sections.

The rest of this article is organized as follows. In Section II, the proposed power converter topology and the control algorithm are presented. Then, the detailed characteristic analysis of the proposed converter is presented in Section III. In Section IV, the experimental results are discussed in detail. Finally, Section V concludes this article.

II. Topology and Control of the Integrated Converter

A. Topology of the Proposed Converter

As shown in Fig. 2, the proposed converter utilizes a three-switch leg to integrate the BBD converter with one phase bridge leg of the TVSI. With only one additional power switch, the three-switch leg can interface the battery source and the *A*-phase winding simultaneously. As compared with the traditional two-stage topology, as shown in Fig. 1, the proposed topology can save 50% power switches and driving circuits in the dc–dc converter part, which is a benefit for reducing the converter size and improving the power density.

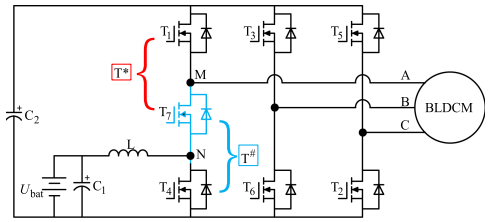

Fig. 2. Integrated power converter for BLDC drives.

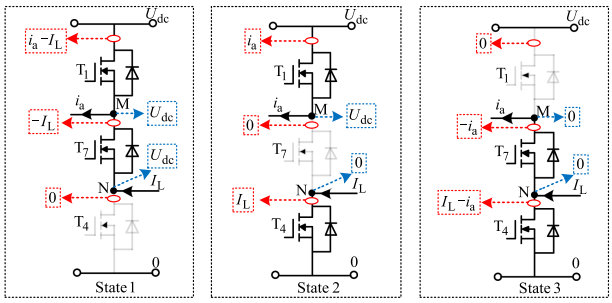

Fig. 3. Operational states of the integrated three-switch leg.

TABLE I
Current Through Each Power Switch and Terminal Voltage at the Three Possible Switching States

State	T_1	T_7	T_4	U_M	U_N	I_{T1}	I_{T7}	I_{T4}
1	On	On	Off	U_{dc}	U_{dc}	i_a- I_L	- I_L	0
2	On	Off	On	U_{dc}	0	i_a	0	I_L
3	Off	On	On	0	0	0	- i_a	I_L- i_a

B. Operational Principle of the Three-Switch Leg

As shown in Fig. 2, the three-switch leg is able to interface the dc source (battery) and ac load (BLDCM drive) through the two terminals *N* and *M*, respectively. To avoid bus voltage shoot through and terminal floating, any two of the three power switches should be turned ON and the third one should be turned OFF. Thus, three possible switching states, as shown in Fig. 3, would be existed. As illustrated in Fig. 3 and Table I, the current flows through each power switch and the terminal voltages of *M* and *N* terminals can be obtained. As can be seen in Fig. 2, if T_1 and T_7 are deemed as a common switch T^*, V_{bat}-*L*-T_4-T^* can construct an equivalent BBD cell to interface the battery source. Similarly, if T_7 and T_4 are deemed as one common switch $T^{\#}$, the T_1-$T^{\#}$ can be considered as an equivalent *A*-phase bridge arm of the TVSI. Thus, if the three-switch leg operates in the three switching states, the BBD cell and the TVSI can be controlled in a decoupled way.

C. Modulation Principle of the Integrated Converter

To avoid error switching states, the modulation process of the three-switch leg should be redesigned. As shown in Fig. 4, the

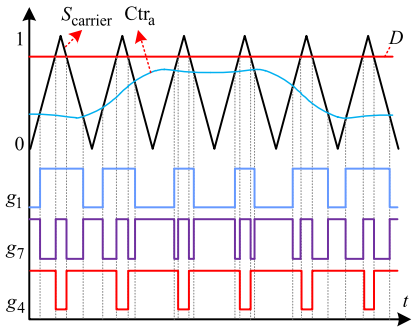

Fig. 4. Principle diagram of the modulation strategies.

A-phase control reference signal of the equivalent three-phase inverter is placed lower than the control reference of the equivalent BBD converter. Based on this constraint, only three switching states, as illustrated in Fig. 3, can be generated, which can ensure the feasible operation of the three-switch leg.

As shown in Fig. 4, the boost duty ratio *D* is placed higher than the BLDCM control reference Ctr_a. Comparing the modulation references with a common triangular carrier signal based on the rules in (1), the driving signals for the upper and lower power switches can be generated as

$$g_1 = \begin{cases} 1 \ (S_{\text{carrier}} \geq Ctr_a) \\ 0 \ (S_{\text{carrier}} < Ctr_a) \end{cases}$$

and

$$g_4 = \begin{cases} 1 \ (D \geq S_{\text{carrier}}) \\ 0 \ (D < S_{\text{carrier}}) \end{cases} \tag{1}$$

where S_{carrier} is the carrier signals; g_1 and g_4 are the gate-driving signals of T_1 and T_4, respectively.

To construct the three switching states, as listed in Table I, the driving signal of the shared switch T_7 is determined by

$$g_7 = \overline{g_1 \ \& \ g_4}. \tag{2}$$

It should be noted here the shared power switch S_7 undergoes twice the number of commutations compared with switches S_1 and S_4 in the same switching period.

Symmetrically, the three-phase control references have a 120° electric angle difference between each other. Thus, the driving signals of the power switches in the *B* and *C* phase legs can be generated with the following logics:

$$g_3 = \overline{g_6} = \begin{cases} 1 \ (S_{\text{carrier}} \geq Ctr_b) \\ 0 \ (S_{\text{carrier}} < Ctr_b) \end{cases}$$

and

$$g_5 = \overline{g_2} = \begin{cases} 1 \ (S_{\text{carrier}} \geq Ctr_c) \\ 0 \ (S_{\text{carrier}} < Ctr_c) \end{cases} \tag{3}$$

where Ctr_b and Ctr_c are the BLDCM control references of phase *B* and *C*, respectively; g_2, g_5, g_3, and g_6 are the gate-driving signals of T_2, T_5, T_3, and T_6, respectively.

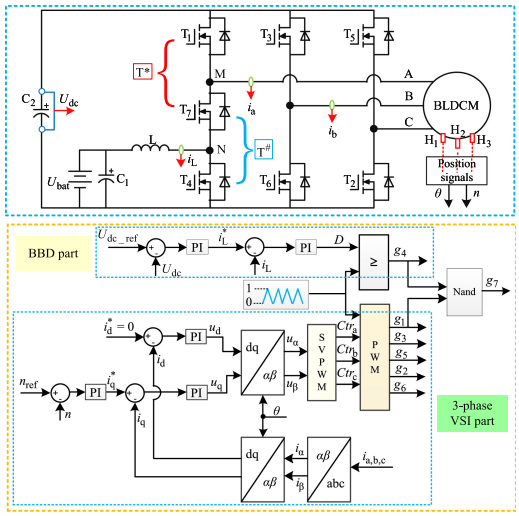

Fig. 5. Control block diagram of the main control strategies.

D. Main Control Algorithm of the Integrated Converter-Based BLDCM Drive

To ensure reliable operation of the integrated converter-based BLDCM drive, the dc bus voltage boosting control and BLDCM driving control should be decoupled with the aforementioned pulsewidth modulation (PWM) modulation scheme. To implement the modulation scheme, the boost duty ratio *D* and the BLDCM control reference Ctr_a–Ctr_c are generated by an FOC algorithm. As shown in Fig. 5, the overall control algorithm consists of the following three parts.

1) *BBD control part*: As can be seen in the converter topology, T_4 and T^* will construct the equivalent BBD converter bridge arm. To control the dc bus voltage, a control configuration with an outer voltage loop plus an inner current loop is selected to generate the modulation reference *D*. Based on the modulation rule, as presented in (1), the gate-driving signals of the power switch T_4 can be generated.
2) *TVSI control part*: In the integrated topology, the T_1-$T^{\#}$, T_3-T_6, and T_5-T_2 will construct the equivalent TVSI for BLDC drive control. In this article, a traditional $i_d = 0$ based FOC algorithm with space vector pulsewidth modulation (SVPWM) technique is developed for BLDCM driving control. As shown in Fig. 5, the direct- and quadrature-axis currents (i_d and i_q) are calculated from the measured two-phase current through *Clark* and *Park* transformations. To ensure reliable rotor speed closed-loop control, an outer rotor speed loop with proportional–integral (PI) regulator is added to generate the current reference i_q^* for tracking. The i_d and i_q are regulated with PI controllers for generating the direct- and quadrature-axis voltages (u_d and u_q). Then, through inverse *Park* transformation, the u_α and u_β can be obtained to perform the SVPWM control. Based on the SVPWM algorithm, the three control references Ctr_a–Ctr_c can be obtained. According to the modulation logics, as presented in (1) and (3), the gate-driving signals for T_1, T_3-T_6, and T_5-T_2 can be obtained.

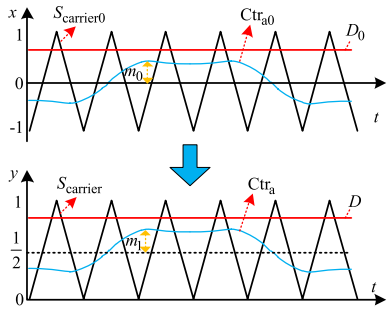

Fig. 6. Linear shift of the modulation and carrier signals.

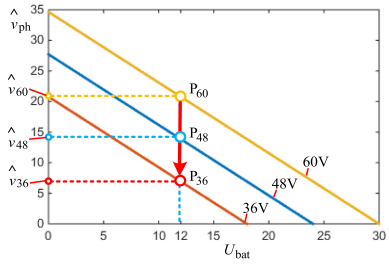

Fig. 7. Boundary line cluster with different dc bus voltages.

3) *Control of the shared power switch* T_7: According to (1), the gate-driving signals of T_1 and T_4 are obtained. Thus, the gate-driving signal of T_7 can be derived by (2) directly.

III. Characteristic Analysis and Discussions

A. Main Control Parameter Analysis

As the boost ratio D should be lower than 1, the maximum magnitude of the Ctr_a–Ctr_c is restricted. Thus, the utilization rate of bus voltage in the integrated converter would be affected. A detailed comparison of the integrated power converter with the traditional TVSI and TVSI-BBD converter is discussed as follows.

1) *Traditional TVSI*: Under the traditional SVPWM control, the maximum peak phase voltage $\hat{v}_{\rm ph}$ can be represented as

$$\hat{v}_{ph\_\max 1} = \frac{1}{\sqrt{3}} U_{\rm dc1} = \frac{1}{\sqrt{3}} U_{\rm bat} \tag{4}$$

where the bus voltage $U_{\rm dc1}$ is equal to the battery voltage $U_{\rm bat}$.

2) *TVSI-BBD converter*: As the front-end BBD converter is added, the maximum peak phase voltage can be represented as

$$\hat{v}_{ph\_\max 2} = \frac{1}{\sqrt{3}} U_{\rm dc2} = \frac{1}{\sqrt{3}} \frac{1}{1-D_1} U_{\rm bat} \tag{5}$$

where $U_{\rm dc2}$ is the bus voltage of the TVSI; D_1 is the boost duty ratio of the front-end BBD converter. As can be seen in (5), the dc bus voltage can be boosted and adjusted with the BBD converter.

3) *Integrated power converter*: In TVSI, the modulation coefficient is defined as

$$m_0 = \frac{\sqrt{3}}{U_{\rm dc}} \hat{v}_{\rm ph}. \tag{6}$$

As illustrated in Fig. 6, the modulation coefficient after linear shift can be expressed as

$$m_1 = \frac{m_0}{2} = \frac{\sqrt{3}\hat{v}_{\rm ph}}{2U_{\rm dc}}. \tag{7}$$

The boost duty ratio D can be expressed by

$$D = 1 - \frac{U_{\rm bat}}{U_{\rm dc}}. \tag{8}$$

According to the modulation principle, the inequality $Ctr_a \leq D$ should be satisfied. Thus

$$D \geq \frac{1}{2} + m_1. \tag{9}$$

According to (7)–(9), the basic relationship among the battery voltage $U_{\rm bat}$, bus voltage $U_{\rm dc}$, and the peak phase voltage $\hat{v}_{\rm ph}$ can be obtained as

$$\hat{v}_{\rm ph} \leq \frac{U_{\rm dc} - 2U_{\rm bat}}{\sqrt{3}}. \tag{10}$$

Based on (5) and (10), to achieve the same maximum peak phase voltage as that in the TVSI-BBD converter, the bus voltage should satisfy the following inequality:

$$U_{\rm dc} \geq \left(2 + \frac{1}{1-D_1}\right) U_{\rm bat} = U_{\rm dc2} + 2U_{\rm bat}. \tag{11}$$

For $0 \leq D_1 < 1$, the minimum boost ratio for the integrated power converter is 3. As can be seen in (11), to obtain the same maximum peak phase voltage as that in the TVSI-BBD converter, the dc bus voltage of the integrated power converter should be higher by a $2U_{\rm bat}$. It is well known that boost converters operate poorly for large values of boost ratio, both in terms of static gain and efficiency. In general application, the boost ratio of the traditional buck/boost dc–dc converter should be lower than 6. Thus, the boost ratio of the integrated converter is within the range [3], [6]. Based on (8), the duty ratio D should be within the range [2/3, 5/6].

If the maximum boost ratio of the integrated converter is 6, it is equivalent to the case in the traditional TVSI-BBD converter with a boost ratio equal to 4. Thus, the integrated converter cannot achieve the same operational performance with the traditional TVSI-BBD converter in an extreme boost ratio. This would be a possible limitation of the integrated converter that needs to be considered.

According to (10), the boundary line clusters for different dc bus voltages 36, 48, and 60 V are parallel lines with a slope of $-2/\sqrt{3}$, which is shown in Fig. 7. As can be seen in this figure, with a fixed battery voltage 12 V, the peak phase voltages, which can be achieved with the integrated converter, are $\hat{v}_{36}$, $\hat{v}_{48}$, and $\hat{v}_{60}$, respectively. The operation performance is equivalent to the TVSI-BBD converter with dc bus voltage 12, 24, and 36 V.

In real application, according to the state of charge of the battery, the terminal voltages of the battery would vary in a certain range (10–15 V in general). Taking $U_{\rm dc} = 60$ V as an example, as shown in Fig. 8, when the battery is discharged, the battery voltage would vary from $U_{\max}$ to $U_{\min}$, and thus, the

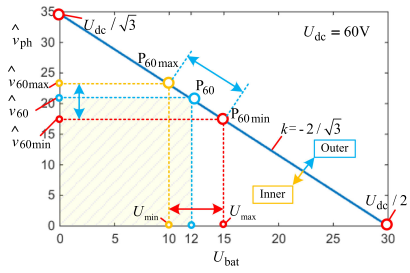

Fig. 8. Bounded operational region considering the variation of battery voltages ($U_{\rm dc} = 60$ V).

maximum operational points of the converter will move from the $P_{60\rm min}$ to $P_{60\rm max}$. The maximum peak phase voltage can then be increased from $\hat{v}_{60\rm min}$ to $\hat{v}_{60\rm max}$ accordingly. Therefore, with the decreasing of battery voltage during the discharge process, the maximum peak phase voltage will increase instead of decreasing. This would be a special feature of the integrated converter.

As can be concluded from (4), (5), and (10), it is clear to see the following differences.

1) The maximum peak voltage in the TVSI will decrease with the decreasing of the battery voltage.
2) In the TVSI-BBD converter, as the dc bus voltage is controlled with a closed-loop controller, the maximum peak phase voltage will not be affected with the decreasing of the battery voltage.
3) The equivalent dc bus voltage provided for the three-phase inverter part in the integrated converter is equal to $U_{\rm dc}-2U_{\rm bat}$, which makes the maximum peak voltage increase during the battery discharging process.

From the point of view of the modulation process, as the battery voltage is decreased, to maintain constant dc bus voltage, the boost duty ratio D should be increased, which can leave space for increasing the BLDCM control reference Ctr_a. Thus, even though the battery voltage is decreased during the discharging process, the integrated converter-based BLDCM drive system can still maintain good speed closed-loop control performance. However, it should be noted here, as compared with the TVSI-BBD converter, to achieve the equivalent BLDCM control performance, that the dc bus voltage of the integrated converter should increase with an additional $2U_{\rm bat}$ voltage. Thus, the increased voltage stresses would be determined by the battery voltage.

B. Analysis and Comparison of Power Losses of the Integrated Converter and TVSI-BBD Converter

For simplicity, only the conduction loss and switching loss of the integrated converter and the TVSI-BBD converter are considered. Some preconditions are set as follows.

1) The BLDCM is controlled under the same load and speed conditions. Thus, the phase current and the equivalent phase voltage are the same in the two converters.
2) The battery-source voltages of the two converters are the same, and the boost duty ratio of the front-end BBD in the TVSI-BBD converter is 0.5.

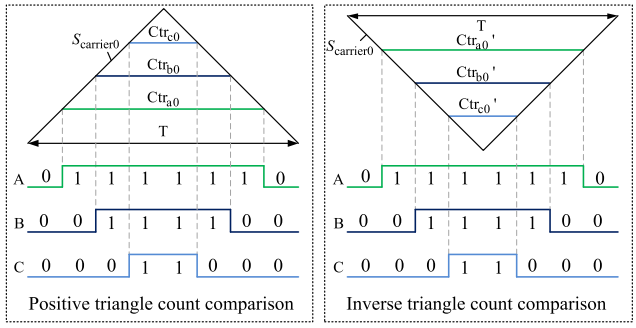

Fig. 9. Principle diagram of the two triangle count comparison methods. Note that: "1" means the upper switch turned ON; "0" means the lower switch turned ON.

3) The $i_d = 0$ based FOC algorithm is used for controlling the BLDCM.
4) The modulation coefficient of the TVSI-BBD converter is $m_2 = 1$.
5) The MOSFET is used as the power switch in this research.

Based on these preconditions, the loss analysis is presented as follows.

1) Basic Modulation Theory: The TVSI modulation coefficients of the two power converters can be represented by

$$\begin{cases} m_2 = \frac{\sqrt{3}}{2U_{\rm bat}}\hat{v}_{\rm ph} \\ m_0 = \frac{(1-D)\sqrt{3}}{U_{\rm bat}}\hat{v}_{\rm ph} \end{cases} \tag{12}$$

where m_2 is the modulation coefficient of the TVSI-BBD converter. When $m_2 = 1$

$$m_0 = 2(1-D). \tag{13}$$

Based on (9) and (13), the boost duty ratio D is within the range [0.75, 1). It should be noted that D is equal to the turn-ON duty ratio of the power switch T_4 in the three-switch leg.

Traditionally, the SVPWM control is equivalent to the SPWM with a third harmonic injection. The amplitude of the third harmonic signal is one-sixth of the sinusoidal reference signal. Thus, the A-phase modulation waveform functions of the two converters ($Ctr_{a0}(t)$ for the integrated power converter and $Ctr_{a2}(t)$ for the TVSI-BBD converter) can be represented by

$$\begin{cases} Ctr_{a2}(t) = \frac{2m_2}{\sqrt{3}}\sin(\omega t) + \frac{m_2}{3\sqrt{3}}\sin(3\omega t) \\ Ctr_{a0}(t) = \frac{2m_0}{\sqrt{3}}\sin(\omega t) + \frac{m_0}{3\sqrt{3}}\sin(3\omega t). \end{cases} \tag{14}$$

According to the modulation waveform, as illustrated in Fig. 6, the upper switch duty ratios of the A-phase leg in the two converters ($g_{a0}(t)$ for the integrated power converter and $g_{a2}(t)$ for the TVSI-BBD converter) can be represented by

$$\begin{cases} g_{a2}(t) = \frac{1-Ctr_{a2}(t)}{2} \\ g_{a0}(t) = \frac{1-Ctr_{a0}(t)}{2}. \end{cases} \tag{15}$$

It should be noted in Fig. 9 the same PWM signals of the traditional three-phase inverter can be generated by both the positive triangle count (PTC) comparison method and inverse triangle count comparison method. However, as shown in Fig. 10, the modulation waveforms of these two count comparison methods have a 180° phase difference. In this article, the PTC method

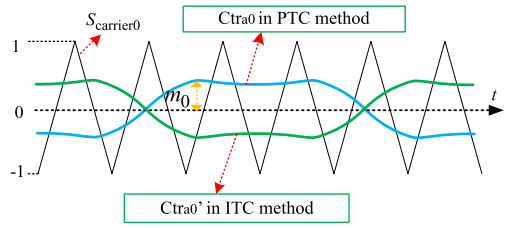

Fig. 10. Modulation waveforms of the two triangle count comparison methods.

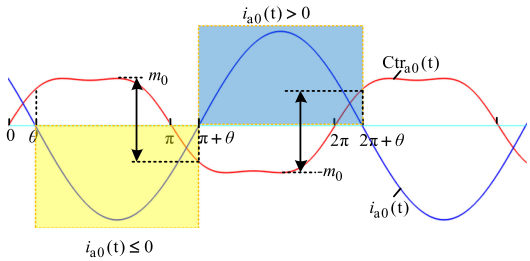

Fig. 11. Relationship between the phase current and the modulation waveform.

is used. In PTC-based SVPWM control, the phase voltage is inversed to the modulation waveform. Thus, if the phase current lags behind the phase voltage by a phase angel θ, the phase currents can be represented by

$$i_a = I_m \sin(\omega t + \pi + \theta). \tag{16}$$

The relationship between the modulation waveform and the phase current is shown in Fig. 11. As can be seen in this figure, when $i_a > 0$

$$-m_0 < Ctr_{a0}(t) < \frac{2m_0}{\sqrt{3}} \sin(\theta) + \frac{m_0}{3\sqrt{3}} \sin(3\theta) \tag{17}$$

and when $i_a \le 0$, there is

$$-\frac{2m_0}{\sqrt{3}} \sin(\theta) - \frac{m_0}{3\sqrt{3}} \sin(3\theta) \le Ctr_{a0}(t) \le m_0. \tag{18}$$

Based on (13) and (15), the range of the duty ratio $g_{a0}(t)$ can be determined as

$$\begin{cases} D - \frac{1}{2} \le g_{a0}(t) \le \frac{1}{2} + \frac{2(1-D)}{\sqrt{3}} [\sin(\theta) + \frac{1}{6} \sin(3\theta)] (ia \le 0) \\ \frac{1}{2} - \frac{2(1-D)}{\sqrt{3}} [\sin(\theta) + \frac{1}{6} \sin(3\theta)] < g_{a0}(t) < \frac{3}{2} - D (ia > 0). \end{cases} \tag{19}$$

2) Relationship Between the Input and Output Powers: According to the energy conservation law, the output power of the battery source should be equal to the sum of converter power loss and motor input power. Thus

$$U_{\text{bat}} I_L = P_{loss} + 3\hat{v}_{\text{ph}} I_m \cos\theta \tag{20}$$

where the converter power loss $P_{\text{loss}} \ge 0$. Thus, based on (12) and (13), (20) can be represented as

$$U_{\text{bat}} I_L = P_{loss} + 2\sqrt{3} U_{\text{bat}} I_m \cos\theta \ge 2\sqrt{3} U_{\text{bat}} I_m \cos\theta. \tag{21}$$

Thus

$$I_m \le \frac{I_L}{2\sqrt{3}\cos\theta}. \tag{22}$$

To simplify the loss analysis, the power factor angle θ within [0, π/6] is used for analysis in this article. Thus

$$I_m \le \frac{I_L}{3}. \tag{23}$$

3) Conduction and Switching Losses Calculation for MOSFET—Basic Theory: In this article, the MOSFET is used as the power switch. In SVPWM control, the upper and lower power switches of each phase leg are conducted complementary, which makes the converter to operate under synchronous rectifying mode. Thus, the freewheeling current will flow through the MOSFET in the inverse direction due to its bidirectional conductivity in synchronous rectifying modes. Thus, the conduction loss of the MOSFET can be represented by

$$P_{\text{on}} = D_{\text{on}} {I_{\text{on}}}^2 R_{\text{on}} \tag{24}$$

where P_{on} is the conduction loss of one power switch, D_{on} is the conduction duty ratio, I_{on} is the average conduction current, and R_{on} is the equivalent conduction resistor of the MOSFET.

The switching loss P_{sw} is composed of turn-ON loss P_{son} and turn-OFF loss P_{soff}

$$P_{\text{sw}} = P_{\text{son}} + P_{\text{soff}} = \frac{1}{2} V_{DS} I_d (t_{\text{on}} + t_{\text{off}}) f_s \tag{25}$$

where V_{ds} is the drain-to-source voltage, I_d is the drain current, f_s is the switching frequency, t_{on} is the sum of the turn-ON delay time and the turn-ON rise time, and t_{off} is the sum of turn-OFF delay time and the turn-OFF falling time.

4) Comparison of the Conduction Loss of the Two Converters: In the BBD part of the TVSI-BBD converter, the turn-ON duty ratio of the lower switch is 0.5. Thus, the conduction losses of the upper and lower switches are equal, which can be represented by

$$P_{on7} = P_{on8} = 0.5 {I_{L2}}^2 R_{\text{on}} \tag{26}$$

where I_{L2} is the inductor current.

In the TVSI part, the conduction losses of the upper switches are equal, which can be calculated as

$$P_{on1} = P_{on3} = P_{on5} = \frac{1}{T_s} \int_0^{T_s} g_{a2}(t) {i_a}^2 R_{\text{on}} dt \tag{27}$$

and the conduction losses of the lower switches are

$$P_{on2} = P_{on4} = P_{on6} = \frac{1}{T_s} \int_0^{T_s} [1 - g_{a2}(t)] {i_a}^2 R_{\text{on}} dt \tag{28}$$

where T_s is a phase current period time of the BLDCM. Thus, the overall conduction losses of the TVSI-BBD converter P_{con2} is

$$P_{\text{cond2}} = {I_{L2}}^2 R_{\text{on}} + \frac{3}{T_s} \int_0^{T_s} {i_a}^2 R_{\text{on}} dt. \tag{29}$$

In the integrated power converter, the conduction loss can be separated into two parts: the conduction loss of *B* and *C* phase legs and the conduction loss of the three-switch leg.

In *B* and *C* phase legs, the conduction loss of the upper switches can be represented by

$$P_{on3} = P_{on5} = \frac{1}{T_s} \int_0^{T_s} g_{a0}(t) {i_a}^2 R_{\text{on}} dt \tag{30}$$

and the conduction losses of the lower switches can be represented by

$$P_{on2} = P_{on6} = \frac{1}{T_s}\int_0^{T_s} [1 - g_{a0}(t)] {i_a}^2 R_{\rm on} dt. \tag{31}$$

In the three-switch leg, the conduction losses can be calculated according to the switching states' manner, as illustrated in Fig. 3. The conduction losses of the three switches T_1, T_7, and T_4 can be represented as

$$\begin{cases} P_{on1} = \frac{R_{\rm on}}{T_s}\int_0^{T_s} [(i_a - I_L)^2(1 - D_{\rm T4}) + {i_a}^2(1 - D_{\rm T7})] dt \\ P_{on7} = \frac{R_{\rm on}}{T_s}\int_0^{T_s} [{I_L}^2(1 - D_{\rm T4}) + {i_a}^2(1 - D_{\rm T1})] dt \\ P_{\rm on4} = \frac{R_{\rm on}}{T_s}\int_0^{T_s} [(I_L - i_a)^2(1 - D_{\rm T1}) + {I_L}^2(1 - D_{\rm T7})] dt \end{cases} \tag{32}$$

where $D_{\rm T1}$, $D_{\rm T4}$, and $D_{\rm T7}$ are the turn-ON duty ratio of the three switches. The $D_{\rm T4}$ is equal to the boost duty ratio D. Based on the switching states' distribution of the three-switch leg, the three duty ratios satisfy the following relationship:

$$\begin{cases} (1 - D_{\rm T1}) + (1 - D_{\rm T7}) + (1 - D_{\rm T4}) = 1 \\ D_{\rm T1} = g_{a0}(t) \\ 0.75 \le D_{\rm T4} = D \le 1. \end{cases} \tag{33}$$

Thus, the overall conduction losses of the three-switch leg can be represented by

$$P_{on1+4+7} = \frac{R_{\rm on}}{T_s}\int_0^{T_s} \begin{matrix}[(I_L - i_a)^2(2 - D - g_{a0}(t)) \\ +{I_L}^2 g_{a0}(t) + {i_a}^2 D] dt.\end{matrix} \tag{34}$$

Based on (29), (30), (31), and (34), the conduction loss power difference between the integrated converter and the TVSI-BBD converter can be expressed as

$$\Delta_{cd} = \frac{R_{\rm on}}{T_s}\int_0^{T_s} \begin{matrix}\{[(I_L - i_a)^2(2 - D - g_{a0}(t)) + {I_L}^2 g_{a0}(t) \\ +{i_a}^2 D] - {I_{L2}}^2 - {i_a}^2\} dt.\end{matrix} \tag{35}$$

As the phase current is a sinusoid signal, when i_a>0, there is

$$\begin{cases} \frac{2}{T_s}\int_0^{T_s/2} {i_a}^2 dt = \frac{{I_m}^2}{2} \\ \frac{2}{T_s}\int_0^{T_s/2} i_a dt = \frac{2I_m}{\pi}. \end{cases} \tag{36}$$

And when $i_a \le 0$, there is

$$\begin{cases} \frac{2}{T_s}\int_0^{T_s/2} {i_a}^2 dt = \frac{{I_m}^2}{2} \\ \frac{2}{T_s}\int_0^{T_s/2} i_a dt = -\frac{2I_m}{\pi}. \end{cases} \tag{37}$$

Taking $\theta = \pi/6$ for an example, when i_a>0, based on (19), (23), (35), and (36), the maximum value of Δ_{cd} can be obtained as

$$\Delta_{cdH} = R_{\rm on}\left[(2 - D){I_L}^2 + \frac{(D - 0.5){I_m}^2}{2} - \frac{2I_m I_L}{\pi} - {I_{L2}}^2\right] \tag{38}$$

and the minimum value of Δ_{cd} is

$$\Delta_{cdL} = R_{\rm on}\left[(2 - D){I_L}^2 + (0.25 + \frac{2 - 2D}{3\sqrt{3}}){I_m}^2 - \frac{18\sqrt{3} + 16 - (16 + 12\sqrt{3})D}{3\sqrt{3}\pi} I_m I_L - {I_{L2}}^2\right]. \tag{39}$$

TABLE II
SPECIFICATIONS OF THE INTEGRATED POWER CONVERTER

Items	Parameter rating
Battery	12V20AH Lead-acid battery
Power switch	MOSFET AOT410, 100V/150A, Ron<6.5mΩ
Inductor	3mH, 10A
Capacitor	1000μF
BLDCM and load machine	60W/24V/3000 r/min
Load resistor	10Ω/200W

In (38) and (39), it is clear that Δ_{cdH} and Δ_{cdL} are monotony decrease functions of the duty ratio D. Thus, when $D = 0.75$, the Δ_{cdH} and Δ_{cdL} reach their maximum values

$$\begin{cases} \Delta_{cdH\max} = R_{\rm on}(1.25{I_L}^2 - {I_{L2}}^2 + 0.125{I_m}^2 - 0.637 I_m I_L) \\ \Delta_{cdL\min} = R_{\rm on}(1.25{I_L}^2 - {I_{L2}}^2 + 0.346{I_m}^2 - 1.2 I_m I_L). \end{cases} \tag{40}$$

In (40), $\Delta_{cdH\max}$ and $\Delta_{cdL\min}$ are monotony decrease functions of the duty ratio I_m. Thus

$$\begin{cases} R_{\rm on}(1.05{I_L}^2 - {I_{L2}}^2) \le \Delta_{cdH\max} \le R_{\rm on}(1.25{I_L}^2 - {I_{L2}}^2) \\ R_{\rm on}(0.89{I_L}^2 - {I_{L2}}^2) \le \Delta_{cdL\min} \le R_{\rm on}(1.25{I_L}^2 - {I_{L2}}^2). \end{cases} \tag{41}$$

Similarly, when $i_a \le 0$, the maximum value of Δ_{cd} can be obtained as

$$\Delta_{cdH} = R_{\rm on}\left[(2 - D){I_L}^2 + (0.75 - 0.5D){I_m}^2 + \frac{10 - 8D}{\pi} I_m I_L - {I_{L2}}^2\right] \tag{42}$$

and the minimum value of Δ_{cd} is

$$\Delta_{cdL} = R_{\rm on}\left[(2 - D){I_L}^2 + (0.25 - \frac{2 - 2D}{3\sqrt{3}}){I_m}^2 + \frac{18\sqrt{3} - 16 - (12\sqrt{3} - 16)D}{3\sqrt{3}\pi} I_m I_L - {I_{L2}}^2\right]. \tag{43}$$

Thus, when $i_a \le 0$ and $D = 0.75$

$$\begin{cases} \Delta_{cdH\max} = R_{\rm on}[1.25{I_L}^2 + 0.375{I_m}^2 + 1.274 I_m I_L - {I_{L2}}^2] \\ \Delta_{cdL\min} = R_{\rm on}[1.25{I_L}^2 + 0.154{I_m}^2 + 0.71 I_m I_L - {I_{L2}}^2]. \end{cases} \tag{44}$$

In (44), $\Delta_{cdH\max}$ and $\Delta_{cdL\min}$ are monotony increase functions of the duty ratio I_m. Thus

$$\begin{cases} R_{\rm on}(1.25{I_L}^2 - {I_{L2}}^2) \le \Delta_{cdH\max} \le R_{\rm on}[1.72{I_L}^2 - {I_{L2}}^2] \\ R_{\rm on}(1.25{I_L}^2 - {I_{L2}}^2) \le \Delta_{cdL\min} \le R_{\rm on}[1.5{I_L}^2 - {I_{L2}}^2]. \end{cases} \tag{45}$$

In real cases, as compared with the input power from the battery source, the conduction loss is quite lower so that the inductor currents of the two converters would be very close. Thus, based on (41) and (45), it is clear that the conduction loss of the integrated converter is higher in the negative current half cycle. But in the positive current half cycle, the conduction losses of the integrated converter are comparable with the TVSI-BBD converter or even lower.

5) Comparison of the Switching Loss of the Two Converters: Based on (25), the switching loss of the TVSI-BBD converter can be represented by

$$\sum P_{sw2} = U_{\mathrm{dc2}} I_{L2}(t_{\mathrm{on}} + t_{\mathrm{off}}) f_s + \frac{3}{T_s}\int_0^{T_s} U_{\mathrm{dc2}} |i_a| (t_{\mathrm{on}} + t_{\mathrm{off}}) f_s dt. \quad (46)$$

In the integrated converter, the switching loss of the power switches T_3, T_6, T_5, and T_2 is equal. The sum of them can be represented by

$$P_{s3+s6+s5+s2} = \frac{1}{2T_s}\int_0^{T_s} U_{\mathrm{dc}} |i_a| (t_{\mathrm{on}} + t_{\mathrm{off}}) f_s dt. \quad (47)$$

In the three-switch leg, the switching loss of the three switches can be expressed as

$$\begin{cases} P_{s1} = \frac{1}{2T_s}\int_0^{T_s} U_{\mathrm{dc}} |i_a| (t_{\mathrm{on}} + t_{\mathrm{off}}) f_s dt \\ P_{s4} = \frac{1}{2} U_{\mathrm{dc}} I_L (t_{\mathrm{on}} + t_{\mathrm{off}}) f_s \\ P_{s7} = P_{s4} + P_{s1}. \end{cases} \quad (48)$$

Thus, the overall switching loss of the integrated power converter can be calculated as

$$\sum P_{\mathrm{sw}} = U_{\mathrm{dc}} I_L (t_{\mathrm{on}} + t_{\mathrm{off}}) f_s + \frac{3}{T_s}\int_0^{T_s} U_{\mathrm{dc}} |i_a| (t_{\mathrm{on}} + t_{\mathrm{off}}) f_s dt. \quad (49)$$

According to (11), the switching loss power difference between the integrated converter and the TVSI-BBD converter can be expressed as

$$\Delta_{\mathrm{SW}} = [U_{\mathrm{dc2}}(I_L - I_{L2}) + 2U_{\mathrm{bat}} I_L](t_{\mathrm{on}} + t_{\mathrm{off}}) f_s + \frac{3}{T_s}\int_0^{T_s} 2U_{\mathrm{bat}} |i_a| (t_{\mathrm{on}} + t_{\mathrm{off}}) f_s dt. \quad (50)$$

As the bus voltage should be higher by at least a $2U_{\mathrm{bat}}$ voltage in the integrated converter, the switching losses would be increased accordingly. As the inductor currents I_L and I_{L2} are very close, the switching loss difference in (51) is only determined by the battery voltage. But as the battery voltage is fixed, the proportion of Δ_{sw} (the switching loss difference of the two converters) in $\sum P_{SW2}$ (the switching loss of the TVSI-BBD converter) will decrease with the increasing of the dc bus voltage of the TVSI-BBD converter. Thus, in the applications with high boost ratio, the effects due to the increased switching loss in the integrated converter can be lowered.

IV. Experimental Results

To verify the validity of the integrated power converter and its control strategies, the experiments have been performed on a rated 60 W BLDCM drive system. The specifications of the integrated power converter are listed in Table II and the overall testbed is shown in Fig. 12.

In the test system, a 12 V/20AH lead-acid battery is used as the power source, and the integrated power converter is built with discrete MOSFET power switches. To construct the load system, two identical BLDCMs are series connected with an elastic shaft coupling. In this structure, one BLDCM is used as the propulsion motor and the other one will operate as a generator to mimic the load machine. The three-phase winding terminals of the load machine are connected to a three-phase diode bridge-based rectifier. The load can be adjusted with the increasing or decreasing of power resistors. The dc bus voltage and two-phase currents are measured with sensors and related conditional circuits. The overall control algorithms of the proposed BLDCM driving systems are implemented in a TMS320F28335 digital signal processor. The detailed experimental results are discussed as follows.

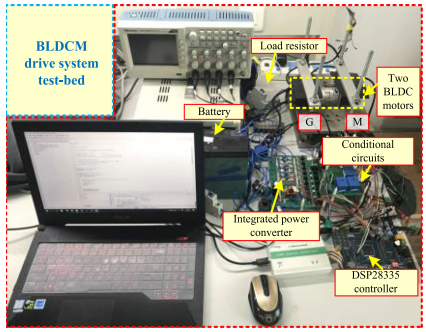

Fig. 12. Testbed of the integrated BLDCM drive system.

The experiment begins with the evaluation of the basic modulation strategies. According to (10) and (11), to achieve equal or higher maximum peak voltage as that in the TVSI-BBD converter with 24V dc bus voltage, in the experiments, the $U_{\mathrm{dc}} = 48$ V and $U_{\mathrm{dc}} = 60$ V are selected for testing. Based on the control block diagram, as shown in Fig. 5, the control of the integrated BBD converter and the TVSI are coupled by controlling the shared power switch T_7. For the integrated dc–dc part, the outer dc bus voltage and inner inductance current-based double closed-loop control strategy is used for generating the boost duty ratio D. And the integrated TVSI is controlled with the $i_d = 0$ based FOC algorithm with SVPWM technique, which can generate the three-phase modulation reference Ctr_a–Ctr_c.

As can be seen in Fig. 13(a) and (b), the boost duty ratio D remains around 0.75 at both 1500 and 2500 r/min, which can ensure a four times voltage boosting. Although the magnitudes of the three-phase modulation references increase with the rising of the rotor speed, they still remain lower than D, which can ensure stable modulation process. Similarly, the cases with $U_{\mathrm{dc}} = 60$ V is also tested at both 1500 and 2500 r/min. As can be seen in Fig. 13(c) and (d), D is around 0.8, which remains higher than Ctr_a–Ctr_c at both 1500 and 2500 r/min. Therefore, the dc bus voltage can be boosted to 60 V reliably. Comparing Fig. 13(a) and (c) or (b) and (d), it is clear that the space between D and the peak value of Ctr_a–Ctr_c can be widen by increasing the reference dc bus voltage, which is in agreement with the boundary line cluster analysis, as illustrated in Fig. 7.

Based on the switching rules, as given in (1) and (3), the gate-driving signals of T_1, T_4, T_2, T_5, T_3, and T_6 can be obtained. To ensure reliable operation of the common three-switch leg, the gate-driving signal of the shared switch T_7 can also be generated by (2). The tested gate-driving signals of the three-switch leg

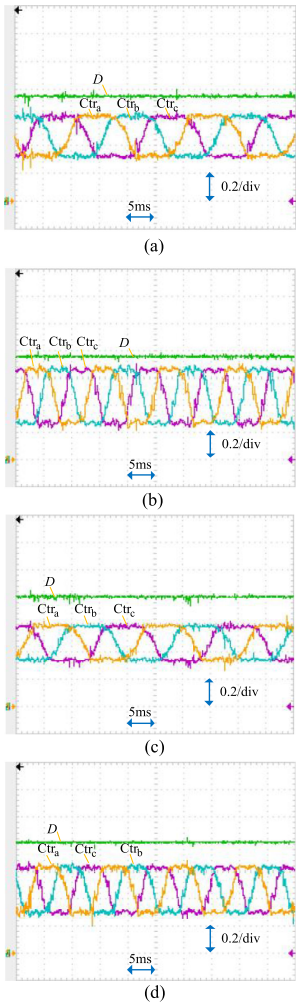

Fig. 13. Modulation waves of the integrated converter under different dc bus voltages and rotor speeds. (a) $U_{\rm dc} = 48$ V; 1500 r/min. (b) $U_{\rm dc} = 48$ V; 2500 r/min. (c) $U_{\rm dc} = 60$ V; 1500 r/min. (d) $U_{\rm dc} = 60$ V; 2500 r/min.

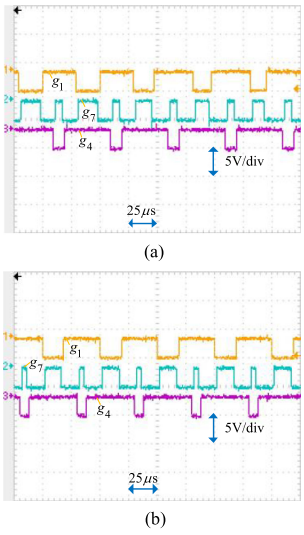

Fig. 14. Gate-driving signals of the common three-switch leg. (a) $U_{\rm dc} = 48$ V. (b) $U_{\rm dc} = 60$ V.

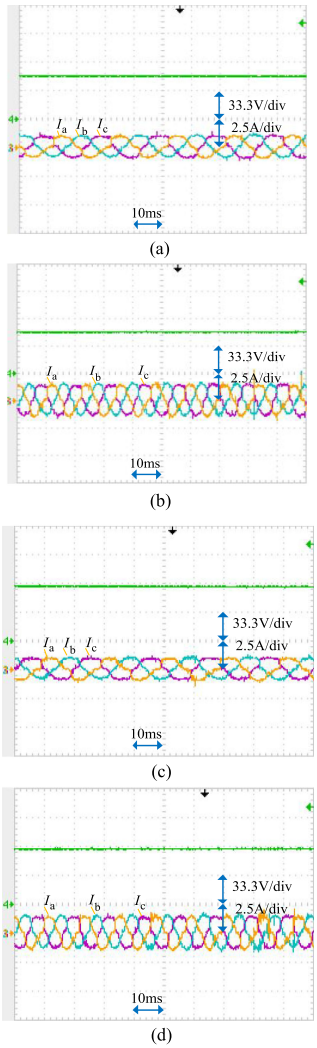

Fig. 15. Three-phase currents and dc bus voltage at steady-state operation under different dc bus voltages and rotor speeds. (a) $U_{\rm dc} = 48$ V; 1500 r/min. (b) $U_{\rm dc} = 48$ V; 3000 r/min. (c) $U_{\rm dc} = 60$ V; 1500 r/min. (d) $U_{\rm dc} = 60$ V; 3000 r/min.

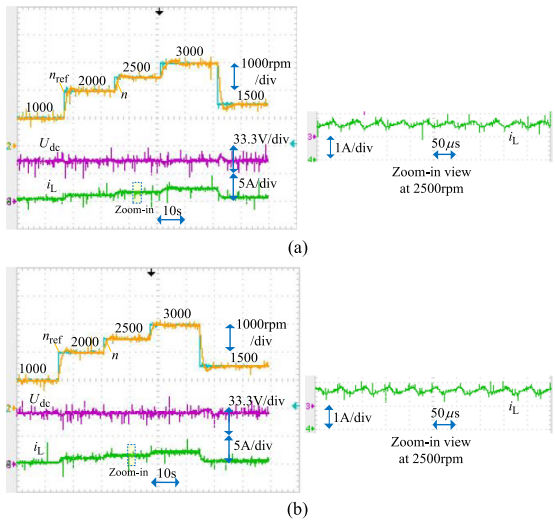

Fig. 16. Speed tracking performance under different speed references and dc bus voltages. (a) $U_{\rm dc} = 48$ V. (b) $U_{\rm dc} = 60$ V.

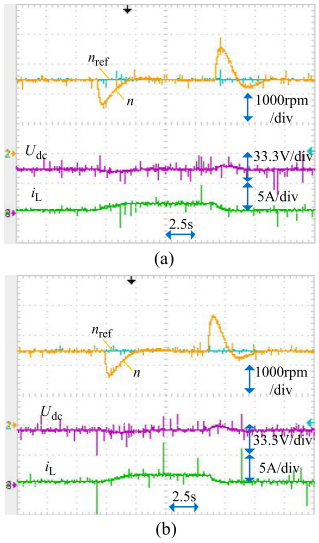

Fig. 17. Speed tracking performance with load mutations at different dc bus voltages. (a) $U_{\rm dc} = 48$ V. (b) $U_{\rm dc} = 60$ V.

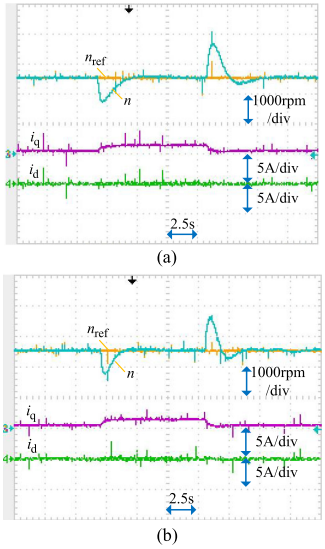

Fig. 18. i_d and i_q waveforms during load mutations at different dc bus voltages. (a) $U_{\rm dc} = 48$ V. (b) $U_{\rm dc} = 60$ V.

under $U_{\rm dc} = 48$ V and $U_{\rm dc} = 60$ V are shown in Fig. 14(a) and (b), respectively. As can be seen in these figures, except for the dead time, there are two power switches turned ON and one power switch turned OFF at any instant, which satisfy the basic modulation principle of the three-switch leg, as illustrated in Fig. 4.

According to the control algorithm, as illustrated in Fig. 5, the steady operation states at 1500 and 2500 r/min are tested in experiments. As shown in Fig. 15(a) and (b), the dc bus voltage can be regulated to maintain the reference value 48 V, and the three-phase currents of the BLDCM are controlled to be sinusoidal stably by the proposed integrated control strategies. Similar results with $U_{\rm dc} = 60$ V are also shown in Fig. 15(c) and (d).

To verify the dynamic operation capability of the proposed BLDCM drive system, the speed closed-loop transition process under different reference speeds is also tested. The cases with $U_{\rm dc} = 48$ V and $U_{\rm dc} = 60$ V are shown in Fig. 16(a) and (b), respectively. As can be seen in these figures, the rotor speed can track the reference values rapidly under sudden speed changes. Both in the steady states and the speed transition instants, the dc bus voltage can be regulated to the references reliably.

Furthermore, the operation performance with load mutations at different dc bus voltages is also tested in the proposed system. As shown in Fig. 17(a) and (b), when a 10 Ω load power resistor is suddenly added and removed from a three-phase diode bridge-based rectifier, the dc bus voltage can still be stably controlled to reference value 48 V and 60 V, respectively. The changes of the i_d and i_q in the FOC algorithm are illustrated in Fig. 18. As can be seen in this figure, with the $i_d = 0$ based FOC algorithm, the load changes can be handled by adjusting the i_q value. Based on the proposed modulation and control strategy, the rotor speed can also be regulated to track the reference (2500 r/min here as an example) reliably, even under sudden load mutations.

V. Conclusion

An integrated power converter and its control strategy is proposed for driving the BLDCM drives. Detailed analysis is discussed, and experimental results are provided for verification, which indicate that the proposed converter-based BLDCM drive system has the following features.

1) A three-switch leg is utilized for achieving the integration of the BBD converter and the TVSI, which can ensure the benefits of reducing the converter size, lowering system costs, and enhancing power density.
2) The proposed FOC algorithm with SVPWM technique can ensure stable dc bus voltage boosting and speed closed-loop control even under speed transitions and sudden load mutations.
3) Although the battery voltage is decreased during the discharging process, the integrated converter-based BLDCM drive system can still maintain good speed closed-loop control performance.
4) As compared with the TVSI-BBD converter, the dc bus voltage of the integrated converter has a $2U_{\rm bat}$ increase. Thus, an additional $2U_{\rm bat}$ voltage stresses would be increased in the drive system. In addition, the increased switching loss is only determined by the battery voltage. With the increase of the boost ratio, the effects due to the increased switching loss can be lowered.

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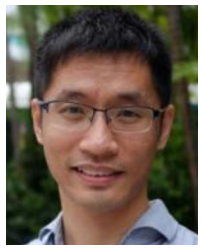

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