An IGBT Current Boosting Method by Using Ultrahigh Driving-Voltage in HVdc Circuit Breaker Applications

Jingfei Wang, Guishu Liang, Xiangyu Zhang, Lei Qi, and Lvyang Chen

***Abstract*—High-voltage direct current (HVdc) circuit breakers based on power electronic technology usually require a large number of insulated-gate bipolar transistors (IGBTs) to achieve large-capacity breaking. The insufficient current capacity is an important reason for the excessive cost of dc circuit breakers. However, the single switching condition in the circuit breaker makes it possible for IGBTs to control the current of several times rated value in a short time. This article proposed an effective current boosting method for IGBT. By applying an unconventionally ultrahigh driving-voltage (UDV) to the gate of devices, the instantaneous current capability of IGBTs can be significantly improved. The possible failure modes and lifetime issues caused by UDV are also discussed in detail. Through comprehensive theoretical calculations and experimental analysis, a proper UDV selection principle for IGBTs in HVdc circuit breakers is proposed. The single device is verified to have the ability to control 31.2 kA current in milliseconds by using UDV. This conclusion can greatly increase the allowable working area of IGBTs, thereby significantly reducing the cost of HVdc circuit breakers.**

***Index Terms*—Current capacity, high-voltage direct current circuit breaker (DCCB), ultrahigh driving-voltage (UDV).**

I. Introduction

HYBRID high-voltage direct current circuit breakers (DCCBs) are the key equipment to remove faults in high voltage direct current transmission (VSC-HVdc) system [1]–[5]. In 2012, ABB proposed a fully controlled hybrid high-voltage DCCB topology. A small number of IGBT devices are used in the main branch to form an auxiliary commutation switch and a fast switch. The transfer branch is formed by a large number of IGBTs connected in series [6]. In 2013, ALSTOM proposed a hybrid DCCB based on thyristor [7]. The power semiconductor devices are thyristor and configure the corresponding arrester according to the voltage level. In 2014, the China Global Energy Interconnection Research Institute developed a 200 kV H-full bridge unit prototype DCCB capable of breaking 15 kA short-circuit current within 3 ms, and successfully applied in the China Zhoushan flexible dc transmission project [6]. In 2019, based on diode full bridge construction proposed by Tsinghua University [8], a DCCB prototype with a rated voltage of 535 kV, a breaking current of 25 kA within 3 ms was proposed. This design was practically applied in China Zhangbei flexible dc transmission project in 2019 [3]. In summary, the DCCB presents a development trend of high operating voltage and larger breaking current. At the same time, in order to meet the needs of higher voltage and current levels, the number of devices used in DCCBs is increasing. Table I presents the basic information of the above-mentioned hybrid DCCBs.

TABLE I
DEVELOPMENT OF HYBRID DCCBS

Country	Switzerland	France	China	China
Rated Voltage	80 kV	120 kV	200 kV	535 kV
Transfer branch composition	IGBT series	Bidirectional Thyristor	H-full bridge	Diode bridge
Transfer branch device	IGBT	Thyristor	IGBT	IGBT
Transfer branch device quantity	20×4	10×8	128×4	320×2
Transfer branch current	9 kA	7.5 kA	15 kA	25 kA
Single device current	9 kA (3 p.u.)	7.5 kA (5 p.u.)*	7.5 kA (2.5 p.u.)*	12.5 kA (4.2 p.u.)*

Note: p.u.—device rated current value.
*Use two parallel devices to withstand peak current stress.

As can be seen from Table I, higher current and voltage levels will bring overcurrent and overvoltage problems. At present, the research focus is mainly on reducing the overvoltage of the device (such as snubber circuit [8], low-stray inductance design [9], and soft turn-OFF control strategy [10]), reducing the dynamic avalanches caused by stray inductance [11], which greatly improves the reliability of the device when it is turned OFF, but it lacks enough research for the upper limit current capacity of the device when it is turned ON. Meanwhile, the maximum current capacity of a single device in mainstream DCCB projects is generally about 10 kA, which is generally

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3–5 times of its own rated current value. In order to obtain larger current capacity, it is generally through the use of parallel devices. Taking Zhangbei HVdc Flexible Transmission Project as an example [3], considering a certain safety margin, the design of the Zhangbei DCCB uses two parallel devices to turn-ON and turn-OFF 25 kA (4–5 times rated current value) fault current. At the same time, for the lifetime of the device itself and safety considerations, the gate driving voltage usually does not exceed the limit given in the device manufacturer's datasheet.

However, parallel devices have problems, such as high economic costs and harmonization of drivers. A lower gate driving voltage will also prolong the ON-state time of the device, resulting in higher ON-state temperature rise. At the same time, in the application of DCCBs, there are papers showing that the device has stronger robustness in single pulse applications [12]–[14], making the application of the device in DCCBs more possible. Therefore, in the application of DCCBs, it is necessary to discuss whether the devices can achieve larger current capacity. If a single device can be used to turn-ON and turn-OFF more than ten times the device rated current value, it can not only solve the reliability problem caused by the parallel connection of devices but also greatly reduce the construction economic cost of the DCCBs.

This article proposed a method of using ultra-high driving-voltage (UDV, much higher than the driving voltage manufacturers recommend) to boost the device's current capacity. By using UDV, it is possible to use a single device (rated current value 3 kA) to turn-ON and turn-OFF the current of 31.2 kA (10.4 times rated current value), meanwhile, make the device not breakdown and the lifetime loss of the device within an acceptable range. To achieve this goal, this article mainly carried out the following works.

The rest of this article is organized as follows. Section II mainly introduces the implementation method of UDV, and analyzes the possible benefits and problems brought by UDV. In Section III, this article analyzes the boost of current capacity by UDV. In Section IV, this article analyzes the impact of UDV on device lifetime. In Section V, the experiment of a single IEGT (a type of IGBT, rated current value 3 kA) device was used to successfully turn-ON and turn-OFF the current of 31.2 kA (10.4 times rated current value) by UDV, which achieved the goal proposed in this article. Finally, Section VI concludes this article.

II. Current Boosting Method By UDV(Ultra Driving-Voltage)

A. Characteristics of Single Pulse Operating Conditions

As shown in Fig. 1(a) and (b), compared with the voltage-source converter applications that IGBT is often used in, the IGBT under the DCCB applications mainly has the following characteristics in the whole process: Compared with the periodic pulse condition of the converter, single pulse applications' ON-state time is longer, gate driving voltage is higher, ON-state temperature is higher, and the current is larger.

The segment timing of the hybrid high-voltage DCCB and its corresponding current waveform are also shown in Fig. 1. First, the power system is in the rated operating state. When the system

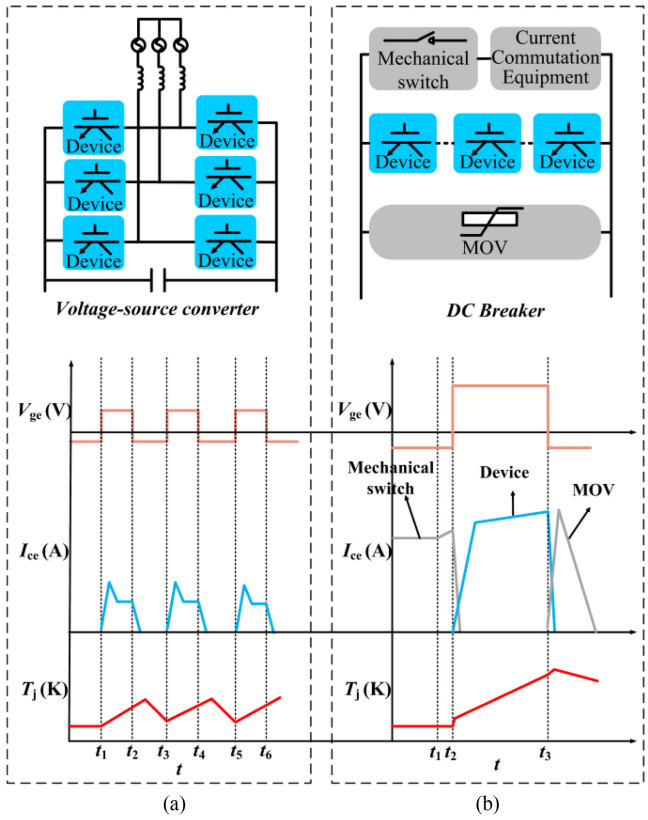


Fig. 1. Characteristics of periodic pulse and single pulse. (a) Periodic pulse. (b) Single pulse.

fails, after a certain fault detection time, the IGBT in the power electronic module of the main branch is blocked, and the current starts to commutate from the main branch to the transfer branch. After that, the first commutation ends and the mechanical switch starts to open. Then, the mechanical switch reaches a sufficient distance to withstand the transient voltage, locks the IGBT of the power electronic module of the transfer branch, and commutates the current to the buffer branch connected in parallel at both ends of the IGBT, and the voltage at both ends of the circuit breaker starts to rise rapidly. When it reaches the operating voltage of the MOV, the fault current starts to commutate to the MOV branch. Finally, the MOV cuts off the fault current, and the DCCB completes the breaking of the fault current.

B. UDV Method Proposed

In the existing high-voltage DCCBs, the gate driving voltage is generally set to be slightly higher than the value recommended by the manufacturer's datasheet (15 V), and a certain gate driving voltage value is usually selected according to the needs of the project but generally does not exceed the maximum value given by the manufacturer's datasheet. This is mainly based on the long-term reliability of the device. However, a large number of papers and experiments show that IGBT has extremely strong robustness under single pulse applications [12]–[14], and the total gate stress time under the DCCB application conditions is usually relatively short. In some

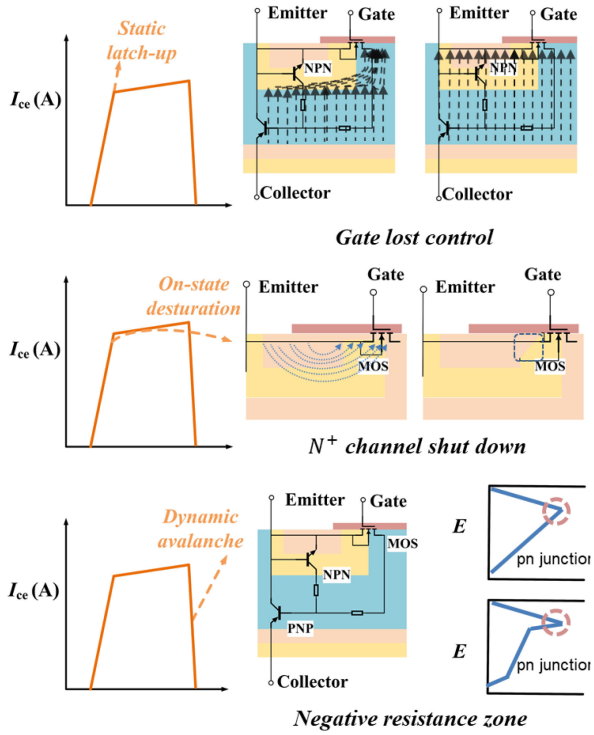


Fig. 2. Three potential failure types.

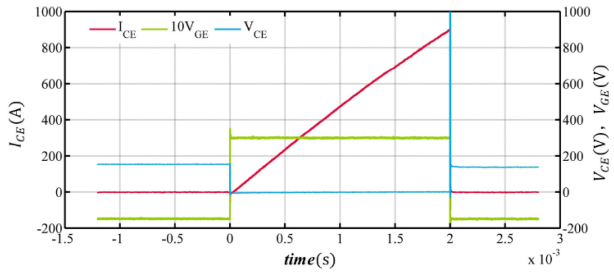


Fig. 3. Single IEGT chip turn-ON and turn-OFF over 12 times rated current value (880 A) (T_j = 298 K, $R_{g,\text{off}}$ = 5 Ω, $V_{g,\text{on}}$ = 30 V, and $V_{g,\text{off}}$ = −10 V).

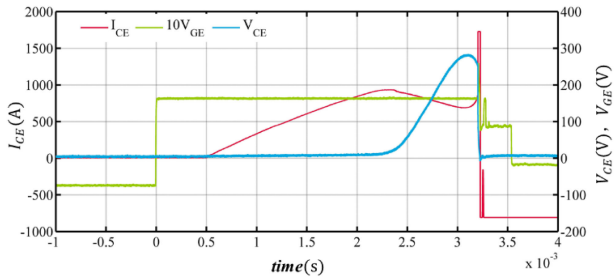


Fig. 4. Two IEGT chip failure after on-state desaturation (two parallel chips, T_j = 298 K, $R_{g,\text{off}}$ = 5 Ω, $V_{g,\text{on}}$ = 17 V, and $V_{g,\text{off}}$ = −9 V).

DCCB projects, gate driving voltages above 20 V have been proven no longer an absolute maximum limit [3]. Combined with the application in the high-voltage DCCB applications, this article proposes a method of using UDV. UDV is usually much higher than the driving voltage value recommended by the manufacturer but not higher than the voltage value of the gate oxide breakdown (generally about 50 V). Devices driven under this condition can usually obtain a larger current capacity, shorter ON-state time required for the same level of current, and reduce the ON-state voltage drop and ON-state temperature rise.

Meanwhile, in the ON-state process, due to the effect of the strong electric field (UDV), the average energy of some carriers is significantly higher than the energy in the equilibrium state or low electric field. Such carriers are called hot carriers, whether they are hot electrons or hot holes and can cross the Si–SiO2 interface barrier and emit gate oxide. The hot carriers that enter the gate oxide either penetrate the oxide or cause an increase over time of the interface state, etc. As a result, the gate threshold voltage $\boldsymbol{V_T}$ drifts, the ON-state resistance R_{on} increases, and the device characteristics are degenerated, affecting the working life of the device and related circuits [15], [16].

C. Potential Failure Types After Increasing Current Capability

Fig. 2 shows three main failure types of IGBT device, the main failure type that may occur during the turn-ON stage of the device is static latch-up. When the collector's current is large to a certain extent, the positive bias voltage is enough to turn ON the parasitic NPN transistor. This will make the n-p-n and p-n-p in a saturated state, so the parasitic transistor is turned ON, and the gate loses control over the collector's current. This is the static latch-up effect of the IGBT. However, with the continuous optimization of the device structure, the current mainstream IGBT devices have strong anti-latch-up ability, which can generally cause the device to desaturate before the latch-up. Sufficiently low $\boldsymbol{N^+}$channel resistance $\boldsymbol{R_b}$ and sufficiently large $\boldsymbol{N^+}$channel doping make the device withstand extreme current stress. In this article, a 4500 V/3000 A planar gate IEGT (a type of IGBT) overcurrent single chip experiment was carried out, and the static latch-up of the device did not occur under the condition of more than 12 times the rated current value, as shown in Fig. 3.

The main failure type that may occur during the ON-state stage of the device is ON-state desaturation. The shutdown of the electron channel causes the resistance of the device to increase. At this time, the power rises quickly, which eventually leads to thermal breakdown, as shown in Fig. 4.

The main failure type that may occur during the turn-OFF stage of the device is dynamic avalanche. Dynamic avalanche may cause the formation of local current filaments due to negative differential resistance. This phenomenon is extremely unstable and may eventually cause thermal breakdown of the device. However, the existing DCCBs have plenty number of methods for reducing overvoltage to prevent the device from dynamic avalanche during the turn-OFF. including snubber circuit and low inductance design [8]–[10]. Therefore, in the analysis of this article, the analysis is not focused on this stage.

III. Analysis of Current Boosting Capacity by UDV(Ultra Driving-Voltage)

A. ON-State Desaturation

After the discussion above, ON-state desaturation is the key factor restricting the improvement of device current capability.

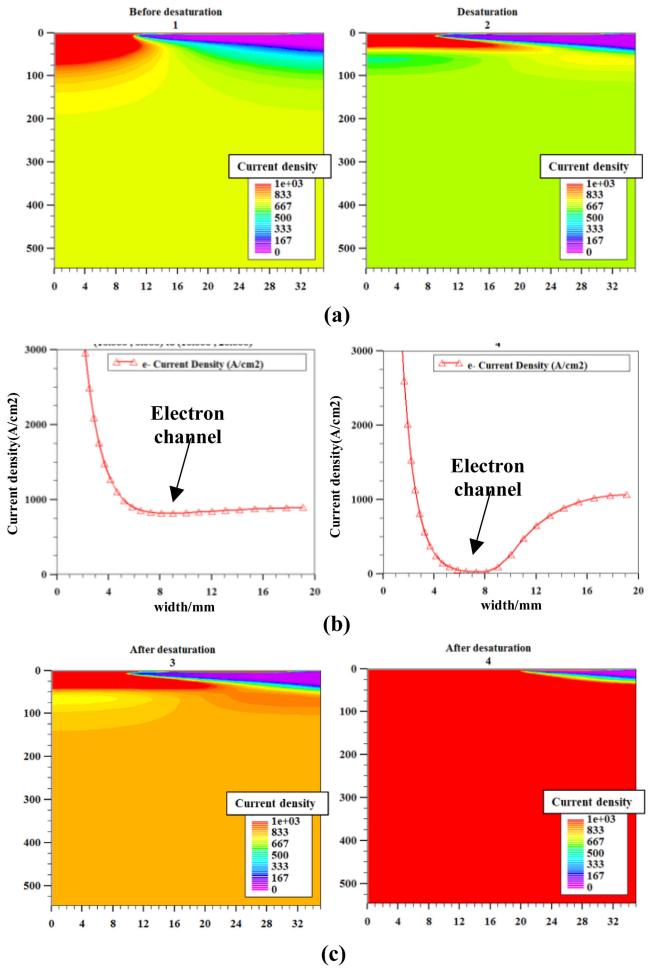


Fig. 5. Whole process from ON-state desaturation to thermal breakdown in TCAD simulation. (a) Electron current density before ON-state desaturation. (b) Electron channel shutdown after ON-state desaturation. (c) Electron current density after ON-state desaturation.

This article performs a TCAD simulation analysis for this phenomenon. Fig. 5 shows the whole process from the ON-state desaturation to the thermal breakdown of an IGBT half-cell.

As shown in Fig. 5, it shows the process of an IGBT half-cell from entering the ON-state desaturation area to the thermal breakdown caused by high power reaching the intrinsic temperature. The temperature rise causes positive feedback and finally leads to the failure.

Fig. 5(a) and (b) shows the process of ON-state desaturation. The carrier distribution in the two half-cells above shows the change process of electron current density. It can be seen that the electron channel has changed significantly. As shown in Fig. 5(b), the two half-cells tangent diagrams above prove that the electron current on the electron channel has shut down. At this time, the half-cell enters the amplification area (linear area) from the saturation area, and the potential difference between the gate and the silicon surface is not enough to satisfy the strong inversion at this time, and the current does not increase anymore.

Fig. 5(c) shows the process of half-cell entering the amplifying area. After the half-cell enters the amplifying area (linear area), the ON-state voltage drop across the collector and emitter begins to rise, and the power loss of the device cell I_{CE} began to increase rapidly, which directly caused the junction temperature to rise. Heat becomes the dominant factor of the cell at this time. Finally, the device fails to short-circuit and eventually thermal breakdown. In the experiment, the surface of the chip where the failure occurred can see an obvious melting area.

B. Analysis of Boosting Current By UDV

Under the condition of using UDV, the current capacity has been greatly improved. At the same time, combined with the previous analysis, the ON-state desaturation of the device is generally the result of the combined effect of the increased current and the increased device junction temperature.

The current in the IGBT is usually composed of two parts, one part is the current after gain in the PIN rectifier, and the other part is the current flowing through the MOSFET electronic channel after it is turned ON [17]. In this article, a method for IGBT calculating desaturation current by fitting PIN gain coefficient α_{PNP} into electronic channel is proposed. When calculating the ON-state current value, the current in the electron channel is the key part of discussion, and the total current has

$$\begin{cases} I_{CE} = \alpha \left(V_{GE} - V_T\right)^{\gamma} \tanh[\theta \left(V_{CE} - V_K\right)^{\lambda}] \\ I_{CE} = \alpha \left(V_{GE} - V_T\right)^{\gamma}, \mathrm{reachesdesaturation}. \end{cases} \tag{1}$$

α is

$$\alpha = \frac{1}{1 - \alpha_{\mathrm{PNP}}} \cdot \frac{W \mu_n C_{\mathrm{OX}}}{L} \tag{2}$$

where L represents the length of the electron channel, Wrepresents the total cross-sectional width of the electronic channel of the device, C_{OX} is the characteristic capacitance of the oxide layer, $\mu_n$is the electron mobility, and α_{PNP} is the current gain coefficient of the PIN rectifier (this value is determined by the structure of the IGBT itself, and the α_{PNP} value is a constant).

The initial ambient temperature of the device and the ON-state temperature rise during the ON-state process will affect the threshold voltage value V_T and the mobility of electrons $\mu_n$of the device.

The change of gate threshold voltage V_T affected by the ambient temperature is not affected by the ON-state temperature rise. The parameters given in the device datasheet can extract the $V_T - \mathrm{Temperature}$ curve, as shown in Fig. 6 (the data comes from the Manufacturer's datasheet, and the ON-state current value is selected at $V_{CE} = 20$ V). In formula (2), the physical meaning contained in the α value is mentioned. The μ_n contained in the α value is the mobility of electrons. In the actual ON-state process, μ_n is affected by the self-temperature rise of the device after the electron channel is opened. On one hand, the process is affected by ON-state time (the value is usually less than 3 ms under DCCB applications). Under this working condition, the cumulative effect of heat cannot be ignored. On the other hand, it also depends on the ambient temperature when the device is turned ON. In this article, using the universal mobility model based on quantum mechanical scattering theory

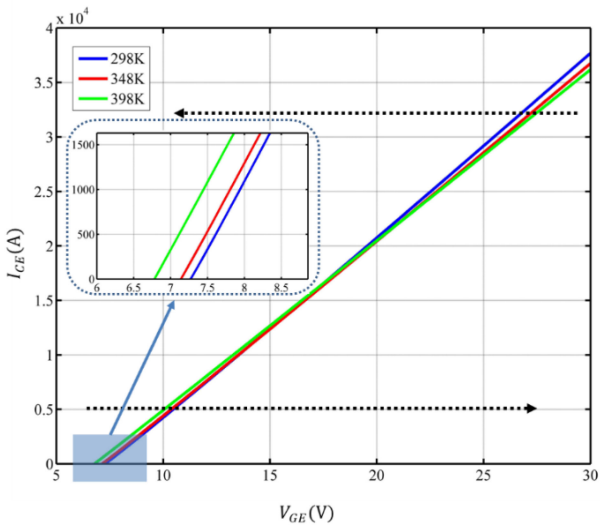


Fig. 6. V_T under different ambient temperature($V_{CE} = 20$ V).

is proposed by Klaassen [18]

$$\mu_n = 1412\left(\frac{300}{T}\right)^{2.28}. \tag{3}$$

Meanwhile, the ON-state temperature rise are affected by various factors (device package structure, heat dissipation system, device topology, gate driving parameters).

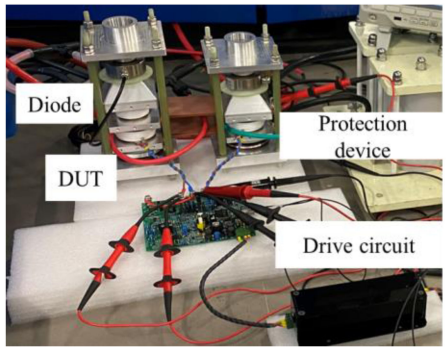
C. IEGT Single Chip Experiment

The chips and devices used in this article are TOSHIBA ST3000GXH24A IEGT, a type of IGBT. Compared with IGBT, it has a hole barrier layer. In the paper of [19], the influence of $\operatorname{arc}\tanh[\theta\,(V_{CE} - V_K)^{\lambda}]$ coefficient under different current densities was analyzed. The conclusion of the article expresses that when the current density of the device is large enough (twice the rated current density), the value is infinitely close to 1, so under the overcurrent conditions discussed in this article, the IE (injection enhanced) effect of the overcurrent capability of the device is considered as a fixed coefficient β when calculating the device ON-state current model. Therefore, for formula (1), there are the following equations when the device is desaturated:

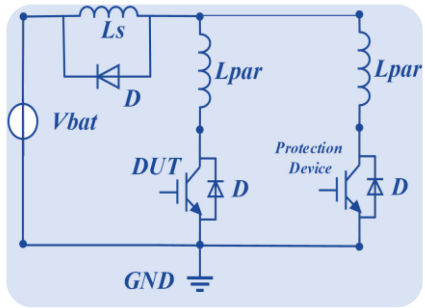
$$I_{CE} = \alpha\,(V_{GE} - V_T)^{\gamma} \cdot \beta, \text{reaches desaturation}. \tag{4}$$

In order to verify the accuracy of the calculation model analyzed in this article, this article first built a single-chip experimental platform as shown in Fig. 7. The platform uses the desaturation protection function. The protection device is triggered by the desaturation signals of the tested chip. After the chip under test is desaturated (the collector voltage is higher than a certain value, this value used in the experiment of this article chooses 160 V), turn OFF the tested single chip and turn ON the protection device. Then, determine the desaturation current value of the chip according to the moment when the ON-state resistance changes.

Aiming at the extraction of parameter V_T and parameter γ, this article uses the experience of calculating the ON-state current



(a)



(b)

Fig. 7. Single chip experiment. (a) Single chip experimental platform. (b) Single chip experimental circuit.

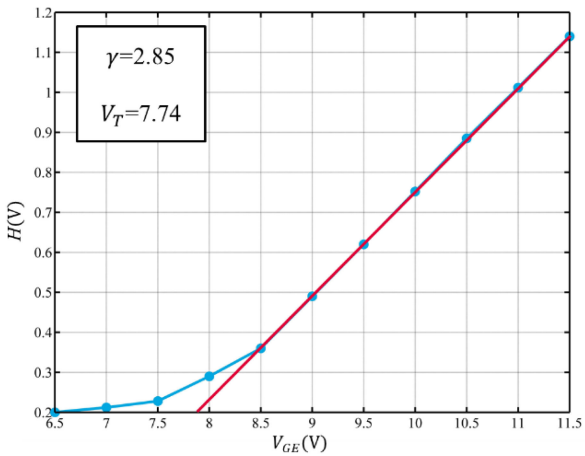


Fig. 8. Extracted of γ and V_T of IEGT chip.

in MOSFET [17] to establish the integral function H suitable for IEGT

$$H(V_{GE}) = \frac{\int_0^{V_{GE}} I_{CE}(V_{GE})dV_{GE}}{I_{CE}(V_{GE})} = \frac{V_{GE} - V_T}{1+\gamma}. \tag{5}$$

The IEGT chips γ and V_T extracted by the H function are shown in Fig. 8 of the saturation area (ohmic area) and the desaturation area (linear area) combined with formula (1), and the extraction results are shown in Fig. 9.

The extraction of parameter α, parameter λ, and parameter θ is mainly extracted by extracting the intersection of the saturation area (ohmic area) and the desaturation area (linear area)

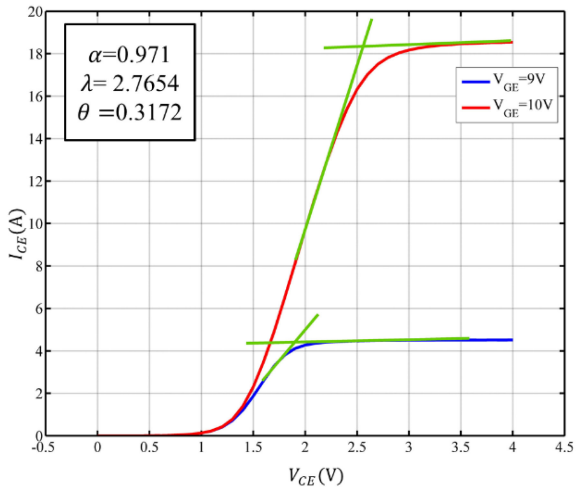


Fig. 9. Extracted of α, λ, and θ of IEGT chip.

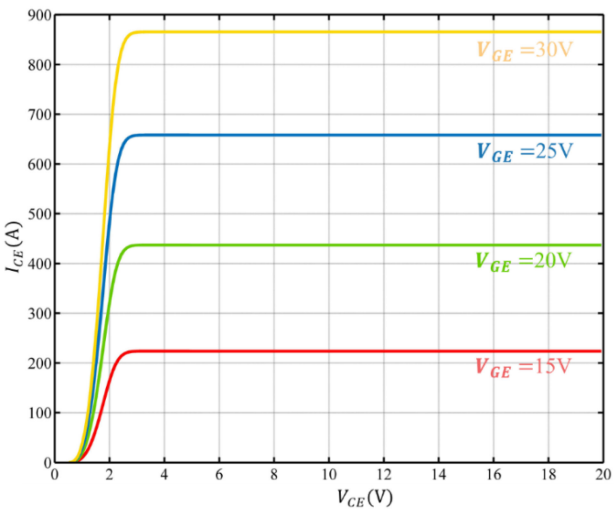


Fig. 10. ON-state current calculation results (single chip).

TABLE II
COMPARISON OF MEASURED VALUES AND CALCULATION RESULTS OF ST3000GXH24A IEGT SINGLE CHIP

Gate driving voltage	Experimental desaturation current	Calculation desaturation current	Relative error	Experimental ON-state voltage drop
15 V	218 A	220 A	0.9%	2.9 V
20 V	430 A	438 A	1.9%	2.6 V
25 V	662 A	660 A	0.3%	2.3 V
30 V	880 A	872 A	0.9%	2.2 V

combined with formula (1), and the extraction results are shown in Fig. 9.

Finally, as shown in Figs. 8 and 9, the parameters of IEGT ON-state current calculation model are extracted.

The single-chip experimental platform is used to compare the measured data with the calculated results, as shown in Fig. 10 and Table II. The measurement result is generally the average of ten data. By comparison of the measured values and calculation results, it can be seen that the calculation method proposed

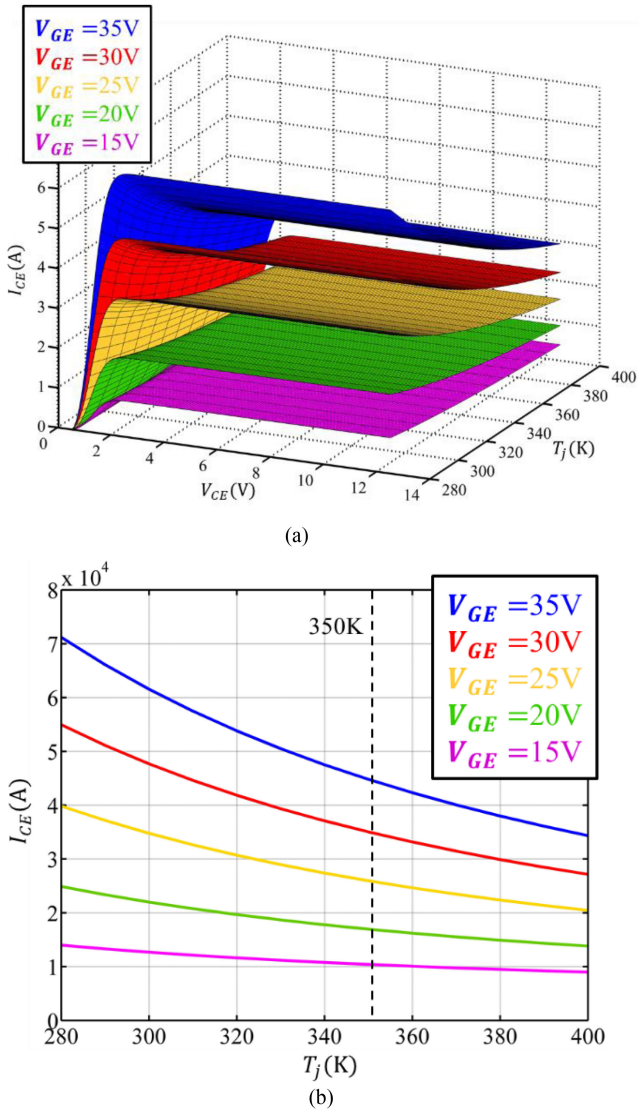


Fig. 11. 3-D static state output characteristics of IEGT. (a) 3-D static state output characteristics. (b) Side view of 3-D static state output characteristics.

in this article has good accuracy, the error is within a certain allowable deviation range. It also can be seen that the higher the gate driving voltage, the lower the voltage drop in the ON-state.

D. IEGT Device Current Calculation Under UDV

After verifying the validity of the calculation method, now we use the manufacturer's datasheet to extract the parameters to predict the desaturation current value, and the threshold voltage value V_T, and the mobility of electrons $\mu_n$as the coefficient of calculation. The calculated results are shown in Fig. 11.

Fig. 11 shows the three-dimensional ON-state current threshold curves of ST3000GXH24A IEGT, respectively, under different gate driving voltages. The paper [20] indicates during the overcurrent process (ON-state time 4 ms, 8 times rated value), the ON-state temperature is 45 K. The ambient temperature is 278–308 K. Therefore, the highest junction temperature is about 350 K.

IV. Analyzing the Impact of UDV(Ultra Driving-Voltage) on Device Lifetime

A. Gate Lifetime Under UDV

Manufacturers usually recommend a voltage of about 15 V for the gate of high-voltage devices, and generally indicate in the datasheet that the gate driving voltage should not exceed 20 V. This voltage is not the gate breakdown voltage of general devices (usually around 45–55 V) [22], which is mainly based on the long-term reliability of the device. However, the working condition of DCCB generally does not require long-term periodic pulse, and the action times is relatively less. Therefore, it is necessary to discuss the degradation of the device when the gate stress time is short but the gate driving voltage is high (UDV).

First, for time-dependent dielectric breakdown (TDDB) under different gate driving voltage stresses, this article adopted the power exponential model as follows [21]:

$$\ln(T_{BD}) = n\ln(V_{GE}) + \ln C + \frac{E_\alpha}{kT} \tag{6}$$

where T_{BD} represents the breakdown time, n is the voltage coefficient, C represents the proportionality constants determined by materials and processes, E_a is the thermal activation energy, and k represents the Boltzmann constant.

The article [22] conducted a comprehensive Weibull distribution TDDB experiment on IGBT devices from different manufacturers, and the conclusions showed that the gate driving voltage will not cause obvious degradation of the gate oxide layer until the gate driving voltage more than 45 V (either extrinsic characteristics or intrinsic characteristics).

For the reliability of the UDV method under the DCCB applications analyzed in this article (take Zhangbei flexible dc transmission project for example, the requirement is 500 movements per year, single pulse time is 3 ms, reclosing breaker pulse 20 ms [3]), a relatively short time gate lifetime aging experiment was adopted to prove the feasibility of the UDV method.

Based on the analysis in Fig. 11, it is believed that the gate driving voltage of 30 V can reach the 10 times the rated current value index proposed in this article. To ensure that, this article carried out the 10 000 s stress time experiment (consider a certain margin in the experiment, the gate driving voltage is 35 V, and the experiment was carried out under the temperature condition of 400 K). Two types of key parameters V_T and $V_{CE(\text{sat})}$ are analyzed using a power analyzer. The experimental method is to use a fixed gate driving voltage to first apply a dc voltage stress to the gate for a certain pulse time (1, 10, 100, 1000, 10 000 s), and then use a power analyzer to extract the static characteristic curve and transfer characteristic curve of IEGT chip. In order to ensure the accuracy of the experiment, the chips in different IEGT devices are selected in this paper.

Fig. 12, respectively, shows the changes of ON-state voltage-drop value $V_{CE(\text{sat})}$ and gate threshold voltage V_T of ST3000GXH24A/ 4500 V/ 3000 A IEGT chip after 35 V gate voltage stress (IMV: Initial measurement value). It can be seen in Fig. 12 that under the gate driving voltage of 35 V, the gate threshold voltage V_T and ON-state voltage-drop $V_{CE(\text{sat})}$ have changed to a certain extent. The red curve represents the initial

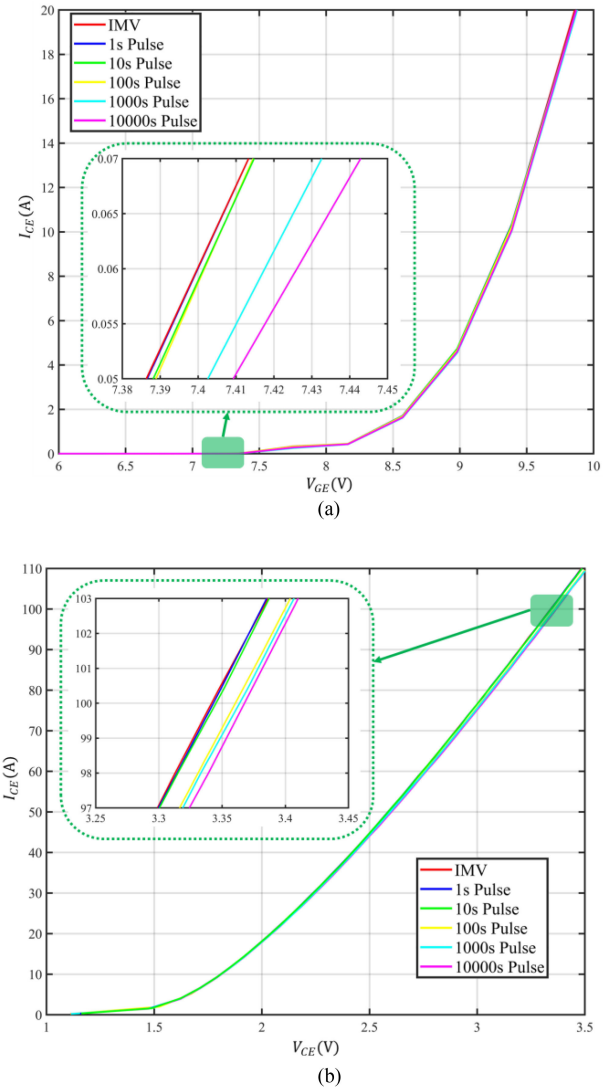


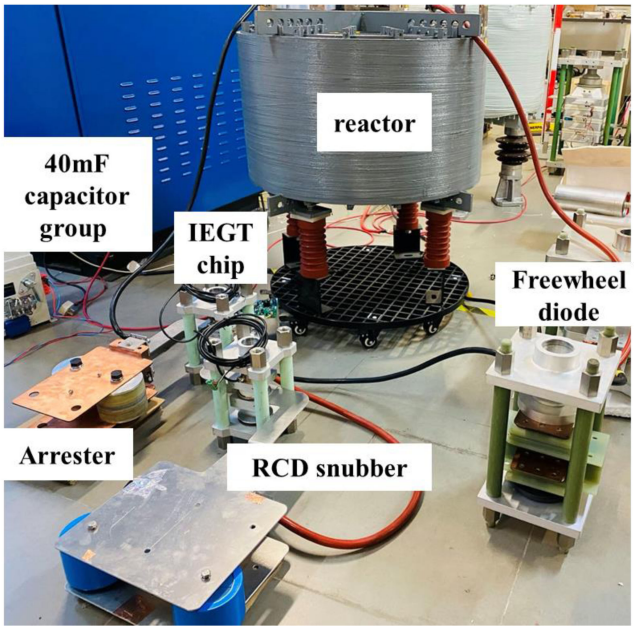
Fig. 12. Change process under gate driving voltage stress for a certain period of time ($T_j = 400$ K and $I_{CE} = 120$ A). (a) IEGT V_T after 35 V gate voltage stress. (b) IEGT $VCE_{(\text{sat})}$ after 35 V gate voltage stress.

measurement value. This curve can be used as a reference. It is found that after 10 000 s of gate driving voltage stress, the gate threshold voltage has drifted by 0.04% (according to the datasheet, the gate threshold voltage V_T is extracted at the collector current $I_{CE} = 60$ mA), and the ON-state voltage-drop has increased by 0.5% (according to the datasheet, the ON-state voltage-drop $V_{CE(\text{sat})}$ is extracted at the collector current $I_{CE} =$ 100 A).

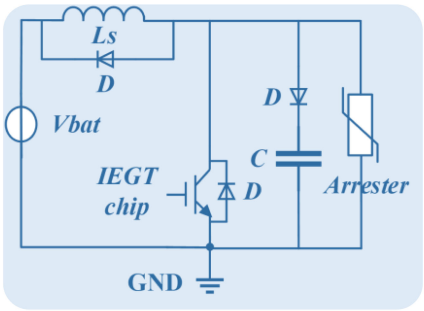
The experimental results show that under the condition of the gate driving voltage within 35 V, the degradation of the gate oxide layer of the device is basically negligible (within the equivalent time period of the DCCB operating conditions).

B. IEGT Single Chip Repetitive Turn-OFF Aging Experiment Under UDV

After the lifetime experiment of the gate under high driving voltage stress, this article considers that the gate driving voltage

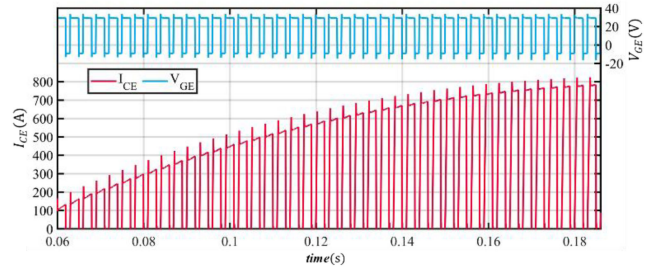


(a)



(b)

Fig. 13. Repetitive turn-OFF aging experiment. (a) Repetitive turn-OFF aging experimental platform. (b) Repetitive turn-OFF aging experiment circuit.



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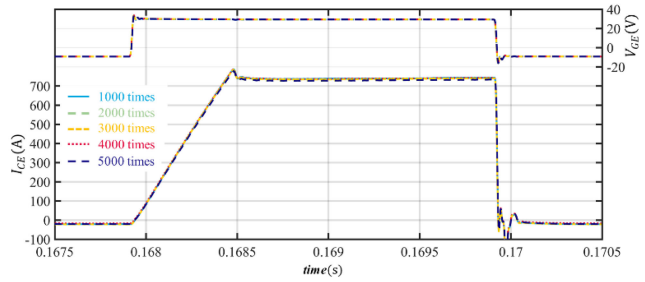

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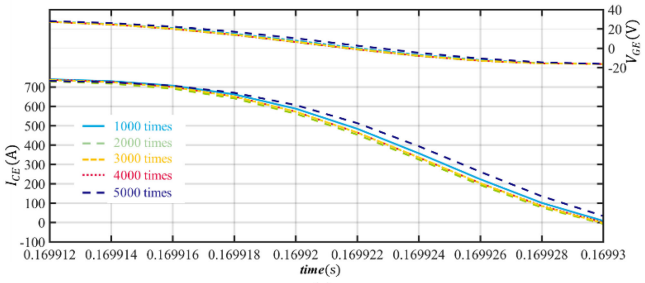


(c)

Fig. 14. Repetitive turn-OFF aging experiment. (a) Multiple pulses waveform. (b) Amplification of single pulse after different aging times. (c) Amplification of turn-OFF stage after different aging times.

of about 30 V can meet the requirements of the device under the DCCB applications (the current capacity of the device can be improved as much as possible while the aging of the gate oxide layer is considered to be within an acceptable range). However, the device usually works in high current condition under the DCCB applications. At this time, only considering the lifetime loss of the gate oxide layer is not enough to fully reflect the reliability of the device under the UDV method, the loss of the device itself is also worth paying attention to.

Therefore, it is necessary to carry out the repetitive high current turn-OFF experiment under UDV. In this article, the experimental platform is set up as shown in Fig. 13. Considering the equivalence of the repeated turn-OFF between the single chip and the device, this article selected IEGT single chip for repetitive high current turn-OFF aging experiment. At the same time, as shown in Fig. 13, an equal-ratio miniature circuit for reducing the dc circuit breaker submodule is built, and the RCD of the snubber circuit and the arrester are matched to meet the requirements of the DCCB equivalent working condition with IEGT single chip.

The experimental method is similar to the double pulse experiment method. Considering the selection of inductance and capacitance, the single pulse is 2 ms, and then the IEGT single chip is OFF-state for 1 ms, and the single period is 3 ms. A group of experiments can be conducted for 50 periods, a total of 100 groups of experiments were conducted. Finally, the single IEGT chip was turn-ON and turn-OFF 5000 times in the DCCB equivalent conditions (estimating the ten-year period of the dc circuit breaker service cycle).

Fig. 14(a) shows the waveforms of multiple pulses in a group of experiment. The gate driving voltage is 30 V (UDV). Due to the LC oscillation method adopted in the experiment, the current passed by a single chip in each pulse is a gradual increase process. In the experiment with 50 periods of pulses as a group, there are 10 periods that exceed the rated current value of the single IEGT chip by more than 10 times (720 A). This may reduce the loss of the single IEGT chip to a certain extent, because in the actual DCCB application scenarios, the DCCBs do not turn OFF the maximum current every time. Therefore, the experiment restores the actual working process of the IEGT devices in the DCCBs in a certain sense [in all pulse periods,

the single IEGT chip exceeds its own rated current value (72 A), exceeds the single IEGT chip rated current value more than 5 times (360 A) by 4000 pulse periods, and exceeds the single IEGT chip rated current value more than 10 times (720 A) by 1000 pulse periods].

Fig. 14(b) shows the waveform of single pulse after different number of aging times, Fig. 14(c) shows the waveform of the turn-OFF stage of single pulse after different number of aging times. It can be seen that under the UDV selected in this article, the IEGT chip has undergone as many as 5000 repetitive turn-OFF waveforms basically with no significant changes. In the local amplification of turn-OFF stage, this article calculates the time from 90% to 10% current value (a definition of turn-OFF time that is typically used) after different aging experiment times, and the result shows that the turn-OFF time before and after the aging experiment changes less than 5%, which fully meets the lifetime requirement in the IEC standard.

The experimental results verify the feasibility of UDV selected after the lifetime analysis in the previous section under the DCCB applications.

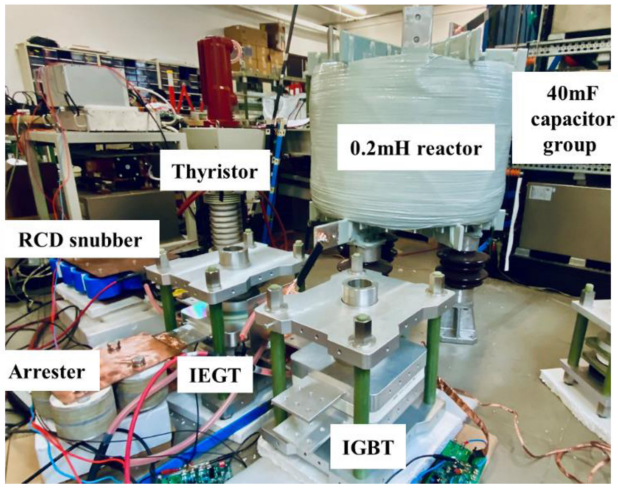
The gate oxide layer aging experiment and the repeated turn-OFF experiment under UDV prove the reliability of the UDV (30 V) selected in this article.

V. Single Device Turn-ON and Turn-OFF 31.2 kA Current by UDV (Ultra Driving-Voltage)

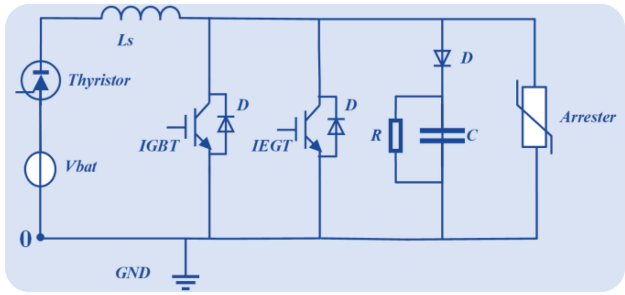
A. Setup of Experimental Platform

In order to achieve the goal of turn-ON and turn-OFF 30 kA in 3 ms proposed in this article, an experimental platform as shown in Fig. 15 was built. The maximum bus voltage of the platform is 5 kV. The high voltage large capacitance of the bus is 20 mF, which is used to support the bus voltage. The current-limiting inductor is 0.2 mH, which is used to control the current change rate. The operating voltage of the buffer capacitor and arrester used in the experimental platform are both 2400 V. At the same time, a full busbars connection method is adopted to reduce stray inductance and increase the current capacity of the experimental platform. In order to verify that static latch-up does not occur, the experimental platform uses a parallel connection of IGBT and IEGT devices to increase the transient current change rate during the turn-ON process of the tested IEGT device. The IGBT selected in the experiment is ABB 5SNA3000K452300, and the IEGT selected is TOSHIBA ST3000GXH24A. The manufacturer's datasheet is shown in Table III. The experimental platform and circuit are shown in Fig. 15.

The experiment first turns ON the parallel IGBT devices, then turns ON the bypass thyristor, after a period of time, turns OFF the IGBT and turns ON the IEGT. As shown in Fig. 15(c), under this condition, the IEGT will withstand a huge current rise rate, which is much greater than the rate of current rise when the IEGT device is turned ON in high-voltage DCCB application. After that, the current enters a steady rise stage. Combining the analysis of Sections III and IV, the gate driving circuit enter voltage is selected 32 V to ensure that the device does not occur ON-state desaturation (considering that the gate driving circuit may generally have an error of 1–2 V (because of the driver



(a)



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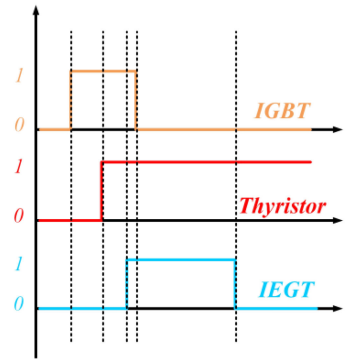


(c)

Fig. 15. Experimental platform and circuit. (a) Experimental platform. (b) Experimental circuit. (c) Digital signal trigger timing in experiment.

TABLE III
Manufacturer's Datasheet [23]

Device	IGBT ABB 5SNA3000K452300	IEGT TOSHIOBA ST3000GXH24A
V_{CE}	4500V	4500V
V_{GE}	±20V	±20V
$I_{CE}(DC)$	3000A	3000A
T_j	-50°C to +150°C	-40°C to +125°C
$V_{CE(sat)}$	2.85V	3.6V
$V_{GE(off)}$	5.3V~7.3V	6.5V~8.5V

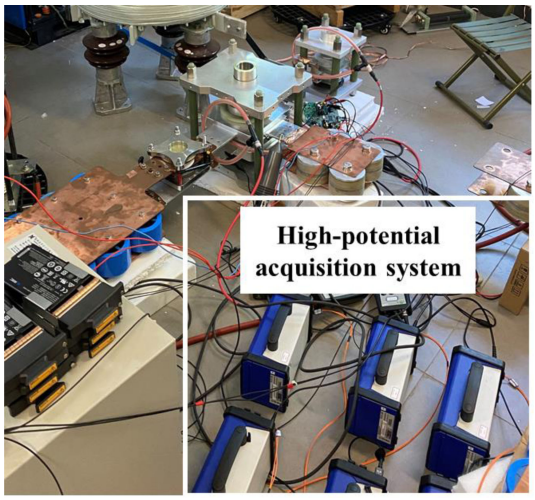


Fig. 16. High-potential acquisition system (during the experiment).

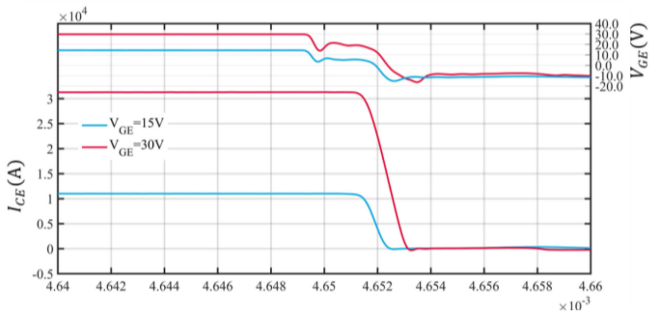


Fig. 17. Single IEGT device turn-OFF current drop period under 15 V driving voltage and 30 V driving voltage ($T_j = 300$ K, $R_{g,\mathrm{on}} = 5\ \Omega$, and $R_{g,\mathrm{off}} = 5\ \Omega$, $V_{g,\mathrm{off}} = -10.2$ V)

circuit loses), the highest gate driving voltage (UDV) should generally not exceed 32 V.

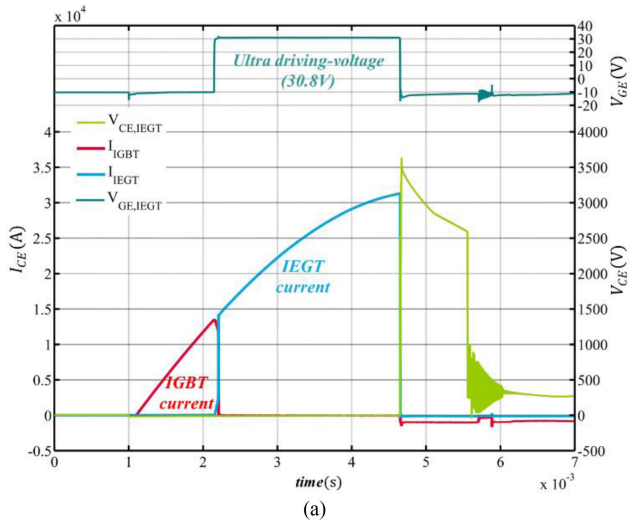
B. Experimental Result

First, due to the huge current and relatively high voltage level, this article does not take the conventional oscilloscope to measure (the conventional oscilloscope may have certain risks for this experiment), this article uses a high potential acquisition system, as shown in Fig. 16.

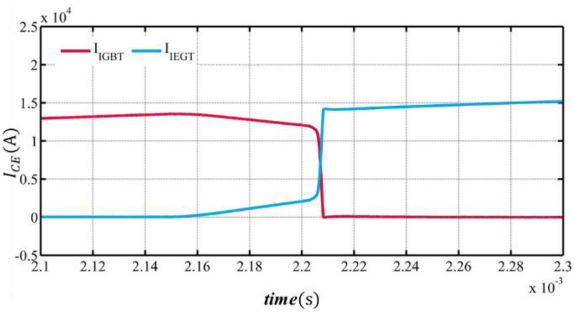
Second, in order to better express the UDV method, this article carried out the turn-ON and turn-OFF experiment under the same conditions ($T_j = 300$ K, $R_{g,\mathrm{on}} = 5\ \Omega$, $R_{g,\mathrm{off}} = 5\ \Omega$, and $V_{g,\mathrm{off}} = -10.2$ V), the experimental waveform is shown in Fig. 17. Fig. 17 shows the turn-OFF waveform at different gate driving voltages and the gate Miller platform.

Finally, as shown in Fig. 18, the experiment carried out in this article verified that neither static latch-up nor ON-state desaturation occurred. The current of 31.2 kA was successfully turned ON and turned OFF in 2.6 ms (<3 ms) under the UDV of 30.8 V (gate driving circuit enter voltage 32 V), which achieved the goal proposed in this article.

The experimental results show that UDV can greatly boost the current capacity of the device under the application of DCCBs, which has significant meaning for engineering applications.



(a)



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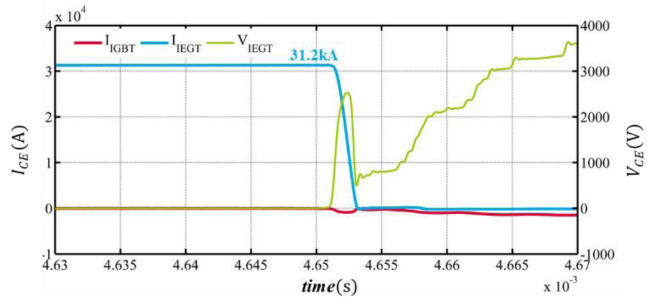

(c)

Fig. 18. Single IEGT device turn-ON and turn-OFF 31.2 kA current ($T_j = 300$ K, $R_{g,\mathrm{on}} = 5\ \Omega$, $R_{g,\mathrm{off}} = 5\ \Omega$, $V_{g,\mathrm{on}} = 30.8$ V, and $V_{g,\mathrm{off}} = -10.2$ V). (a) Whole process of turn-ON and turn-OFF. (b) Process of IEGT turn-ON. (c) Process of IEGT turn-OFF.

Taking Zhangbei high-voltage DCCB as an example, the devices in the circuit breaker can be reduced from 640 to 320, which is a huge reduction of construction costs.

VI. Conclusion

This article proposed a method of using UDV to boost the IGBT device's current capacity. In order to achieve this goal, this article mainly carried out the following work.

First, through the analysis of potential devices' failure types and calculation of ON-state current, the current boundary under different gate driving voltages is established. Then, through the establishment of a device lifetime test method suitable for

DCCB applications, the impact of UDV on the device lifetime is analyzed, combined with the experimental results, a proper UDV selection principle for IGBTs in HVdc circuit breakers is proposed. Finally, the current of 31.2 kA was successfully turned ON and turned OFF in 2.6 ms under the UDV of 30.8 V. The current capacity of the IGBT devices in DCCB is increased from 3–5 times rated value to 10.4 times rated value.

The conclusions presented in this article have greatly improved the current capacity of IGBT devices in the DCCB applications, and provided new ideas for the design of DCCBs.

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