A Step-Up Reconfigurable Multimode *LLC* Converter Module With Extended High-Efficiency Range for Wide Voltage Gain Application in Medium Voltage DC Grid Systems

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***Abstract*—In this article, a new modular multimode reconfigurable step-up resonant converter that is capable of extending very high efficiency from full load to reduced load conditions is proposed for wide voltage gain application in medium voltage dc (MVdc) grid system. The proposed converter module is able to switch from a hybrid control scheme that consists of variable frequency and phase shift control to pulsewidth modulation (PWM) control in the auxiliary switch of the output voltage quadrupler (VQ). In addition, the input bridge can also be reconfigured to a half-bridge mode to suit high input voltage range while utilizing a hybrid control technique that consists of variable frequency and asymmetrical PWM control. With the proposed approach, the converter module is able to achieve constant output voltage regulation without requiring a wide spectrum of switching frequency or phase shift control. Hence, close-to resonance operation with very high efficiency can be maintained for a wide range of input voltage and loading conditions. Soft switching operations are always guaranteed for all the primary side switches, the output diodes and the auxiliary switch in the VQ. The steady-state and dynamic performance of the proposed modular multimode step-up converter are validated through simulation results on a silicon carbide (SiC) based 360 V–1 kV/16 kV, 80-kW system and experimental results on a proof-of-concept 150–400 V/6.6 kV, 10-kW SiC laboratory prototype. Results confirmed that the efficiency is maintained between 97.8% and 99.1% from full load to at least 20% load condition for the specified input voltage range.**

***Index Terms*—High voltage gain, hybrid control, medium voltage, multimode, reconfigurable dc/dc converter, resonant converter, silicon carbide (SiC), soft switching.**

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I. Introduction

ACCORDING to the International Energy Agency, about 11% of the global population does not have access to electricity. The biggest challenge remains in the most remote areas globally and in sub-Saharan Africa, where renewable energy systems can be the best possible option [1]. Thanks to the advancement of high-power converters with high voltage gains, the paradigm shift from ac grids to dc counterparts is now feasible [2]. The output voltage level of a typical wind turbine generator or a photovoltaic (PV) inverter is usually in the range of 380–690 V and 280–370 V, respectively [3]. Therefore, a step-up ac transformer is used to integrate the low output voltage of the wind turbine generator and solar PV arrays into a medium voltage grid. The line-frequency (50/60 Hz) power transformers, however, are heavy and bulky. Recently, the use of a medium voltage dc (MVdc) grid, as shown in Fig. 1, has been presented as an alternative power architecture to replace the line frequency transformers by using MV step-up dc/dc converters [3], [4]. In addition, MVdc grid offers other advantages, such as the reduced number of power cables for long distance power transmission, elimination of phase synchronization, and reduced maintenance cost when compared with conventional MVac transmission.

Table I presents the MVdc voltage classes [5]. Various types of medium-to-high frequency step-up power converters for renewable energy applications have been presented in the literature. The authors in [6]–[8] have discussed many forms of medium-to-high frequency step-up power converters for renewable energy applications. Due to the high efficiency, high power density, low EMI, and soft-switching capability, *LLC* resonant converters are receiving special attention among the different topologies given in the literature [8], [9]. However, the *LLC* resonant converters have an unfavorable extra wide-switching frequency range in wide gain range applications. This has various disadvantages, including a restricted soft-switching range, a larger core size dictated by the lowest switching frequency, and restricted light-load regulation abilities. In reality, because of their intrinsic intermittency, various compromises between conversion efficiency and operating range are still required to satisfy the requirement of

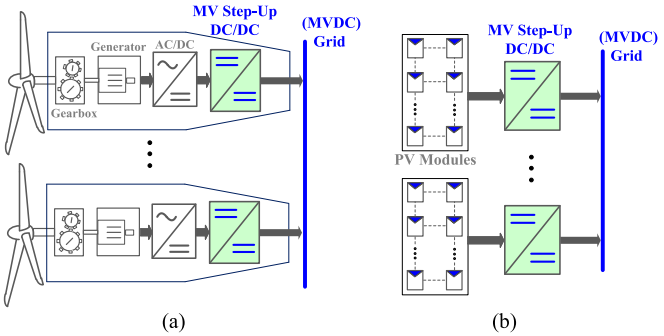


Fig. 1. Medium voltage dc (MVdc) collection system for (a) wind energy systems and (b) solar farms.

TABLE I
RECOMMENDED MVDC VOLTAGE CLASSES [5]

	MVDC Class (kV)
Already Established Classes	1.5, 3, 6, 12, 18
Future Design Classes	24, 30

wide voltage gain range in renewable energy systems (e.g., wide range of solar irradiation level and wind speed) [10].

To address these challenges, various studies have been conducted to improve the efficiency of *LLC* converters over a wide range of input and output voltages. These studies may be divided into four categories as follows.

1) Reconfiguration of the resonant tank [11]–[14].
2) Modification on primary-side switch network [15], [16].
3) Modifying the control and modulation strategies [17], [18].
4) Modification on secondary-side rectifier [10], [19].

Changing the resonant parameters is the first category. The voltage gain characteristic of *LLC* converter is highly dependent to the resonant parameters (i.e., L_r, C_r, and L_m). Changing the resonant parameters can, therefore, provide a wider voltage control range. The challenge with resonant tank reconfigurations is that parameter design of resonant components becomes extremely difficult. Furthermore, adding more resonant components is no longer the best option, as frequent mode transitions reduce overall efficiency and decrease transient response [20]. Furthermore, the sudden mode change causes a high current overshoot problem in some structures, such as [12]–[14].

The second category is based on the use of reconfigurable primary-side structures. Transitioning from a full bridge to a half-bridge converter is the most promising topology in this category [15], [16]. Existing converters with reconfigurable primary-side structures, however, employ an additional bidirectional switch, which contributes to the conduction loss and complexity.

The third category focuses on changing the control and modulation techniques. Burst mode control solutions are given in [17] and [18] to increase the light load regulation capacity and efficiency of the *LLC* converter. However, the controller design is highly intricate, there is a high-frequency oscillation and EMI problems are produced.

The final category is based on modifying the secondary-side structure. The rectifier structures can be reconfigured to be a full-bridge rectifier, a voltage doubler, or a voltage quadrupler rectifier. As a result, the output voltage range is expanded.

In [16] and [17], a bidirectional switch is used on the primary side to build a dual-bridge *LLC* resonant converter, and some of the diodes in the secondary-side rectifier are replaced with semiconductor switches, similar to [11]. In [21], a pulsewidth modulation (PWM) voltage quadrupler rectifier with a constant frequency is introduced. However, the secondary side rectifier employs a PWM MOSFET and a voltage doubler cascaded with a voltage quadrupler, which increases the number of components and reduces efficiency. A constant frequency resonant converter with semiactive phase-shifted voltage multiplier was presented in [22]. However, this converter is not able to maintain high efficiency for a wide range of loading conditions. In addition, the converter is not able to regulate the output voltage at rated power condition during low-input voltage range.

In the existing topologies, the covered voltage gain is limited. The proposed converter in this article overcomes this issue by adding only one switch. In this article, a new step-up resonant converter is proposed for step-up voltage conversion in MVdc applications. The proposed converter consists of a reconfigurable primary-side inverter and a PWM-controlled voltage quadrupler that requires only one additional auxiliary switch compared to the traditional voltage quadrupler. By controlling the duty ratio of the auxiliary switch (S_x) on the secondary side as well as restructuring the primary side inverter, a wide range of voltage gain can be realized in the proposed converter within a narrow range of switching frequency. The proposed converter controls the output voltage by adaptively changing the configuration at the input and controlling the duty ratio of the voltage multiplier in the output. Unlike the phase shifted full bridge that lose the soft switching of one leg as the load changes, the proposed converter maintains soft switching for the entire range of loading conditions and voltage gains. The proposed MVdc step-up converter is extended to the modular structure with independent controller for each module. The modular structure employs an input-parallel-output-series (IPOS) system that enhances the balanced operation of the modular converter. The proposed converter is suitable for grid-connected renewable energy systems, in particular photovoltaic systems, with a wide-input voltage range and different grid voltage levels.

The rest of this article is organized as follows. Section II gives the description of the proposed converter's structure, the converter's characteristics, and operating principles. Section III provides the proposed converter's steady-state analysis. Section IV demonstrates the performance of the proposed circuit by PSIM simulations on a modular 80 kW, 360–1 kV/16k V and experimental results on a laboratory scale 10 kW, 150–400 V/6.6k-V prototype with four modules. Finally, Section V concludes this article.

II. PROPOSED CONFIGURABLE TOPOLOGY

A. Topology Description

Fig. 2 illustrates the modular structure and schematic of one module of the proposed *LLC* resonant converter. The primary

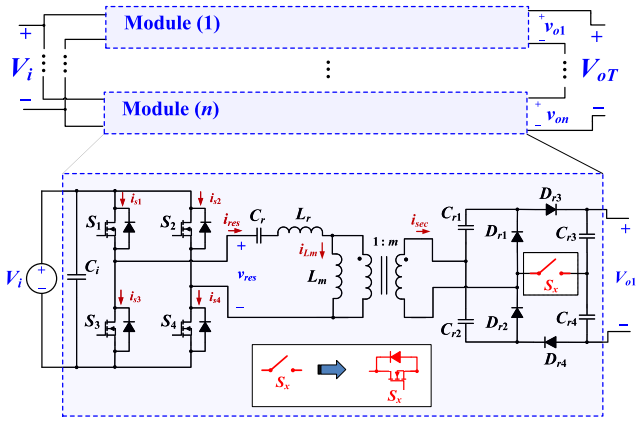


Fig. 2. Topology of the proposed configurable *LLC* converter.

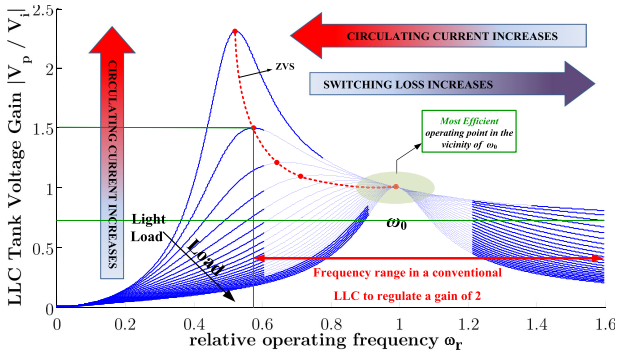


Fig. 3. Voltage gain of typical *LLC* as a function of ω_r for $k = 3$.

side is a full-bridge (FB) inverter with an *LLC* resonant tank. The resonant tank consists of a resonant capacitor (C_r), a resonant inductor (L_r), and a 1:m transformer with the magnetizing inductance of L_m. The secondary side is composed of a voltage quadrupler rectifier with an added switch (S_x) that operates with the same switching frequency of the inverter side switches (S_1-S_4). The primary side FB inverter can be restructured to a half-bridge configuration by turning OFF S_2 and turning ON S_4. In fact, the transition in the primary side does not require any extra switches, which offers low complexity and volume of the converter. By restructuring the primary side, as well as controlling the duty ratio of the auxiliary switch (S_x) on the secondary side a wide range of voltage gain can be realized in the proposed converter. Hence, a narrow range of switching frequency can be realized for S_1–S_4 and S_x. As discussed in the introduction, the conventional *LLC* resonant converters with wide voltage gain have undesirable extra wide switching frequency range. As illustrated in Fig. 3, the optimal balance between the circulating-current and switching loss occurs around the series resonant frequency ω_0, where *LLC* converters exhibit the maximum efficiency [23]. With a narrow operating frequency range in the vicinity of ω_0, the proposed modular converter provides high efficiency in a wide range of loading conditions and voltage gains.

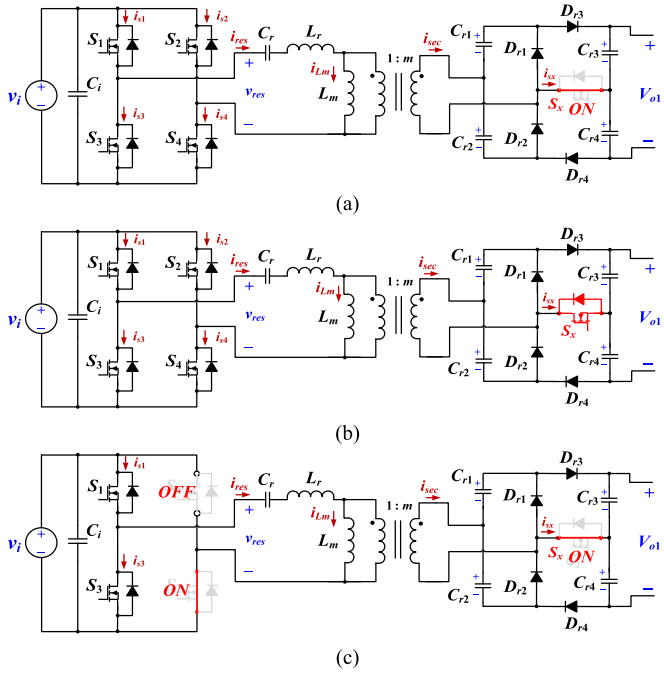


Fig. 4. Different modes of operation in the proposed converter. (a) Mode I: FB inverter and VQ rectifier. (b) Mode II: FB inverter and PWM-VQ rectifier. (c) Mode III: HB inverter and VQ rectifier.

B. Operation Principles

Three modes of operation are shown in Fig. 4. In mode I, the primary side is configured as a FB inverter; this mode provides the highest voltage gain. The equivalent circuit of this operation mode is illustrated in Fig. 4(a). In FB mode, the output voltage is controlled by a hybrid control scheme that employs frequency modulation (FM) and phase-shift modulation (PSM). The operating waveforms of FB inverter with the secondary side acts as a voltage quadrupler is shown in Fig. 5. In mode II, the duty ratio in the auxiliary switch S_x is controlled to regulate the output voltage. It should be noted that when S_x is ON, the voltage multiplier acts as a voltage quadrupler (VQ) rectifier and when S_x is OFF, acts as a voltage doubler (VD). The voltage gain in the voltage multiplier rectifier is linearly proportional to the duty ratio of S_x, and can change from two to four times of the secondary-side square wave voltage of the HF transformer.

In mode III, the primary side acts as a half-bridge (HB) inverter by turning OFF S_2 and turning ON S_4. This mode of operation is illustrated in Fig. 4(c). In HB operation mode of the proposed converter, the output voltage is controlled by hybrid FM and asymmetrical PWM (APWM). In the proposed converter, C_r has two functions. First, it acts as a resonant capacitor in the *LLC* tank; and second, in asymmetrical operation of the proposed converter in HB mode, C_r also acts as a dc-blocking capacitor to avoid core saturation in the high-frequency transformer. Therefore, without any extra switch in the primary side, the converter can be reconfigured from FB to HB. Operating waveforms of HB inverter in Mode III, with secondary side acts as a VQ (S_x: ON) are shown in Fig. 6.

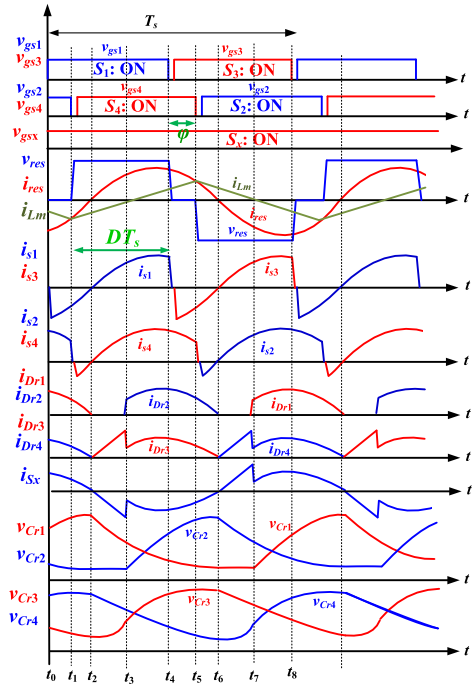


Fig. 5. Key operating waveforms in Mode I, FB + VQ (S_x : ON).

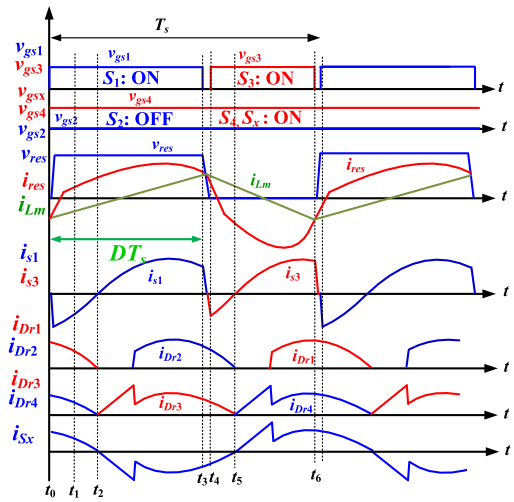


Fig. 6. Key operating waveforms in Mode III, HB + VQ (S_x : ON).

The operation principles of the primary-side switches S_1-S_4 are similar to the phase-shifted full-bridge *LLC* resonant converter. However, unlike the conventional phase-shifted FB, the proposed converter maintains soft switching for a wide range of loading conditions and voltage gains without any extra auxiliary circuit on the primary side. Fig. 7 shows the operating waveforms in Mode II. The operation principle of the converter in Mode II with respect to the secondary side, PWM-controlled voltage quadrupler, shown in Fig. 8, is described below.

[t_0<t<t_3]: At $t = t_0$, auxiliary switch S_x is turned ON. During this time, $i_{\rm res}$ is negative. On the secondary side, the negative secondary current ($i_{\rm sec}$) discharges C_{r2} and charges C_{r4} through D_{r4} and S_x. The voltage across C_{r1} is constant and C_{r3} is discharged to the load.

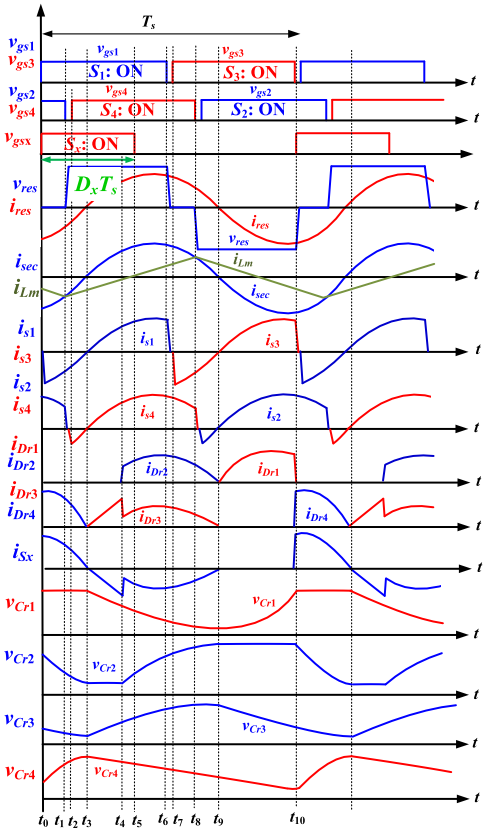


Fig. 7. Key operating waveforms in Mode II: FB + (PWM VQ).

[t_3<t<t_4]: At $t = t_3$, $i_{\rm res}$ changes its polarity from negative to positive. On the secondary side, $i_{\rm sec}$ also changes its polarity at $t = t_3$. Hence, the auxiliary MOSFET current i_{sx} becomes zero and the current flowing through the S_x MOSFET is now conducted by the body diode. This means that zero voltage switching (ZVS) turn-OFF is achieved for S_x. The positive $i_{\rm sec}$ discharges C_{r1} and charges C_{r3} through D_{r3} and the antiparallel diode of S_x.

[t_4<t<t_9]: At $t = t_4$, D_{r2} begin conducting a portion of the secondary current $i_{\rm sec}$ and charging C_{r2} since $v_{\rm sec}$ reaches v_{Cr2}. Hence, considering an ideal condition without any parasitic elements, a sudden current drop can be observed in D_{r3} and S_x body diode. At $t = t_4$, S_x gate signal ($v_{\rm gsx}$) is removed, but the body diode of the auxiliary switch continues to conduct until it becomes zero at $t = t_9$. Hence, zero reverse recovery loss can be obtained for the body diode of S_x.

[t_9<t<t_{10}]: At $t = t_9$, C_{r3} that has been already charged to $2v_{\rm sec(max)}$ is higher than $v_{\rm sec}$+v_{Cr1}, hence, D_{r3} and S_x antiparallel diode are reverse biased and stop conducting. During the negative half cycle of $v_{\rm sec}$, C_{r1} charges to $v_{\rm sec(max)}$. C_{r3} and C_{r4} are discharged to the load.

III. Analysis and Design Considerations

To perform the steady-state analysis of the proposed topology the following assumptions are made.

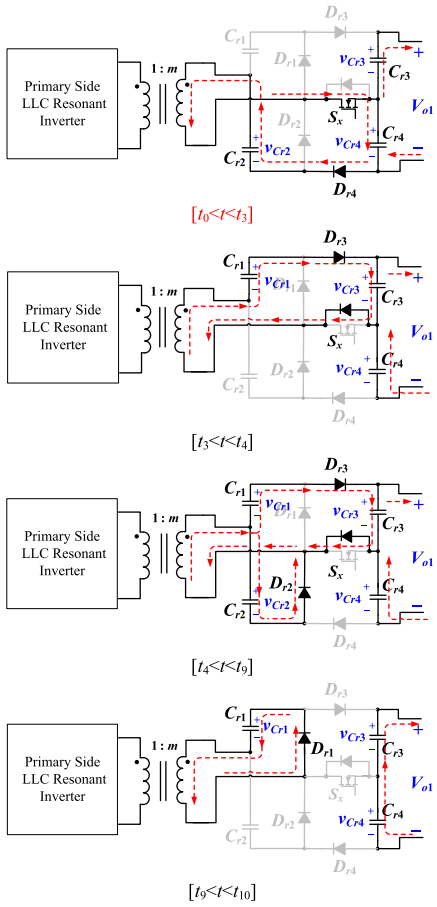


Fig. 8. Operating stages within a switching period (t_0–t_9) in Mode II.

1) All the components, including semiconductor switches and diodes are ideal.
2) The delays between the switches gating signals are neglected.
3) The effect of snubber capacitors is neglected.

A. Voltage Gain

The Fourier series representation of the input voltage to the resonant circuit in Modes I and II is given by [24]

$$v_{\text{res}} = \frac{4V_i}{\pi} \sum_{h=1,3,5,..}^{\infty} \left(\frac{1}{h} \sin(h\pi D) \sin\left(\frac{h\pi}{2}\right) \sin(h\omega t) \right) \tag{1}$$

where D represents the duty ratio (shown in Fig. 5) and h represents the hth harmonics. The relative angular operating frequency (ω_r) is given by (2), where ω represents the angular operating frequency $\omega = 2\pi f_s$. ω_0 represents the angular resonant frequency (3), and Q is the quality factor that is given by (4) as follows:

$$\omega_r = \frac{\omega}{\omega_0} \tag{2}$$

$$\omega_0 = \frac{1}{\sqrt{L_r C_r}} \tag{3}$$

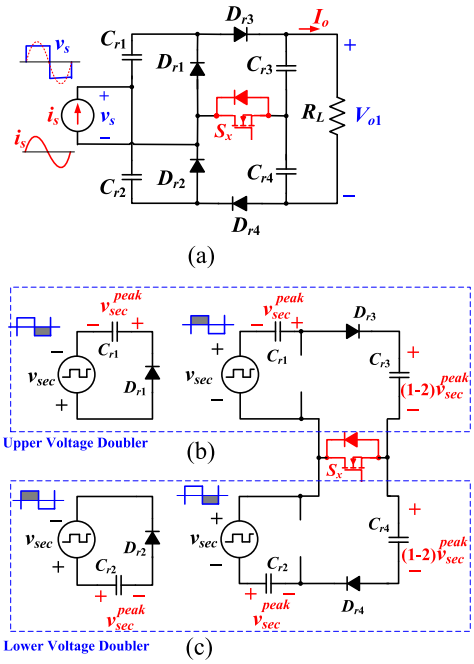


Fig. 9. Operating principles of (a) the secondary-side PWM-based voltage quadrupler formed by a stacked combination of two voltage doublers: (b) Upper voltage quadrupler and (c) lower voltage quadrupler.

$$Q = \frac{L_r \omega_0}{R_{ac}}. \tag{4}$$

R_{ac} is the equivalent ac resistance and is different for each mode of operation. The *LLC* resonant converter uses a capacitive output filter and, therefore, both voltage doubler (VD) and voltage quarupler (VQ) can be employed at the output rectifying stage in the proposed converter. The VD and VQ rectifiers offer the advantage of balanced voltage stress on the capacitors and diodes, which is of great importance in step-up MV converters.

The PWM-based voltage multiplier rectifier on the secondary side is illustrated in Fig. 9, in which the VQ rectifier is formed by a stacked combination of two VDs connecting through an extra switch (S_x). Each VD is separately shown in Fig. 9(b) and (c) and composed of two circuits: A clamper and a peak detector (half-wave rectifier). C_{r1} and C_{r2} charge to the peak of v_{sec} on the negative and positive half cycle of v_{sec}, respectively. During the positive half cycle, diode D_{r1} is reversed biased and C_{r1}, which is already charged to $v_{\text{sec(max)}}$, is placed in series with the input voltage source (v_{sec}). Thus, diode D_{r3} rectifies up to a total of 2 $v_{\text{sec(max)}}$ across C_{r3}. Similarly, the lower VD [Fig. 9(c)] rectifies up to a total of 2 $v_{\text{sec(max)}}$ across C_{r4} on the negative half cycle of v_{sec}. By controlling the duty ratio of switch S_x, the output capacitors (C_{r3} and C_{r4}) can be charged from one to two times of $v_{\text{sec(max)}}$. Therefore, the output voltage is regulated up to four times of the peak square-wave input voltage ($v_{\text{sec(max)}}$).

Since *LLC* resonant circuit drives the rectifier with a current source, a square wave of voltage appears at the input to the rectifier. The equivalent ac resistance R_{ac} for VD is given by

$$I_s(\text{rms})|_{VD} = \frac{\pi}{\sqrt{2}} I_o \tag{5}$$

$$V_s(\text{rms})|_{VD} = \frac{\sqrt{2}}{\pi} V_{o1} \tag{6}$$

$$R_{ac}|_{VD(S_x:\text{off})} = \frac{V_s(\text{rms})}{I_s(\text{rms})} = \frac{2}{\pi^2} R_L\,. \tag{7}$$

Similarly, the equivalent ac resistance for VQ is given by

$$R_{ac}|_{VQ(S_x:on)} = \frac{V_s(\text{rms})}{I_s(\text{rms})} = \frac{1}{2\pi^2} R_L\,. \tag{8}$$

Also, the equivalent ac resistance R_{ac} for PWM-VQ is

$$R_{ac}|_{\text{PWM}-VQ)} = \frac{V_s(\text{rms})}{I_s(\text{rms})} = {D_x}^2 \frac{2}{\pi^2} R_L \tag{9}$$

where D_x is the duty ratio of S_x. The voltage gain of each *LLC* resonant circuit is given by

$$\frac{V_p}{V_{res}} = \frac{1}{\sqrt{\left(1 + \frac{1}{k}\,(1 - \frac{1}{{\omega_r}^2})\right)^2 + \left(Q(\omega_r - \frac{1}{\omega_r})\right)^2}} \tag{10}$$

where V_p is the rms voltage of the primary-side transformer, and k is the ratio of the high-frequency transformer magnetizing inductance (L_m) to the resonant inductance (L_r) and is given by

$$k = \frac{L_m}{L_r}. \tag{11}$$

A typical voltage gain of *LLC* resonant tank was shown in Fig. 3. In addition to ω_0, there is also another resonant frequency in the *LLC* tank between $(L_r + L_m)$ and C_r

$$\omega_p = \frac{1}{\sqrt{(L_r + L_m)C_r}}. \tag{12}$$

At no load, the angular operating frequency ω, moves toward ω_p and as the load increases ω approaches ω_0. According to literature, the best operating points exist in the vicinity of the series resonant frequency (ω_0), where the benefits of the *LLC* converter are maximized. Since the magnetizing current (also called circulating current) flows only in the primary side, it does not contribute to the power transferred from the primary-side source to the secondary-side load. By operation of the converter around ω_0, the primary side presents a smaller circulating current in the resonant circuit which reduces the conduction loss [25]. However, the main challenge at these operating points is the light load regulation. Operation above the series resonant frequency may cause significant frequency increases under light-load conditions. In the proposed converter, however, the switching frequency maintain in a very narrow range by adaptively changing the configurations and employing hybrid control techniques.

In half bridge (Mode III), the asymmetrical square voltage generated at the output of inverter v_{res} can be represented by [26]

$$v_{\text{res}} = V_i d + \sum_{h=1}^{\infty} \left(\frac{\sqrt{2}\,V_i}{h\pi} \sqrt{1 - \cos\left(2h\pi D\right)} \sin\left(h\omega t + \theta_h\right) \right). \tag{13}$$

TABLE II
VOLTAGE GAIN IN EACH MODE OF OPERATION

Mode	Voltage Gain	Quality Factor
I	$\frac{V_{o1}}{V_i} = \frac{16m\sqrt{\sum_{h=1,3,5,\ldots}^{\infty}\left[\frac{1}{h}\sin(h\pi D)\sin(\frac{h\pi}{2})\right]^2}}{2\pi\sqrt{\left(1+\frac{1}{k}(1-\frac{1}{\omega_r^2})\right)^2 + \left(Q\,(\omega_r - \frac{1}{\omega_r})\right)^2}}$	$Q = \frac{2\pi^2 L_r \omega_0}{R_L}$
II		$Q = \frac{\pi^2 L_r \omega_0}{2{D_x}^2 R_L}$
III	$\frac{V_{o1}}{V_i} = \frac{4m\sqrt{\sum_{h=1}^{\infty}\left[\frac{1}{h}\sqrt{1-\cos(2h\pi D)}\right]^2}}{\pi\sqrt{\left(1+\frac{1}{k}(1-\frac{1}{\omega_r^2})\right)^2 + \left(Q\,(\omega_r - \frac{1}{\omega_r})\right)^2}}$	$Q = \frac{2\pi^2 L_r \omega_0}{R_L}$

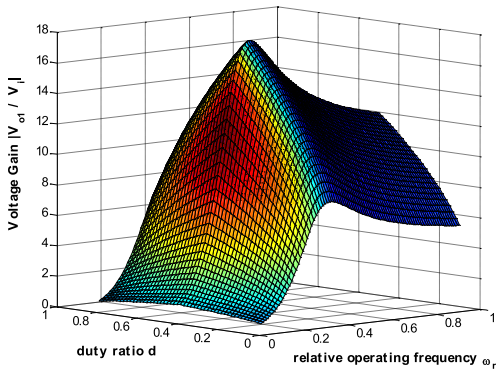


Fig. 10. Voltage gain in FB mode as a function of ω_r and D for $k = 7$, $Q = 0.3$.

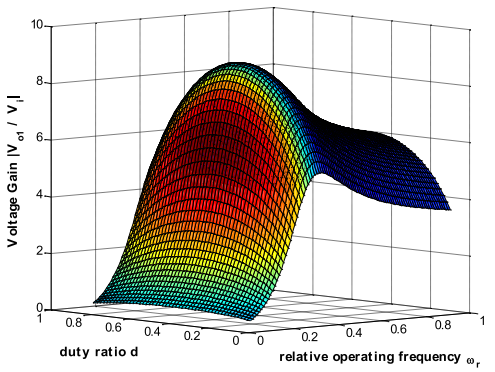


Fig. 11. Voltage gain in HB mode as a function of ω_r and D for $k = 7$, $Q = 0.3$.

Due to the dc blocking function of C_r in APWM modes (i.e., Mode III), only ac components of v_{res} are applied to the resonant circuit.

By finding the rms value of the input voltage to the resonant circuit (v_{res}), a high-frequency transformer with 1:m turns ratio, as well as considering different equivalent ac resistance R_{ac} for each mode of operation. The voltage gain in each mode of operation is presented in Table II.

A plot of voltage gain in Modes I and III as a function of duty ratio (D) and relative operating frequency (ω_r) are shown in Figs. 10 and 11, respectively. Comparing these figures shows that the sensitivity of the voltage gain to the duty ratio in FB mode

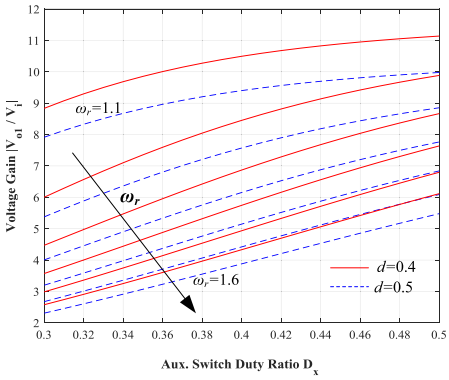


Fig. 12. Voltage gain in Mode II as a function of duty ratio in S_x (D_x).

is higher than HB mode. To be more precise, the derivative of voltage gain in Modes I and mode III with respect to the duty ratio (D) is given by (14). This equation shows that by changing the duty ratio in FB mode the rate of change in the voltage gain is $2\sqrt{2}$ higher than HB mode

$$\frac{\partial G_1}{\partial d}\Big/\frac{\partial G_3}{\partial d} = \frac{2\sqrt{1-\cos(2\pi D)}}{\sin(\pi D)} = \frac{2\sqrt{2}\,|\sin(\pi D)|}{\sin(\pi D)}\bigg|_{0<d<1} = 2\sqrt{2}. \tag{14}$$

When the converter operates in Mode II, the switching frequency and phase shift remain constant and only the duty ratio in the auxiliary switch (D_x) is used to regulate the output voltage. A plot of voltage gain in Mode II as a function of D_x is shown in Fig. 12. It can be observed that the voltage gain is almost linearly proportional to the duty ratio D_x.

B. ZVS Performance

The resonant current i_{res} in Mode I is derived from (1) and given by

$$i_{\text{res}} = \frac{4V_i}{\pi\,|Z_i|}\sum_{h=1,3,5,..}^{\infty}\left(\frac{1}{h}\sin(h\pi D)\sin\left(\frac{h\pi}{2}\right)\sin\left(h\omega t-\varphi_{Zi}\right)\right) \tag{15}$$

where $|Z_i|$ represents the magnitude of the input impedance of the resonant circuit and ϕ_{Zi} is the phase angle of the input impedance as follows:

$$|Z_i| = R_{ac}\sqrt{\left(\frac{(k\,Q\,\omega_r)^2}{1+(k\,Q\,\omega_r)^2}\right)^2+\left(\frac{k\,Q\,\omega_r}{1+(k\,Q\,\omega_r)^2}+Q\,\left(\omega_r-\frac{1}{\omega_r}\right)\right)^2} \tag{16}$$

$$\varphi_{Z_i} = \tan^{-1}\left(\frac{k\,Q\omega_r+Q\,\left(\omega_r-\frac{1}{\omega_r}\right)\left(1+(k\,Q\omega_r)^2\right)}{(k\,Q\omega_r)^2}\right). \tag{17}$$

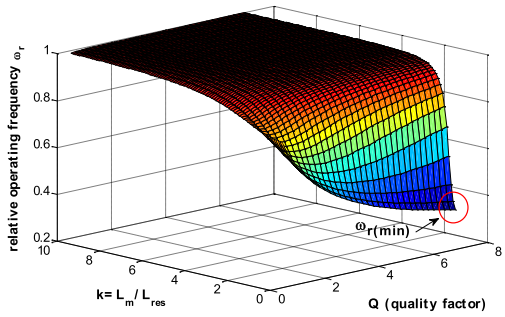


Fig. 13. Minimum relative operating frequency ω_r as a function of k and Q.

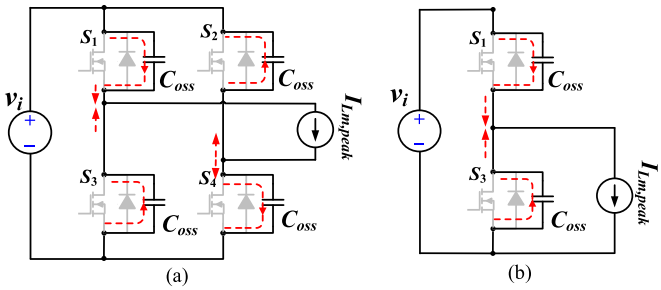


Fig. 14. Equivalent circuit during the dead time in (a) FB Modes (I, II) and (b) HB Modes (III).

The minimum relative angular operating frequency ($\omega_{r(\min)}$) is defined as the point that peak voltage gain is occurred. Thus, by finding the areas where the imaginary part of the input impedance Z_i equals zero (or $\phi_{Zi}=0$), $\omega_{r(\min)}$ can be found

$$\omega_{r(\min)} = \sqrt{\frac{k^2Q^2+\sqrt{k^4Q^4-2k^3Q^2+2k^2Q^2+k^2+2k+1}-k-1}{2k^2Q^2}}. \tag{18}$$

ZVS operation can be obtained by operating the converter in the inductive region or when $\omega_r > \omega_{r(\min)}$. A plot of (18) as a function of k and Q has been shown in Fig. 13. Considering the fact the converter should always operate in inductive region, the minimum switching frequency can be found at high quality factor values (maximum output power), low k ratio, and minimum input voltage. Typically, 10%–20% of the maximum output voltage gain is required as a margin to avoid the capacitive region [27]. Hence, (1.1–1.2)$\times\omega_{r(\min)}$ will be considered as the lower limit of operating frequency in the design procedure.

Since the increase of L_m reduces the circuiting current, L_m should be designed to be as large as possible. However, the upper limit of L_m can be found based on the ZVS requirements. Fig. 14 shows the equivalent circuit of both FB and HB modes during the dead time. The peak magnetizing current must discharge the MOSFET's output capacitance to zero during dead time to ensure ZVS. The maximum magnetizing currents can be calculated as

$$I_{Lm(\max)} = \begin{cases} \frac{V_i}{8L_m f_s} & for\ \ HB \\ \frac{V_i}{4L_m f_s} & for\ \ FB. \end{cases} \tag{19}$$

In order to improve the accuracy of analysis, the stray capacitances (C_{stray}), such as transformer primary-side parasitic

capacitance should be considered

$$I_{Lm(\max)} \cdot \frac{1}{f_s} \geq V_i \left(2C_{\text{oss}} + C_{\text{stray}}\right). \tag{20}$$

By substituting (20) in (19), the upper limit of magnetizing inductor for both FB and HB operating modes can be derived by

$$L_{Lm} \leq \frac{t_{\text{dead}}}{8\left(2C_{\text{oss}} + C_{\text{stray}}\right) f_{s(\max)}} \quad \text{for } HB \tag{21}$$

$$L_{Lm} \leq \frac{t_{\text{dead}}}{4\left(2C_{\text{oss}} + C_{\text{stray}}\right) f_{s(\max)}} \quad for\ FB. \tag{22}$$

As phase shift increases in PSM control mode, achieving ZVS is becoming more difficult for the lagging leg (S_2, S_4), whereas ZVS can be always obtained for the leading lag (S_1, S_3) assuming that the switching frequency is above the resonant frequency.

To turn ON S_2 and S_4 under ZVS, as shown in Fig. 5, the resonant current i_{res} should force the antiparallel diodes to conduct prior to the turn-ON instants of the switches. This means that the resonant current at $t = t_1$ must be negative ($i_{\text{res}}(t_1)<0$), or correspondingly resonant current at $t = t_5$ must be positive ($i_{\text{res}}(t_5)>0$). Considering the first harmonic approximation, the resonant current at $t = t_1$ can be determined from

$$i_{\text{res}}(t = t_1) = \frac{4V_i}{\pi\left|Z_i\right|} \sin(\pi D) \sin\left(\phi - \varphi_{Zi}\right) < 0 \rightarrow . \tag{23}$$

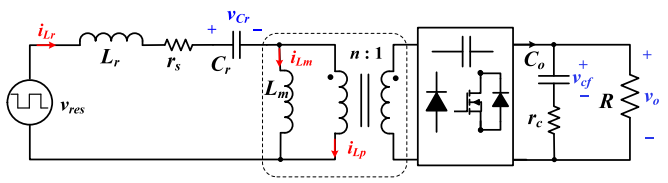


Fig. 15. Equivalent circuit of the proposed *LLC* resonant converter with PWM-VQ.

Hence, the upper limit of the phase shift ($\varphi_{\max}$) can be obtained by

$$\phi_{\max} = \tan^{-1}\left(\frac{k\,Q\,\omega_r + Q\left(\omega_r - \frac{1}{\omega_r}\right)\left(1 + \left(k\,Q\,\omega_r\right)^2\right)}{\left(k\,Q\,\omega_r\right)^2}\right). \tag{24}$$

C. Small Signal Model

Equivalent circuit of the proposed *LLC* resonant converter with PWM-VQ is shown in Fig. 15. To analyze the presented control algorithm, the small-signal model and the control-to-output transfer functions are obtained using extended describing function (EDF) [28]. After finding the steady-state solutions, the complete linearized small-signal models can be established by perturbing the system around operating points: $\omega_s = \Omega_s +$

$$A = \begin{bmatrix}
-\frac{r_s + R_{ac}\frac{I_{pc}^2}{I_{pp}^2}}{L_s} & -\frac{\Omega_s L_s + R_{ac}\frac{I_{ps}I_{pc}}{I_{pp}^2}}{L_s} & -\frac{1}{L_s} & 0 & \frac{R_{ac}\frac{I_{pc}^2}{I_{pp}^2}}{L_s} & -\frac{R_{ac}\frac{I_{ps}I_{pc}}{I_{pp}^2}}{L_s} & -\frac{\frac{4n}{\pi}\frac{I_{ps}}{I_{pp}}}{L_s} \\
\frac{r_s}{L_r}\cdot\frac{\alpha\beta}{(\alpha^2+\beta^2)} - \Omega_s & -\frac{R_{ac}}{L_r}\cdot\frac{\alpha^2}{(\alpha^2+\beta^2)} & 0 & -\frac{1}{L_s} & -\frac{R_{ac}\frac{I_{ps}I_{pc}}{I_{pp}^2}}{L_s} & \frac{R_{ac}\frac{I_{ps}^2}{I_{pp}^2}}{L_s} & -\frac{\frac{4n}{\pi}\frac{I_{pc}}{I_{pp}}}{L_s} \\
\frac{1}{C_s} & 0 & 0 & -\Omega_s & 0 & 0 & 0 \\
0 & \frac{1}{C_s} & \Omega_s & 0 & 0 & 0 & 0 \\
\frac{R_{ac}\frac{I_{pc}^2}{I_{pp}^2}}{L_m} & -\frac{R_{ac}\frac{I_{ps}I_{pc}}{I_{pp}^2}}{L_m} & 0 & 0 & -\frac{R_{ac}\frac{I_{pc}^2}{I_{pp}^2}}{L_m} & \frac{R_{ac}\frac{I_{ps}I_{pc}}{I_{pp}^2}}{L_m} + \Omega_s & \frac{\frac{4n}{\pi}\frac{I_{ps}}{I_{pp}}}{L_m} \\
-\frac{R_{ac}\frac{I_{ps}I_{pc}}{I_{pp}^2}}{L_m} & \frac{R_{ac}\frac{I_{ps}^2}{I_{pp}^2}}{L_m} & 0 & 0 & -\frac{R_{ac}\frac{I_{ps}I_{pc}}{I_{pp}^2}}{L_m} + \Omega_s & -\frac{R_{ac}\frac{I_{ps}^2}{I_{pp}^2}}{L_m} & -\frac{\frac{4n}{\pi}\frac{I_{pc}}{I_{pp}}}{L_m} \\
\frac{2n}{\pi C_f}\frac{I_{ps}}{\sqrt{{I_{ps}}^2+{I_{pc}}^2}}\frac{R}{R+r_c} & \frac{2n}{\pi C_f}\frac{I_{pc}}{\sqrt{{I_{ps}}^2+{I_{pc}}^2}}\frac{R}{R+r_c} & 0 & 0 & -\frac{2n}{\pi C_f}\frac{I_{ps}}{\sqrt{{I_{ps}}^2+{I_{pc}}^2}}\frac{R}{R+r_c} & -\frac{2n}{\pi C_f}\frac{I_{pc}}{\sqrt{{I_{ps}}^2+{I_{pc}}^2}}\frac{R}{R+r_c} & \frac{1}{C_f}\frac{1}{R+r_c}
\end{bmatrix}$$

$$B = \begin{bmatrix}
(-\omega_0 I_c) & \frac{4n}{\pi L_r}\sin\left(\frac{\pi d}{2}\right) \\
(\omega_0 I_s) & 0 \\
(-\omega_0 V_c) & \frac{4n}{\pi L_m}\sin\left(\frac{\pi d}{2}\right) \\
(\omega_0 V_s) & 0 \\
(-\omega_0 I_{mc}) & 0 \\
(\omega_0 I_{ms}) & 0 \\
0 & 0
\end{bmatrix}$$

$$C = \begin{bmatrix}
\frac{R\times r_c}{R+r_c}\frac{2n}{\pi}\frac{I_{ps}}{\sqrt{{I_{ps}}^2+{I_{pc}}^2}} & \frac{R\times r_c}{R+r_c}\frac{2n}{\pi}\frac{I_{pc}}{\sqrt{{I_{ps}}^2+{I_{pc}}^2}} & 0 & 0 & -\frac{R\times r_c}{R+r_c}\frac{2n}{\pi}\frac{I_{ps}}{\sqrt{{I_{ps}}^2+{I_{pc}}^2}} & -\frac{R\times r_c}{R+r_c}\frac{2n}{\pi}\frac{I_{pc}}{\sqrt{{I_{ps}}^2+{I_{pc}}^2}} & \frac{R}{R+r_c}
\end{bmatrix}, \quad D = 0 \tag{25}$$

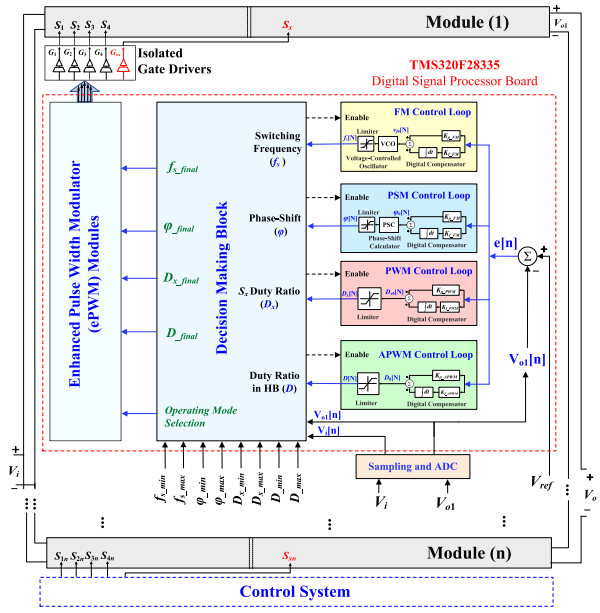


Fig. 16. Overall control system of the proposed converter.

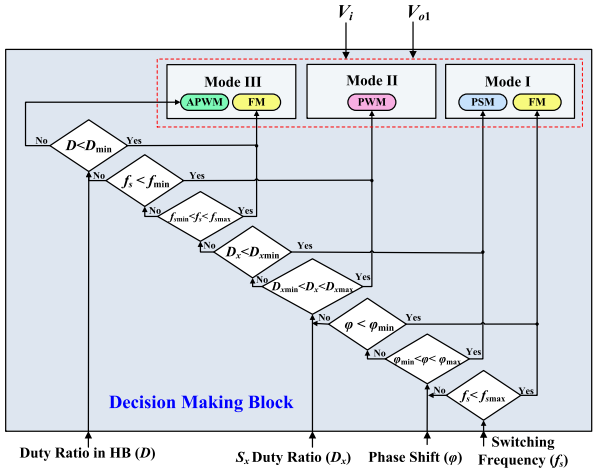


Fig. 17. Structure of the decision making block per module.

$\hat{\omega}_s$and $d = D + \hat{d}$. The small signal transfer function can be derived on the basis of the state-space method, where A, B, C, and D are given by (25) shown at the bottom of the next page. Hence, the control to output transfer functions with respect to switching frequency and duty ratio can be expressed

$$G_{v\omega}(s) = \left.\frac{\hat{v}_o(s)}{\hat{\omega}_{sn}(s)}\right|_{\hat{d}(s)=0} = C(1,:)\,(sI - A)^{-1}\,B(1,:) \tag{26}$$

$$G_{vd}(s) = \left.\frac{\hat{v}_o(s)}{\hat{d}(s)}\right|_{\hat{\omega}_{sn}(s)=0} = C(1,:)\,(sI - A)^{-1}\,B(2,:). \tag{27}$$

For Mode II that operates with S_x duty ratio control, the operating frequency and phase shift are kept constant. It was

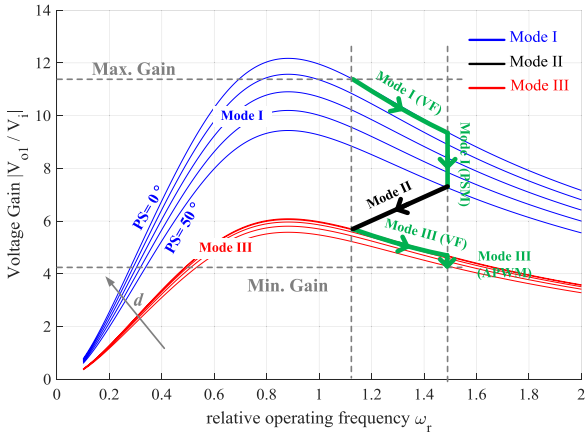


Fig. 18. Voltage gains and operation region at different duty ratios and $Q = 1.2$ for each mode of operation versus the conventional *LLC*.

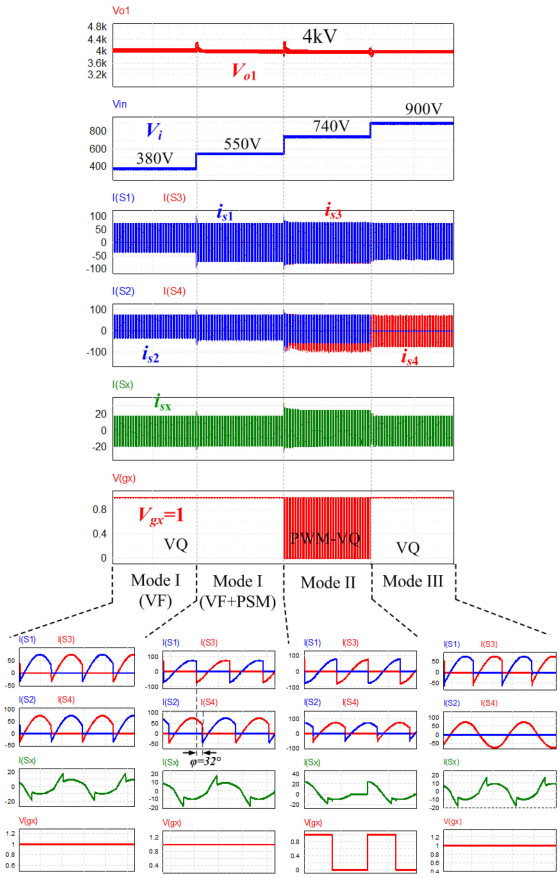


Fig. 19. (a) Dynamic response and steady-state waveforms in high power PSIM simulation.

shown that the equivalent ac resistance is a function of D_x and the voltage gain is almost linearly proportional to the D_x.

D. Control Design

The modular structure of the proposed converter along with the decision-making block have been demonstrated in Figs. 16 and 17, respectively.

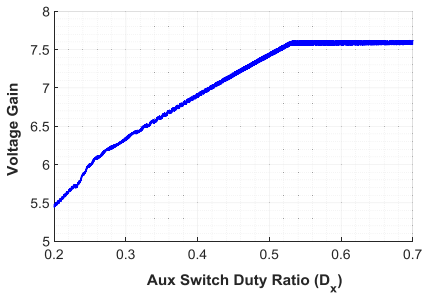


Fig. 20. Voltage gain as a function of aux. switch duty ratio D_x.

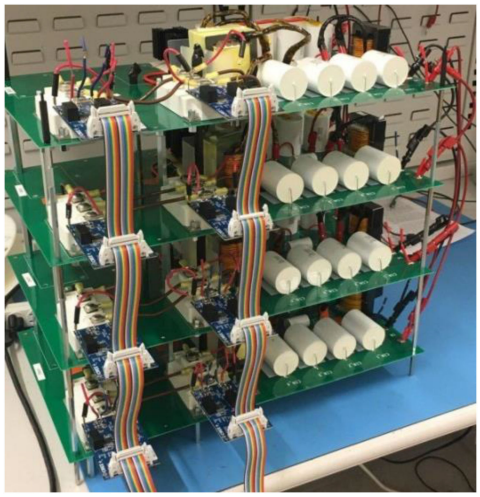
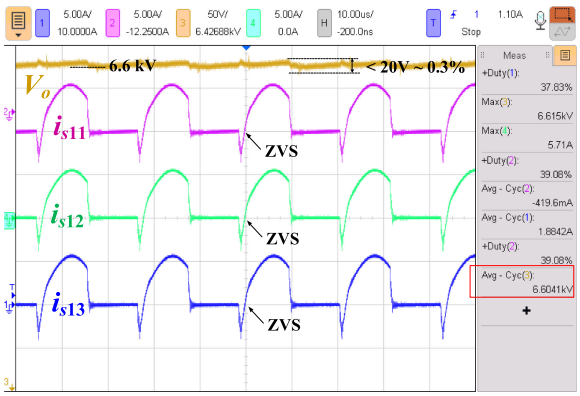


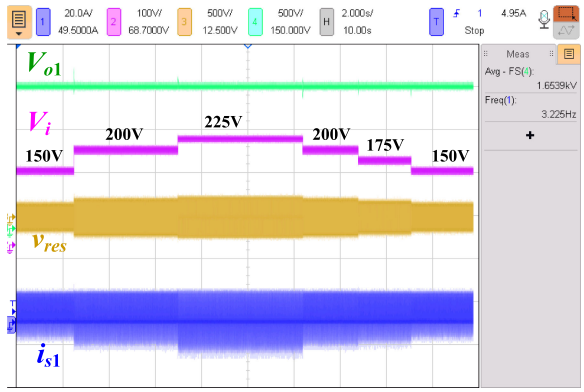
Fig. 21. Photograph of the modular experimental prototype.



[V_o: 1kV/div; i_{s11}, i_{s12}, i_{s13}: 10A/div; time: 10μs/div]

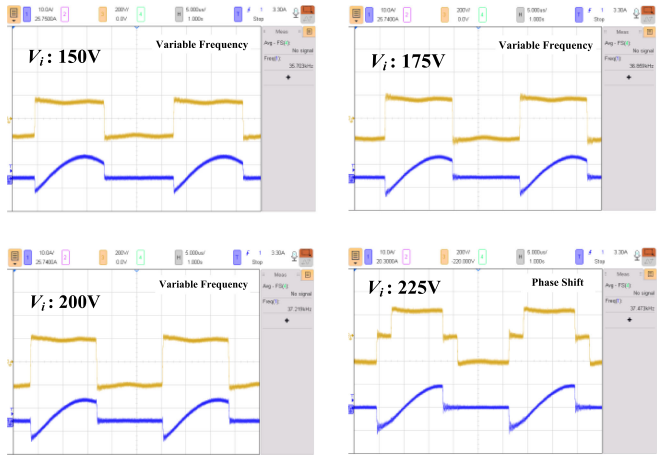
Fig. 22. Measured switching waveforms of modules with 6.6-kV output.

In the proposed control system, four digital control loops [1) frequency modulation (FM), 2) phase shift modulation (PSM), 3) duty ratio control of S_x, 4) APWM] have been developed to regulate the output voltage, where each module has its own dedicated control system. TSM320F28335 Digital Signal Controller with enhanced PWM (ePWM) peripherals is used to implement the control structure and generate the required gate signals. Among four abovementioned loops, variable frequency has been considered to be the primary control method.



[V_{o1}: 500V/div; V_i: 100V/div; v_{res}: 500V/div; i_{s1}: 20A/div; time: 2s/div]

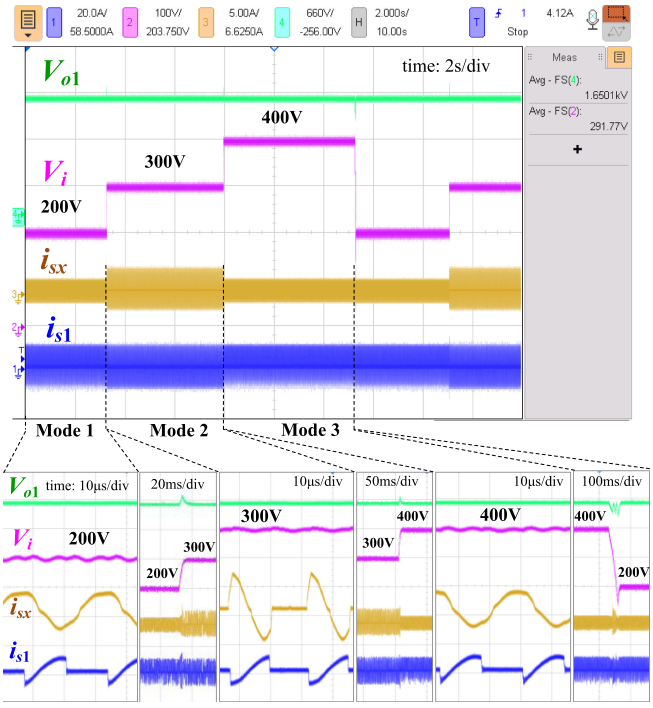
(a)



(b)

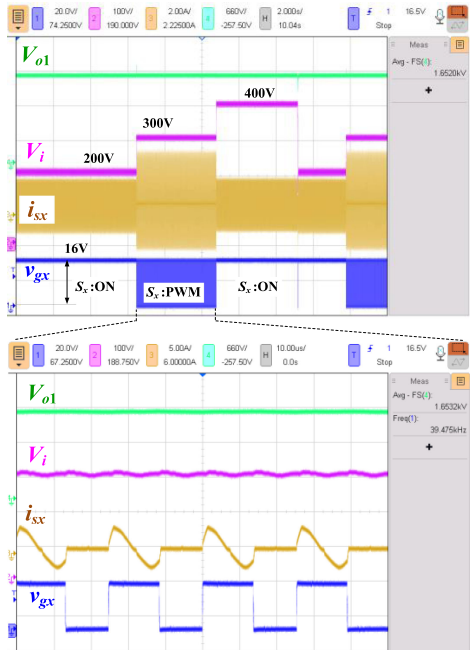
Fig. 23. Dynamic performance of the proposed converter in Mode I: FB, with variable frequency and PSMs.

The mode of operation in the control system is selected according to the input voltage, the reference output, and the output voltage. The initial mode of operation in the inverting block is set to FB and in the rectifying block is set to VQ. In Mode I, as shown in Fig. 17, FM and PSM have been employed. Frequency modulation is first employed to regulate the output voltage for a portion of the loading condition. As the converter gain is reduced further, the switching frequency reaches the upper limit ($f_{s\max}$). At this point the control system is switched from VF to PSM control in the same mode of operation, while the switching frequency stays constant at its maximum value ($f_{s\max}$). By changing the phase shift between the inverting legs (φ) from $\varphi_{\min}$ to $\varphi_{\max}$ the output voltage is regulated. By further reducing the converter gain, the phase shift reaches its upper limit ($\varphi_{\max}$) and the mode of operation switches from Mode I to Mode II, where the phase shift is kept constant and a PWM signal is applied to the auxiliary switch in the rectifying block and the duty ratio of S_x (D_x) is controlled to regulate the output voltage. During this mode, if the duty ratio exceeds its limit ($D_{x\max}$), the mode of operation switches from II to III. In Mode III, the operation in the inverting block is set to HB and the auxiliary switch in the rectifying block is switched ON, while the output voltage is regulated once again by means of



[V_{o1}: 660V/div; V_i: 100V/div; i_{sx}: 5A/div; i_{s1}: 20A/div]

Fig. 24. Dynamic performance and smooth transition between three modes of operations.



Upper :[V_{o1}: 660V/div; V_i: 100V/div; i_{sx}: 5A/div; v_{gx}: 20V/div; time: 2s/div]
Lower :[V_{o1}: 660V/div; V_i: 100V/div; i_{sx}: 5A/div; v_{gx}: 20V/div; time: 2s/div]

Fig. 25. Performance of the proposed converter in different modes of operation along with the auxiliary switch waveforms.

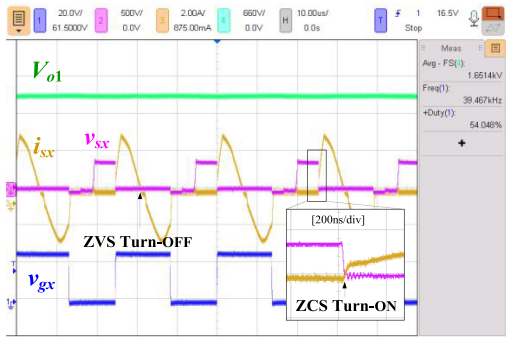
the variable frequency control. In the same manner, by further reducing the converter gain and with the switching frequency exceeding the upper limit, the control loop shifts from variable frequency to APWM control. In APWM control, the duty ratio D (shown in Fig. 5) is used to regulate the output voltage.

The corresponding voltage gain curves in three operation modes are plotted in Fig. 18. It can be observed that the switching frequency range in the proposed converter is significantly narrower than conventional operation region. With the squeezed frequency range, parameter design of resonant components is easier and L_m can be larger so the primary-side circulating current is reduced. In addition, in the proposed control system, since individual controller is being used to control the output voltage of each module, all the output capacitor voltages are balanced.

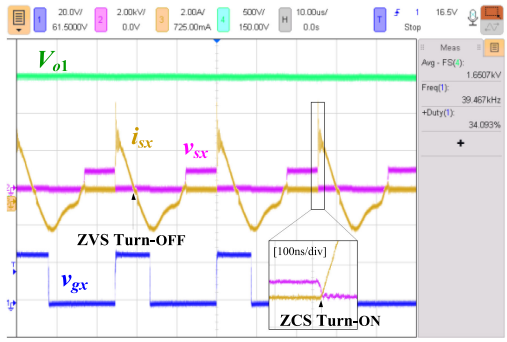
IV. Simulations and Experimental Results

A. Full-Scale Simulation Verification

To illustrate the performance of proposed converter, an 80-kW modular dc–dc converter with four modules is simulated in PSIM. The input voltage ranges 360 V–1 kV, while the output voltage is regulated at 16 kV. Table III contains detailed information on the specifications and circuit components. The dynamic performance and key simulation results of the converter at steady-state full-load are shown in Fig. 19. It can be observed that by applying the step voltages in the input, the circuit can smoothly change the modes of operation. With changes from 380 to 550 V, the converter remains in Mode I, while the switching

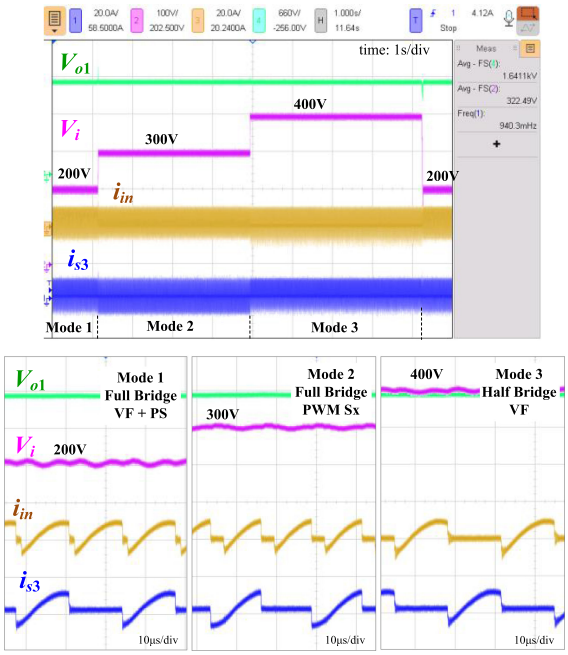


(a)



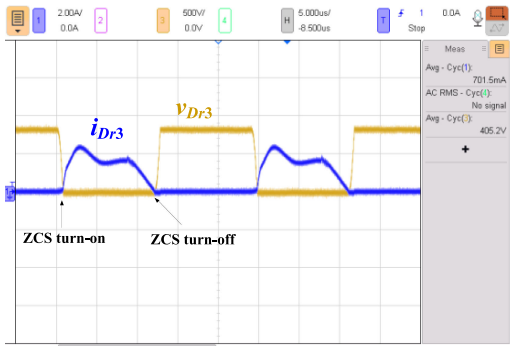
(b)

Fig. 26. Auxiliary switch S_x waveforms. (a) Full load. (b) Reduced load. (a) [V_{o1}: 660 V/div; V_{sx}: 500 V/div; i_{sx}: 2 A/div; V_{gsx}: 20 V/div; time: 10 μs/div; time (zoom-box): 200 ns/div]. (b) [V_{o1}: 500 V/div; V_{sx}: 2 kV/div; i_{sx}: 2 A/div; V_{gsx}: 20 V/div; time: 10 μs/div; time (zoom-box): 200 ns/div].



[V_{o1}: 660V/div; V_i: 100V/div; i_{in}: 20A/div; i_{s3}: 20A/div; time (upper): 1s/div; time (lower): 10µs/div]

Fig. 27. Performance of the converter in different modes of operation.



[v_{Dr1}: 500V/div; i_{Dr3}: 2A/div; time: 5µs/div]

Fig. 28. Measured SiC diode waveforms in voltage quadrupler.

frequency changes from 35.5 to 37 kHz (f_{smax}) and 32° phase shift is applied to the inverter to regulate each converter module at 4 kV. By applying the next step voltage, input voltage is increased to 740 V. Since increasing the phase shift to the 50° ($\varphi_{\max}$) is insufficient to regulate the output voltage, the converter switches to Mode II, where a PWM signal is applied to the auxiliary switch. In the last step voltage (V_i = 900 V), the primary-side FB inverter is reconfigured to the HB and smoothly transitions to Mode III. Voltage gain in Mode II of the high power simulation is shown in Fig. 20. It can be seen that similar to Fig. 12, voltage gain is almost linearly proportional to the aux. switch duty ratio D_x until it reaches its maximum voltage gain.

B. Scaled-Down Experimental Verification

A 150–400 V/6.6-kV proof-of-concept prototype that consists of four modules has been built and tested to validate the functionalities of the proposed converter. The switching frequency is

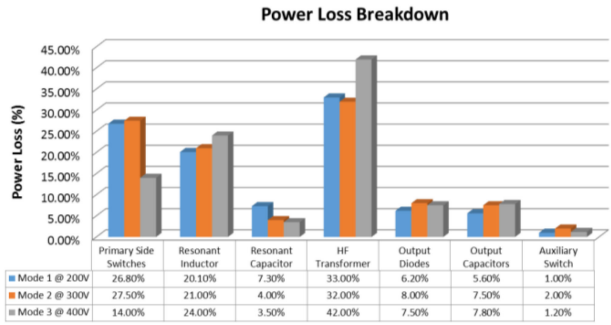


Fig. 29. Power loss breakdown per module at different modes of operations.

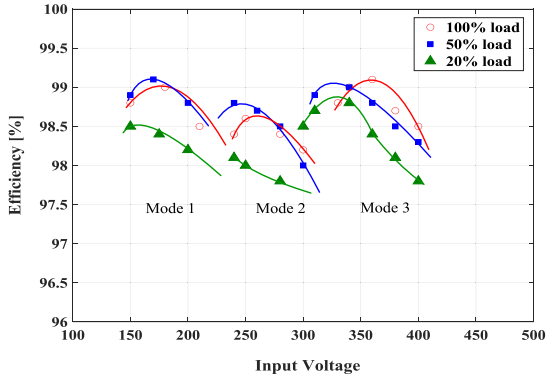
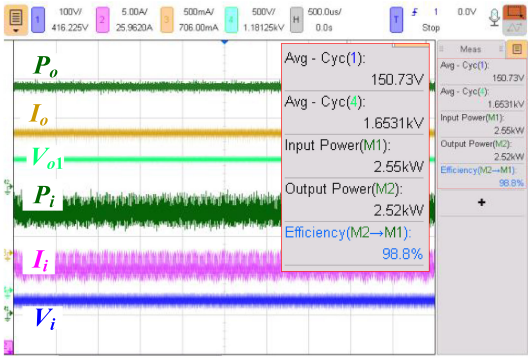


Fig. 30. Measured efficiency of the experimental prototype.

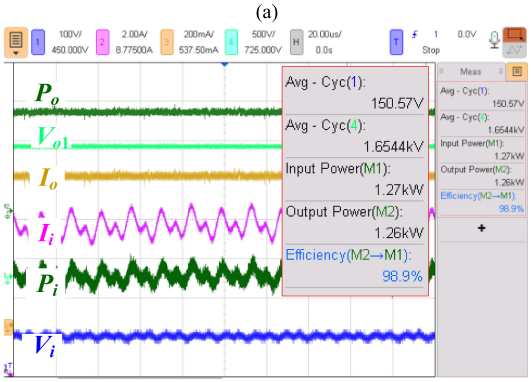
in the range of 35–37.5 kHz. A photograph of the experimental prototype is shown in Fig. 21.

The prototype was tested at different input voltages and loading conditions. Fig. 23 shows the switch current in different modules and the 6.6k-V output voltage with less than 0.3% ripple. This figure also verifies the balanced operation of the modular system with identical current sharing for each module. The performance of the proposed converter in Mode I (FB + VQ) with variable frequency and PSMs has been shown in Fig. 23. It can be observed that by increasing the input voltage first variable frequency is used to regulate the output voltage at 1.65 kV (per module). Once the switching frequency reaches its maximum (f_{smax} = 37.5 kHz) PSM modulation is employed. Soft switching is obtained for switches in both leg 1 and leg 2.

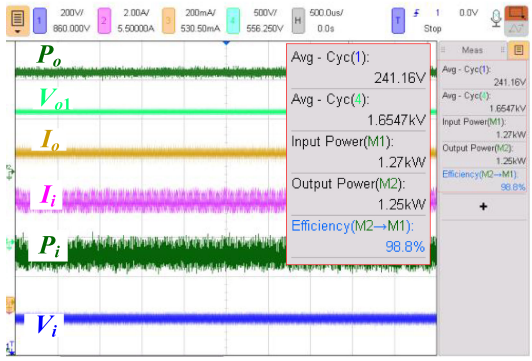
The dynamic performance, smooth transition between three modes of operations as well as steady-state waveforms of switches S_1 and auxiliary switch S_x are shown in Fig. 24. With a step change from 200 to 300 V, the converter smoothly switches from Mode 1 to Mode 2. By applying another step change in the input to 400 V the converter transitions to Mode 3. It can be observed that soft switching is always maintained. Changing from voltage quadrupler in Mode 1 to PWM-VQ can be also detected from the S_x gating signal that is illustrated in Fig. 25. Soft switching performance of the SiC auxiliary MOSFET (ZVS turn-OFF and zero current switching (ZCS) turn-ON) at full-load and reduced-load conditions can be observed in Fig. 26. Transition in the primary-side inverter (from FB in Mode 1 or 2 to HB in Mode 3) can be realized from the input current i_{in} in Fig. 27. The SiC Schottky diode waveforms employed in the



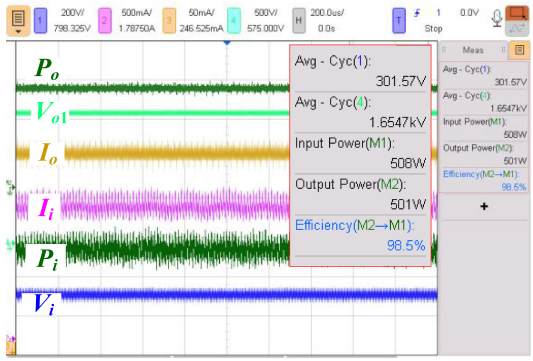
[V_{o1}: 500V/div; I_o: 0.5A/div; V_i: 100V/div; I_i: 5A/div; time: 500μs/div]
(a)



[V_{o1}: 500V/div; I_o: 0.2A/div; V_i: 100V/div; I_i: 2A/div; time: 20μs/div]
(b)



[V_{o1}: 500V/div; I_o: 0.2A/div; V_i: 200V/div; I_i: 2A/div; time: 500μs/div]
(c)



[V_{o1}: 500V/div; I_o: 50mA/div; V_i: 200V/div; I_i: 0.5A/div; time: 200μs/div]
(d)

Fig. 31. Per module efficiency of the converter at different loading conditions and input voltages. (a) $V_i = 150$ V, full-load (2.5 kW per module). (b) $V_i = 150$ V, half load (1.25 kW per module). (c) $V_i = 240$ V, half load (1.25-kW per module). (d) $V_i = 300$ V, 20% load (500 W per module).

TABLE III
CIRCUIT SPECIFICATIONS AND COMPONENTS IN THE EXPERIMENTAL PROTOTYPE

SPECIFICATIONS			
		PROTOTYPE	HIGH POWER SIMULATIONS
Rated Power		10 kW (2.5kW per module)	80 kW (20kW per module)
DC Input Voltage V_i		150V – 400 V_{DC}	360V – 1 kV_{DC}
Output Medium Voltage V_o		6.6 kV_{DC} (1.65 kV per module)	16 kV_{DC} (4 kV per module)
Voltage Ripple % ($\Delta V_o / V_o$)		~ 0.3%	~ 0.5%
Output Voltage Overshoot		6.6 – 8%	4.5 – 5%
Number of Modules n		4	4
Input Voltage (Voltage Gain)	Mode I	V_i: 150-240V (Gain: 11-6.9)	V_i: 360-600V (Gain: 11-6.7)
	Mode II	V_i: 240-330 (Gain: 6.9-5)	V_i: 600-750V (Gain: 6.9-5.3)
	Mode III	V_i: 330-400 (Gain: 5-4.1)	V_i: 750-1000V (Gain: 5.3-4)
Min and Max switching frequencies (f_{smin} - f_{smax})		35-37.5kHz	35.5-37kHz
Max phase shift (φ_{max})		50°	50°
CIRCUIT COMPONENTS			
		PROTOTYPE	HIGH POWER SIMULATIONS
SiC MOSFET Modules S_{11}~ S_{14}		CAS120M12BM2 *Wolfspeed* 1200V, 193A	CAS120M12BM2 *Wolfspeed* 1200V, 193A
Gate Driver		CGD15HB62P1 *Wolfspeed*	-
Resonant Capacitors C_{r1}~ C_m		942C16P1K-F (0.1μF, 1.6kV)	B25835T2104K7 (0.1μF, 3kV)
High Freq. Transformers L_{m1}~ L_{mn}		1.5mH (1:3) N87: 2×E65/32/27	1.5mH (1:3)
Resonant Inductors L_{r1}~ L_{rn}		211μH N87: E55/28/21	211μH
SiC Schottky Diodes D_{r1}~ D_{r4}		GB05MPS17-247, *GeneSiC* (1.7kV, 13A)	GB05MPS33-263 × *GeneSiC* (3.3kV, 14A)
Auxiliary SiC MOSFET S_x		C2M0045170D *Cree/Wolfspeed* 1700V, 72A	G2R120MT33J *GeneSiC* (3.3kV, 35A)
Output Capacitors C_{11}~ C_{n2}		4 × 940C20W1K-F (1μF, 2 kV)	4 × T50W1NR-F (1μF, 5 kV)
DSP Controller		TMS320F28335	-

voltage quadrupler rectifier is shown in Fig. 28 that can obtain ZCS turn-ON and turn-OFF.

Fig. 29 shows the power loss breakdown of the key components per module in the converter.

In the proposed converter, soft switching has been achieved for all semiconductors for a wide range of voltage gain and loading conditions. Hence, the majority of the power loss is because of the conduction loss of the components and the core loss in the magnetics.

Fig. 30 shows the efficiency of the experimental prototype at different input voltages (150–400 V) and loading conditions (20%, 50%, and 100%). The captured efficiency at some operating points is shown in Fig. 31.

A comparison between the proposed topology and some recently reported *LLC*-derived wide gain range topologies is presented in Table IV. As shown, the proposed topology is featured

TABLE IV
COMPARISON WITH STATE-OF-THE-ART WIDE GAIN RANGE LLC TOPOLOGIES

Topology	Number of						Modulation	f_{smax}/f_{smin}	Input Voltage	Output Voltage	Tested Power Range	Efficiency Range
	Switches	Diodes	Additional Component	L_r	C_r	Transformer						
FB-Three Level LLC [29]	6	6	0	2	1	1	PSM + PWM	1	385V	225-378V	0.7-6.6kW	94.7-98.1%
Dual-Transformer-Based DAB [30]	6	0	0	1	2	2	PSM + PWM	1	120-240V	96V	0.1-1kW	90-95%
Interleaved FB-LLC with hybrid rectifier [31]	8	6	0	2	2	2	FM + PSM	~2	400V	150-500V	0.7-3.5kW	94-98%
A Structure-Reconfigurable Series Resonant [15]	5	3	2	1	1	1	PWM	1	30-60V	200/400V	50-500W	92-97%
Proposed Multi-Mode *LLC* (this work)	4	4	1	1	1	1	FM + PSM + APWM	1.1	150-400V	1.65kV (per module)	500W-2.5kW (per module)	97.8-99.1%

with moderate MOSFETs and diodes counts, with comparatively narrow switching frequency range. Compared with the literature, the proposed topology demonstrates very high efficiency (at least 97.8%) for a wide range of voltage gain and load conditions.

V. CONCLUSION

In this article, a very high-efficiency modular reconfigurable multimode *LLC* converter has been presented for wide voltage gain application in MVdc grid system. Three distinct operating modes have been presented in this work step-up *LLC* resonant converter application. By reconfiguring the *LLC* converter module with a mode change from hybrid control scheme that uses variable frequency and phase-shift control to PWM control of the auxiliary switch in the output voltage quadrupler, as well as providing the option to switch the input bridge circuit to HB mode, the proposed approach has shown to be able to maintain very high power efficiency for a wide range of input voltage and loading conditions. The detailed descriptions and theoretical analysis of each operating mode have been discussed in this article.

To verify the functionalities of the proposed modes of operation in *LLC* step-up resonant converter, both steady-state and dynamic performance have been provided on a high power 80 kW, 360 V–1 kV/16-kV system, and a laboratory scale 150–400 V/6.6 kV, 10-kW SiC hardware prototype. Final results confirmed that the proposed design was able to maintain an efficiency between 97.8% and 99.1% for a wide range of loading conditions. Future works will be conducted on optimizing the overall dynamic performance of step-up converter system.

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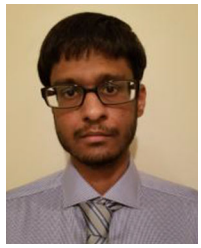

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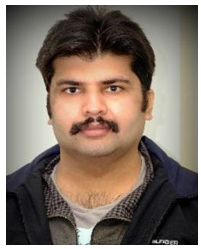

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