A Simple Model Predictive Instantaneous Current Control for Single-Phase PWM Converters in Stationary Reference Frame

Lin Peng, Lei Ma, *Member, IEEE*, Wensheng Song, *Member, IEEE*, and Haoran Liu

***Abstract*—The traditional proportional–integral (PI) based current control for single-phase pulsewidth-modulation (PWM) converters in railway traction applications either has a steady-state error or a poor dynamic response. Deadbeat instantaneous current control (ICC) cannot eliminate the steady-state error due to approximation errors of the linear extrapolation. Compared with PI-based direct current control, continuous-control-set (CCS) model predictive control (MPC) implemented in a *d-q* frame offers better performance, but its dynamic response is still slower than ICC. To solve these problems, a simple model predictive (MP) ICC scheme for single-phase PWM converters is proposed in this article. The optimal modulation function is calculated in the stationary reference frame by the CCS-MPC principle without β-axis current estimation and reference frame transformation. The proposed MP-ICC scheme can keep the fast dynamic response characteristics of ICC and achieve zero steady-state error. In addition, it has the advantages of low current harmonics and low computational complexity. The influence of the inductance parameter mismatch on the current loop is analyzed in detail, and a phasor-method-based inductance parameter online estimation is developed. This solution can be executed during the idle time of the digital processor without making the control delay longer. Finally, a comprehensive experimental comparison with four existing current control schemes is conducted to verify the feasibility and effectiveness of the proposed scheme.**

***Index Terms*—Model predictive instantaneous current control (MP-ICC), modulation function optimization, parameter sensitivity, single-phase pulsewidth-modulation (PWM) converter, stationary reference frame.**

I. Introduction

COMPARED with a traditional diode or thyristor converters, the single-phase pulsewidth-modulation (PWM) converter has advantages of high-power factor, low current harmonics, and bidirectional flow of energy. It is the key component in the control structure of many grid-interfaced systems including renewable energy [1], [2], uninterruptible power supplies [3], electric railway traction systems [4], and power electronic transformers [5]. PWM converters are normally controlled by a classical dual closed-loop system, that is, the outer loop for dc-link voltage regulation and the inner loop for line current regulation. Among them, the performance of the current loop is essential to achieve a sinusoidal line current with low harmonic distortion [6].

Over the years, various current control strategies have been proposed. Based on whether a separate modulator is employed, these schemes can be classified into two main categories. The first category schemes without a modulator can track the reference current by directly generating the switching state and achieve fast dynamic performance [6], [7], such as hysteresis current control [8] and finite-control-set model predictive control (MPC) [9], [10]. However, a significant shortcoming is that the unfixed switching frequency will result in a difficult filter design. The second category schemes with a modulator can achieve the fixed switching frequency to reduce current ripples, such as proportional–integral (PI) based control [11]–[14], proportional–resonant (PR) based control [16], deadbeat (DB) control [17], and continuous-control-set MPC (CCS-MPC) [18]–[23]. Among them, the PI-based current control strategies have been widely applied for single-phase PWM converters in railway traction applications [12], [14].

The current control strategies with a modulator are normally based on the average model. According to the reference frame of controller operation, these schemes can be categorized into the following two classes.

1) Stationary reference frame control, such as PI-based instantaneous current control (ICC) [11], [12], PR-based ICC, and DB-ICC. Among them, PI-based or DB-ICC offers a fast dynamic response, but there is a steady-state error due to the low-order controller or approximation errors of the linear extrapolation. PR-based ICC eliminates the steady-state error by a high-order controller with an infinite gain at the target (resonant) frequency, but it is sensitive to small variations in the grid-side frequency [16].

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2) Direct-quadrature (*d-q*) synchronous reference frame control, also known as *d-q* control, such as PI-based direct current control (DCC) [13], [14] and CCS-MPC based on the *d-q* frame. Among them, PI-based DCC uses two PI controllers to track active (*d*-axis) and reactive (*q*-axis) currents in the *d-q* frame, respectively, and achieve zero steady-state error. However, the dynamic response of PI-based DCC is slow, and the parameters tuning of multiple PI controllers is a cumbersome process [15].

MPC has gained more and more attention in PWM converters thanks to its simplicity and superior control performance. Among diverse MPC schemes, CCS-MPC aims to predict and optimize the modulation function and can realize the fixed switching frequency with modulators. The main disadvantage of CCS-MPC is heavy online computation caused by solving system constraints [18]. Some alternative schemes have been proposed to deal with part or all of the optimization problems offline to reduce computation burden [19]–[24]. Many existing CCS-MPC schemes for single-phase PWM converters are realized in the *d-q* frame [22]–[24]. Compared with PI-based DCC, these control strategies can provide better steady-state performance and faster dynamic response. However, in the *d-q* control for single-phase PWM converters, the imaginary (β)-axis signal must be created to establish a two-phase (α-β) stationary frame to realize reference frame transformation. This will increase the complexity of the controller structure and degrade the dynamic performance of the current loop [13]. Therefore, compared with the stationary-reference frame control, such as ICC, although *d-q* control strategies can achieve zero steady-state error by low-order controllers, the dynamic performance is slower.

Synchronous sampling technology has been widely used in digital processors to obtain high control accuracy. Signals are sampled at the peak and/or valley of the triangular carrier to detect the average current excluding the switching noise [25]–[27]. The control delay between sampling and duty-cycle-updating will affect the robust performance of the current loop and should be as small as possible [28]. The control delay in the regular sampling is one or half carrier period [27]. DB control can be used to compensate for the control delay, but it is sensitive to system parameters [17]. A real-time computation method with dual sampling mode in [29] is proposed to reduce the control delay to a quarter of the carrier period. The traditional multisampling method in [30] can reduce control delay to be close to the computational duration, that is, the sum of sampling and modulation function calculation. However, duty-cycle-updating is executed multiple times in one carrier period, so the switching noise will be introduced into the current loop and the switching frequency may be increased. In contrast, the multisampling method with a minimum sampling interval in [23] and [31] increases the update frequency of the modulation function value through the high sampling frequency, the duty cycle is still updated at the peak and valley of the triangular carrier. In this way, the switching frequency is constant, and the switching noise can be avoided. However, the control delay is still determined by the computational burden, so simplifying the control scheme can further increase the sampling frequency to improve the control accuracy of the system.

It is well known that parameter mismatch (especially the grid-side inductance) is a problem that MPC must solve. Various inductance parameter identification and estimation methods have been reported in [20]–[24]. Luenberger observer and least-squares estimation were proposed in [20] and [21], but their implementation in digital controllers is complicated. Some simplified methods based on the controller characteristics were proposed in [22]–[24]. However, these methods are realized in the *d-q* frame, and the two proposed methods in [22] and [23] are only available for the PWM rectifier with a unity power factor. Meanwhile, the execution period of these methods is the same as the sampling period, which leads to a longer control delay.

In this article, a simple model predictive ICC (MP-ICC) scheme for the single-phase PWM converter in a stationary reference frame is proposed to achieve zero steady-state error. The proposed scheme determines the cost function with the CCS-MPC principle, and then, the optimal modulation function is predicted by minimizing the cost function, thereby simplifying controller structure, eliminating approximation error, and retaining fast dynamic response. The influence of the inductance parameter mismatch on the current loop is analyzed in detail, and a phasor-method-based inductance parameter online estimation solution is proposed to improve the robustness of the current control loop. The proposed solution is suitable for any operating mode and can be executed during the idle time of the digital processor, so the control delay will not become longer. To verify the advantages of the proposed scheme, the proposed scheme and four exiting current control strategies are tested and compared on a single-phase two-level converter experimental prototype. The involved methods are PI-based ICC [11], DB-ICC [17], PI-based DCC [13], and model predictive DCC (MP-DCC). Among them, MP-DCC is derived from a model predictive direct power control strategy reported in [22] to facilitate the comparison of the performance of the current loop.

The rest of this article is organized as follows. The system configuration and mathematical model of a single-phase two-level PWM converter are described in Section II. The MP-ICC scheme is proposed in Section III. In Section IV, the inductance parameter mismatch is analyzed, and a phasor-method-based inductance parameter online estimation solution is presented. In Section V, the control diagram and flowchart of the proposed MP-ICC scheme are described. The experimental results are presented and discussed in Section VI. Finally, Section VII concludes this article.

II. System Description and Mathematical Model

The equivalent circuit topology of a single-phase two-level PWM converter with a unipolar sinusoidal PWM (SPWM) modulator in the China railways high-speed electric multiple units (EMUs) is depicted in Fig. 1 [14], where R and L are the equivalent resistance and inductance of the grid-side, respectively. R_{L} is the equivalent resistance load of the dc-link connected with the filter capacitance C_{d}. Four power switches S_1–S_4 with antiparallel diodes are used to generate two voltage levels on the converter's leg-a and -b. u_{m} is the modulation function output

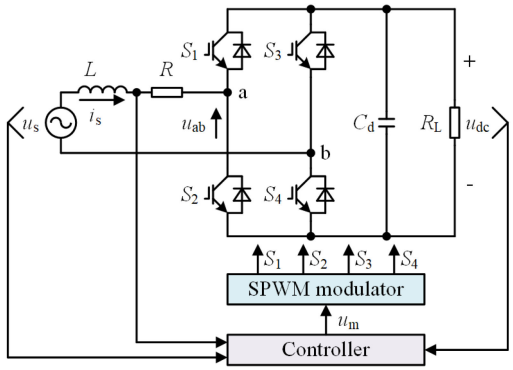

Fig. 1. Topology of the single-phase PWM converter with a modulator.

by the controller, which is used as the input of the modulator to generate the pulsed voltage to drive power switches.

The grid-side equivalent resistance R is usually very small, so it can be ignored. Applying Kirchhoff's voltage law (KVL) to the grid-side loop, the voltage equation can be written as

$$u_{ab} = u_s - L\frac{di_s}{dt} \tag{1}$$

where u_s, i_s, and u_{ab} represent the grid-side voltage, line current, and H-bridge input voltage, respectively.

The PWM modulator can be modeled as a unity gain [14], the relationship between u_{ab}, the dc-link voltage u_{dc}, and the modulation function u_m can be expressed as

$$u_{ab} = u_m u_{dc}. \tag{2}$$

Substituting (2) into (1), u_m is derived as

$$u_m = \frac{1}{u_{dc}}(u_s - L\frac{di_s}{dt}). \tag{3}$$

III. Model Predictive ICC

A. Instantaneous Current Prediction

The SPWM modulator in Fig. 1 is configured in a double-update mode, and the multisampling method with minimum sampling interval in [23] and [31] is adopted. The sampling and duty-cycle-updating process are shown in Fig. 2, where u_t is the triangular carrier. v_a and v_b represent the state of the converter's leg-a and -b, respectively. i_{ave} is the idea line current without ripple when the modulating function is u_m. T_{PWM} is the carrier period. T_c is the duty-cycle-updating period and is equal to half of T_{PWM}. T_s is the sampling period. n represents the nth sampling instant. k represents the kth duty-cycle-updating instant. The relationship between n and k is defined as

$$n = gk, (g = T_c/T_s) \tag{4}$$

where g is an integer to keep the sampling synchronized with the duty-cycle-updating.

As shown in Fig. 2, sampling and modulation function calculation are performed in each sampling period, and then, the obtained modulation function value is immediately written into the shadow register of the PWM module of the digital controller.

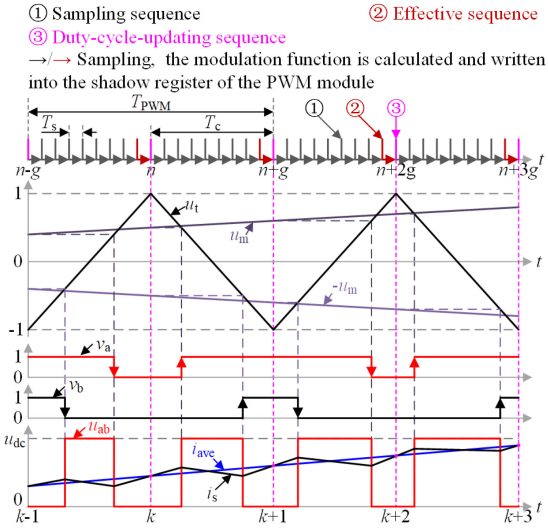

Fig. 2. Sampling and duty-cycle-updating process.

According to the update rule of the double-update mode, only the latest modulation function value $u_m(n-1)$ can be effectively applied to the converter at the kth duty-cycle-updating instant. When T_s is very small, the error between $u_m(n-1)$ and $u_m(k)$ can be ignored, synchronous sampling is realized, and the duty-cycle-updating period T_c is the actual control period of the current loop.

Based on the synchronous sampling and PWM modulation principle, the sampled current $i_s(k)$ equals the average current $i_{ave}(k)$ at the kth instant [31]. Considering that the control period T_c is much smaller than the fundamental period of the grid-side voltage u_s, a good discretization accuracy can be obtained by the linearization model discretized with T_c. The Euler forward approximation is applied to (3), and the instantaneous current $i_s(k+1)$ at the $(k+1)$th control instant is derived as

$$i_s(k+1) = \frac{T_c}{L}[u_s(k) - u_m(k)u_{dc}(k)] + i_s(k). \tag{5}$$

B. Cost Function Formulation

The control objective of the current loop is to track the reference current i_{ref} without the steady-state error. Based on the model predictive theory, the cost function J must be related to the instantaneous value of the line current i_s and the reference current i_{ref}. In the stationary reference frame, both i_s and i_{ref} are ac signals, and their instantaneous values are not equal at two adjacent control instants. At the kth control instant, the cost function $J(k)$ should evaluate the error between i_s and i_{ref} at the $(k+1)$th control instant and can be defined as [22], [23]

$$J(k) = [i_{ref}(k+1) - i_s(k+1)]^2. \tag{6}$$

C. Modulation Function Optimization

To minimize the cost function $J(k)$ in (6), the appropriate modulation function $u_m(k)$ should satisfy as

$$\frac{\partial J(k)}{\partial u_m(k)} = 0. \tag{7}$$

Substituting (6) into (7) and solving, the condition for obtaining the optimal solution of $u_{\mathrm{m}}(k)$ is

$$i_{\mathrm{s}}(k+1) = i_{\mathrm{ref}}(k+1). \tag{8}$$

Then, substituting (8) into (5), $u_{\mathrm{m}}(k)$ is derived as

$$u_{\mathrm{m}}(k) = \frac{u_{\mathrm{s}}(k)}{u_{\mathrm{dc}}(k)} - \frac{L[i_{\mathrm{ref}}(k+1) - i_{\mathrm{s}}(k)]}{u_{\mathrm{dc}}(k)T_{\mathrm{c}}} \tag{9}$$

where $u_{\mathrm{s}}(k)$, $u_{\mathrm{dc}}(k)$, and $i_{\mathrm{s}}(k)$ can be obtained directly from sensors at the kth control instant. $i_{\mathrm{ref}}(k+1)$ is the instantaneous value of the reference current at the $(k+1)$th control instant, which needs to be predicted by $i_{\mathrm{ref}}(k)$.

In the stationary reference frame, the grid-side voltage u_{s} can be defined as

$$u_{\mathrm{s}} = U_{\mathrm{sm}} \cos(\omega t) \tag{10}$$

where U_{sm} and ω are the peak value and the fundamental angular frequency of u_{s}, respectively. So, i_{ref} can be defined as

$$i_{\mathrm{ref}} = I_{\mathrm{refm}} \cos(\omega t + \varphi_{\mathrm{i}}) \tag{11}$$

where I_{refm} is the peak value of i_{ref}. φ_{i} is the phase difference from i_{ref} to u_{s}. Furthermore, i_{ref} can also be expressed with the dq-axis components as

$$i_{\mathrm{ref}} = i_{d\mathrm{ref}} \cos \omega t - i_{q\mathrm{ref}} \sin \omega t \tag{12}$$

where $i_{d\mathrm{ref}}$ is the d-axis component of i_{ref}, which is equal to the output of the voltage loop. $i_{q\mathrm{ref}}$ is the q-axis component of i_{ref} and is usually set to a constant.

Since the control period T_{c} is much smaller than the fundamental period of u_{s}, ω and $i_{d\mathrm{ref}}$ in (12) can be regarded as constants in one control period. Thus, $i_{\mathrm{ref}}(k+1)$ is derived as

$$\begin{aligned} i_{\mathrm{ref}}(k+1) = {} & i_{d\mathrm{ref}}(k) \cos[\omega(k+1)T_{\mathrm{c}}] \\ & - i_{q\mathrm{ref}}(k) \sin[\omega(k+1)T_{\mathrm{c}}]. \end{aligned} \tag{13}$$

Substituting (13) into (9), $u_{\mathrm{m}}(k)$ is derived as

$$\begin{aligned} u_{\mathrm{m}}(k) = {} & \tfrac{u_{\mathrm{s}}(k)}{u_{\mathrm{dc}}(k)} - \tfrac{L}{u_{\mathrm{dc}}(k)T_{\mathrm{c}}} \{ i_{d\mathrm{ref}}(k) \cos[\omega(k+1)T_{\mathrm{c}}] \\ & - i_{q\mathrm{ref}}(k) \sin[\omega(k+1)T_{\mathrm{c}}] - i_{\mathrm{s}}(k) \}. \end{aligned} \tag{14}$$

If the adopted converter operates as a rectifier with the unity power factor, $i_{q\mathrm{ref}}$ is equal to zero. $u_{\mathrm{m}}(k)$ can be simplified as

$$\begin{aligned} u_{\mathrm{m}}(k) = {} & \frac{u_{\mathrm{s}}(k)}{u_{\mathrm{dc}}(k)} \\ & - \frac{L}{u_{\mathrm{dc}}(k)T_{\mathrm{c}}} \{ i_{d\mathrm{ref}}(k) \cos[\omega(k+1)T_{\mathrm{c}}] - i_{\mathrm{s}}(k) \}. \end{aligned} \tag{15}$$

From (14) and (15), only the sampled values at the kth control instant are used to calculate $u_{\mathrm{m}}(k)$, so switching noise is avoided in the current loop. In addition, the representation of $u_{\mathrm{m}}(k)$ in (14) and (15) is simple. The computational duration will be reduced, so the sampling period can be smaller to improve the control accuracy.

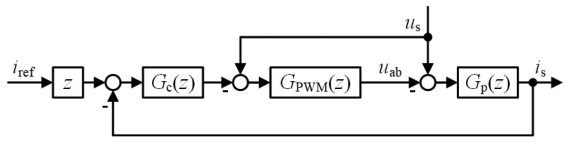

Fig. 3. Block diagram of the current loop of the proposed scheme.

IV. Analysis and Compensation of Inductance Parameter Mismatch

From (9), the accuracy of the modulation function $u_{\mathrm{m}}(k)$ is affected by the grid-side equivalent inductance L. Inductance parameter mismatch affects the control accuracy of the current loop and even leads to system instability [22]–[24], [26].

A. Stability Analysis

The structure of the current loop of the proposed scheme is shown in Fig. 3, where $G_{\mathrm{c}}(z)$, $G_{\mathrm{PWM}}(z)$, and $G_{\mathrm{p}}(z)$ represent the model of controller, PWM modulator, and converter, respectively. Let L_{m} be the inductance value used in the proposed scheme, λ is the inductance parameter mismatch ratio, that is, $L_{\mathrm{m}} = \lambda L$. According to (5) and (9), $G_{\mathrm{p}}(z)$ and $G_{\mathrm{c}}(z)$ are derived as follows, respectively:

$$\begin{cases} G_{\mathrm{c}}(z) = \frac{L_m}{T_{\mathrm{c}}} = \frac{\lambda L}{T_{\mathrm{c}}} \\ G_{\mathrm{p}}(z) = \frac{T_{\mathrm{c}}}{(z-1)L}. \end{cases} \tag{16}$$

Applying the zero-order hold (ZOH) model to the unipolar SPWM modulator and ignoring the control delay, the z-domain open-loop transfer function of the current loop can be derived as [26]

$$G_{\mathrm{o}}(z) = \frac{\lambda}{z-1}. \tag{17}$$

Thus, the characteristic equation of the closed-loop system is derived as

$$z - 1 + \lambda = 0. \tag{18}$$

According to Routh's stability criterion, the range of λ for system stability is $0 < \lambda < 2$. As analyzed in [26], the ZOH model of the SPWM is not enough accurate, the range of λ will be smaller than the above analysis result.

B. Control Performance Analysis

For PWM converters with nonlinearities, its linearization model cannot accurately describe the system characteristics, but it can be used to learn the changing trend of the system. From (17), the z-domain closed-loop transfer function $G(z)$ of the current loop can be derived as

$$G(z) = \frac{\lambda}{z - 1 + \lambda}. \tag{19}$$

Assuming that the current loop is stable, let the control period T_{c} be equal to 0.25 ms and substitute different inductance parameter mismatch ratios ($\lambda = 0.5$, 1, 1.5) into (19) for the following analysis.

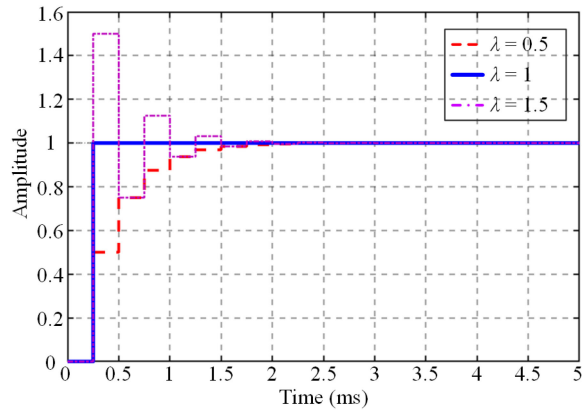

Fig. 4. Step response of $G(z)$ for different λ (λ =0.5, 1, 1.5).

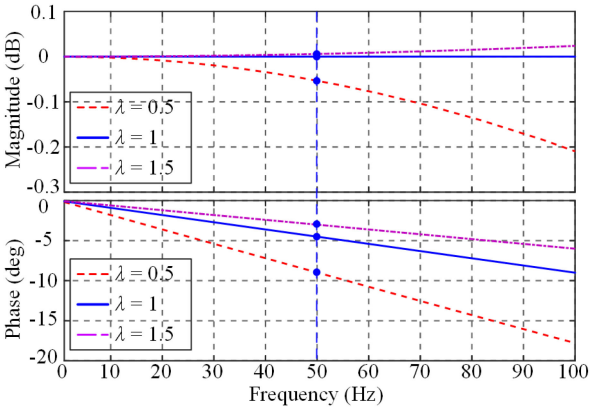

Fig. 5. Bode diagram of $G(z)$ for different λ (λ =0.5, 1, 1.5).

First, the step response of $G(z)$ is shown in Fig. 4. The dynamic performance of $G(z)$ is optimal in the nominal state ($\lambda = 1$), otherwise, the settling time of the current loop will increase. In addition, if $L_{\rm m} \le L$ ($0 < \lambda \le 1$), there is no overshoot in the current loop; if $L_{\rm m} > L$ ($1 < \lambda < 2$), overshoot and oscillation exist in the current loop. In all cases, the current loop can quickly enter the steady state within one or several control periods.

Second, replace L in (9) with $L_{\rm m}$, then substitute (9) into (5). The steady-state error between the reference current and the line current at the (k+1)th instant can be derived as

$$i_{\rm ref}(k+1) - i_{\rm s}(k+1) = (1-\lambda)[i_{\rm ref}(k+1) - i_{\rm s}(k)]. \quad (20)$$

Obviously, there is a steady-state error in the current loop when the inductance parameter is mismatched ($\lambda \neq 1$).

Third, Fig. 5 shows the Bode diagram of $G(z)$ with different λ. Around the fundamental frequency (50 Hz), the magnitude–frequency response is basically unchanged, but the phase–frequency response changes significantly. This result can be expressed as follows:

$$\begin{cases} \varphi_{\rm i} \downarrow, (0 < \lambda < 1) \\ \varphi_{\rm i} \uparrow, (1 < \lambda < 2). \end{cases} \quad (21)$$

It means that there is a phase error between the reference current and the line current when the inductance parameter is mismatched. That is, if $L_{\rm m} < L$ ($0 < \lambda < 1$), $i_{\rm s}$ will lag behind $i_{\rm ref}$; if $L_{\rm m} > L$ ($1 < \lambda < 2$), the line current $i_{\rm s}$ will lead $i_{\rm ref}$.

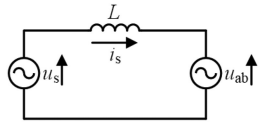

Fig. 6. Equivalent model of the current loop in the steady state.

C. Inductance Parameter Estimation

According to the stability and control performance analysis of the current loop, the current loop can quickly enter the steady state when it is stable. Therefore, the grid-side equivalent inductance L can be estimated based on the steady state of the current loop. Ignoring higher order harmonics, the grid-side loop of the adopted converter can be equivalent to a single-phase ac sinusoidal circuit shown in Fig. 6. In the steady state, sinusoidal analysis operations can be simplified by phasors. The phasor model of the current loop can be expressed as

$$\mathbf{U}_{\rm ab} = \mathbf{U}_{\rm s} - {\rm j}\omega L \mathbf{I}_{\rm s}, \quad (22)$$

where $\mathbf{U}_{\rm s}$, $\mathbf{I}_{\rm s}$, and $\mathbf{U}_{\rm ab}$ are the phasor of the grid-side voltage $u_{\rm s}$, the line current $i_{\rm s}$, and the H-bridge input voltage $u_{\rm ab}$, respectively.

From (22), the estimated value $L_{\rm e}$ of L is derived as

$$L_{\rm e} = {\rm Re}\left\{\frac{\mathbf{U}_{\rm s} - \mathbf{U}_{\rm ab}}{{\rm j}\omega \mathbf{I}_{\rm s}}\right\}. \quad (23)$$

The phasor $\mathbf{X}(t)$ can be expressed by the α–β frame, and the relationship between the sinusoidal signal $x(t)$ and $\mathbf{X}(t)$ is defined as

$$x(t) = {\rm Re}\{\mathbf{X}(t)\} = {\rm Re}\{x_\alpha(t) + {\rm j}x_\beta(t)\} \quad (24)$$

where $x_\alpha(t)$ is the real part of $\mathbf{X}(t)$ and is equal to $x(t)$. $x_\beta(t)$ is the imaginary part of $\mathbf{X}(t)$, which is orthogonal to $x(t)$ and usually lags $x(t)$ by a quarter of the period.

Applying (24) into (23), $L_{\rm e}$ can be expressed as

$$L_{\rm e} = {\rm Re}\left\{\frac{(u_{\rm s} - u_{\rm ab}) + {\rm j}(u_{{\rm s}\beta} - u_{{\rm ab}\beta})}{\omega i_{{\rm s}\beta} - {\rm j}\omega i_{\rm s}}\right\} \quad (25)$$

where $u_{{\rm s}\beta}$, $i_{{\rm s}\beta}$, and $u_{{\rm ab}\beta}$ are the orthogonal components of $u_{\rm s}$, $i_{\rm s}$, and $u_{\rm ab}$, which can be obtained by the second-order generalized integral (SOGI) method. The damping factor of SOGI is set to 1.57 to obtain the fastest response [32].

Since L will not change abruptly in practice, and all signals in (25) are ac sinusoidal variables with the same frequency as the fundamental frequency of the grid-side voltage, $L_{\rm e}$ can be calculated at a lower frequency. Considering the current ripple, a low-pass filter can be applied to keep $L_{\rm e}$ smooth. In addition, the proposed solution in (25) is based on the phase method, so it is suitable for any operating mode.

V. Description of the Proposed MP-ICC Scheme

The control diagram of the proposed MP-ICC scheme is illustrated in Fig. 7, which mainly consists of the voltage loop

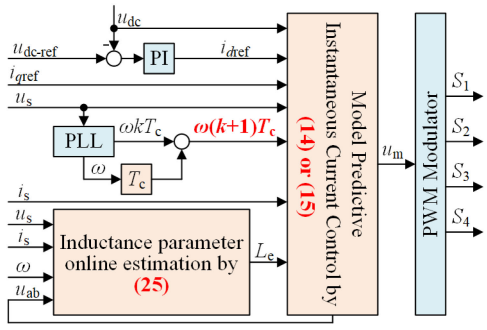

Fig. 7. Control diagram of the proposed MP-ICC scheme.

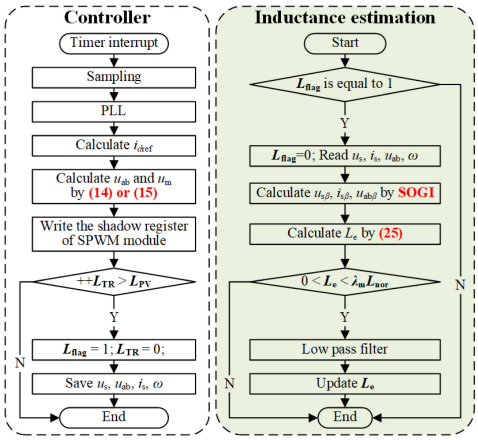

Fig. 8. Flowchart of the proposed MP-ICC scheme.

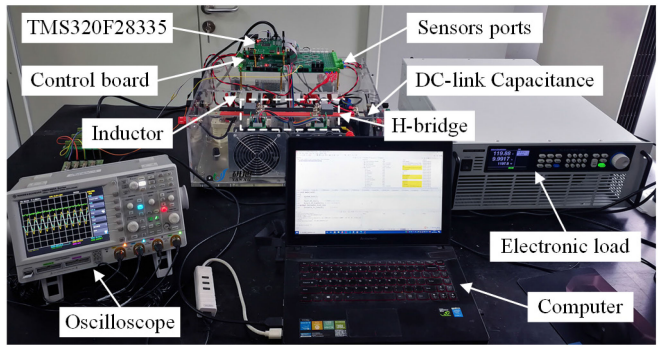

Fig. 9. Photograph of the experimental platform.

TABLE I
ELECTRICAL PARAMETERS OF THE SYSTEM

Parameters	Values
Grid-side voltage U_s / V	60
Grid-side equivalent inductance L / mH	5.6
DC-link buffer capacitance C_d / μF	4700
DC-link reference voltage $U_{dc\text{-}ref}$ / V	120
DC-link rated current $i_{dc\text{-}rate}$ / A	8
Switching frequency f_{pwm} / kHz	4
Sampling frequency f_s / kHz	40
The parameter K_p in the PI-based ICC	2.0
The parameter K_i in the PI-based ICC	0.8
The parameter K_p in the PI-based DCC	1.6
The parameter K_i in the PI-based DCC	16.3

for dc-link voltage regulation by a PI controller, the current loop for line current tracking by the proposed MP-ICC, and the inductance parameter mismatch compensation module with the proposed phasor-method-based parameter online estimation solution. It can be noticed that the proposed scheme neither needs to estimate the grid-side voltage and the line current like DB control nor does it need to estimate the β-axis current and transform reference frame like d-q control. And, no parameters need to tune like PI-based current control.

The flowchart of the proposed MP-ICC scheme is illustrated in Fig. 8, which consists of the control module and the inductance parameter estimation module. The control module is executed at the sampling frequency by a timer interrupt, and the inductance parameter estimation module is executed at the idle time of the digital controller. $L_{\rm TR}$, $L_{\rm PV}$, and $L_{\rm flag}$ are the control variables of the inductance parameter estimation module. Among them, $L_{\rm TR}$ records the number of the timer interrupt, $L_{\rm PV}$ and $L_{\rm flag}$ is the execution period and flag, respectively. Therefore, the executing frequency of the inductance parameter estimation module is lower than the sampling frequency.

From (25), L_e will be too large when i_s is closed to zero, and L_e will be equal to zero when u_s is equal to zero, these results are abnormal. A judgment condition is used to exclude abnormal values and is expressed as

$$0 < L_{\rm e} < \lambda_{\rm m} L_{\rm nor} \tag{26}$$

where $L_{\rm nor}$ is the nominal value of L, $\lambda_{\rm m}$ represents the upper limit of the inductance parameter mismatch ratio λ. Considering the practice applications, $\lambda_{\rm m}$ can be set to 2.

The inductance parameter online estimation module operates during the idle time of the digital processor, so the proposed scheme has the advantages of small computational burden, easy hardware implementation, and possibly using a low-cost digital controller.

VI. EXPERIMENTAL RESULTS

A single-phase two-level converter prototype is constructed to verify the feasibility and effectiveness of the proposed MP-ICC scheme. The steady-state and dynamic performances of the proposed MP-ICC scheme are compared with those of PI-based ICC, DB-ICC, PI-based DCC, and MP-DCC. The experimental prototype is shown in Fig. 9, which consists of the IGBT modules, power switch drive and protection circuit, signal sampling and processing circuit, and digital controller (TMS320F28335). The parameters of the experimental system are listed in Table I, where PI parameters of the voltage loop in all tested schemes are set to the same value, and PI controller parameters of the current loop have been well tuned based on the dynamic response and steady-state performance. Except for DB-ICC, the other four schemes use the multisampling method with minimum sampling interval. Differential probes are used to suppress interference pulses in measured signals.

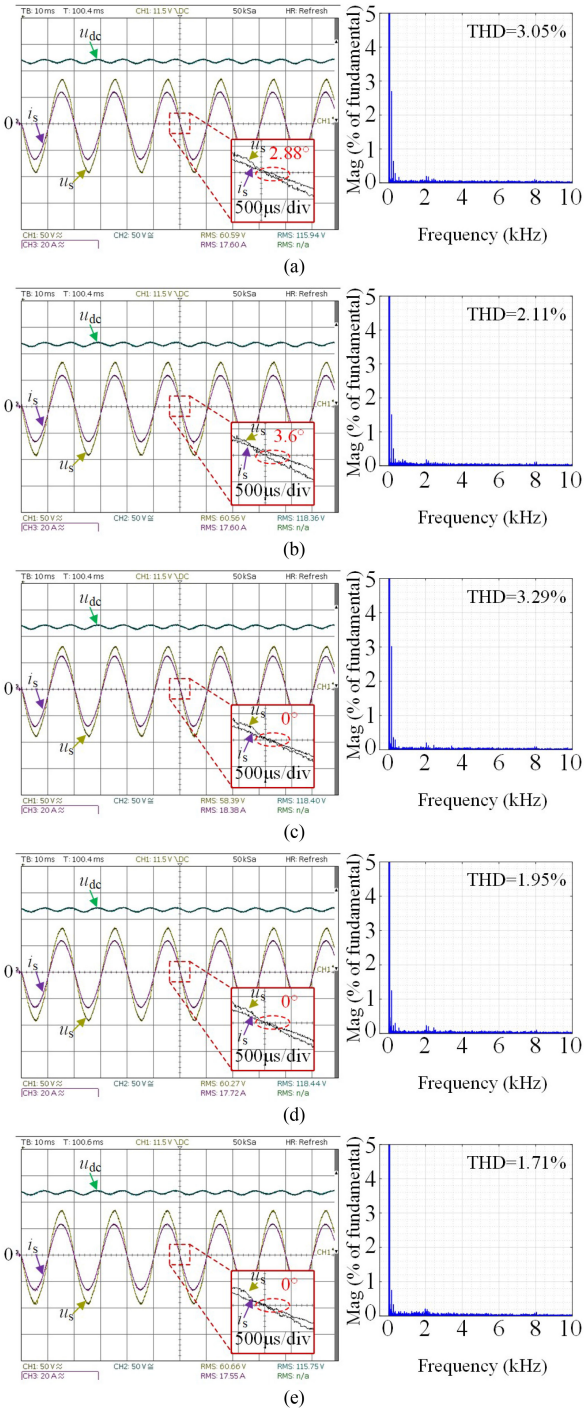

Fig. 10. Steady-state experimental results comparison of five schemes with rated load (u_s, u_{dc}: 50 V/div, i_s: 20 A/div, time: 10 ms/div). (a) PI-based ICC. (b) DB-ICC. (c) PI-based DCC. (d) MP-DCC. (e) MP-ICC.

A. Steady-State Performance

To test the steady-state performance of five schemes, the adopted converter operates with rated load, and the q-axis reference current i_{qref} is set to zero to realize the unit power factor. The steady-state experimental waveforms of the grid-side voltage u_s, dc-link voltage u_{dc}, and line current i_s, and the FFT analysis results of i_s are shown in Fig. 10.

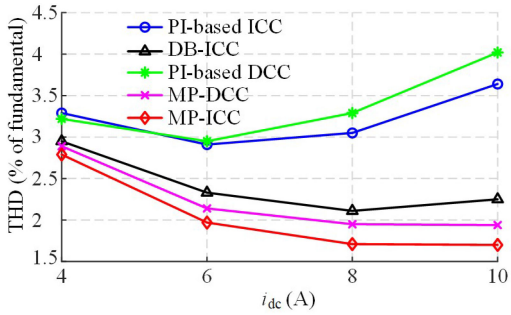

Fig. 11. Current THD curves of five schemes with different loads.

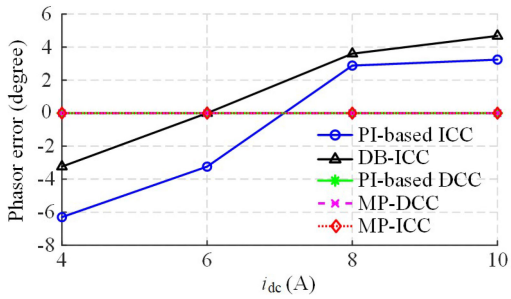

Fig. 12. Phase error curves of five schemes with different loads.

From Fig. 10, in these five schemes, the line current i_s is sinusoidal and approximately in phase with u_s. Comparing the partially enlarged details shown in Fig. 10(a) and (e), it can be observed that there are steady-state errors in PI-based ICC and DB-ICC, about 2.88 in Fig. 10(a) and 3.6 in Fig. 10(b), respectively. In contrast, as shown in Fig. 10(c) and (e), PI-based DCC, MP-DCC, and the proposed MP-ICC realize zero steady-state error.

In Fig. 10, the higher order harmonics of is in these five schemes mainly distribute around twice the switching frequency, that is 8 kHz. The reason is that the SPWM modulator is adopted in all schemes. Among the five schemes, the current total harmonic distortion (THD) of the proposed MP-ICC scheme in Fig. 10(e) is the lowest, about 1.71%. The current THDs of MP-DCC in Fig. 10(d) and DB-ICC in Fig. 10(b) are slightly higher than that of the proposed scheme, about 1.95% and 2.11%, respectively. The current THD of PI-based ICC in Fig. 10(a) is higher than that of MP-DCC and DB-ICC, about 3.02%. The current THD of PI-based DCC in Fig. 10(c) is the highest, about 3.29%.

Current THD curves of five schemes with different loads are shown in Fig. 11. In the proposed MP-ICC scheme and MP-DCC, the THD values will decrease as the load increases. The THD changing trend of DB-ICC is similar to the proposed scheme, but its current THD increases under heavy load. The current THDs of PI-based ICC and DCC only reach the minimum value at only a certain operating point. Compared with the other four schemes, the proposed scheme has the lowest current THD under different loads.

Fig. 12 shows phase error curves of five schemes with different loads. It can be observed that the phase errors of PI-based DCC,

MP-DCC, and proposed MP-ICC are zero. However, the phase error of PI-based ICC and DB-ICC is zero at only a certain operating point.

From Figs. 11 and 12, the MP-DCC and the proposed MP-ICC scheme can achieve global optimal control. However, PI-based ICC, PI-based DCC, and DB-ICC can only achieve local optimal control.

Experimental results verify that in the nominal system, the proposed MP-ICC scheme has advantages of zero steady-state error and low current harmonics.

B. Dynamic Performance

To test the dynamic response of these five control schemes when the reference current step changes, the q-axis reference current $i_{q\mathrm{ref}}$ is set to zero, and the d-axis reference current $i_{d\mathrm{ref}}$ is step down from 75% to 50% rated current. The change instant is set at the peak of the grid-side voltage. The experimental waveforms of the grid-side voltage u_{s}, the line current i_{s}, and the reference current i_{ref} are shown in Fig. 13. Since i_{ref} is directly output by the digital-to-analog conversion module and measured by an ordinary probe, there are some interference pulses.

From Fig. 13, all five schemes can reach the steady state with a short settling time when i_{ref} changes. Comparing the partially enlarged details shown in Fig. 13(a) and (e), the settling time of the proposed MP-ICC scheme in Fig. 13(e) is the shortest, about 1.5 ms. The settling times of PI-based ICC and DB-ICC in Fig. 13(a) and (c) are slightly longer than that of the proposed scheme, about 2.8 ms and 2 ms, respectively. The settling time of MP-DCC in Fig. 13(d) is longer than that of PI-based ICC and DB-ICC, about 6. 8ms. The settling time of PI-based DCC in Fig. 13(c) is the longest, about 12.8 ms.

The proposed MP-ICC is combined with the voltage outer-loop to construct a complete double closed-loop system for the dc-link load mutation test, and the dc-link load is stepped between 75% and 100% rated load. Fig. 14 shows experimental waveforms of the grid-side voltage u_{s}, dc-link voltage u_{dc}, and line current i_{s}. In the steady state, u_{dc} is stable, and i_{s} is in phase with u_{s}. When the dc-link load changes, u_{dc} can be stabilized after a short transient process, the settling time is about 100 ms. It should be noted that the settling time of the voltage loop is much longer than that of the current loop. The reason is that the stability of u_{dc} is mainly affected by the voltage loop and load changes cannot directly reflect the dynamic performance of the current loop.

Experimental results verify that the dynamic response of the proposed MP-ICC scheme is faster than the other four schemes. Meanwhile, the proposed scheme can be applied to the adopted converter and ensure its normal operation.

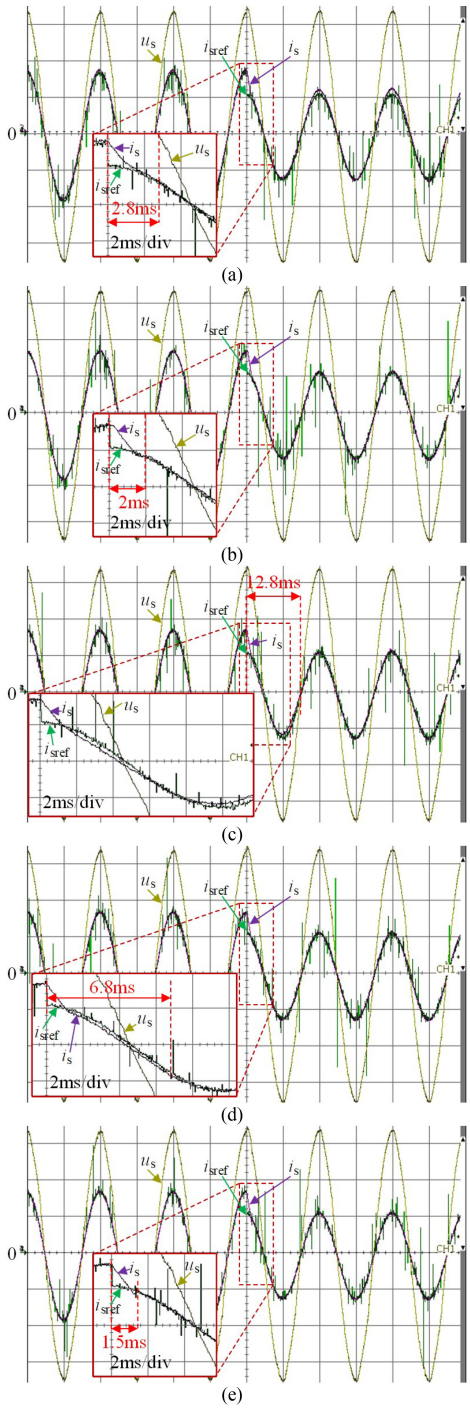

Fig. 13. Dynamic response comparison of five schemes when the reference current step down from 75% to 50% rated current (u_{s}: 25 V/div, i_{s}, i_{ref}: 10 A/div, time: 10 ms/div). (a) PI-based ICC. (b) DB-ICC. (c) PI-based DCC. (d) MP-DCC. (e) MP-ICC.

C. Online Estimation of Inductance Parameter

To test the effect of the inductance parameter mismatch on the current loop and the effectiveness of the proposed phasor-method-based inductance parameter online estimation solution, the inductance value L_{m} in the proposed scheme is changed to simulate the inductance parameter mismatch. The inductance parameter mismatch ratio λ is set to 150% and 200%, respectively. The experimental waveforms of the grid-side voltage u_{s}, the dc-link voltage u_{dc}, and the line current i_{s} are shown in Fig. 15, where L_{mark} represents the operating mark of the inductance parameter estimation module, which is output by an IO port of the digital controller. The inductance estimation module operates when L_{mark} is at a high level, otherwise, it does

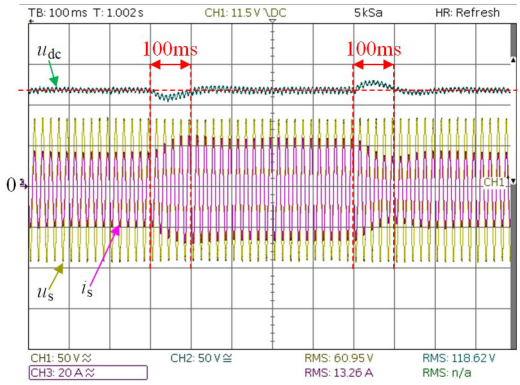

Fig. 14. Dynamic experimental waveforms of the proposed MP-ICC scheme when the dc-link load changes abruptly (u_s, u_{dc}: 50 V/div, i_s: 20 A/div, time: 100 ms/div).

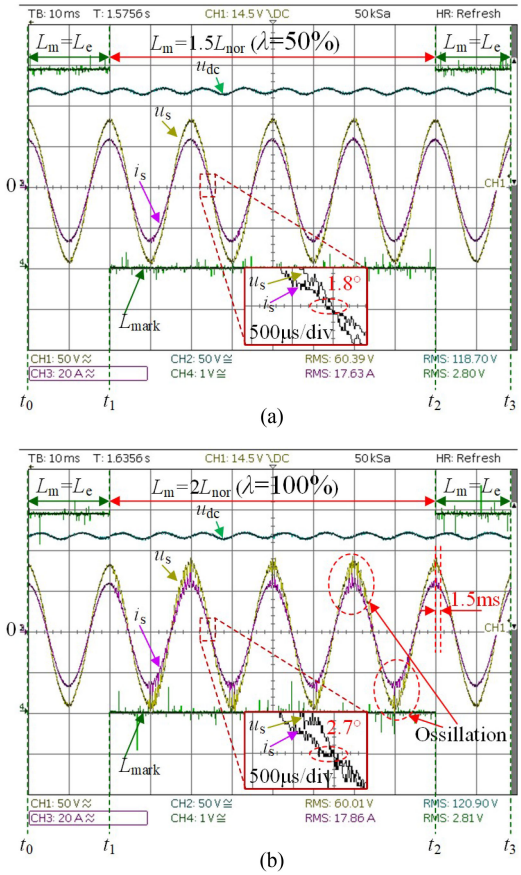

Fig. 15. Experimental waveforms with different inductance parameter mismatch ratios λ when the proposed inductance parameter estimation solution executes periodically. (u_s, u_{dc}: 50 V/div, i_s: 20 A/div, time: 10 ms/div). (a) $L_m = 1.5L_{nor}$ ($\lambda = 150\%$). (b) $L_m = 2L_{nor}$ ($\lambda = 200\%$).

not work. The execution frequency of the estimation module is set to a quarter of the sampling frequency, that is, 10 kHz.

During t_1–t_2, the inductance parameter estimation module does not operate, $L_m = 1.5L_{nor}$ ($\lambda = 150\%$) in Fig. 15(a), $L_m = 2L_{nor}$ ($\lambda = 200\%$) in Fig. 15(b). As shown in Fig. 15(a) and (b), the inductance parameter mismatch will cause phase error of the line current. In Fig. 15(a), i_s is sinusoidal but leads

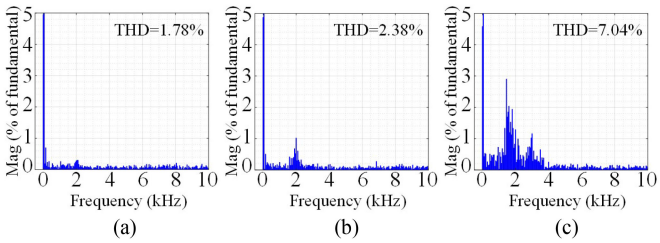

Fig. 16. FFT analysis results of the line current with different inductance parameter mismatch ratios λ. (a) $L_m = L_e$. (b) $L_m = 1.5L_{nor}$ ($\lambda = 150\%$). (c) $L_m = 2L_{nor}$ ($\lambda = 200\%$).

u_s by about 1.8°. In Fig. 15(b), i_s is oscillating, and the phase error increases to about 2.7°. Meanwhile, u_s has also oscillated because the experimental prototype is powered by an autotransformer. It means that the system is unstable. Besides, u_{dc} remains unchanged when the inductance parameter is mismatched. This is because the output active power of the converter can be kept constant under the action of the voltage loop.

During t_0–t_1 and t_2–t_3, the inductance parameter estimation module operates. From Fig. 15(a) and (b), the inductance parameter estimation module starts to operate at t_3 instant, the phase error can be quickly eliminated, i_s is sinusoidal and in phase with u_s. Meanwhile, it can be observed that the convergence time of the proposed inductance parameter estimation solution is about 1.5 ms from Fig. 15(b).

Fig. 16 shows FFT analysis results of the line current with different inductance parameter mismatch ratios λ. Among them, Fig. 16(a) shows the result when the inductance estimation module operates. The current THD is the lowest, about 1.78%, which is very close to the current THD (1.71%) of the nominal system in a steady state. In the case that the inductance estimation module does not work, the current THD increases to about 2.38% in Fig. 16(b) when $L_m = 1.5L_{nor}$ ($\lambda = 150\%$), and the current THD increases to about 7.04% in Fig. 16(c) when $L_m = 2L_{nor}$ ($\lambda = 200\%$).

Experimental results show that the inductance parameter mismatch will lead to the phase error of the line current and the current harmonics increase. The proposed inductance parameter estimation solution can quickly eliminate the phase error and perform harmonic compensation.

D. Overall Performance Evaluation of the Proposed Scheme

According to the above experimental results, a comprehensive performance comparison between the proposed MP-ICC scheme and the other four current control strategies is listed in Table II. Because the duty-cycle-updating of the five control schemes is executed at the peak and valley of the triangular carrier, their switching frequencies are all 4 kHz. For these four existing schemes, stationary reference frame control such as PI-based ICC and DB-ICC have fast dynamic responses, but there are steady-state errors. In contrast, *d-q* control strategies such as PI-based DCC and MP-DCC can achieve zero steady-state error by low-order controllers, but their dynamic response is slower. Furthermore, in the same reference frame, compared with the traditional PI-based current control, predictive control

TABLE II
PERFORMANCE COMPARISON OF FIVE CONTROL SCHEMES

Performance	PI-based ICC	DB-ICC	PI-based DCC	MP-DCC	Proposed MP-ICC
Switching frequency	4kHz	4kHz	4kHz	4kHz	4kHz
Power factor angle	3.6°	3.96°	0°	0°	0°
Current THD	3.05%	2.11%	3.29%	1.95%	1.71%
Number of PI controller	2	1	3	1	1
Settling time	2.8ms	2ms	12.8ms	6.8ms	1.5ms
Steady-state error	Yes	Yes	No	No	No
Reference frame transformation	No	No	Yes	Yes	No
Complexity	Normal	Normal	Complex	Normal	simple
[a] Computational burden	2.8μs	2.5μs	8.4μs	8.2μs	1.8μs
Sensitivity to inductance	No	Yes	No	Yes	Yes

[a]Only include the executing time of the current control scheme.

has salient advantages of fast dynamic response and good steady-state performance. The proposed MP-ICC scheme combines advantages of the other four schemes, including fast dynamic response, low current harmonics. Importantly, it has a simple control structure and realizes zero steady-state current error in the stationary reference frame. Besides, the computational burden of the proposed scheme is the smallest among the five schemes.

VII. CONCLUSION

A simple MP-ICC scheme for single-phase PWM converters was proposed in this article. The optimal modulation function is directly calculated in the stationary reference frame with the CCS-MPC principle. The derived modulation function can realize zero steady-state error and has a simple control structure. The influence of the inductance parameter mismatch on the current loop was analyzed in detail. Then, a phasor-method-based inductance parameter online estimation solution was developed, which can operate at a lower frequency without making the control delay longer. By comparing the experimental results of four existing schemes for single-phase PWM converters, the proposed MP-ICC scheme is characterized by the following features.

1) Compared with PI-based ICC and DB-ICC in the stationary reference frame, the proposed scheme can achieve zero steady-state error and lower current harmonics.
2) Compared with the PI-based DCC and MP-DCC in the *d-q* frame, the proposed scheme delivers a faster dynamic response and lower computational burden.
3) Compared with the traditional PI-based current control schemes such as PI-based ICC and DCC, the proposed scheme provides faster dynamic response and lower current harmonics. Importantly, it does not require complex tuning of PI parameters.
4) Compared with the MP-DCC scheme, the proposed MP-ICC scheme has a simpler control structure, faster dynamic response, and lower computational burden.
5) The proposed inductance parameter online estimation solution can effectively eliminate the influence of an inductance parameter mismatch to improve the robustness of the current loop. In addition, it can operate at a low frequency to reduce the computational burden.

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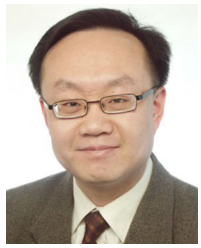

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