A Second Harmonic Current Suppressing Method Based on Negative-Order Capacitor

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***Abstract*—In microgrid system, current in dc bus may contain a lot of undesired low-order harmonics when converters are employed, especially the second harmonic current (SHC). To address the issue, this article proposes a method based on fractional-order capacitor (FOC) to suppress the SHC. The FOC, of which the order α is "−1," has the same characteristics of dc blocking and ac conducting as conventional capacitor; while it can resonate with a conventional capacitor like an inductor, which could be called a negative-order capacitor (NOC) as well. The proposed circuit has good SHC suppression performance, faster dynamic response, and soft switching realization. It parallels on the dc side of an inverter instead of the large bus capacitor, increasing power density and reducing design cost and loss. The secondary power will only circuit between the ac side of inverter and the NOC circuit. In addition, the NOC circuit can adjust zero impedance to specific harmonics; so it can be expanded to suppress harmonic current at other frequencies in the system. The simulation and experimental results are presented to validate the feasibility of the proposed method.**

***Index Terms*—Fractional-order capacitor (FOC), power decoupling, second harmonic current (SHC) suppression.**

I. Introduction

THE reliability of the microinverter is becoming a crucial feature in the ac-module distributed generation (DG) units. Secondary harmonic in current or voltage caused by converters is one of the most common and serious problems to the DGs. Especially, the undesired second harmonic current (SHC) may affect the realization of maximum power point tracking (MPPT) in photovoltaic (PV) applications [1], [2], shorten the lifespan of fuel cells, reduce the soft switching range of converters [3], [4], cause torque ripple for motor load, and induce loss [5], [6].

The easiest way to suppress SHC is to employ an electrolytic capacitor or a low resonant frequency *LC* passive filter. However, when a large electrolytic capacitor is employed as the dc bus capacitor of a rectifier or an inverter, it would inevitably shorten the operation lifetime and increase the volume. So, other two more useful kinds of methods have been employed to reduce or eliminate the SHC. The first category is to employ advanced control scheme. The second category is to employ active power filter (APF) based on power decoupling, which theoretically provides an equivalent large energy storage element for pulsating power.

The advanced control scheme approach is usually applied to the multistage converters to suppress SHC. It aims to get larger port-impedance at $2f_o$ (twice the ac-line frequency) of dc bus or build a virtual passage into which the SHC flows [7]. The virtual impedance inserted into the control loop can increase the open-loop output impedance of dc−dc converter at $2f_o$. A front-end regulator employed for an *LLC*-contained inverter is discussed in [8]. And a notch filter employed in voltage loop could reduce the voltage loop gain at $2f_o$. However, the notch filter may reduce the phase margin at the corresponding zero crossing and weaken the stability of the voltage loop. So, a modified resonant regulator is proposed in [9] to improve the system stability. In PV generation system, in order to realize MPPT while without strict voltage requirements, an adaptive dc bus voltage can be employed to reduce ripple current [10]. But when the bus voltage is required to be constant, other methods must be found. In [11] and [12], a load current feed-forward control is used to incorporate virtual impedance to the output of a front-end converter, building a low-impedance passage in dc bus capacitor for SHC. No more modifications are needed for the voltage closed-loop controller. But it may increase the battery degradation and the component stress of the front-end dc−dc converter. A proportional−integral resonant controller [13] and an additional ripple current feedback channel [14] can be employed to the increase of the closed-loop output impedance of the front-end dc−dc converter at $2f_o$. With an active damping scheme [15] or an adaptive sliding mode control [16], the controller damps the resonant peak resulted by the input filter capacitor and the boost inductor, achieving high-voltage loop bandwidth with adequate phase margin. However, a large dc bus capacitor or inductor is still required in the advanced control scheme methods for limiting the dc bus voltage or current ripple, respectively. Currently, these methods do not have much potential for increasing power density. Although the total volume of energy storage elements required in the circuit has been reduced, the reduction margin is limited.

The second category to reduce or eliminate SHC is to employ power decoupling based APF instead of large dc capacitor, which can be categorized into two groups in terms of the applied locations: 1) dc side and 2) ac side [17]. The ability to suppress SHC is not determined by locations but by the amount of pulsating energy that can be stored.

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At the dc side, a two-terminal active-capacitor converter is employed in [18] and [19], which has self-power scheme. The proposed method expands the modulated maximum of bus capacitor voltage. But this extra range is less than half of the bus voltage. An electrolytic capacitor-less SHC compensator with hybrid one-cycle control is proposed in [20], presenting perfect steady-state performance. But the bandwidth limitation of voltage controller may lead to voltage distortion when load jumping. A symmetrical half-bridge circuit with power decoupling proposed in [21] greatly reduces the capacitance of the bus capacitor. But the additional inductor is relatively large and soft switching for switches has never been realized completely. What is worse, the voltage ripple on dc bus may be concentrated on the uncontrolled capacitor, resulting in voltage ripple component between two capacitors. Meanwhile, there may be asymmetrical dc bias as well. Some multilevel modular inverters can be seen as inverters that are integrated by multiple APFs. The self-balance of the capacitor voltage at the switching frequency disperses the pulsating power at the $2f_o$. In [22], a switched-capacitor converter with high efficiency is employed. But it achieves high efficiency only when the output voltage is close to the predetermined voltage. A quasi-resonant switched-capacitor multilevel inverter is proposed in [23]. The self-voltage balancing is achieved without any high-frequency balancing algorithm. The quasi-resonant circuit can suppress the current spikes, while making the converter control more complicated, and the relative large capacitors are needed. At the ac side, an inductance-based APF using the leakage inductance of the machine windings is proposed in [24] for electric vehicles (EVs). The pulsating is stored in the leakage inductance of the machine windings. However, it is uneconomical to apply to the occasions where there is no large inductance. In [25], an EV battery charger based on differential interleaved boost converter is proposed with no bulky electrolytic capacitor. But half of the switches (4 out of 8) cannot achieve soft switching, meaning high requirements for the heat dissipation of the system. Generally speaking, the sizes of energy storage units in these methods are smaller. But extra circuit is added, which may decrease stability, increase complexity, and introduce loss.

The above power decoupling based methods also can be categorized into two groups in terms of the main body of energy storage: 1) capacitor [18]–[23] and 2) inductor [23]–[25]. The concept of fractional-order circuit has been proposed already [26]–[29], such as fractional-order capacitors (FOCs) and inductors. With the frequency changing, the equivalent impedance of FOC also changes. Sometimes, it can be negative resistance.

To address the above issue, this article proposes a method based on FOC with $\alpha = -1$, which could be called negative-order capacitor (NOC) in this article, to suppress the pulsating power. The NOC is connected in series with a conventional capacitor to form an NOC branch, parallel on the dc bus instead of the large electrolytic capacitor. So, the bus capacitor only needs to filter out the harmonics of the switching frequency. The pulsating power only circuits between the inverter and the proposed SHC suppression circuit, without flowing into power sources or front stage of cascade system. In theory, the proposed method could provide zero impedance to second-order current component and suppress SHC completely, which improves the lifespan and upgrades the operation performance for power supply. The rest of this article is organized as follows. The theoretical analysis of the proposed method is introduced in Section II. The simulation and experimental results are illustrated in Section III. Finally, Section IV concludes this article.

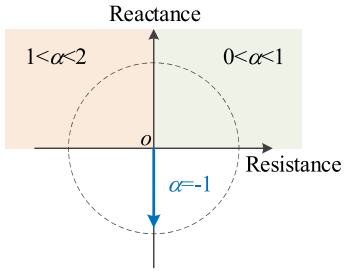


Fig. 1. Impedance-phase diagram of FOC.

II. Suppression Principle and NOC Operation Analysis

A. Concept of NOC Circuit

The current−voltage relationship of a conventional capacitor is described by first-order calculus as

$$i_c(t) = C\frac{du_c(t)}{dt} \tag{1}$$

while in contrast to the integer-order capacitor, the FOC is

$$i_c(t) = C_\alpha \frac{d^\alpha}{dt^\alpha} u_c(t) \tag{2}$$

where α is the order, with $0 < \alpha < 2$, d^α/dt^α is the fractional-order derivative operator, and C_α is the equivalent capacitance value. The impedance of an FOC is described as

$$Z = \frac{1}{\omega^\alpha C_\alpha}\cos(0.5\pi\alpha) - j\frac{1}{\omega^\alpha C_\alpha}\sin(0.5\pi\alpha) \tag{3}$$

where ω is the operating angular frequency.

When ω or α changes, both the capacitance and resistance of an FOC change. With an additional free variable α, fractional-order devices can be more flexible to adapt to different needs. When α extends to a negative number, the minus sign in the sin symbol in (3) can be brought to C_α to obtain the negative capacitance and Z would increase as ω increases.

The phase diagram of the impedance is shown in Fig. 1. Conventionally, the FOC has the order from 0 to 2. When the order belongs to (1, 2), there is negative resistance to generate power, and when the order belongs to (0, 1), there will be positive resistance to consume power. In the positive half-plane, the FOC presents capacitive and variable positive or negative resistance. When α becomes -1, the capacitor has the same impedance angle of the integer-order inductor. Then, current−voltage relationship of the NOC C_{noc} is described as

$$u_{c'}(t) = C_{\text{noc}}\frac{di_{c'}(t)}{dt}. \tag{4}$$

The NOC presents inductance in ac signal. So, the equivalent capacitance of NOC is opposite to that of conventional

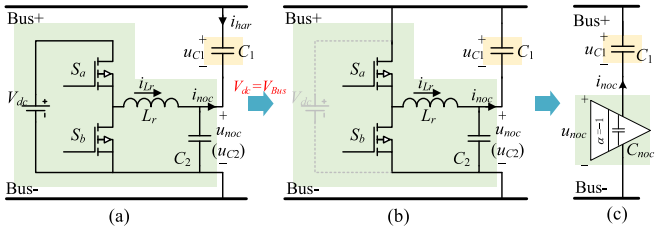


Fig. 2. Harmonic absorption circuit based on NOC (FOC with order $\alpha = -1$). (a) Primary two-terminal FOC. ($u_{\rm noc}$ and u_{C2} share the same port, $u_{\rm noc} = u_{C2}$). (b) Derived NOC topology. (c) Simplified schematic diagram of NOC.

capacitors. According to the calculation formula of equivalent capacitance value when connecting capacitors in series

$$C_{\text{eq}-\omega} = \frac{C \cdot C_{\rm noc}}{C + C_{\rm noc}}. \tag{5}$$

When $C_{\rm noc}$ is close to $-C$, the $C_{\rm eq}$ may be equivalent to a very large capacitance value for a specific frequency. Such a large capacitance $C_{\text{eq-}\omega}$ can replace the conventional large electrolytic capacitor to suppress the SHC on the dc bus.

The green part in Fig. 2(a) denotes the two-terminal FOC, which contains a capacitor C_2, an inductor L_r, two switches S_a and S_b, and an independent dc power supply $V_{\rm dc}$. In Fig. 2(a), C_1 and $C_{\rm noc}$ share the same current $i_{\rm har}$, while the ac components of their voltages vary oppositely, behaving as a conventional *LC* resonance. But the voltages of C_1 and $C_{\rm noc}$ both have a dc bias, which is different with normal inductor behavior. Thus, it is called NOC.

As the dc bus voltage will become constant after the SHC suppression, the independent dc source $V_{\rm dc}$ in the place of virtual $V_{\rm dc}$ provides power for the FOC. Namely, if $V_{\rm dc}$ is set to equal dc bus voltage, the bus can replace the independent dc source $V_{\rm dc}$ directly. Furthermore, the switches S_a and S_b can be connected directly to the dc bus finally, as shown in Fig. 2(b). Furthermore, it could be simplified as shown in Fig. 2(c).

B. Secondary Pulsating Power Decoupling Principles Based on NOC

Take the single-phase inverter output voltage $u_{\rm o}$ and current $i_{\rm o}$ as

$$\begin{cases} u_{\rm o} = U_{\rm o} \sin \omega t \\ i_{\rm o} = I_{\rm o} \sin(\omega t + \theta). \end{cases} \tag{6}$$

Then, the output power p_o will yield

$$p_{\rm o} = u_{\rm o} i_{\rm o} = \frac{U_{\rm o} I_{\rm o}}{2} \left[\cos\theta - \cos\left(2\omega t + \theta\right)\right]. \tag{7}$$

Such pulsating power contains a dc component and a 2-ω ac component, causing SHC at the dc bus.

Considering constant voltage characteristics of the power supply, the output current of the power supply will contain a double frequency component $i_{\text{in-2nd}}$ with a magnitude of

$$i_{\rm in-2nd} = -\frac{U_{\rm o} I_{\rm o}}{2U_{\rm bus}} \cos(2\omega t + \theta). \tag{8}$$

In order to suppress the pulsating power, an equivalent NOC branch to absorb the SHC is proposed in Fig. 2. The NOC $C_{\rm noc}$ consists of S_a, S_b, L_r, and C_2.

The voltages in circuits can be written in (9) as follows:

$$\begin{cases} u_{C1} = kU_{\rm bus} + u_h \\ u_{C2} = (1-k)U_{\rm bus} - u_h \\ u_h = U_h \sin(\omega t + \beta) \end{cases} \tag{9}$$

where u_h is the modulation voltage; U_h and β denote the amplitude and the phase of u_h, respectively; k is the proportion factor, which determines the dc voltage bias of C_1 and C_2 in the NOC.

The principle of ripple suppression can be started from the perspective of the power. The power of all the energy storage elements $p_{\rm NOC}$ in NOC branch is

$$p_{\rm NOC} = u_{C1} \cdot C_1 \frac{du_{C1}}{dt} + u_{C2} \cdot C_2 \frac{du_{C2}}{dt} + i_{Lr} \cdot L_r \frac{di_{Lr}}{dt}. \tag{10}$$

When $C_1 = C_2 = \rm C$, $k = 0.5$, and L_r is small enough, $p_{\rm NOC}$ can be simplified as

$$p_{\rm NOC} = 2Cu_h \frac{du_h}{dt} = \omega C U_h^2 \sin(2\omega t + 2\beta). \tag{11}$$

The SHC can be absorbed completely when the power of NOC equals the secondary pulsating power in magnitude while opposite in phase; therefore

$$\begin{cases} \omega C U_h^2 = \frac{U_{\rm o} I_{\rm o}}{2} \\ \sin(2\omega t + 2\beta) = \cos(2\omega t + \theta). \end{cases} \tag{12}$$

So, U_h and β should satisfy the following conditions:

$$\begin{cases} U_h = \sqrt{\frac{U_{\rm o} I_{\rm o}}{2\omega C}} \\ \beta = \frac{\pi}{4} + \frac{\theta}{2}. \end{cases} \tag{13}$$

Then, the power supply current only contains the dc component, and the SHC is transferred to the NOC branch. As seen from (13), the phase difference between the modulation voltage phase β and the load impedance phase θ is fixed to $\pi/4$. When the original inversion system works stably with θ in $(-\pi,\pi]$, the method can absorb SHC under the corresponding modulation phase.

C. Mode Analysis of NOC Circuit

In line voltage period, there could be a division of three zones for NOC, according to the direction of inductor current i_{Lr} during a switching operation period, as illustrated in Fig. 3(a).

Zone $\mathbf{D_2}$: i_{Lr} changes direction during switching operation period, as shown in Fig. 3(b).

Zone $\mathbf{D_1}$: $i_{Lr} > 0$ and u_{C2} rises, as shown in Fig. 3(c).

Zone $\mathbf{D_3}$: $i_{Lr} < 0$ and u_{C2} drops, as shown in Fig. 3(d).

In zone D_2, zero voltage switching (ZVS) turn-ON is realized for S_a and S_b.

Mode I: S_a is turned ON and S_b is turned OFF. When i_{Lr} is positive as the red line in Fig. 4(a), dc voltage charges L_r and C_2 through S_a. i_{Lr} increases in a positive direction, and u_{C2} rises simultaneously. When i_{Lr} is negative as the blue line in Fig. 4(c), L_r and C_2 return energy to dc bus through the body diode of S_a. i_{Lr} decreases in a negative direction and u_{C2} drops.

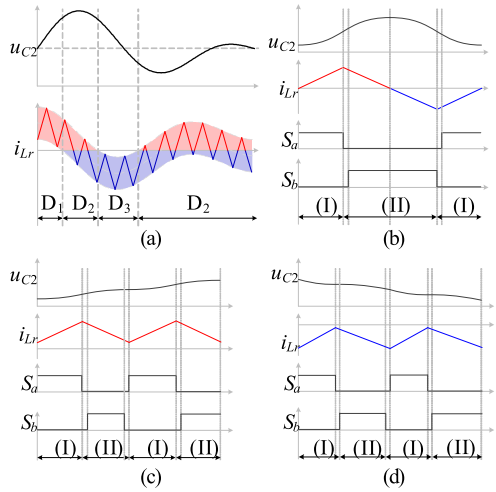


Fig. 3. Typical operation waveforms in NOC circuit. (a) i_{Lr} and u_{C2} at line voltage period. (b) i_{Lr} and u_{C2} during D_2. (c) i_{Lr} and u_{C2} during D_1. (d) i_{Lr} and u_{C2} during D_3.

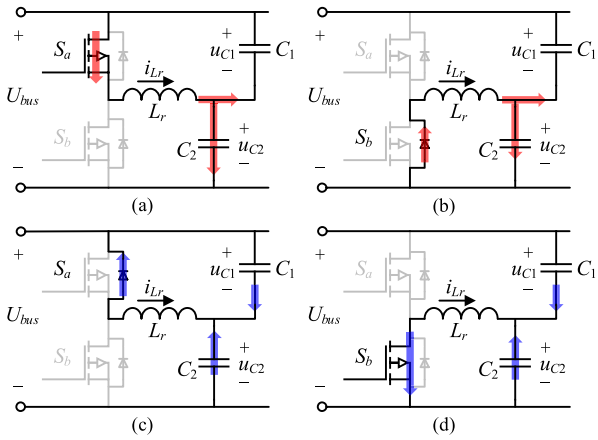


Fig. 4. Operation modes in NOC circuit. (a) Mode I, $i_{Lr} > 0$. (b) Mode II, $i_{Lr} > 0$. (c) Mode I, $i_{Lr} < 0$. (d) Mode II, $i_{Lr} < 0$.

Mode II: S_a is turned OFF and S_b is turned ON. When i_{Lr} is positive as the red line in Fig. 4(b), L_r charges C_2 through the body diode of S_b. i_{Lr} decreases in the positive direction, and u_{C2} rises. When i_{Lr} is negative as the blue line in Fig. 4(d), C_2 charges L_r through S_b. i_{Lr} increases in the negative direction, and u_{C2} drops simultaneously.

D. Circuit Parameter Design

As seen from the theoretical derivation in Sections II-A and II-B, the voltage of capacitors $C_{\rm noc}$ and C has a dc bias. The higher the voltage of U_h, more is the power stored in the branch. When C_1 and C_2 have the same capacitance, U_h achieves the maximum. So, it yields

$$U_h \le \frac{1}{2}U_{\rm bus}. \tag{14}$$

In theory, when U_h is equal to half of $U_{\rm bus}$, the branch obtains the largest secondary pulsation power absorption ability. At the moment, the total instantaneous power of the branch is equal to

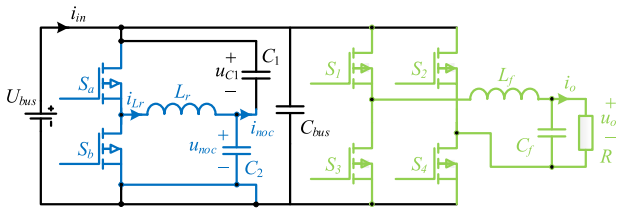


Fig. 5. Diagram of NOC circuit with a single-phase inverter (the blue part is NOC and the green part is inverter).

the second pulsating power

$$\omega C U_h^2 = \frac{\omega C U_{\rm bus}^2}{4} = p_{\rm pul} \tag{15}$$

where $p_{\rm pul}$ represents the pulsating power. As seen from (15), the capacitance value in the NOC yields

$$C_{\rm min} = \frac{4p_{\rm pul}}{\omega U_{\rm bus}^2}. \tag{16}$$

In order to reduce the influence from the resonance between $L_{\rm r}$ and C_2, according to IEEE 519 (each odd content of the first 11th harmonics shall not be greater than 4%), the resonance frequency of $L_{\rm r}$ and C_2 should be 11 times larger than the line frequency $f_{\rm o}$ (50Hz, the frequency of inverter output voltage). Then, the maximum inductance of $L_{\rm r}$ yields

$$L_{\rm r-max} = \frac{1}{(22\pi f_{\rm o})^2 C_2}. \tag{17}$$

To filter out the harmonic at the switching frequency $f_{\rm s}$, the cutoff frequency should be ten times smaller than f_s. Then, the minimum inductance of L_r yields

$$L_{\rm r-min} = \frac{1}{(20\pi f_{\rm s})^2 C_2}. \tag{18}$$

And from mode analysis of NOC circuit, if the value of $L_{\rm r}$ ($L_{\rm r} > 0$) is set to be smaller, the range of zone D_2 may be longer, resulting in easier ZVS realization. But too small a value may increase the total harmonic distortion (THD).

E. Harmonic Suppression Control Strategy

The diagram of NOC circuit (the blue part) with a single-phase inverter (the green part) is shown in Fig. 5. The control objective is the voltage difference between the two capacitors (the conventional capacitor and the NOC). The voltage of conventional capacitor C_1 is u_{C1} and the port voltage of NOC $C_{\rm noc}$ is $u_{\rm noc}$. The system block diagram is shown in Fig. 6.

By sampling output voltage u_o and current i_o, the pulsating power can be obtained. Through a proportional–resonant (PR) controller (resonant frequency is $2f_{\rm o}$, where $f_{\rm o}$ is the frequency of output voltage), pure secondary power will be used as the power decoupling input of NOC branch. The high gain at $2f_{\rm o}$ of PR controller makes the impedance of NOC branch very small at $2f_{\rm o}$. Then the reference modulation voltage $u_{h\text{-ref}}$ can be obtained by (13). In voltage control loop, the voltages u_{C1} and $u_{\rm noc}$ of the NOC branch are obtained by (9). The other PR controller is used to make difference of u_{C1} and $u_{\rm noc}$ follows the reference value

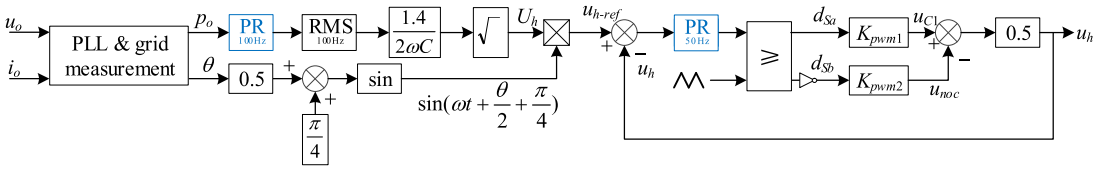


Fig. 6. System block diagram of NOC branch ($K_{\rm pwm}$ is the gain of generation of PWM wave. d_{Sa} and d_{Sb} are the duties of S_a and S_b, respectively).

$u_{h\text{-ref}}$ closely. Then, real-time NOC voltages, u_{C1} and $u_{\rm noc}$, are detected. According to (9), the difference value of u_{C1} and $u_{\rm noc}$ is equal to $2u_h$

$$u_{C1} - u_{\rm noc} = 2u_h. \tag{19}$$

In this way, errors caused by control and parasitic parameters may be divided equally between the two capacitors. Finally, the SHC is suppressed under closed-loop control.

Due to the digital control with high speed sampling and short step, the transfer function brings little delay. Meanwhile, the effect of delay to the amplitude can be ignored for rms calculation due to its periodic calculation. So, the delay mainly affects the phase. Fortunately, on the one hand, the harmonics ripple is periodic; on the other hand, in engineering implementation, the phase delay can be compensated by fine-tuning the value of "$\pi/4$" in the phase control part of Fig. 6.

The state-space averaging approach is also applied to analyze the NOC circuit. Considering $C_1 = C_2 = C$ in the decoupling capacitor circuit, the open-loop input impedance of decoupling capacitor $Z_{\rm i}$ can be derived as

$$Z_{\rm i} = \frac{1}{C_1 s} + \frac{1}{C_2 s}. \tag{20}$$

The closed-loop input admittance of the decoupling capacitor can be expressed as

$$Y_{\rm ic} = \frac{1}{Z_{\rm i}} - \frac{A_v K_v H_v K_{\rm pwm} G_{\rm id}}{1 + K_v H_v K_{\rm pwm} G_{\rm id}} \tag{21}$$

where A_v is the open-loop voltage magnification, which can be expressed as

$$A_v = d_{Sb}. \tag{22}$$

The duty cycle of S_b is d_{Sb}, which can be expressed as

$$d_{Sb} = \frac{1}{2}\left(1 + \frac{v_m}{V_{\rm tri}}\right) \tag{23}$$

where v_m is the reference sinusoidal wave of $u_{\rm noc}$, and $V_{\rm tri}$ is the peak of the triangular wave.

K_v is the voltage feedback coefficient, and H_v is the transfer function of voltage controller and is given by

$$H_v = K_p + \frac{K_i}{s}. \tag{24}$$

$K_{\rm pwm}$ is the transfer function of pulsewidth modulator (PWM), and $Z_{\rm i}$ is the open-loop input impedance of decoupling capacitor.

$$G_{\rm id} = \frac{-U_{\rm bus} C s}{2L_{\rm r} C s^2 + 1} \cdot (2d_{Sb} - 1). \tag{25}$$

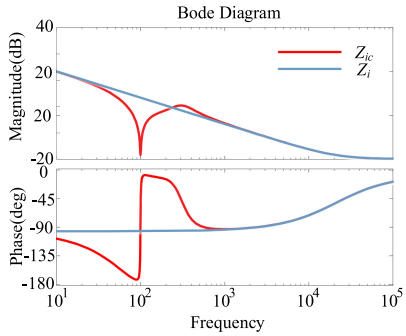


Fig. 7. Bode plots of $Z_{\rm i}$ and $Z_{\rm ic}$ ($Z_{\rm i}$ is the open-loop port-impedance of NOC branch and $Z_{\rm ic}$ is the closed-loop port-impedance).

The closed-loop input impedance of decoupling capacitor can be expressed as

$$Z_{\rm ic} = 1/Y_{\rm ic}. \tag{26}$$

The bode diagram of $Z_{\rm i}$ and $Z_{\rm ic}$ is shown in Fig. 7, where $Z_{\rm i}$ is the open-loop input impedance of NOC branch and $Z_{\rm ic}$ is the closed-loop input impedance. As seen from Fig. 7, $Z_{\rm i}$ has high magnitude in the low-frequency range. The characteristic of $Z_{\rm i}$ is equivalent to two capacitors C_1 and C_2 connected in series. The magnitude of $Z_{\rm ic}$ is very low to a valley value at $2f_{\rm o}$, suggesting a short circuit for the $2f_{\rm o}$ current harmonics.

III. Simulation and Experimental Results

In order to verify the feasibility of the proposed method, simulation was first performed in *Saber* software. The circuit diagram utilized in the simulation is shown in Fig. 5.

Considering the power rating of the microinverter and the theoretical derivation in the previous section, the specific circuit parameters are shown in Table I.

The simulation results are shown in Figs. 8–13. When NOC is inactivated, the waveforms of output voltage $u_{\rm o}$, input current $i_{\rm in}$, and capacitor C_2 voltage $u_{\rm noc}$ are shown in Fig. 8. Because when NOC is inactivated, C_2 behaves as a conventional capacitor, dividing the bus voltage equally with C_1. And $i_{\rm in}$ pulsates severely. Carrying out Fourier analysis for the input current $i_{\rm in}$, the amplitude of the SHC is 79.4% of dc component.

When NOC is activated, the waveforms and Fourier analysis of $i_{\rm in}$ are shown in Figs. 11 and 12, respectively. C_1 and C_2 both have a same dc bias, while their ac voltages vary oppositely. The SHC is reduced to 0.08% of dc component. However, the other low-order harmonic currents increase slightly.

In order to further verify the proposed method adaptation for suppressing the secondary ripple current under various types

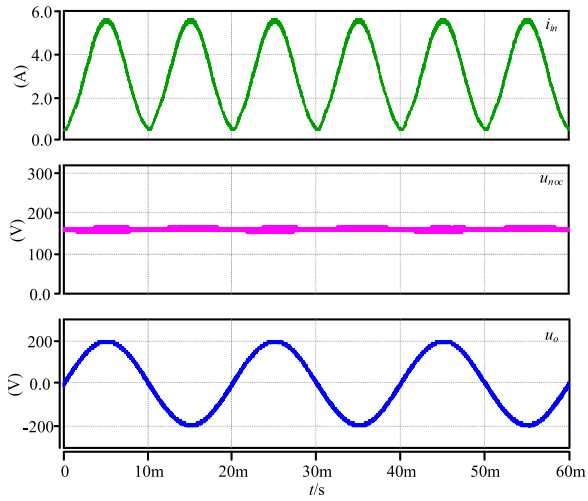


Fig. 8. Simulation waveforms of input current $i_{\rm in}$, NOC port voltage $u_{\rm noc}$, and output voltage $u_{\rm o}$ when NOC is inactivated under *R* load.

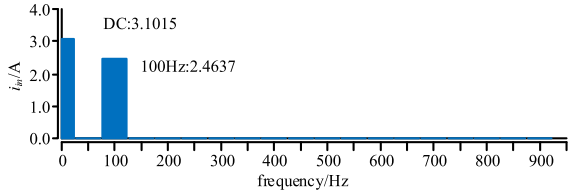


Fig. 9. Fourier analysis of $i_{\rm in}$ when NOC is inactivated under *R* load.

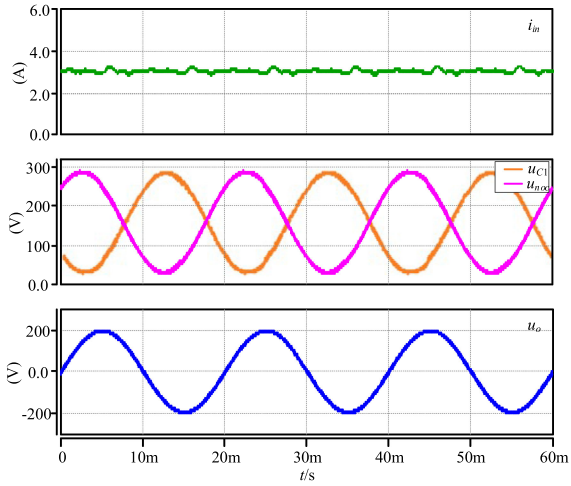


Fig. 10. Simulation waveforms of $i_{\rm in}$, u_{C1}, $u_{\rm noc}$, and $u_{\rm o}$ when NOC is activated under *R* load.

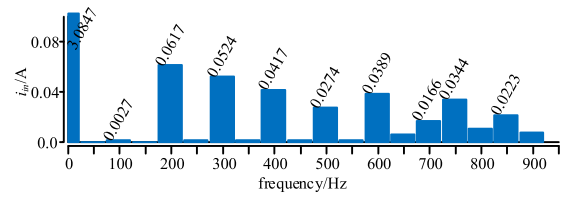


Fig. 11. Fourier analysis of $i_{\rm in}$ when NOC is activated under *R* load.

TABLE I
PARAMETERS OF THE PROTOTYPE AND SPECIFICATIONS OF THE UTILIZED COMPONENT

	Parameter	Value
Specification	Bus voltage U_{bus}	320V
	Bus capacitor C_{bus}	1μF
	Switching frequency f_s	10kHz
NOC circuit	Capacitor C_1	150μF
	Capacitor C_2	150μF
	Inductor L_r	120μH
H-bridge inverter	Output voltage u_o	200V
	Output frequency f_o	50Hz
	Load R_o	25Ω
	Filter capacitor C_f	1μF
	Filter inductor L_f	2.5mH

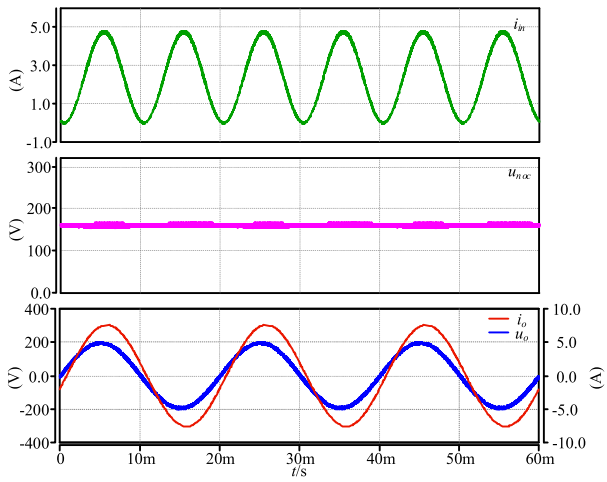


Fig. 12. Simulation waveforms of $i_{\rm in}$, $u_{\rm noc}$, and $u_{\rm o}$ when NOC is inactivated under *RL* load.

of loads, simulations are performed under resistive−inductive (*RL*) load. Under an *RL* load test, a 25-Ω resistor series with a 19-mH inductor is employed and the results are shown in Figs. 12 (NOC is inactivated) and 13 (activated). The 100-Hz component of the input current only accounts for 0.3% of dc component. It verifies that the proposed method can absorb the secondary current ripple well even when the inverter powers a nonpure resistive linear load, only adjusting the voltage phase β.

The above simulation results have verified the feasibility of the proposed method, and the experiment is implemented for further verification. The experimental parameters and the prototype are shown in Table I (the same as simulation) and Fig. 14, respectively.

When NOC is inactivated, the output voltage $u_{\rm o}$ and input current $i_{\rm in}$ are shown in Fig. 15(a). The inverter powers a pure resistive load and the output power fluctuates at twice the frequency. Hence, the input current $i_{\rm in}$ contains secondary harmonic, which accounts for 88.9% of dc component as seen in Fig. 15(b). The output voltage is a standard sine wave with peak voltage of 196 V and frequency of 50 Hz, as seen from the Fourier analysis of $u_{\rm o}$ in Fig. 15(c).

When NOC is activated, the key waveforms are shown in Fig. 16. The SHC is reduced to 2.04% of dc component. And

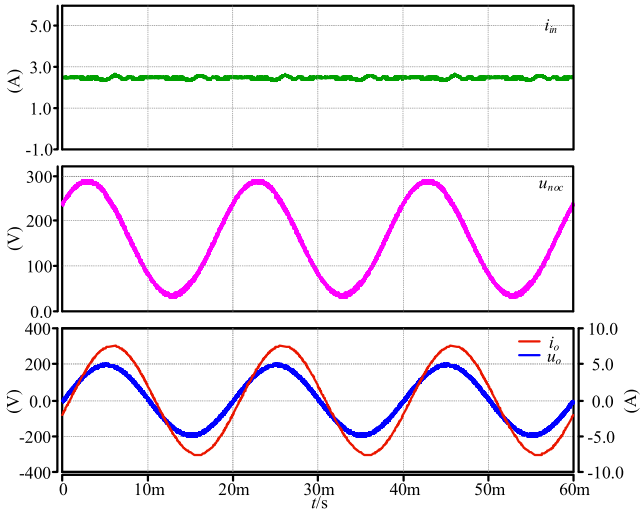


Fig. 13. Simulation waveforms of i_{in}, u_{C2}, and u_{o} when NOC is inactivated under *RL* load.

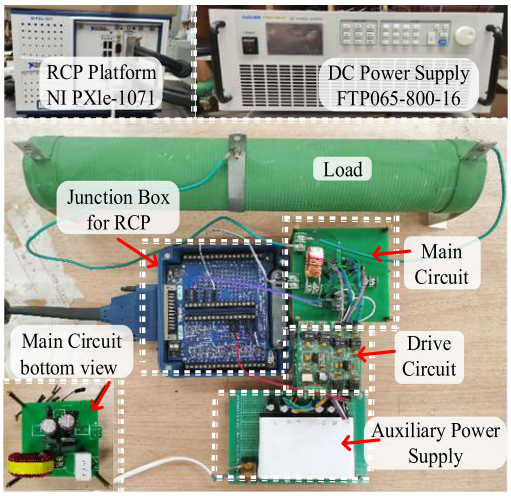


Fig. 14. Experimental equipment and prototype of the proposed circuit.

the components of other low-order harmonic currents increase slightly, which is the same as simulation. As seen from the right table in Fig. 16(b), the Fourier analysis results from the scope, the largest low-order harmonic current is 115 mA at 650 Hz, which is the 13th-order harmonic and accounts for 4.20% of dc component. The Fourier analysis of u_{noc} is shown in Fig. 16(c). It is a 50-Hz sine wave with a dc bias of 157 V (almost half the input voltage). And the amplitude of 50 Hz component closes to 120 V. The Fourier analysis of output voltage u_{o} is shown in Fig. 16(d). As seen in Fig. 16(d), there is little difference from the output voltage waveform when NOC is inactivated, which fully shows that the NOC branch has little influence on ac output side.

The port voltage u_{noc} and port current i_{noc} of C_{noc} to suppress SHC are shown in Fig. 17, where u_{noc} leads i_{noc} by a quarter of a cycle. Consistent with theoretical analysis, the NOC has the inductive port characteristics, and the equivalent capacitance of NOC is opposite to that of conventional capacitor.

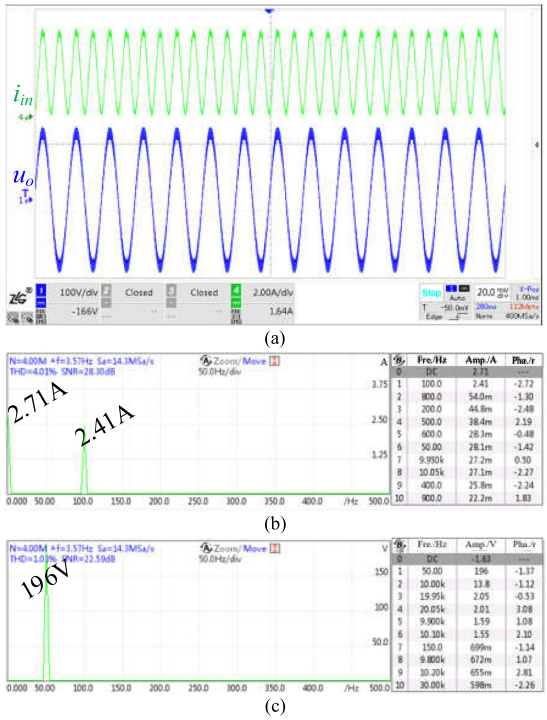


Fig. 15. Experimental key waveforms when NOC is inactivated under *R* load. (a) i_{in} and u_{o}. (b) Fourier analysis of i_{in}. (c) Fourier analysis of u_{o}.

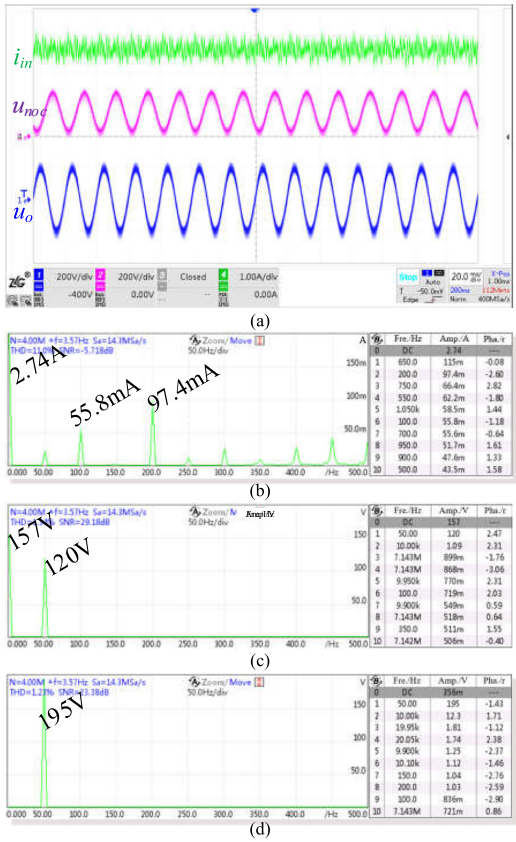


Fig. 16. Experimental key waveforms when NOC is activated under *R* load. (a) i_{in}, u_{C2}, and u_{o}. (b) Fourier analysis of i_{in}. (c) Fourier analysis of u_{C2}. (d) Fourier analysis of u_{o}.

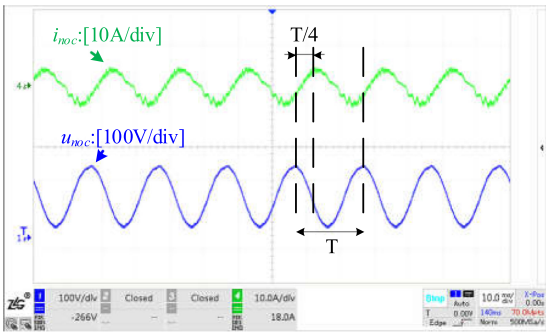
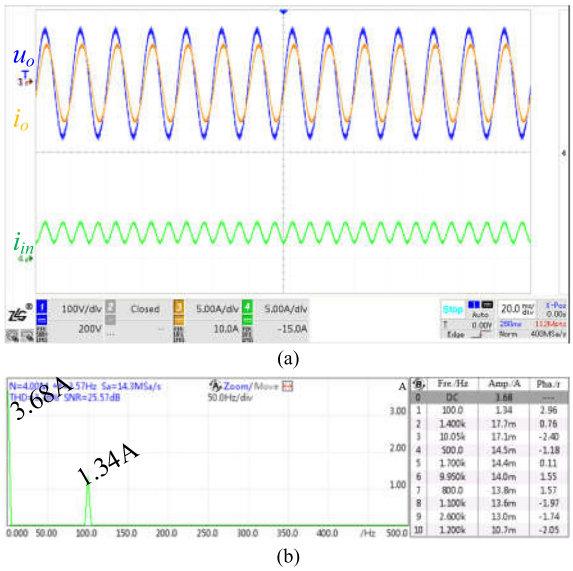


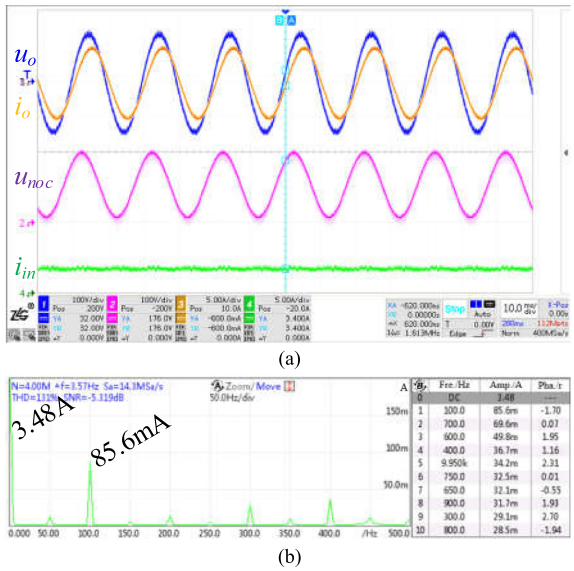
Fig. 17. Waveforms of U_{noc} and I_{noc} when NOC suppresses second harmonic current.



(a)

(b)

Fig. 18. Experimental key waveforms when NOC is inactivated under *RL* load. (a) i_{in}, i_{o}, and u_{o}. (b) Fourier analysis of i_{in}.



(a)

(b)

Fig. 19. Experimental key waveforms when NOC is activated under *RL* load. (a) i_{in}, i_{o}, u_{noc}, and u_{o}. (b) Fourier analysis of i_{in}.

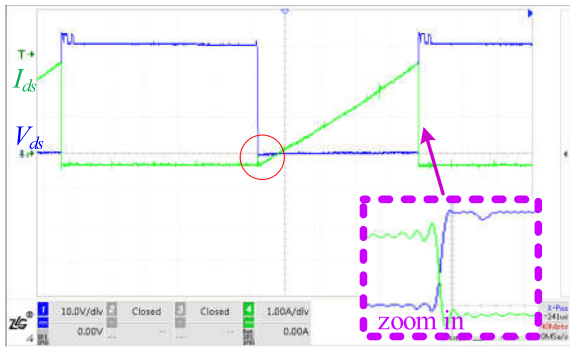


Fig. 20. Experimental waveforms of the current I_{ds} and voltage V_{dc} of S_b in switching cycle.

In the case of *RL* load (19-mH series with 25 Ω, the same as simulation), the experimental results also prove the feasibility of the proposed method. When NOC is inactivated, the key waveforms are shown in Fig. 18. The SHC accounts for 36.4% of dc component. When NOC is inactivated, as shown in Fig. 19, the SHC is reduced to 85.6 mA, which is only 2.46% of dc component.

The soft switching realization in the NOC branch is shown in Fig. 20. As shown in the red circle, the current I_{ds} changes from negative to positive value by about 5 μs after the V_{ds} drops to 0 V, which verifies the realization of ZVS turn-ON. The turn-OFF process is zoomed in the purple box in Fig. 19, where I_{ds} and V_{ds} have little overlap. Due to the output capacitance for the switch and the low inductance, the voltage across the switch will rise gradually, but the current falls quickly. So, the turn-OFF loss becomes small and it could be ignored. In summary, the soft switching of the proposed branch has been realized. And the measured conversion efficiency is shown in Fig. 21. The blue line represents the efficiency curve of the H-bridge inverter in which NOC is inactivated. When the NOC is activated, the efficiency curve of the H-bridge inverter is shown with the orange line. As seen, when the NOC is activated, the overall conversion efficiency of the system has about 2% reduction due to the additional power loss from the NOC circuit.

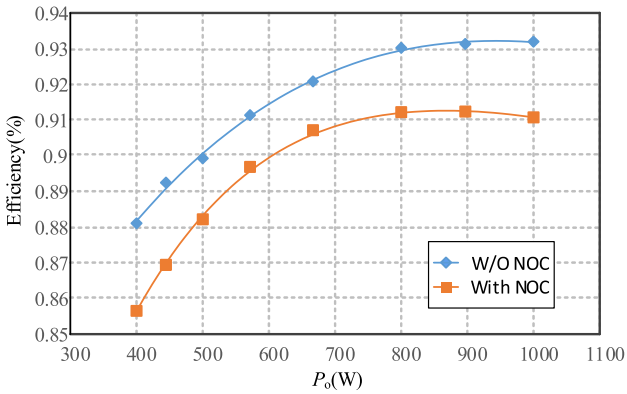


Fig. 21. Measured conversion efficiency.

The waveforms of start-up process for the NOC circuit are shown in Fig. 22(a). It takes 5.2 ms about a quarter of line

TABLE II
PERFORMANCE COMPARISON OF SECONDARY RIPPLE SUPPRESSION

Paper	Power level/line voltage/frequency	Capacitors number and value	Inductance value	Switches number	Harmonic content	Rectifier /Inverter	Q
[18]	2kW/450V/60Hz	100μF/430μF	94μH	4	Current 15%	Inverter	0.068
[19]	750W/200V/60Hz	110μF/470μF/3μF	750μH	4	Current 4.6%	Rectifier	0.084
[20]	1kW/380V/50Hz	100μF/820μF	2mH	2	Current 4.0%	Inverter	0.078
Proposed	800W/320V/50Hz	150μF/150μF/1μF	120μH	2	Current 4.2%	Inverter	0.092

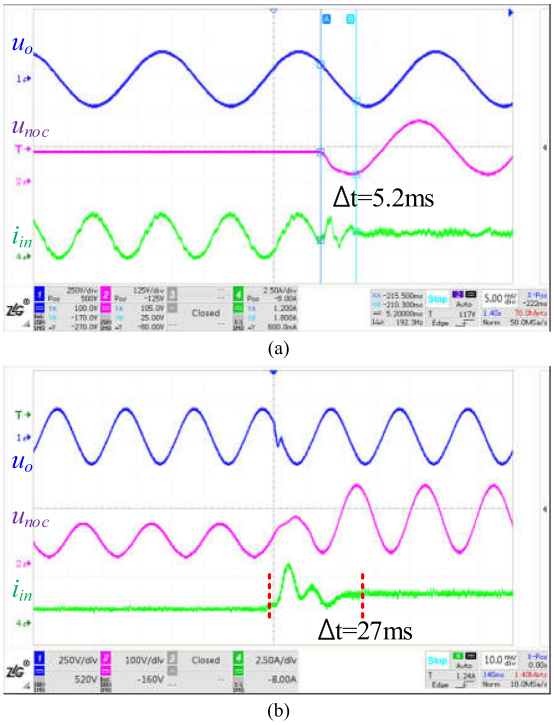


Fig. 22. Dynamic response of NOC branch. (a) At the moment the NOC is cut in. (b) Load step-change when NOC is activated.

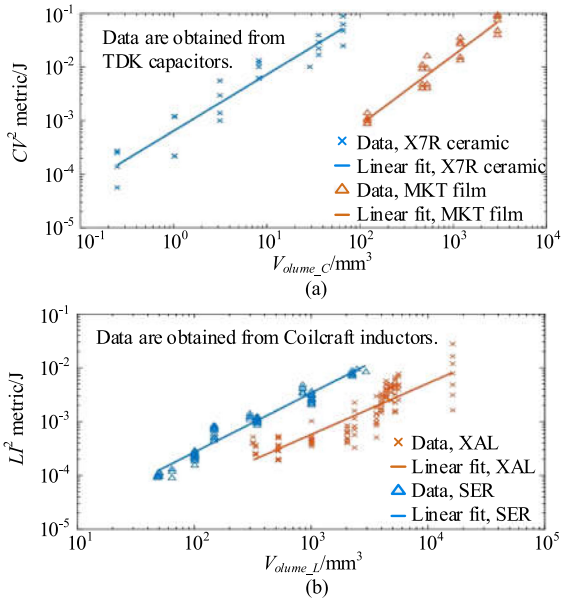


Fig. 23. Relationship between the volume of passive devices and stored energy. (a) Volume V_{olume_C} versus capacitance value C and withstand voltage V. (b) Volume V_{olume_L} versus inductance value L and maximum operating current I.

voltage period, to reach the stable voltage value. Although the input current $i_{\rm in}$ oscillates slightly at the startup process, it can quickly approach stable state as well. The output voltage goes on maintaining high quality waveform during the start-up process, which further shows that the NOC branch has little influence on the inverter output voltage and owns the plug-in/plug-out characteristics.

The dynamic response waveform of load step-change is shown in Fig. 22(b). When the load step changes from 50 to 25 Ω, the output voltage $u_{\rm o}$ only produces a small oscillation and it takes about 27 ms for the input current $i_{\rm in}$ to enter a new steady state. The port voltage $u_{\rm noc}$ of the NOC will also return quickly to follow new reference.

Fig. 22 shows the relationship between the volume of capacitor and inductor versus stored energy, respectively, where C, V, L, and I denote the capacitance value, the withstand voltage, the inductance value, and the maximum operating current, respectively. The capacitor volume V_{olume_C} and the inductor volume V_{olume_L} can be calculated based on the orange fitting line in Fig. 23(a) with the expression of (27) and Fig. 23(b) with the expression of (28), respectively. Results show the superiority of the proposed method in absorbing secondary harmonic

$$\lg CV^2 = 1.3846 \cdot \lg V_{olume\_C} - 5.7692 \tag{27}$$

$$\lg LI^2 = 0.8823 \cdot \lg V_{olume\_L} - 6.1294. \tag{28}$$

A coefficient Q, in J/mm^3, is introduced to characterize the ripple absorption effect at unit power density. Its definition is written as

$$Q = \frac{P}{V_{olume\_C} + V_{olume\_L}} \cdot \frac{1}{r} \tag{29}$$

where P represents the power level, r means harmonic content, V_{olume_C} represents the volume of the capacitor used, and V_{olume_L} represents the volume of the inductor used.

Table II presents the performance comparison of secondary ripple absorption between the proposed method and the counterparts. In [18], a circuit composed of two capacitors of 100 and 430 μF, a 94-μH inductor, and four switches is employed to suppress the current ripple at dc bus, and the harmonic current is reduced to 15% of dc component. In [19], three capacitors of 110, 470, and 3 μF, an inductor of 750 μH, and four switches are employed to suppress the current ripple at the dc bus of a rectifier,

where the secondary ripple amplitude is reduced to 4.6%. In [20], the small capacitor employed in the additional circuit is only 100 μF. However, the huge inductor and bus capacitor will decrease the power density. In the proposed method, only two 150-μF capacitors, one 120-μH inductor, and two switches are employed to suppress the SHC at dc bus. The secondary harmonic amplitude is reduced to 2.04% of dc component, while the 13th-order harmonic is increased to 4.10%.

IV. Conclusion

An NOC (FOC with $\alpha = -1$) based method is proposed to suppress SHC on the dc side of a voltage source inverter.

1) It develops the concept of fractional capacitor and applies it into power decoupled occasion: The impedance of capacitor could be expanded to all the real number fields from traditional positive integer fields. Inductive and capacitive reactance could be unified to deal with.
2) It proposes a fractional capacitor without additional power supply and presents a control method to realize fractional capacitor, including obtaining the reference voltage and control strategy. The NOC is proposed to achieve the equivalent zero impedance for the specific order harmonics to absorb the current harmonics, reducing the volume of energy storage components required in the system.
3) The NOC works in parallel on the dc bus with little influence to the output side. Meanwhile, the pulsating power is only circuited between the ac output side and the NOC branch, which improves the lifespan and stability of the power supply greatly.
4) The proposed method has low cost (one inductor, two switches, two capacitors, and simple control) compared with the counterparts. The small value of inductance helps the harmonics absorbing branch to realize soft switching operation and reducing loss.

In the microgrid system, when multiple kinds of converters are linked to the bus, the bus current contains not only the second harmonic but also other frequencies within the harmonic current. Meanwhile, the first-order current harmonic may result from asymmetric capacitance or equivalent series resistances themselves. Such cases will be concerned in the future work.

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