A Power-Efficient Resonant Current Mode Receiver With Wide Input Range Over Breakdown Voltages Using Automated Maximum Efficiency Control

Hyun-Su Lee, *Student Member, IEEE*, Jisan Ahn, *Student Member, IEEE*, Kyeongho Eom, *Student Member, IEEE*, Woojoong Jung, *Student Member, IEEE*, Seung-Ju Lee, *Student Member, IEEE*, Yeon-Woo Jung, *Student Member, IEEE*, Se-Un Shin, *Member, IEEE*, and Hyung-Min Lee, *Member, IEEE*

***Abstract*—This article proposes a series-*LC* resonant current mode receiver (RCM R_X) for wirelessly powered battery chargers. With a series-*LC* scheme, the RCM R_X can operate at higher resonant voltages than transistor breakdown voltages, enabling robust near-field wireless power transfer. In the series-*LC* RCM R_X, a dual automated maximum efficiency control (AMEC) and a passive zero-current detector (ZCD) adaptively adjust operation states, ensuring nonresidual energy in the R_X *LC* tank at the end of the charging mode. Moreover, the passive ZCD operation algorithm increases the power delivered to the load or battery by minimizing the idle period between charging and resonant modes. The 180-nm standard CMOS chip, which used only 1.8-V transistors, can operate with 6.84× higher resonant voltage up to 12.32 V than the transistor breakdown voltage, 1.8 V, while receiving an input power up to 169 mW, enabling a wide input range over variable coil distances. The proposed system achieves the measured power conversion efficiency up to 84.9% at the input power of 16.8 mW.**

***Index Terms*—Automated maximum efficiency controller, implantable medical devices (IMD), near field, nonresidual energy, resonant current mode (RCM), series *LC*, transistor breakdown voltage, wide input range, wireless power transfer (WPT).**

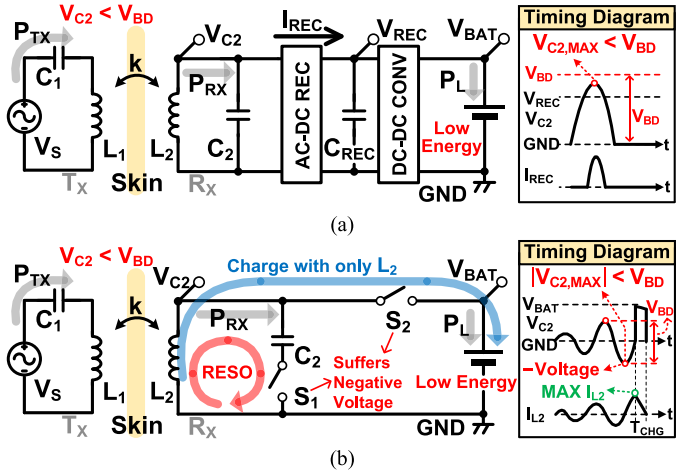


Fig. 1. Conceptual diagrams of the conventional (a) VM rectifier and (b) parallel-*LC* RCM R_X.

I. Introduction

IMPLANTABLE medical devices (IMDs) have been widely used for various applications, such as neural recording for brain diagnosis [1], deep brain stimulation for neurological diseases [2], cochlear implant for the auditory disorder [3], and electroencephalography (EEG) monitoring for epilepsy control [4]. These IMDs operate with an internal battery, and the battery can be charged by wireless power transfer (WPT) through coupled inductive coils, which is a noninvasive process. Recently, IMDs integrating numerous units such as optical stimulation, electrical stimulation, and neural recording with multichannels in a single chip have been studied [5]–[9], which require supply power up to tens of milliwatt from the battery. To provide massive power to the IMDs from the battery, ac voltage in a receiver (R_X) coil, which can be received from a transmitter (T_X), should be large enough. However, with up-to-date technologies, the ac voltage cannot exceed the transistor breakdown voltages, which reduces the power delivered to the battery or load (PDL) and may cause safety concerns.

Fig. 1(a) shows the conventional structure of the voltage mode (VM) rectifier [10]–[28]. The ac–dc rectifier generates dc voltage V_{REC} with ac voltage V_{C2} received from T_X. When V_{C2} is larger than V_{REC}, the rectifier current I_{REC} charges rectifier output capacitor C_{REC}. The dc–dc converter converts V_{REC} to the battery voltage V_{BAT}. However, when the VM rectifier receives power over a short coil distance, which increases the coupling coefficient k, the R_X coil voltage can exceed the transistor breakdown voltage V_{BD} [13]. This may cause

Manuscript received August 17, 2021; revised November 6, 2021 and January 4, 2022; accepted February 2, 2022. Date of publication February 14, 2022; date of current version March 24, 2022. This work was supported by the Technology Innovation Program under Grant 20010712 funded by the Ministry of Trade, Industry and Energy (MOTIE), South Korea. Recommended for publication by Associate Editor J. Acero. *(Corresponding authors: Se-Un Shin; Hyung-Min Lee.)*

Hyun-Su Lee, Jisan Ahn, Kyeongho Eom, Woojoong Jung, and Hyung-Min Lee are with the School of Electrical Engineering, Korea University, Seoul 02841, South Korea (e-mail: abagnale1994@korea.ac.kr; promise0w0@korea.ac.kr; ukh95@korea.ac.kr; dneld156@korea.ac.kr; hyungmin@korea.ac.kr).

Seung-Ju Lee, Yeon-Woo Jung, and Se-Un Shin are with the Department of Electrical Engineering, Ulsan National Institute of Science and Technology, Ulsan 44919, South Korea (e-mail: leesj96@unist.ac.kr; yeonu21@unist.ac.kr; seuns@unist.ac.kr).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3151427.

Digital Object Identifier 10.1109/TPEL.2022.3151427

serious damages to 0the human body as well as IMDs while charging the battery with smaller V_{C2} than V_{BD} will result in a lower PDL (P_L), which may not be suitable for power-hungry applications. Moreover, the distance between $\mathrm{T_X}$ and $\mathrm{R_X}$ coils should be carefully considered for safe WPT. To prevent the transistor breakdown by excess WPT over a short distance, IMDs typically adopt overvoltage protection depending on resonant voltage levels across the $\mathrm{R_X}$ coil [14]. However, those methods, at a short coil distance, lead to poor power conversion efficiency (PCE) defined as P_L divided by the received power P_{RX} and power transfer efficiency (PTE) defined as P_L divided by the transmitted power P_{TX}.

Fig. 1(b) shows the conventional structure of a parallel-*LC* resonant current mode (RCM) $\mathrm{R_X}$ [29]–[33]. The parallel-*LC* RCM $\mathrm{R_X}$ boosts a small input voltage over a few resonant cycles until inductor current I_{L2} reaches its maximum and charges the battery directly with I_{L2}. However, the conventional parallel-*LC* RCM $\mathrm{R_X}$ suffers from a negative resonant capacitor voltage V_{C2} so that a resonant switch $\mathrm{S_1}$ and a charging switch $\mathrm{S_2}$ should be carefully designed [29]. Moreover, V_{C2} cannot exceed breakdown voltages of $\mathrm{S_{1,2}}$, decreasing the received wireless power in the $\mathrm{R_X}$, P_{RX}. The degradation of P_{RX} leads to lower power transferred to the battery (PDL), which may not be an optimal choice for power-hungry devices. Thus, the parallel-*LC* RCM $\mathrm{R_X}$ cannot operate efficiently at a short coil distance due to higher V_{C2}. Also, to increase the efficiency at a larger coil distance, the time-interleaved scheme, which alternately charges two resonant capacitors for continuous operation, has been introduced [30]. However, this parallel-*LC* RCM receiver suffers from the limited Rx input power due to the larger coil distance and smaller input voltage V_{C2} in the resonant $\mathrm{R_X}$ *LC* tank, degrading the PDL.

On the other hand, a series-*LC* RCM $\mathrm{R_X}$ was proposed to operate with higher resonant voltages [34], [35]. However, it needs a reliable sensing circuit to detect the point where the resonant voltage becomes zero and to control the RCM operation while requiring an auxiliary high-speed comparator and additional power consumption. The conventional series-*LC* RCM $\mathrm{R_X}$ also suffers from efficiency degradation due to residual energy, which is stored in the resonant capacitor but not transferred to the battery during the charging period.

To overcome these limitations, this article proposes a dual automatic maximum efficiency controller (AMEC) with two digital feedback for the series-*LC* RCM $\mathrm{R_X}$ structure to efficiently charge the battery until the residual power in the *LC* tank becomes zero and to reliably transfer the power with higher resonant voltages than the breakdown voltage. In addition, the proposed algorithm with a zero-current detector (ZCD) can minimize the idle period between charging and resonant modes, increasing the PDL and PTE [36].

The rest of this article is organized as follows. Section II describes the operation principle of the proposed series-*LC* RCM $\mathrm{R_X}$, and Section III explains the detailed circuits and algorithms. Theoretical analysis of the series-*LC* RCM $\mathrm{R_X}$ with dual AMEC compared to conventional RCM $\mathrm{R_X}$ is presented in Section IV. Section V verifies the series-*LC* RCM $\mathrm{R_X}$ with chip measurement results. Finally, Section VI concludes this article.

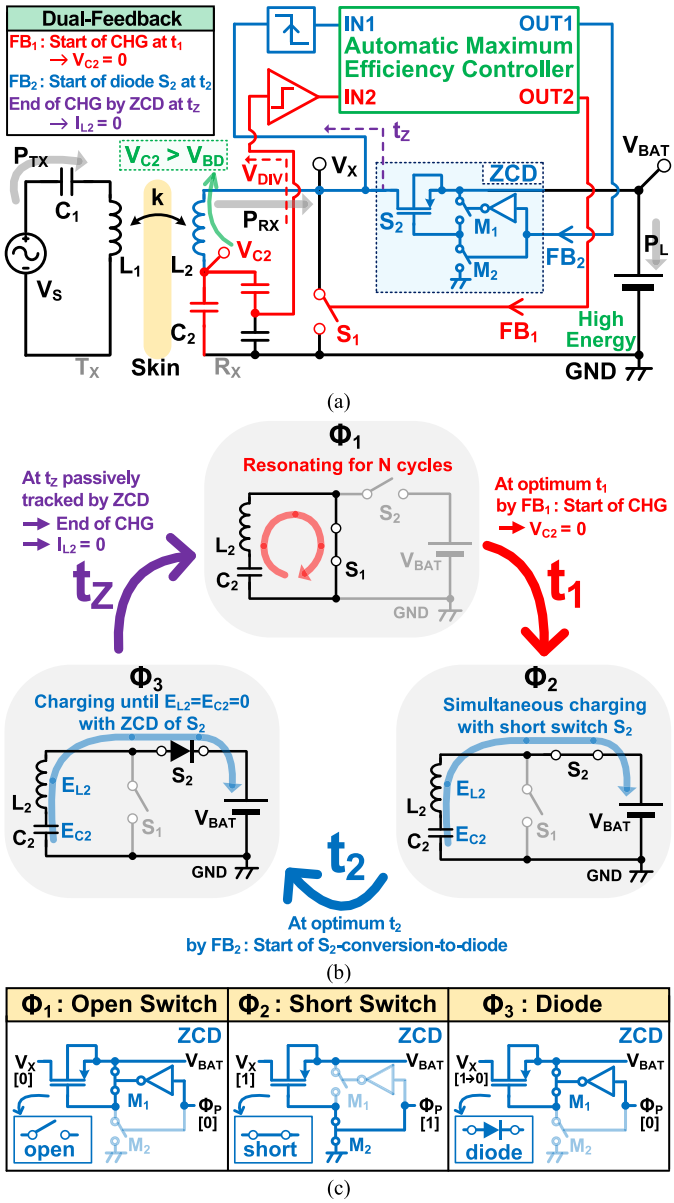


Fig. 2. Conceptual diagrams of the (a) proposed series-*LC* RCM Rx with dual AMEC, (b) operation phases, and (c) ZCD configurations.

II. System Architecture

Fig. 2(a) shows the proposed series-*LC* RCM $\mathrm{R_X}$ with dual AMEC for the battery charger. The series-*LC* RCM $\mathrm{R_X}$ consists of an $\mathrm{R_X}$ coil L_2, a resonant capacitor C_2, dual AMEC, resonant switch $\mathrm{S_1}$, and ZCD. The ZCD includes a charging power switch $\mathrm{S_2}$, the gate driving switches $\mathrm{M_{1,2}}$, and an inverter. $\mathrm{M_1}$ (PMOS) and $\mathrm{M_2}$ (NMOS) support the ZCD operation by connecting the gate of $\mathrm{S_2}$ to either V_{BAT} of ground (GND) while requiring much smaller costs such as silicon area and power consumption compared to the power switches, $\mathrm{S_1}$ (NMOS) and $\mathrm{S_2}$ (PMOS).

The series-*LC* RCM R_X has two operation modes with two switches, S_1 and S_2. 1) Resonant mode: S_1 connects V_X to *GND* to boost the capacitor voltage V_{C2} received from the T_X while S_2 is opened. 2) Charging mode: S_1 opens and S_2 connects V_X to V_{BAT} to transfer energy from L_2C_2 tank to the battery. Just before the end of energy transfer, S_2 is converted to a diode, transferring all the energy until the residual energy of L_2C_2 tank is zero.

The dual AMEC uses two digital feedback, FB_1 and FB_2, to transfer all energies in L_2C_2 as shown in Fig. 2(a). FB_1 senses V_{C2} and finds the optimum end-of-resonance timing, which is equal to a start-of-charging timing, t_1. This timing is reflected in the control signal of S_1 and makes V_{C2} become zero at the end of charging. Also, the diode mode in S_2 ends passively by ZCD operation at t_Z when the current flows through S_2, I_{S2}, becomes zero. t_Z determines the end-of-charging timing, which becomes a start-of-resonance timing in the next period again without the idle period. FB_2 senses t_Z and finds the optimum S_2-conversion-to-diode timing t_2. This t_2 is reflected in the control signal of S_2 to ensure safe and efficient charging. Consequently, the proposed series-*LC* RCM R_X simultaneously charges the battery until V_{C2} and I_{L2} are zero at the end of charging.

Fig. 2(b) shows the three operation phases of series-*LC* RCM R_X and Fig. 2(c) shows three configurations in three operation phases of ZCD. The phase Φ_1 is the resonant mode and phases $\Phi_{2,3}$ are charging modes.

Operation Φ_1: In phase Φ_1, S_1 closes and V_X is connected to the *GND*. As M_1 closes and M_2 opens in ZCD, S_2 operates as an open switch. Thus, L_2C_2 tank resonates for multiple resonant cycles to increase V_{C2}.

Operation Φ_2: At the optimum t_1 by FB_1, the operation phase Φ_2 starts. It is noted that the optimum t_1 determines the capacitor voltage V_{C2} to become zero at the end of charging, t_Z. In phase Φ_2, S_1 opens. Also, as M_1 opens and M_2 closes in ZCD, S_2 is converted to a shorted switch. Thus, V_X is connected to V_{BAT} and simultaneously delivers the energy in L_2, E_{L2}, and the energy in C_2, E_{C2}, to the battery.

Operation Φ_3: At the optimum t_2 by FB_2, the operation phase Φ_3 starts. In the phase Φ_3, M_1 closes and M_2 opens in ZCD, and S_2 can be reconfigured to a diode. Also, the body diode between drain and body of S_2 is in the same direction as the reconfigured S_2 diode, and they are connected in parallel. The diode-connected S_2 transfers the rest of E_{L2} and E_{C2} to the battery, until the current flowing through S_2, I_{S2}, becomes zero, leading V_X to fall from V_{BAT} to *GND*. Then, the diode operation of S_2 ends and S_2 is converted to an open switch, generating the end-of-charging timing, t_Z. Indeed, t_Z is passively tracked by ZCD operation, and at this timing, I_{L2} is zero. Accordingly, FB_2 determines t_2 in the next period to be closer to the $I_{S2} = 0$ timing, t_Z. Next, at passively tracked t_Z, the phase Φ_1 starts immediately again and resonates V_{C2}. Thus, the idle time between charging and resonant modes can be eliminated, thereby raising the charging period per sum of charging, resonant, and idle period, which means that PDL can be increased. Consequently, thanks to the dual AMEC, the energy in the L_2C_2 tank can be completely transferred to the battery, while resulting in no residual energy

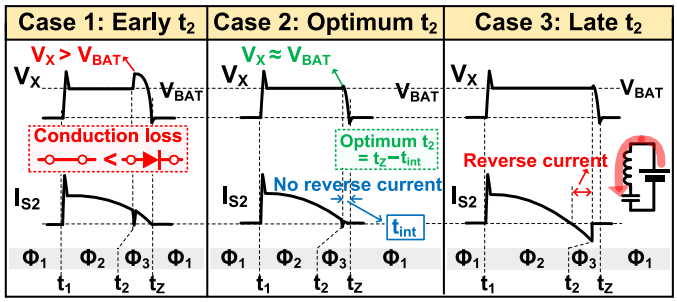


Fig. 3. Operation waveforms of V_X and I_{S2} according to the timing of t_3.

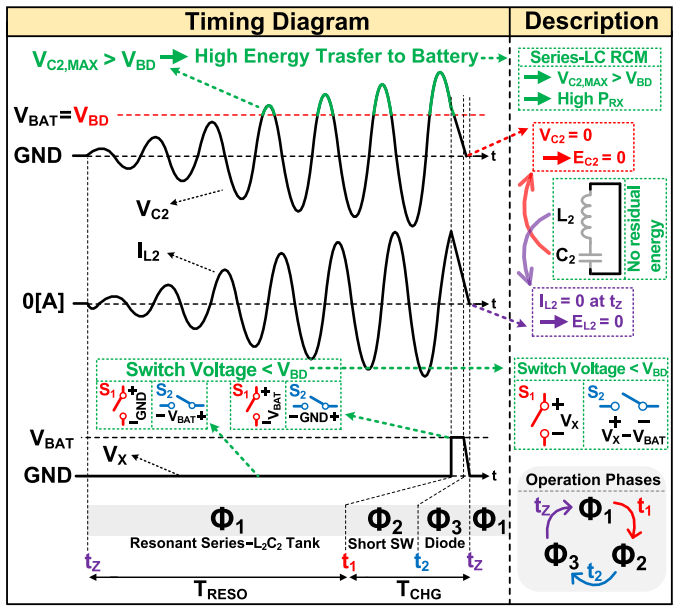


Fig. 4. Timing diagram of the proposed series-*LC* Rx receiving resonant voltages over the transistor breakdown voltage.

across L_2 and C_2 at the end of charging, improving PCE and PTE for near-field resonant-mode WPT.

The optimum S_2-conversion-to-diode timing t_2 by FB_2 is needed for safe charging and achieving high PCE as shown in Fig. 3. When t_2 comes too earlier, charges can be accumulated in the V_X node, resulting in a large voltage that can damage switches in Φ_3. Also, since conduction loss of the diode-connected S_2 in Φ_3 is higher than the shorted switch S_2 in Φ_2, the duration of Φ_3 should be as small as possible to achieve high PCE. On the other hand, when t_2 comes later, the reverse current flows from V_{BAT} to the L_2C_2 tank, degrading PCE. Accordingly, there is an optimum point of t_2 for high PCE, and this t_2 is the time just before t_Z by predetermined interval time delay, t_{int}. This t_{int} is employed to guarantee timing margins for reliable operation. In conclusion, FB_2 senses t_Z and sets the optimum S_2-conversion-to-diode timing, t_2, for the next period so that $t_2 + t_{int}$ becomes closer to t_Z for safe and efficient charging operation. Also, the optimum t_2 and diode-connected ZCD operation prevent the reverse current in Φ_2 and Φ_3, as shown in Fig. 3.

Fig. 4 shows the timing diagram of the series-*LC* RCM R_X receiving power over transistor breakdown voltage, V_{BD}. Also,

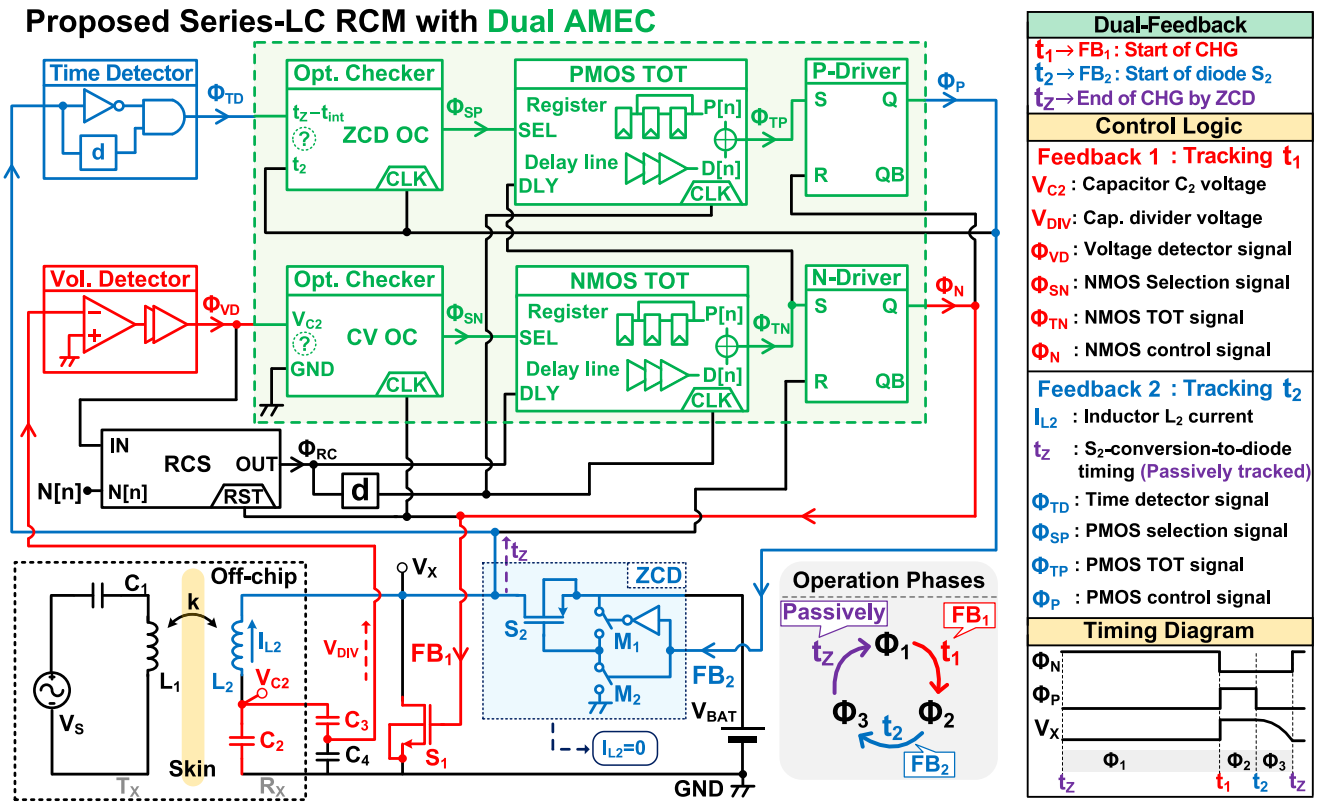


Fig. 5. Overall system architecture of the proposed series-*LC* RCM receiver with dual AMEC.

this series-*LC* scheme produces a larger resonant voltage V_{C2} across L_2 and C_2 with a voltage higher than the transistor breakdown voltage at short coil distances while at the same time resulting in high PDL (P_L) due to the high P_{RX}. In addition, unlike the conventional series-*LC*, which connects one terminal of L_2 to the ground, the proposed series-*LC* RCM $\mathrm{R_X}$ connects C_2 to the ground for reliable wide-range sensing of resonant voltages. Then, an on-chip capacitor-dividing voltage detector senses the large V_{C2} and provides the divided signal to the AMEC without transistor breakdown.

Moreover, the maximum voltages of $\mathrm{S_{1,2}}$ are the same as V_{BAT}, which is lower than V_{BD}. During the resonant mode Φ_1, $\mathrm{S_1}$ closes and $\mathrm{S_2}$ opens, connecting a switching node voltage V_X to the ground. Then, the maximum voltage stress across $\mathrm{S_1}$ and $\mathrm{S_2}$ are equal to *GND* and V_{BAT}, respectively. During the charging mode Φ_2 $\mathrm{S_1}$ opens and $\mathrm{S_2}$ closes, connecting V_X to V_{BAT}. Then, the maximum voltage stress across $\mathrm{S_1}$ and $\mathrm{S_2}$ are equal to V_{BAT} and *GND*, respectively. Since V_X can be defined as *GND* or V_{BAT}, $\mathrm{S_1}$ and $\mathrm{S_2}$ always have limited voltage stress below V_{BAT} despite the larger V_{C2} than transistor breakdown voltage V_{BD}.

III. Circuit Implementation

A. Overall System

Fig. 5 shows the overall system structure of the proposed series-*LC* RCM $\mathrm{R_X}$ with dual automated maximum efficiency control (AMEC) and passive ZCD operation, resulting in non-residual energy in L_2C_2 tank at the end of the charging mode and no idle time between charging and resonant modes. The dual AMEC, resonant cycle selector (RCS), ZCD, and two power switches $\mathrm{S_{1,2}}$ are integrated inside the chip, and the passive components, such L_2 and C_2, are external components, which have higher allowable voltage stress than on-chip transistors. The dual AMEC includes optimum checkers (OC), tick-tock optimum trackers (TOT), and switch drivers to control $\mathrm{S_1}$ and $\mathrm{S_2}$. The dual AMEC uses dual digital feedback, $\mathrm{FB_1}$ and $\mathrm{FB_2}$, to track optimum t_1 and t_2 for the next period, respectively. It is noted that t_Z is passively tracked by the passive ZCD operation.

Feedback 1 (FB1) tracking t_1: An on-chip capacitor divider with C_3 and C_4 converts V_{C2} to V_{DIV}, which has a lower voltage level than transistor breakdown voltages V_{BD}. A comparator-based voltage detector compares V_{DIV} to *GND* and generates a digital signal Φ_{VD}, which can be used for an RCS to determine the number of resonance cycles by generating Φ_{RC}. A capacitor voltage (CV) OC, synchronized with an NMOS control signal, Φ_N, as clock (CLK), monitors Φ_{VD} and provides NMOS selection signal Φ_{SN}, to adjust t_1 for start timing of phase Φ_2 in the next period. An NMOS TOT adjusts $\mathrm{S_1}$ turn-OFF timing t_1 depending on the state of Φ_{SN} for the next period by providing NMOS TOT signal Φ_{TN}. An N-driver generates Φ_N by using Φ_{TN} and V_X to control $\mathrm{S_1}$. It is noted that Φ_N, which falls to *GND* at t_Z by the passive ZCD operation, can be used to immediately start the phase Φ_1. This $\mathrm{FB_1}$ makes V_{C2} become zero at the end-of-charging timing in a steady state.

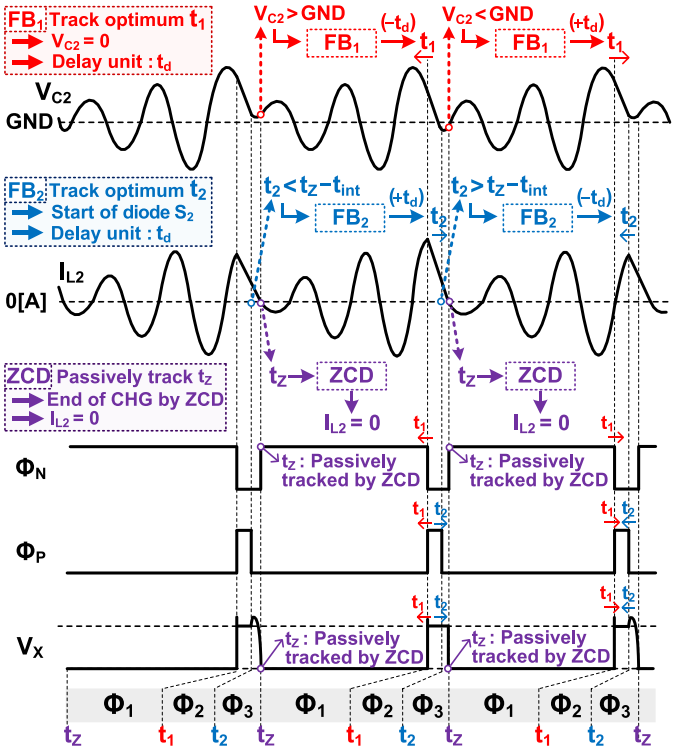


Fig. 6. Timing diagram of dual AMEC and passive ZCD operation.

Feedback 2 (FB2) tracking t_2: A ZCD time detector (TD) detects t_Z, falling time of V_X, and generates Φ_{TD}. A ZCD OC, synchronized with PMOS control signal Φ_P, as *CLK*, utilizes Φ_{TD} that rises at t_Z and Φ_P that falls at t_2 to generate PMOS selection signal Φ_{SP}. Φ_{SP} adjusts t_2 for start timing of phase Φ_3 in the next period to obtain the optimal start time of the S_2-conversion-to-diode. As we mentioned in Fig. 3, $t_Z - t_{\mathrm{int}}$ has to be the same as t_2 for high PCE and safety issues. Thus, the ZCD OC delays the t_2 by t_{int}, generating $t_2 + t_{\mathrm{int}}$. Also, comparing t_Z and $t_2 + t_{\mathrm{int}}$ is the same as comparing $t_Z - t_{\mathrm{int}}$ and t_2. A PMOS TOT adjusts the S_2-conversion-to-diode timing t_2 for the next period by providing PMOS TOT signal Φ_{TP}. Then, a P-driver generates Φ_P to control S_2. This FB_2 ensures safe charging and achieving high PCE.

Passively tracking t_Z: The passive ZCD operation tracks the timing when I_{S2} becomes zero t_Z. This passive tracking makes $I_{L2} = 0$ at the end-of-charging timing. At t_Z, the charging phase Φ_3 ends and immediately starts the resonant phase Φ_1 again. Since the next resonant phase starts just after the charging phase ends unlike conventional RCM R_X, there is no idle period between charging and resonant periods, which increases the PDL.

Fig. 6 shows the timing diagram of dual AMEC and passive ZCD operation. In the case of FB_1, when *VC2* is higher than *GND* at t_Z, FB_1 expedites t_1 in the next period by the delay unit, t_d (about 3.6 ns in this article). On the other hand, when *VC2* is lower than the *GND*, FB_1 delays t_1 in the next period by t_d. Thus, *VC2* stays around *GND* to extract all the energy of the resonant tank in a steady state. It should be noted that reducing the delay unit t_d has the benefit of increasing PCE while slowing down the tracking speed until it reaches the steady state. In the case of FB_2, when t_2 is earlier than $t_Z - t_{\mathrm{int}}$, FB_2 delays t_2 in the next period by t_d. On the other hand, when t_2 is later than $t_Z - t_{\mathrm{int}}$, FB_2 expedites t_2 in the next period by t_d. Thanks to the passive ZCD operation, t_Z can be extracted whenever $I_{L2} = 0$.

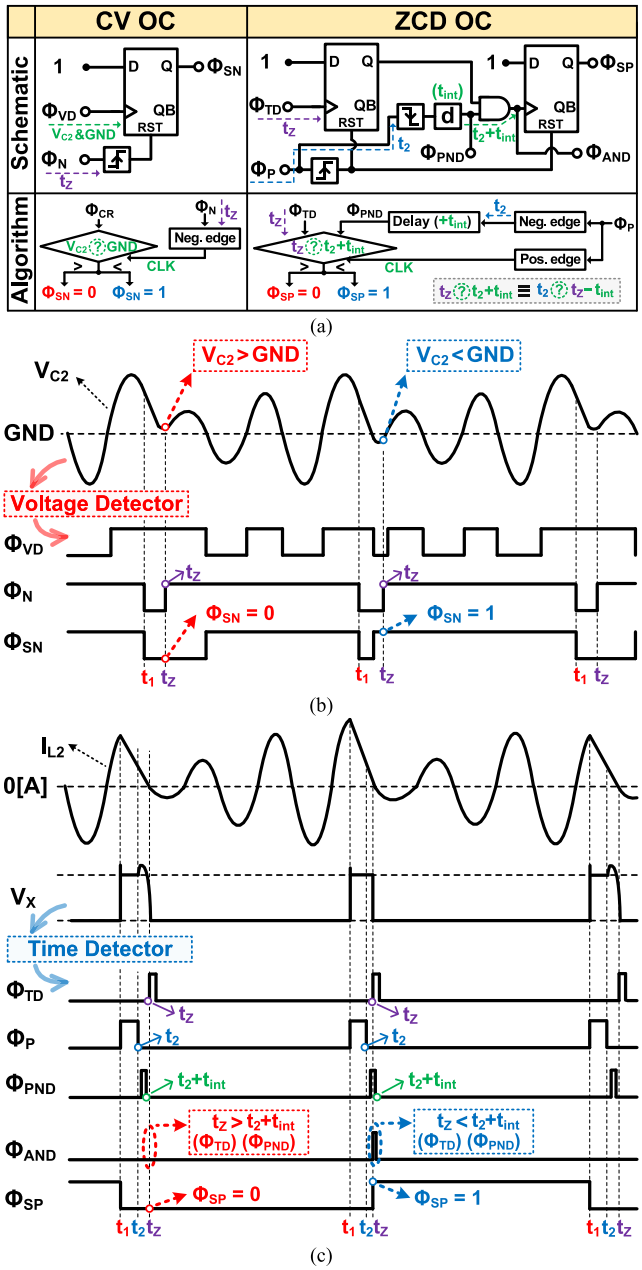


Fig. 7. (a) Schematic diagram and algorithm of the OC. Timing diagrams of the (b) CV OC and (c) ZCD OC.

B. Optimum Checkers (OC)

The OC oversees the previous state and determines whether the start timing of the next state should be delayed or expedited by providing Φ_{SN} and Φ_{SP}. The proposed dual AMEC includes two OC, which are CV OC and ZCD OC as shown in Fig. 7. The CV OC consists of D-flipflop (D-FF) and a positive edge

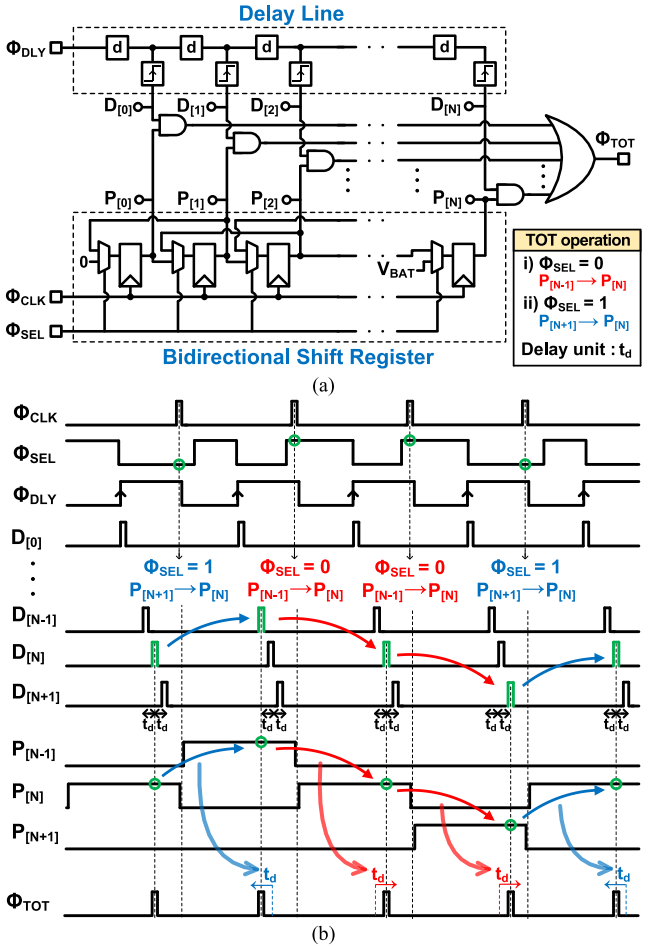


Fig. 8. (a) Schematic diagram and (b) timing diagram of the TOT.

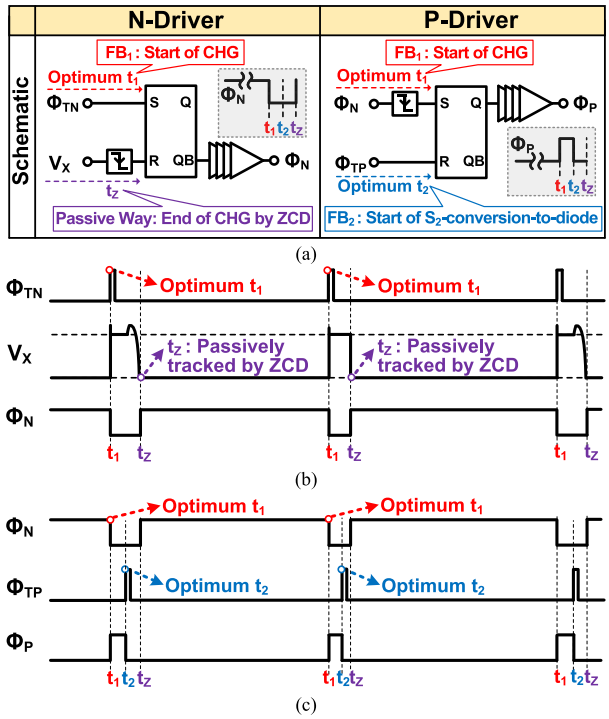


Fig. 9. (a) Schematic diagrams of the drivers. Timing diagrams of the (b) N-driver and (c) P-driver.

trigger. The voltage detector compares *VC2* and *GND* at t_Z and generates a digital signal $\Phi_{\rm VD}$. Also, Φ_N rises at t_Z, and positive edge triggered, acting as a reset signal of D-FF. When *VC2* is higher than *GND*, Φ_{SN} is 0 at t_Z, on the other hand, if *VC2* is lower than *GND*, Φ_{SN} is 1 at t_Z.

ZCD OC consists of two D-FFs, positive or negative edge trigger, AND-gate, and delay line with $t_{\rm int}$ delay unit. $\Phi_{\rm TD}$, the output of TD, rises at t_Z. Also, Φ_P falls at t_2 and is delayed by $t_{\rm int}$, generating $\Phi_{\rm PND}$. The AND-gate generates $\Phi_{\rm AND}$ from $\Phi_{\rm TD}$ and $\Phi_{\rm PND}$ by checking if there is an overlapped duration between t_Z and $t_2 + t_{\rm int}$. If t_Z is later than $t_2 + t_{\rm int}$, $\Phi_{\rm AND}$ is 0 at t_Z, on the other hand, if t_Z is earlier than $t_2 + t_{\rm int}$, $\Phi_{\rm AND}$ is 1 at t_Z. $\Phi_{\rm AND}$ acts as a clock signal of D-FF and generates Φ_{SP}. Note that comparing t_Z and $t_2 + t_{\rm int}$ is the same as comparing $t_Z - t_{\rm int}$ and t_2.

C. Tick-Tock Optimum Tracker

Fig. 8 shows the schematic and timing diagrams of the TOT, which delays or expedites the next state by t_d. The TOT consists of delay lines, bidirectional shift registers, and an OR-gate to sum the outputs of delay lines and shift registers. *D[n]* is a delay line output depending on Φ_{DLY}, while a delay unit has a delay of t_d. *P[n]* is a shift register output with a clock signal Φ_{CLK} and an input shift parameter Φ_{SEL}, which adjusts the *P[n]* array to transit to either left or right to select the optimal *D[n]*. Then, outputs of AND-gates from *D[n]* and *P[n]* pass through the OR-gate, resulting in $\Phi_{\rm TOT}$, which is the optimum delayed signal by t_d. For example, if Φ_{SEL} is 1, the *P[n]* array shifts to the left. Then, the next period of $\Phi_{\rm TOT}$ is expedited by t_d. On the other hand, if Φ_{SEL} is 0, the *P[n]* array shifts to the right, delaying by t_d in the next period of $\Phi_{\rm TOT}$.

The NMOS TOT receives Φ_{SN} as an input of Φ_{SEL} in TOT, which has the information whether V_{C2} is higher or lower than *GND*. Then, it outputs Φ_{TN}, the optimum delayed or expedited by t_d, to have $V_{C2} = 0$ at the end of charging. Thus, V_{C2} at the end of the charging mode stays close to *GND* as it moves up and down. In order to minimize the difference between V_{C2} and *GND* to achieve high PCE, t_d has to be decreased.

Likewise, the PMOS TOT receives Φ_{SP} as an input of Φ_{SEL} in TOT, which has the information whether t_2 is earlier or later than $t_Z - t_{\rm int}$. The output of the PMOS TOT Φ_{TP} is optimally delayed or expedited by t_d to achieve safe charging and high PCE. Thus, S_2-conversion-to-diode timing t_2 stays close to $t_Z - t_{\rm int}$ as it moves up and down. The small t_d is also preferred to minimize the difference between t_2 and $t_Z - t_{\rm int}$ for safe charging and high PCE.

D. Switch Drivers

Fig. 9 shows the N-driver and P-driver, which control the NMOS power switch S_1 and the PMOS power switch S_2, respectively. The N-driver consists of an SR-latch, a negative edge trigger, and multiple power buffers. Φ_{TN} rises at optimum t_1 by $\rm FB_1$ and V_X falls at t_Z, which is passively tracked by ZCD.

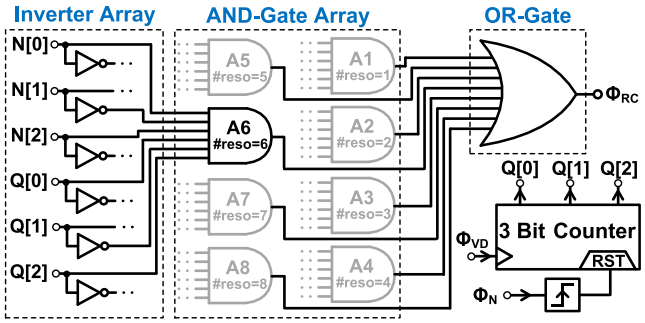


Fig. 10. Schematic of the RCS for operation with six resonant cycles.

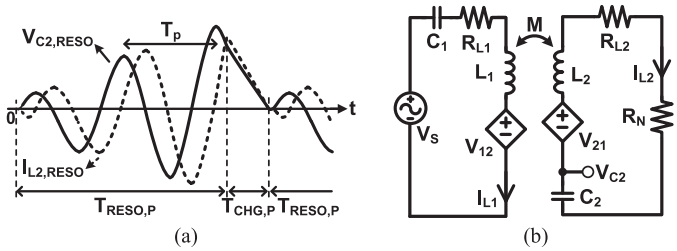


Fig. 11. (a) Conceptual waveforms of the proposed series-*LC* R_X and (b) equivalent models for the resonant mode.

Φ_{TN} and V_X act as SR-latch inputs and generate Φ_N falling at t_1 and rising at t_Z. Also, in the P-driver composed of the SR-latch and multiple power buffers, Φ_{TP} rises at optimum t_2 by FB_2 and Φ_N falls at t_1 by FB_1. Φ_{TP} and Φ_N act as SR-latch inputs and generate Φ_P rising at t_1 and falling at t_2.

E. Resonant Cycle Selector (RCS)

Fig. 10 shows the schematic diagram of RCS for the case of six resonance cycles. The RCS consists of a 3-b counter, inverter array, AND-gate array, and OR-gate. The 3-b counter divides Φ_{VD} with a reset signal as Φ_N and outputs *Q[0]* to *Q[2]*. External voltages, *N[0]* to *N[2]*, decide the number of resonant cycles. The RCS output signal Φ_{RC} becomes 1 as *N[0]* to *N[2]* are equal to *Q[0]* to *Q[2]*, respectively. For example, to determine six resonant cycles, $N[0] = 1$, $N[1] = 0$, and $N[2] = 1$ should be applied, then the AND-gate A_6, which receives inputs of *N[0]*, inverted *N[1]*, *N[2]*, *Q[0]*, inverted *Q[1]*, and *Q[2]*, produces a periodic signal proportional to six. Since only A_6 has an output of 1 out of 8 AND-gates, the OR-gate outputs only A_6 output, generating Φ_{RC}. However, Φ_N rises at t_Z, which is passively tracked by ZCD operation, and acts as a reset signal, leading the next resonant mode to start just after the charging mode ends. Thus, the idle period between charging and resonant periods is removed, enhancing the PDL.

The RCS, voltage detector, TD, and dual AMEC, which consists of OCs, TOTs, and switch drivers, are not limited to specific frequencies. However, the proposed system operation at higher frequencies requires more bias current for the high-speed voltage detector and a smaller time delay in TOT.

IV. Theoretical Analysis

A. Maximum Resonant Voltage in Resonant Mode

The proposed series-*LC* RCM R_X can receive resonant voltage V_{C2} higher than transistor breakdown voltage V_{BD} realizing near-field wirelessly-powered medical devices. To describe this, this section suggests a new indicator, which is the ratio of the maximum peak-to-peak resonant voltage amplitude over the transistor breakdown voltage ($= V_{C2,pp}/V_{BD}$), to quantify the capability of high resonant voltage in R_X.

Since the algorithm with passive ZCD operation immediately starts the next resonant period right after the charging period ends, which means $T_{IDLE,P} = 0$ as shown in Fig. 11(a), the operation of the proposed RCM R_X can be divided into two modes. First, in the resonant mode, which is shown as $0 < t < T_{RESO,P}$ with an equivalent model of Fig. 11(b), the energy in L_2C_2 tank resonates for multiple cycles. Second, in the charging mode, where $T_{RESO,P} < t < T_{RESO,P} + T_{CHG,P}$, the FB_1 senses the V_{C2} in previous end-of-charging timing and tracks the next optimum start-of-charging timing so that make $V_{C2} = 0$ at the end of charging. Also, the charging period ends when I_{L2} equals zero with passive ZCD operation, leading all the energy in L_2C_2 tank to transfer to the battery.

Fig. 11(b) shows the equivalent model for the resonant mode, in which the resonant period is T_p and the resonant frequency is $\omega = 2\pi/T_p$. The voltage source of T_X can be modeled as $V_S(t) = V_0 \cos(\omega t)$. The ON-resistance of S_1 is R_N. The equivalent-series-resistance of L_1 and L_2 are R_{L1} and R_{L2}, respectively. V_{12} and V_{21} are equal to $-j\omega MI_{L2}$ and $j\omega MI_{L1}$, respectively, where M is the mutual inductance between L_1 and L_2. The steady-state condition of V_{21} in Fig. 11(b) can be calculated as

$$V_{21} = \frac{j\omega M V_S}{R_{L1} + \frac{\omega^2 M^2}{R_{L2}+R_N}}. \tag{1}$$

$I_{L2}(t)$ in the resonant mode can be derived from

$$V_{21}\ (t) = \frac{1}{C_2}\int_0^t I_{L2}\,(t)\,dt + L_2\frac{dI_{L2}\,(t)}{dt} + (R_{L2}+R_N)I_{L2} \tag{2}$$

with Kirchhoff's voltage law. Considering the initial condition of $I_{L2}(0) = 0$ and $V_{C2}(0) = 0$. The solution of $I_{L2}(t)$ at the resonant mode $I_{L2,RESO}(t)$ can be written as

$$I_{L2,RESO}\ (t) = \frac{|V_{21}|}{R_{L2}+R_N}\left(1 - e^{-\alpha t}\right)\sin(wt) \tag{3}$$

where α is $(R_{L2} + R_N)/2L_2$ [37]. Also, $V_{C2}(t)$ of the resonant mode $V_{C2,RESO}(t)$ can be written as

$$\begin{aligned} V_{C2,RESO}\ (t) &= \frac{1}{C_2}\int_0^t I_{L2}\,(t)\,dt \\ &= \frac{1}{C_2}\frac{|V_{21}|}{R_{L2}+R_N} \\ &= \frac{\alpha\omega e^{-\alpha t}\sin(wt) + (\omega^2 e^{-\alpha t} - \omega^2 - \alpha^2)\cos(wt) + \alpha^2}{\omega^3 + \alpha^2\omega}. \end{aligned} \tag{4}$$

As plotted in Fig. 12, the maximum of V_{C2} until $t = T_{RESO}$, $V_{C2,RESO,MAX}(t)$, increases and reaches the saturated voltage

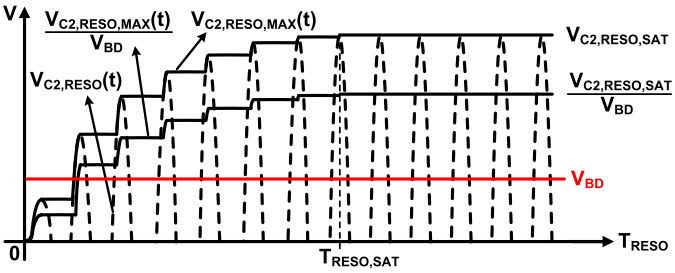


Fig. 12. Conceptual waveforms of the received V_{C2} and V_{C2}/V_{BD}.

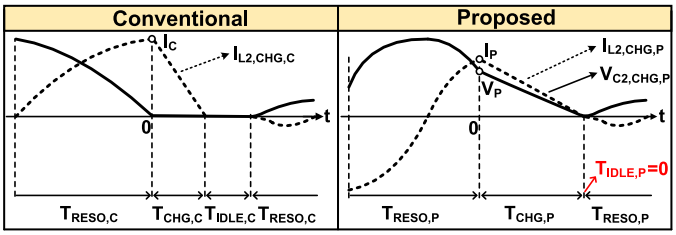


Fig. 13. Conceptual waveforms in the charging mode.

$V_{C2,\mathrm{RESO,SAT}}$ at $T_{\mathrm{RESO,SAT}}$. This $V_{C2,\mathrm{RESO,SAT}}$ can be written as

$$V_{C2,\mathrm{RESO,SAT}} = \frac{1}{C_2}\,\frac{|V_{21}|}{R_{L2}+R_N}\,\frac{\omega^2+2\alpha^2}{\omega^3+\alpha^2\omega}. \tag{5}$$

The suggested indicator, $V_{C2,\mathrm{pp}}/V_{\mathrm{BD}}$, for series-*LC* RCM $\mathrm{R_X}$ can be written as $V_{C2,\mathrm{RESO,MAX}}(t)/V_{\mathrm{BD}}$ for $T_{\mathrm{RESO}} < T_{\mathrm{RESO,SAT}}$ and $V_{C2,\mathrm{RESO,SAT}}/V_{\mathrm{BD}}$ for $T_{\mathrm{RESO}} > T_{\mathrm{RESO,SAT}}$. Unlike parallel-*LC* RCM $\mathrm{R_X}$ and VM $\mathrm{R_X}$, $V_{C2,\mathrm{RESO,SAT}}/V_{\mathrm{BD}}$ can be greater than 1 for series-*LC* RCM $\mathrm{R_X}$, meaning that the series-*LC* scheme can receive larger voltage than the parallel-*LC* scheme. A large resonant voltage V_{C2}, which is supremely above the transistor breakdown voltage V_{BD}, allows for greater input power, extending the wide input range.

B. Efficiency Comparison in Charging Mode

In the proposed series-*LC* RCM $\mathrm{R_X}$, the dual AMEC and passive ZCD operation charge the battery until I_{L2} and V_{C2} are equal to zero. On the other hand, conventional RCM $\mathrm{R_X}$ sends the energy to the battery when the resonant current peaks [34]. However, simultaneously charging the battery with L_2 and C_2 in the proposed RCM $\mathrm{R_X}$ has an advantage compared to charging the battery with only L_2 in conventional RCM $\mathrm{R_X}$ as shown in Fig. 13. This section compares the power losses including switching loss P_{SW} and conduction loss P_{COND} in the charging mode.

For a fair comparison, four assumptions for the conventional RCM $\mathrm{R_X}$ are needed. One is that the conventional RCM $\mathrm{R_X}$ has no residual energy at the end of charging, despite the absence of dual AMEC, and the second is that the conventional RCM $\mathrm{R_X}$ has a series-*LC* scheme. Third, energy stored in L_2C_2 tank at the start of charging, which is $t = 0$, for both conventional and proposed RCM $\mathrm{R_X}$ are the same. Finally, total period T_{TTL}, which is $T_{\mathrm{RESO}} + T_{\mathrm{CHG}} + T_{\mathrm{IDLE}}$, for conventional and proposed RCM $\mathrm{R_X}$ are $T_{\mathrm{TTL},C}$ and $T_{\mathrm{TTL},P}$, respectively, and are the same. Here, $T_{\mathrm{IDLE},P}$ in the proposed RCM $\mathrm{R_X}$ is zero while $T_{\mathrm{IDLE},C}$ in the conventional RCM $\mathrm{R_X}$ is not zero. In $T_{\mathrm{IDLE},C}$, the conventional RCM $\mathrm{R_X}$ remains the switching state of power switches open, and the next resonant period starts when $T_{\mathrm{CHG},C} + T_{\mathrm{IDLE},C}$ becomes $0.25T_p$ [34].

If the same sizes of the power switches are used for both conventional and proposed RCM $\mathrm{R_X}$, then $C_{G,\mathrm{NMOS}}$ and $C_{G,\mathrm{PMOS}}$, which are NMOS and PMOS gate capacitors, respectively, are the same. Thus, the switching energy loss when switching states changes is the same in both conventional and proposed RCM $\mathrm{R_X}$. As the transitions of switching state occur two times either from the resonant mode to the charging mode or from the charging mode to the resonant mode, the switching power loss P_{SW} can be written as

$$P_{\mathrm{SW},C} = P_{\mathrm{SW},P} = 2(C_{G,\mathrm{NMOS}} + C_{G,\mathrm{PMOS}})V_{\mathrm{BAT}}^2/T_{\mathrm{TTL}}. \tag{6}$$

Here, the switching power loss P_{SW} is independent of P_{IN}.

For the conventional RCM $\mathrm{R_X}$, the charging period starts as the I_{L2} peaks, and the linearized I_{L2} in the charging mode $I_{L2,\mathrm{CHG},C}(t)$ can be written as

$$I_{L2,\mathrm{CHG},C}(t) = I_C - \frac{I_C}{T_{\mathrm{CHG},C}}t \tag{7}$$

where I_C is the peak current of the charging period. Since energy stored in inductor L_2 transfers to the battery, the relationship is obtained as

$$\frac{1}{2}L_2I_C^2 = \frac{1}{2}\,I_CV_{\mathrm{BAT}}T_{\mathrm{CHG},C} \tag{8}$$

$$T_{\mathrm{CHG},C} = \frac{L_2I_C}{V_{\mathrm{BAT}}}\,. \tag{9}$$

The conduction loss of conventional RCM $\mathrm{R_X}$, $P_{\mathrm{COND},C}$, with associating (9) can be written as

$$\begin{aligned} P_{\mathrm{COND},C} &= \frac{1}{T_{\mathrm{TTL},C}}\int_0^{T_{\mathrm{CHG},C}} I_{L2,\mathrm{CHG},C}^2(t)\,dt\cdot R_P \\ &= \frac{1}{T_{\mathrm{TTL},C}}\,\frac{T_{\mathrm{CHG},C}I_C^2}{3}\cdot R_P \\ &= \frac{1}{T_{\mathrm{TTL},C}}\,\frac{L_2I_C^3}{3V_{\mathrm{BAT}}}\cdot R_P \end{aligned} \tag{10}$$

where the ON-resistance of $\mathrm{S_2}$ is R_P. Also, R_P is constant during the charging period for simple calculations.

For the proposed RCM $\mathrm{R_X}$, the charging period ends when the I_{L2} and V_{C2} become zero due to dual AMEC. The linearized I_{L2} in the charging mode, $I_{L2,\mathrm{CHG},P}(t)$ can be written as

$$I_{L2,\mathrm{CHG},P}(t) = I_P - \frac{I_P}{T_{\mathrm{CHG},P}}t \tag{11}$$

where I_P is the peak current of the charging period. V_{C2} in the charging mode $V_{C2,\mathrm{CHG},P}(t)$ can be derived as quadratic function and can be written as

$$V_{C2,\mathrm{CHG},P}(t) = V_P - \frac{1}{C_2}\int_0^t I_{L2}(t)\,dt$$

$$= V_P - \frac{1}{C_2}\left(I_P t - \frac{I_P t^2}{2T_{\mathrm{CHG},P}}\right) \tag{12}$$

where V_P is the peak voltage of the charging period. From the final condition of $V_{C2,\mathrm{CHG},P}(T_{\mathrm{CHG},P}) = 0$, (12) can be rewritten as

$$T_{\mathrm{CHG},P} = \frac{2C_2V_P}{I_P}. \tag{13}$$

Since energy stored in inductor L_2 and capacitor C_2 transfers to the battery, the relationship is obtained as

$$\frac{1}{2}C_2V_P^2 + \frac{1}{2}L_2I_P^2 = \frac{1}{2}I_PV_{\mathrm{BAT}}T_{\mathrm{CHG},P}. \tag{14}$$

From (13) and (14), V_P and I_P can be derived as

$$V_P = \frac{2T_{\mathrm{CHG},P}^2V_{\mathrm{BAT}}}{T_{\mathrm{CHG},P}^2 + 4L_2C_2}, \quad I_P = \frac{4C_2T_{\mathrm{CHG},P}V_{BAT}}{T_{\mathrm{CHG},P}^2 + 4L_2C_2}. \tag{15}$$

The conduction loss of proposed RCM $\mathrm{R_X}$, $P_{\mathrm{COND},P}$, with associating (13) can be written as

$$\begin{aligned} P_{\mathrm{COND},P} &= \frac{1}{T_{\mathrm{TTL},P}}\int_0^{T_{\mathrm{CHG},P}} I_{L2,\mathrm{CHG},P}^2(t)\,dt \cdot R_P \\ &= \frac{1}{T_{\mathrm{TTL},P}}\frac{T_{\mathrm{CHG},P}I_P^2}{3}\cdot R_P \\ &= \frac{1}{T_{\mathrm{TTL},P}}\frac{2C_2V_PI_P}{3}\cdot R_P. \end{aligned} \tag{16}$$

As mentioned in assumption, L_2C_2 tank energy at the start of charging, which is $t = 0$, for both conventional and proposed RCM $\mathrm{R_X}$ is the same, and the relationship can be written as

$$\frac{1}{2}C_2V_P^2 + \frac{1}{2}L_2I_P^2 = \frac{1}{2}L_2I_C^2. \tag{17}$$

From (8) and (15), (17) can be rewritten as

$$\frac{8C_2L_2}{T_{\mathrm{CHG},P}^2 + 4C_2L_2}T_{\mathrm{CHG},P}^2 = T_{\mathrm{CHG},C}^2. \tag{18}$$

From (9) and (16), $P_{\mathrm{COND},C}/P_{\mathrm{COND},P}$ can be written as

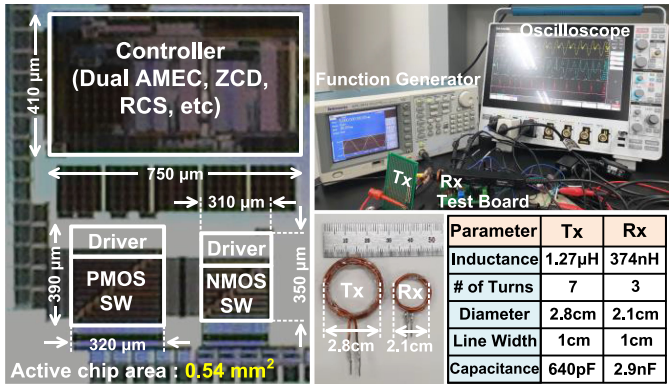
$$\frac{P_{\mathrm{COND},C}}{P_{\mathrm{COND},P}} = \frac{\frac{L_2I_C^3}{V_{\mathrm{BAT}}}}{2C_2V_PI_P}. \tag{19}$$

From (8), (15), and (18), (19) can be rewritten as

$$\frac{P_{\mathrm{COND},C}}{P_{\mathrm{COND},P}} = \sqrt{\frac{2T_{\mathrm{CHG},P}^2}{L_2C_2} + 8}. \tag{20}$$

Since $2T^2{}_{\mathrm{CHG},P}/L_2C_2 + 8 > 1$, so $P_{\mathrm{COND},C}/P_{\mathrm{COND},P} > 1$, which means that the proposed RCM $\mathrm{R_X}$ has lower conduction power loss in the charging mode than conventional RCM $\mathrm{R_X}$.

Since $P_{\mathrm{SW},C} = P_{\mathrm{SW},P}$ and $P_{\mathrm{COND},C} > P_{\mathrm{COND},P}$, the power delivered to the battery is higher for the proposed RCM $\mathrm{R_X}$ with same energy in L_2C_2 tank at the start of charging. Moreover, these result is extracted when the residual energy at the end of the charging mode is zero for the conventional RCM $\mathrm{R_X}$ according to the assumption. As considering the residual energy of the conventional RCM $\mathrm{R_X}$ in the calculation, $P_{\mathrm{COND},C}/P_{\mathrm{COND},P}$ will be greater than (20). Therefore, the proposed series-*LC* RCM $\mathrm{R_X}$ with dual AMEC is theoretically verified as an efficient WPT solution for IMDs.



Parameter	Tx	Rx
Inductance	1.27μH	374nH
# of Turns	7	3
Diameter	2.8cm	2.1cm
Line Width	1cm	1cm
Capacitance	640pF	2.9nF

Fig. 14. Chip photograph with floorplan and test setup with coil parameters.

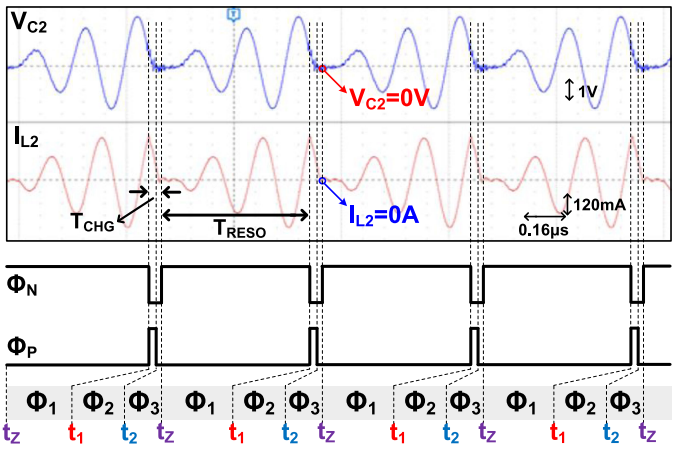


Fig. 15. Measured waveforms of V_{C2} and I_{L2} showing nonresidual energy at the end of the charging mode.

V. Measurement Results

The proposed series-*LC* RCM $\mathrm{R_X}$ with dual AMEC using 180-nm 1P6M standard CMOS process occupies an active chip area of 0.54 $\mathrm{mm^2}$ while utilizing only 1.8-V transistors. Fig. 14 shows chip micrograph and proof-of-concept series-*LC* RCM $\mathrm{R_X}$ chip measurement setup. Also, the parameters of spiral $\mathrm{T_X}$ coil, L_1, and $\mathrm{R_X}$ coils, L_2, are presented and were designed for WPT at the resonant frequency of 5 MHz. In $\mathrm{T_X}$ stage, the function generator (AFG3011) drives L_1 with 40 $\mathrm{V_{pp}}$ and the series-L_1C_1 resonant stage amplifies the magnetic flux between two coils. In $\mathrm{R_X}$ stage, series-L_2C_2 tank connected to the proposed chip achieves V_{C2}, larger than transistor breakdown voltage V_{BD}. The dual AMEC also achieves nonresidual energy at the end of the charging mode regardless of resonant cycles N and coil distance d.

Fig. 15 shows the measured waveforms with $N = 3$ focusing on the end-of-charging timing when $V_{C2} = 0$ and $I_{L2} = 0$ by the proposed dual AMEC and passive ZCD operation. The two digital feedback of dual AMEC adaptively track the optimum

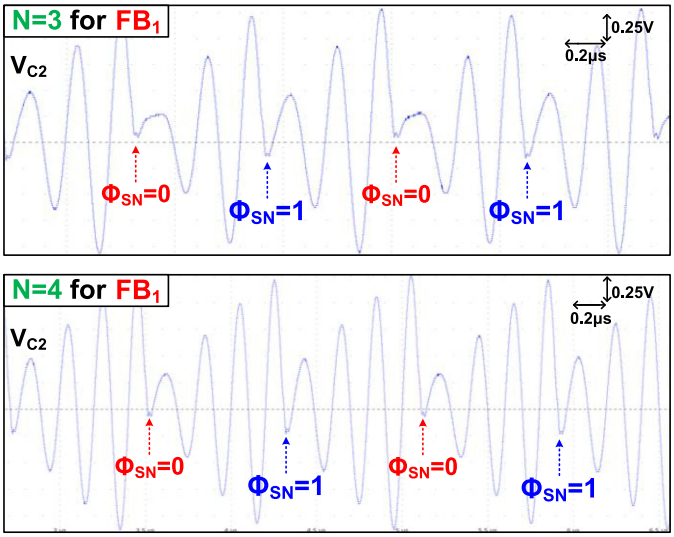


Fig. 16. Measured waveforms of V_{C2} when NMOS TOT tracks $V_{C2} = 0$.

start of charging timing t_1 and optimum S_2-conversion-to-diode timing t_2. Also, passive ZCD operation passively tracks the end-of-charging timing t_Z. With these tracked timings, the NMOS and PMOS control signals, which are Φ_N and Φ_P, respectively, adaptively determine the operation states of power transistors. Finally, the nonresidual energy of L_2C_2 tank at the end-of-charging timing will lead to a high PCE.

Measured waveforms of V_{C2} in Fig. 16 show that dual AMEC tracks the optimum points for $V_{C2} = 0$ by feedback 1 with resonant cycles of 3 and 4. When V_{C2} is higher than *GND*, Φ_{SN} becomes 0. Then, the start time of the next charging period will be delayed by 3.6 ns. When V_{C2} is lower than *GND*, the next charging period will start early by 3.6 ns. Thus, the charging period can adaptively end when V_{C2} is close to *GND*. It is noted that the smaller delay unit than 3.6 ns can further make V_{C2} at the end of the charging mode closer to *GND,* achieving higher PCE.

Fig. 17 shows the maximum peak-to-peak resonant voltage amplitudes $V_{C2,\mathrm{pp}}$, which are 12.32 V and 8.72 V for resonant cycles of 2 and 3, respectively, while the battery voltage V_{BAT} is set as same as V_{BD}, which is 1.8 V. The case of $N = 2$ was measured at a coil distance of 10 mm while the case of $N = 3$ was measured at a larger coil distance of 23 mm, where the R_X input power decreases and the optimum $N = 3$ can be used. The ratios of the maximum peak-to-peak resonant voltage over the output voltage ($= V_{C2,\mathrm{pp}}/V_{\mathrm{BD}}$) are 6.84 and 4.84 for resonant cycles of 2 and 3, respectively, enabling much higher resonant voltages than the supply or transistor breakdown voltages. Considering that $V_{C2,\mathrm{pp}}/V_{\mathrm{BD}}$ is lower than 1 in VM and parallel-*LC* RCM structures, the series-*LC* RCM scheme can be robust to higher voltage stress. In other words, while the voltage of off-chip components L_2 and C_2 reach over V_{BD} in the series-*LC* RCM, the voltage stress of on-chip transistors stays under V_{BD}, ensuring safety concerns.

Fig. 18 shows the measured PCE and PTE as a function of coil distance *d*, peak-to-peak resonant voltage amplitude $V_{C2,\mathrm{pp}}$, and R_X input power P_{RX} while the T_X voltage source V_S drives L_1

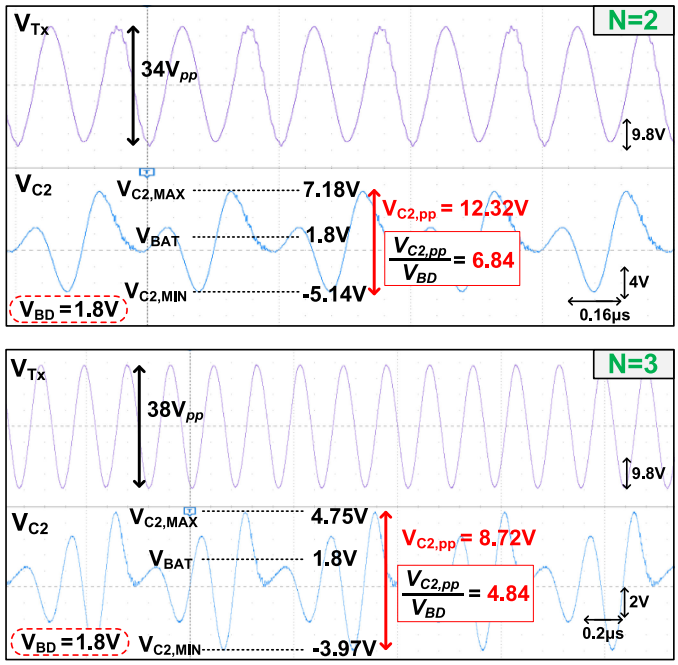


Fig. 17. Measured waveforms of the maximum V_{C2} when $V_{\mathrm{BD}} = 1.8$ V.

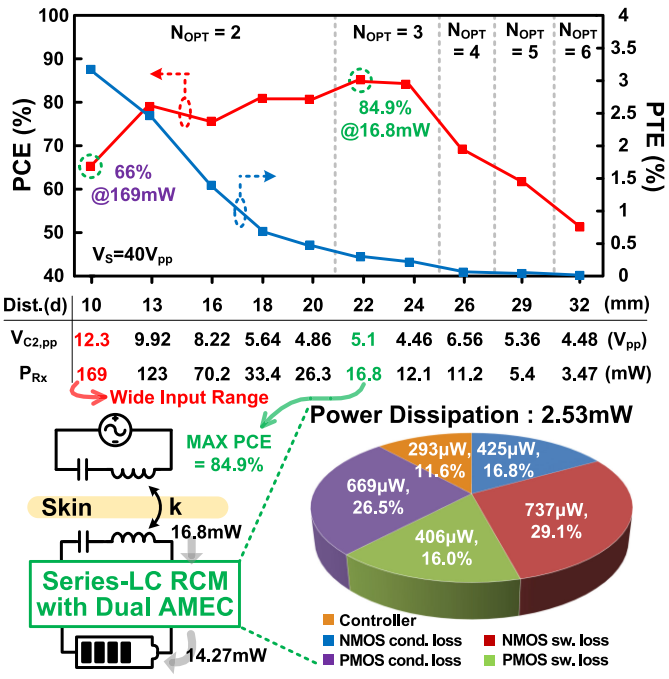


Fig. 18. Measured PCE and PTE over coil distance along with power loss breakdown at the input power of 16.8 mW.

with 40 V_{pp}. Each efficiency point was measured with optimum resonant cycles. At the coil distance of 10 mm, the proposed R_X achieves the maximum resonant amplitude of 12.32 V_{pp} and PTE of 3.27% for $V_{\mathrm{BAT}} = 1.8$ V at $P_{\mathrm{RX}} = 169$ mW. The measured PTE was limited to around 3.27% at a 10 mm distance, and we estimated that suboptimal coils, e.g., with lower quality factors, may decrease the coil link efficiency ($= P_{\mathrm{RX}}/P_{\mathrm{TX}}$) and

TABLE I
PERFORMANCE COMPARISON

	TCAS1 2020 [16]	JSSC 2019 [22]	JSSC 2017 [20]	TBCAS 2019 [32]	JSSC 2020 [30]	JSSC 2019 [31]	This Work
Rx Structure	VM	VM	VM	RCM/Boost Conv.	RVM	Parallel-LC RCM	**Series-LC RCM**
Application	WPT	WPT	WPT	WPT	Battery Charger	WPT	**Battery Charger**
Process Tech. [μm]	0.18	0.065	0.18	0.35	0.18	0.35	**0.18**
Resonant Freq. [MHz]	40.68	13.56	144	1	13.56	1	**5**
Robust to Voltage Stress	No	No	No	No	No	No	**Yes**
$V_{IN,MAX}$ / V_{BD} @1.8V	< 1	< 1	< 1	< 1	1.7 (3Vpp/1.8V)	< 1	**6.84 (12.32Vpp/1.8V)**
Input Range	N/A ~ 70mW	N/A	N/A	N/A ~ 45mW	1mW ~ 48mW	10μW ~ 24mW	**3.47mW ~ 169mW**
Max. Efficiency Tracker (Tracking poins/ #Comp.)	No	No	No	No	Yes (1 / 1)	No	**Yes (2 / 1)**
Residual power in Rx	Yes	Yes	Yes	Yes, but recycles	Yes	Yes, but recycles	**No**
Period between Chg&Reso	N/A	N/A	N/A	N/A	0	N/A	**0**
Max. PCE (@ Rx P_{IN})	80.9% (@ 70mW)	75.4% (@ 12mW)	66.5% (@ 150μW)	75.3% (@ 4.7mW)	67.8% (@ 11mW)	75% (@ 18mW)	**84.9% (@ 16.8mW)**
Max. PTE (@ Rx P_{IN}, d=1cm)	N/A	N/A	2.04% (@ 225μW)	N/A	N/A	N/A	**3.27% (@ 169mW)**
Max. PTD [mW/cm^2] (@ d)* (Rx coil area [cm^2], PDL)	N/A (N/A, 56.6mW)	2.42 (@ N/A) (3.8, 9.2mW)	8.1 (@ 1cm) (0.0864, 0.7mW)	11.8 (@ N/A) (3.8, 45mW)	40.2 (@ 1cm) (0.49, 19.7mW)	N/A (N/A, 18mW)	**32.4 (@ 1cm) (3.46, 112mW)**
# Off-Chip Cap.	1	1	2	3	2(+ Off-Chip Ind.)	3	**1**
Inductance of Rx coil	170nH	N/A	23.7nH	4.5μH	137nH	13μH	**350nH**
Active Area [mm^2]	1.58	5.11	0.078	1.35	1.25	2.4	**0.54**

[a] PTD (Power Transfer Density) = PDL/R_X coil area.

PTE ($= P_L/P_{TX}$). At a distance of 10 mm, the 6.84× higher resonant voltage amplitude than the battery voltage ensures a wide input range over breakdown voltages in the proposed series-*LC* RCM R_X. In addition, the maximum PDL was 112 mW at a coil distance of 10 mm, and the maximum power transfer density was 32.2 mW/cm^2 at the Rx coil area of 3.46 cm^2. The maximum PCE was 84.9% at an input power of 16.8 mW thanks to the dual AMEC and passive ZCD operation, as the power loss break down was analyzed based on simulations at this point. As shown in the pie chart, the controller circuits, including dual AMEC, voltage detector, TD, RCS, ESD protection, and other logics, consume the power of 293 μW (11.6% of total power dissipation and 1.74% of total input power), which should be further optimized to maximize the PCE. Among total power dissipation of 2.53 mW, the NMOS switch (S_1) has the conduction and switching losses of 425 μW (16.8%) and 737 μW (29.1%), respectively, and the PMOS switch (S_2) has the conduction and switching losses of 669 μW (26.5%) and 406 μW (16%), respectively. It can be noted that the maximum PCE of 84.9% with P_{RX} of 16.8 mW can be also obtained at a smaller coil distance, e.g., 10 mm, by decreasing V_{TX}, which can optimize both PTE and PCE at the same condition.

For a fair comparison, Table I summarizes the key performance of the proposed series-*LC* RCM R_X with dual AMEC compared to the state-of-the-art wireless power R_X designed for IMDs. The series-*LC* scheme ensures the robust RCM operation against on-chip transistor voltage stress, which can charge the battery to 1.8 V with higher resonant voltages up to 12.32 V_{pp} while the maximum voltage stress of on-chip power switches stays under transistor breakdown voltage, 1.8 V. Also, this series-*LC* scheme for R_X stage allows maximum input power to reach 169 mW, expanding the input power range and enabling near-field WPT. Moreover, it achieves a competitive peak efficiency of 84.9% due to dual AMEC with two digital feedback. It should be noted that the proposed system still needs the optimized coils to further improve the coil link efficiency and PTE.

VI. CONCLUSION

The proposed series-*LC* RCM R_X can operate with 6.84× higher resonant voltage amplitude than transistor breakdown voltages, enabling robust near-field WPT against voltage stress. The RCM R_X also achieves highest input power of 169 mW compared to the previous publications, extending input power and PDL ranges. In addition, the dual AMEC and passive ZCD operation lead to a complete energy transfer from L_2C_2 tank to the battery, resulting in high PCE. Moreover, the proposed algorithm with passive ZCD operation eliminates the idle period between charging and resonant periods, improving PDL. Therefore, the proposed series-*LC* RCM R_X with dual AMEC can provide power-efficient and overvoltage-tolerant solutions for near-field WPT applications.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), South Korea.

REFERENCES

[1] R. Chen, A. Canales, and P. Anikeeva, "Neural recording and modulation technologies," *Nature Rev. Mater.*, vol. 2, no. 16093, pp. 1–16, Jan. 2017.
[2] H. Kassiri *et al.*, "Rail-to-rail-input dual-radio 64-channel closed-loop neurostimulator," *IEEE J. Solid-State Circuits,* vol. 52, no. 11, pp. 2793–2810, Nov. 2017.
[3] S.-H. Wang *et al.*, "Design of a bone-guided cochlear implant microsystem with monopolar biphasic multiple stimulations and evoked compound action potential acquisition and its in vivo verification," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 3062–3076, Oct. 2021.
[4] S.-Y. Lee *et al.*, "A programmable wireless EEG monitoring SoC with open/closed-loop optogenetic and electrical stimulation for epilepsy control," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2019, pp. 372–373.
[5] C. Lee, B. Johnson, and A. Molnar, "An on-chip 72×60 angle-sensitive single photon image sensor array for lens-less time-resolved 3-D fluorescence lifetime imaging," in *Proc. Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2014, pp. 1–2.
[6] H.-M. Lee, K. Y. Kwon, W. Li, and M. Ghovanloo, "A power-efficient switched-capacitor stimulating system for electrical/optical deep brain stimulation," *IEEE J. Solid-State Circuits*, vol. 50, no. 1, pp. 360–374, Jan. 2015.

[7] S. Moazeni *et al.*, "A mechanically flexible implantable neural interface for computational imaging and optogenetic stimulation over $5.4\times5.4\text{mm}^2$ FoV," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2018, pp. 288–289.

[8] Y. Jia *et al.*, "A trimodal wireless implantable neural interface system-on-chip," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1207–1217, Dec. 2020.

[9] J. Charthad *et al.*, "A mm-sized wireless implantable device for electrical stimulation of peripheral nerves," *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 2, pp. 257–270, Apr. 2018.

[10] X. Li, C.-Y. Tsui, and W.-H. Ki, "A 13.56 MHz wireless power transfer system with reconfigurable resonant regulating rectifier and wireless power control for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 978–989, Apr. 2015.

[11] Y. Lu, X. Li, W.-H. Ki, C.-Y. Tsui, and C. P. Yue, "A 13.56 MHz fully integrated 1X/2X active rectifier with compensated bias current for inductively powered devices," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 66–67.

[12] K.-G. Moh *et al.*, "A fully integrated 6W wireless power receiver operating at 6.78 MHz with magnetic resonance coupling," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2015, pp. 230–231.

[13] H.-M. Lee and M. Ghovanloo, "An adaptive reconfigurable active voltage doubler/rectifier for extended-range inductive power transmission," *IEEE Trans. Circuits Syst. II,* vol. 60, no. 10, pp. 707–711, Oct. 2013.

[14] H.-M. Lee and M. Ghovanloo, "An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1749–1760, Aug. 2011.

[15] L. Hu, L. Cheng, Y. Yao, T. S. Yim, W.-H. Ki, and C.-Y. Tsui, "A 40.68 MHz active rectifier with hybrid delay compensation scheme," in *Proc. IEEE Asia Pacific Conf. Circuits Syst.*, 2018, pp. 501–504.

[16] L. Cheng, X. Ge, L. Hu, Y. Yao, W.-H. Ki, and C.-Y. Tsui, "A 40.68-MHz active rectifier with hybrid adaptive on/off delay-compensation scheme for biomedical implantable devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 2, pp. 516–525, Feb. 2020.

[17] X. Li, X. Meng, C.-Y. Tsui, and W.-H. Ki, "Reconfigurable resonant regulating rectifier with primary equalization for extended coupling- and loading-range in bio-implant wireless power transfer," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 6, pp. 875–884, Dec. 2015.

[18] D. Ahn, S. Kim, J. Moon, and I.-K. Cho, "Wireless power transfer with automatic feedback control of load resistance transformation," *IEEE Trans. Power Electron.*, vol. 31, no. 11, pp. 7876–7886, Nov. 2016.

[19] Y.-S. Hwang, C.-C. Lei, Y.-W. Yang, J.-J. Chen, and C.-C. Yu, "A 13.56-MHz low-voltage and low-control-loss RF-DC rectifier utilizing a reducing reverse loss technique," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6544–6554, Dec. 2014.

[20] C. Kim, S. Ha, J. Park, A. Akinin, P. P. Mercier, and G. Cauwenberghs, "A 144-MHz fully integrated resonant regulating rectifier with hybrid pulse modulation for mm-sized implants," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3043–3055, Nov. 2017.

[21] M. Kiani, B. Lee, P. Yeon, and M. Ghovanloo, "A Q-modulation technique for efficient inductive power transmission," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2839–2848, Dec. 2015.

[22] D. Ye, Y. Wang, Y. Xiang, L. Lyu, H. Min, and C.-J. R. Shi, "A wireless power and data transfer receiver achieving 75.4% effective power conversion efficiency and supporting 0.1% modulation depth for ASK demodulation," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1386–1400, May 2020.

[23] F. Mao, Y. Lu, and R. P. Martins, "A reconfigurable cross-connected wireless-power transceiver for bidirectional device-to-device wireless charging," *IEEE J. Solid-State Circuits*, vol. 54, no. 9, pp. 2579–2589, Sep. 2019.

[24] C. Huang, T. Kawajiri, and H. Ishikuro, "A 13.56 MHz wireless power transfer system with enhanced load-transient response and efficiency by fully integrated wireless constant-idle-time control for biomedical implants," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 538–551, Feb. 2018.

[25] S. Roy, A. N. M. W. Azad, S. Baidya, and F. Khan, "A comprehensive review on rectifiers, linear regulators, and switched-mode power processing techniques for biomedical sensors and implants utilizing in-body energy harvesting and external power delivery," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12721–12745, Nov. 2021.

[26] D. Newell and M. Duffy, "Review of power conversion and energy management for low-power, low-voltage energy harvesting powered wireless sensors," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9794–9805, Oct. 2019.

[27] Y. Lu, M. Huang, L. Cheng, W. Ki, S.-P. U, and R. P. Martins, "A dual output wireless power transfer system with active rectifier and three-level operation," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 927–930, Feb. 2017.

[28] J. Lim, B. Lee, and M. Ghovanloo, "A multiphase resonance-based boosting rectifier with dual outputs for wireless power transmission," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2680–2689, Mar. 2020.

[29] M. Choi, T. Jang, J. Jeong, S. Jeong, D. Blaauw, and D. Sylvester, "A current-mode wireless power receiver with -32 dBm sensitivity for implantable systems," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 2880–2892, Dec. 2016.

[30] S.-U. Shin, M. Choi, S. Jung, H.-M. Lee, and G.-H. Cho, "A time-interleaved resonant voltage mode wireless power receiver with delay-based tracking loops for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 55, no. 5, pp. 1374–1385, May 2020.

[31] H. S. Gougheri and M. Kiani, "An inductive voltage-/current-mode integrated power management with seamless mode transition and energy recycling," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 874–884, Mar. 2019.

[32] H. S. Gougheri, P. Graybill, and M. Kiani, "A dual-output reconfigurable shared-inductor boost-converter/current-mode inductive power management ASIC with 750% extended output-power range, adaptive switching control, and voltage-power regulation," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 5, pp. 1207–1217, Oct. 2019.

[33] H. S. Gougheri and M. Kiani, "Self-regulated reconfigurable voltage/current-mode inductive power management," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3056–3070, Nov. 2017.

[34] H. S. Gougheri and M. Kiani, "Current-based resonant power delivery with multi-cycle switching for extended-range inductive power transmission," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1543–1552, Sep. 2016.

[35] K.-S. Yoon, S.-H. Lee, I.-K. Cho, H.-J. Lee, and G.-H. Cho, "Dual receiver coils wireless power transfer system with interleaving switching," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 10016–10020, Dec. 2018.

[36] S.-U. Shin, S.-W. Hong, H.-M. Lee, and G.-H. Cho, "High-efficiency hybrid dual-path step-up DC–DC converter with continuous output-current delivery for low output voltage ripple," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 6025–6038, Jun. 2020.

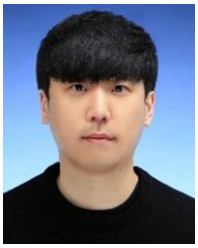
[37] B. Lee, P. Yeon, and M. Ghovanloo, "A multicycle q-modulation for dynamic optimization of inductive links," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5091–5100, Aug. 2016.

Hyun-Su Lee (Student Member, IEEE) received the B.S. and M.S. degrees in electrical engineering in 2018 and 2021, respectively, from Korea University, Seoul, South Korea, where he is currently working toward the Ph.D. degree.

His current research interests include the designs of biomedical integrated circuits such as wireless power transfer, data telemetry, and ultrasound systems.

Jisan Ahn (Student Member, IEEE) received the B.S. degree in energy systems engineering from Chung-Ang University, Seoul, South Korea, in 2021. He is currently working toward the M.S. degree in semiconductor system engineering with Korea University, Seoul.

His research interests include analog/mixed-signal integrated circuits and wireless power/data transfer circuits for biomedical implantable systems.



Kyeongho Eom (Student Member, IEEE) received the B.S. degree (*magna cum laude*) in electrical engineering in 2020 from Korea University, Seoul, South Korea, where he is currently working toward the joint M.S./Ph.D. degree.

His current research interests include analog circuit design for biomedical applications, especially neural stimulation ICs.

Woojoong Jung (Student Member, IEEE) received the B.S. degree from the School of Electrical and Electronics Engineering, Chung-Ang University, Seoul, South Korea, in 2018. He is currently working toward the M.S. and Ph.D. joint degree in electrical engineering from Korea University, Seoul.

His current research interests include dc–dc switching converter and power management ICs.

Seung-Ju Lee (Student Member, IEEE) received the B.S. degree in display engineering from Dankook University, Cheonan, South Korea, in 2021. He is currently working toward the integrated master's and Ph.D. degrees with the Department of Electrical Engineering, Ulsan National Institute of Science and Technology, Ulsan, South Korea.

His research interests include analog-integrated circuit designs such as power management IC, linear regulators, switched capacitors/inductive converters, and hybrid converter topology.

Yeon-Woo Jung (Student Member, IEEE) received the B.S. degree in display engineering from Dankook University, Cheonan, South Korea, in 2021. She is currently working toward the M.S. degree with the Department of Electrical Engineering, Ulsan National Institute of Science and Technology, Ulsan, South Korea.

Her current research interests include the design of analog-integrated circuits such as power management IC and energy harvesting interface circuits.

Se-Un Shin (Member, IEEE) received the B.S. degree in electronics engineering from Kyungpook National University, Daegu, South Korea, in 2013, and the integrated M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2018.

From 2018 to 2019, he was with the University of Michigan, Ann Arbor, MI, USA, where he was involved in the development of low-power analog circuit design and automation as a Postdoctoral Associate. From 2019 to 2020, he was a Faculty with the School of Electronics and Electrical Engineering, Dankook University, Cheonan, South Korea. Since 2021, he has been with the Department of Electrical Engineering, Ulsan National Institute of Science and Technology, Ulsan, South Korea, where he is currently an Assistant Professor. His current research interests include analog-integrated circuit design and power management IC design, energy harvesting, battery charger, wireless power transfer systems, switched capacitor/inductive converters, and hybrid converter topology.

Hyung-Min Lee (Member, IEEE) received the B.S. degree (*summa cum laude*) in electrical engineering from Korea University, Seoul, South Korea, in 2006, the M.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology, Daejeon, South Korea, in 2008, and the Ph.D. degree in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2014.

From 2014 to 2015, he was with the Massachusetts Institute of Technology as a Postdoctoral Researcher. From 2015 to 2017, he was with the IBM T. J. Watson Research Center as a Research Staff Member. In 2017, he joined the School of Electrical Engineering, Korea University, where he is currently an Associate Professor. His research area includes analog/mixed-signal IC and microsystem design for biomedical, sensor, power management, and IoT applications.

Prof. Lee was a recipient of the Silver Prizes in the 16th and 18th Human-Tech Thesis Prize Contest from Samsung Electronics, South Korea, in 2010 and 2012, respectively, and the Commendation Award in the 4th Outstanding Student Research Award from TSMC, Taiwan, in 2010.