A New Fault-Tolerant Multilevel Inverter Structure With Reduced Device Count and Low Total Standing Voltage

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***Abstract*—A new fault-tolerant (FT) multilevel inverter (MLI) structure that can tolerate the faults on the switches and sources is introduced in this article. The presence of redundant states in the proposed structure ensures the FT capability, which is an important requirement for emergency loads. Initially, the operation of the proposed FTMLI for fault-free and different fault conditions under symmetric and asymmetric source configurations is discussed. Furthermore, this article explores the ability of the proposed topology operating at different voltage levels in positive and negative half cycles of the output voltage to improve the reliability of the system. For this case, the modified pulsewidth modulation control strategy ensuring minimized lower order harmonics and zero dc offset is presented. The feasibility of the proposed topology is verified through simulation and experimental studies. Lower total standing voltage, reduced switch count, higher efficiency, and improved reliability are the key features of the proposed topology. A comprehensive evaluation and comparative study are performed to evaluate the performance of the proposed MLI over other structures.**

***Index Terms*—Fault-tolerant topology, multilevel inverter (MLI), pulsewidth modulation (PWM), total standing voltage (TSV).**

I. Introduction

THE adverse impact of electromagnetic interference on telecommunication systems, biomedical equipment, remote military secured systems, and ship propulsion systems is huge. For uninterrupted power supply in these applications, the battery-fed inverters with higher voltage levels at the output are often preferred. In addition, the inverters with higher output voltage levels are used in ground power units of electric aircraft to increase carrier ratio [1] and single-phase grid-connected systems [2]. Most of the converters used in the above applications have the power rating of less than 10 kW. Furthermore, the inclusion of fault tolerance to the inverters in the critical applications mentioned above avoids expensive shutdown. In addition, these multilevel inverters (MLI) are widely used in motor drives [3], [4], power quality enhancement devices, high-voltage dc transmission systems [5], and electrical vehicles [6]. Higher device count, capacitor voltage unbalancing, and lack of reliability are the main limitations of the well-established classical MLIs [7]. Several reduced switch count MLI topologies are introduced in the literature to address the above issues. In [8], a new configuration of symmetrical MLI topology with fewer switches is presented; nonprovision of asymmetric dc source configurations and high voltage stress across the converter switches are the main drawbacks of topology. A novel MLI structure with submultilevel units [9] generates higher voltage levels in both symmetric and asymmetric modes at the cost of increased switch count and higher total standing voltage (TSV). The topologies presented in [10]–[13] generate higher voltage levels with fewer components. Yet, these topologies require an additional H-bridge circuit for polarity reversal, which leads to higher TSV. On the other hand, the topologies [14]–[16] produce positive and negative voltage levels without using any H-bridge circuit. An asymmetric MLI [14] obtained from the back-to-back connection of two T-type structures creates more voltage levels at the output, but this topology has the drawback of higher TSV. A nine-level hybrid MLI resulting from the cascaded connection of a three-level active neutral point clamped (3L-ANPC) unit and flying capacitor H-bridge with low TSV is presented in [15]. The new switched capacitor MLI [16], with T-type and cross-connected units, exhibits the high-quality output waveform with low voltage stress on the switches, but it requires a mixture of unidirectional and bidirectional semiconductor power switches making the system bulky.

The event of fault occurrence in a switch or source for the above topologies leads to complete system failure and these unexpected failures cause an increased levelized cost [17]. In this scenario, the most cost-effective solution is to increase the reliability of the inverter by incorporating fault tolerance. Many circuit-topologies consisting of fault-tolerant (FT) features are reported in the literature; CHBMLI topologies presented in [18]–[20] have FT capability at the cost of a higher number of devices. Besides, the switches in topology [20] have to withstand more voltage during post-fault reconfiguration. A single-phase FTMLI topology [21] derived from the combination of a 3L-ANPC and a two-level half-bridge inverter has the energy balancing capability among input dc sources in addition to the FT capabilities. However, this topology cannot tolerate the faults on

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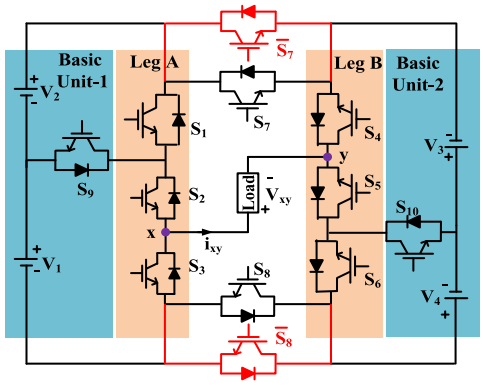

Fig. 1. Proposed FTMLI topology.

the middle switches, and it also uses a bidirectional switch and center tap transformer, which makes the system bulky and costly. In [22], two FT structures, namely partial FT and complete FT structures, are proposed. The two structures use bidirectional switches to accommodate the faults on the switches. The presence of bidirectional switches increases the cost and reduces the efficiency of the system. A T-type MLI [23] with a redundant leg is presented for tolerating the faults in multiple legs. However, the operation under fault cases with redundant leg has higher losses due to the presence of two switches and six diodes in the conduction path. A novel FTMLI structure [24] derived from the combination of conventional MLI topologies preserves the output power under all fault conditions. But this structure requires a more significant number of components. An NPC-based FTMLI topology [25] completely tolerates the single- and multiswitch faults without any bidirectional switches. Nevertheless, the redundant leg made up of six switches increases the losses in the inverter. A reliable and efficient MLI topology that can tolerate the open circuit (OC)/short circuit (SC) faults in sources and OC faults in the switches is introduced in [26]. The main drawback of this topology lies in the utilization of a bidirectional switch configured by a single unidirectional switch and four diodes. Due to this, the TSV of the inverter is very high. The modular multilevel converters provide fault-tolerant features but have a drawback of higher device count [27], [28].

A new FTMLI structure to address the drawbacks of the above topologies has been presented in this article. The salient features of the proposed topology are reduced device count, lower TSV, capable of tolerating single and multiswitch faults, operates under symmetric and asymmetric modes, and absence of bidirectional switches.

Furthermore, the control configuration to utilize skipped level output voltage for the proposed topology in minimizing lower order harmonics is elaborated.

II. Proposed FTMLI

The power circuit of the proposed topology is depicted in Fig. 1. Switches S_1, S_2, and S_3 form leg A, and S_4, S_5, and S_6 form the leg B. The two basic units 1 and 2 are connected to the legs A and B, and each basic unit comprises of two dc sources and one power switch. The intermittent switches

TABLE I
Switching States for Symmetric Mode Under Healthy Conditions

S_1	S_2	S_3	S_4	S_5	S_6	$S_7/\overline{S_7}$	$S_8/\overline{S_8}$	S_9	S_{10}	State no	V_{xy}
0	0	1	0	1	0	0	1	0	1	P_{11}	+V
0	1	0	0	1	1	0	1	1	0	P_{12}	
0	0	1	1	0	0	0	1	0	0	P_{21}	+2V
1	1	0	0	1	1	0	1	0	0	P_{22}	
0	1	0	0	1	0	0	1	1	1	P_{23}	
0	1	0	1	0	0	0	1	1	0	P_{31}	+3V
1	1	0	0	1	0	0	1	0	1	P_{32}	
1	1	0	1	0	0	0	1	0	0	P_{41}	+4V
0	0	1	0	1	1	0	1	0	0	Z_{01}	0
1	1	0	1	0	0	1	0	0	0	Z_{02}	
0	1	0	1	0	0	1	0	1	0	N_{11}	-V
1	1	0	0	1	0	1	0	0	1	N_{12}	
0	0	1	1	0	0	1	0	0	0	N_{21}	-2V
1	1	0	0	1	1	1	0	0	0	N_{22}	
0	1	0	0	1	0	1	0	1	1	N_{23}	
0	0	1	0	1	0	1	0	0	1	N_{31}	-3V
0	1	0	0	1	1	1	0	1	0	N_{32}	
0	0	1	0	1	1	1	0	0	0	N_{41}	-4V
1=Switch ON, **0**= Switch OFF											

S_7 and S_8 make the connection between two legs A and B; here, two redundant switches $\overline{S_7}$ and $\overline{S_8}$ are connected across S_7 and S_8, respectively, to incorporate full fault tolerance. In addition, the proposed inverter has the bidirectional power flow (four-quadrant operation) capability in all voltage levels for all fault conditions and hence the operation of the proposed FTMLI is not affected by the nature of the load. Furthermore, the proposed topology can operate under symmetric and asymmetric dc source configurations.

A. Symmetric Mode of Operation

According to the switching Table I, the proposed MLI with symmetrical dc sources ($V_1 = V_2 = V_3 = V_4 = V$) generates the nine-level output waveform under fault-free conditions. From the table, it can be noticed that the proposed MLI contains more redundant switching states. As a result, it can tolerate the various types of switches and/or source faults.

TSV is one of the significant parameters influencing the MLI cost and is equal to the sum of the blocking voltages of all switches. The blocking voltages of the switches presented in the proposed topology are given as

$$\left.\begin{array}{l} V_{S_1} = V_{S_2} = V_{S_5} = V_{S_6} = V_{S_9} = V_{S_{10}} = V \\ V_{S_3} = V_{S_4} = 2V; V_{S_7} = V_{S_8} = 4V \end{array}\right\}. \quad (1)$$

Therefore, the TSV of the proposed topology in symmetric mode is equal to 18 V and is less compared to the recently proposed topologies. However, under the fault-free mode of operation, the switches S_3, S_4, S_7, and S_8 are subjected to block more voltage and become more vulnerable to a fault. To avoid the risk of failure, these switches are operated at the near fundamental frequency. Table II presents the available switching states and voltage levels of the proposed topology for different fault conditions under symmetric mode. It can be noticed that the proposed MLI can tolerate the faults on single and multiple switches. Here, the fault cases are divided into seven groups

TABLE II
SWITCHING STATES FOR OC FAULT CONDITIONS IN SYMMETRIC MODE

Faulty switches/sources	Group	Voltage levels with state numbers								
		+4V	+3V	+2V	+V	0	-V	-2V	-3V	-4V
$S_1/S_1S_7/S_1S_8/S_1S_{10}$	1	X	P_{31}	P_{21}	P_{11}	Z_{01}	N_{11}	N_{21}	N_{31}	N_{41}^*
$S_3/S_3S_7/S_3S_8/S_3S_{10}$		P_{41}^*	P_{31}	P_{22}/P_{23}	P_{12}	Z_{02}	N_{11}/N_{12}	N_{22}/N_{23}	N_{32}	X
$S_4/S_4S_7/S_4S_8/S_4S_9$		X	P_{32}	P_{22}/P_{23}	P_{11}	Z_{01}	N_{12}	N_{22}/N_{23}	N_{31}	N_{41}^*
$S_6/S_6S_7/S_6S_8$		P_{41}^*	P_{31}	P_{21}	P_{11}	Z_{02}	N_{11}	N_{21}	N_{31}	X
S_6S_9		P_{41}^*	P_{32}	P_{21}	P_{11}	Z_{02}	N_{12}	N_{21}	N_{31}	X
$S_2/S_2S_7/S_2S_8/S_2S_9$	2	X	X	P_{21}	P_{11}^*	Z_{01}	X	N_{21}	N_{31}^*	N_{44}^*
S_5/S_6S_{10}		P_{41}^*	P_{31}^*	P_{21}	X	Z_{02}	N_{11}^*	N_{21}	X	X
S_1S_2/S_1S_9		X	X	P_{21}	P_{11}^*	Z_{01}	X	N_{21}	N_{31}^*	N_{41}^*
S_1S_4		X	X	P_{23}	P_{11}^*	Z_{01}	X	N_{23}	N_{31}^*	N_{41}^*
$S_5S_6/S_5S_7/S_5S_8/S_5S_{10}$		P_{41}^*	P_{31}^*	P_{21}	X	Z_{02}	N_{11}^*	N_{21}	X	X
S_2S_{10}		X	X	P_{21}	X	Z_{01}	X	N_{21}	X	N_{41}
S_3S_6		P_{41}^*	P_{31}^*	P_{23}	X	Z_{02}	X	N_{23}	X	X
S_3S_9		P_{41}^*	P_{32}^*	P_{22}	X	Z_{02}	N_{12}^*	N_{22}	X	X
S_4S_{10}		X	P_{31}^*	P_{22}	P_{12}^*	Z_{01}	X	N_{22}	N_{32}^*	N_{41}^*
S_5S_9		P_{41}^*	X	P_{21}	X	Z_{02}	X	N_{21}	X	X
S_7/S_7S_8	3	P_{41}	P_{31}	P_{21}	P_{11}	Z_{02}	N_{11}	N_{21}	N_{31}	N_{41}
S_8		P_{41}	P_{31}	P_{21}	P_{11}	Z_{02}	N_{11}	N_{21}	N_{31}	N_{41}
$S_9/S_7S_9/S_8S_9$		P_{41}	P_{32}	P_{21}	P_{11}	Z_{02}	N_{12}	N_{21}	N_{31}	N_{41}
$S_{10}/S_7S_{10}/S_8S_{10}$		P_{41}	P_{31}	P_{21}	P_{12}	Z_{02}	N_{11}	N_{21}	N_{32}	N_{41}
V_1V_2	4	X	X	P_{21}	P_{11}	Z_{02}	N_{12}	N_{22}	X	X
V_3V_4		X	X	P_{22}	P_{12}	Z_{02}	N_{11}	N_{22}	X	X
V_1V_3	5	X	X	X	P_{11}	Z_{02}	N_{11}	X	X	X
V_2V_4		X	X	X	P_{12}	Z_{02}	N_{12}	X	X	X
S_9S_{10}	6	P_{41}	X	P_{21}	X	Z_{02}	X	N_{21}	X	N_{41}
S_2S_4	7	X	X	X	P_{11}	Z_{01}	X	X	N_{31}	N_{41}^*
S_3S_5		P_{41}^*	P_{31}	X	X	Z_{02}	N_{11}	X	X	X

X = unavailable switching states, * = unutilized switching states

based on the available voltage levels and are briefly explained in Section IV.

B. Asymmetric Mode of Operation

Under healthy conditions, the proposed topology with asymmetric dc sources ($V_1 = V_2 = V$ and $V_3 = V_4 = 3\ V$) generates a 17-level output voltage consisting of $\pm 8\ V$, $\pm 7\ V$, $\pm 6\ V$, $\pm 5\ V$, $\pm 4\ V$, $\pm 3\ V$, $\pm 2\ V$, $\pm V$, and zero levels. Table III displays the switching states for each voltage level under normal conditions. For the same number of switches, the proposed MLI produces more voltage levels in this mode compared to the symmetric mode. The TSV of the proposed MLI in asymmetric mode is obtained similarly to that of symmetric mode and is equal to 36 *V*. Table IV presents the switching scheme of the proposed topology for different fault cases under asymmetric mode. The failure of all switch groups other than group 5 leads to skipped level output voltage, and the control strategy needs to be changed for all these instances. A detailed description of the modified pulsewidth modulation (PWM) control technique for skipped level output and various fault conditions under asymmetric mode is presented in Sections III and IV, respectively.

TABLE III
SWITCHING STATES FOR ASYMMETRIC MODE UNDER HEALTHY CONDITIONS

S_1	S_2	S_3	S_4	S_5	S_6	$S_7/\overline{S_7}$	$S_8/\overline{S_8}$	S_9	S_{10}	State no	V_{xy}
0	1	0	0	1	1	0	1	1	0	P_1	+V
1	1	0	0	1	1	0	1	0	0	P_2	+2V
0	0	1	0	1	0	0	1	0	1	P_3	+3V
0	1	0	0	1	0	0	1	1	1	P_4	+4V
1	1	0	0	1	0	0	1	0	1	P_5	+5V
0	0	1	1	0	0	0	1	0	0	P_6	+6V
0	1	0	1	0	0	0	1	1	0	P_7	+7V
1	1	0	1	0	0	0	1	0	0	P_8	+8V
0	0	1	0	1	1	0	1	0	0	Z_1	0
1	1	0	1	0	0	1	0	0	0	Z_2	
0	1	0	1	0	0	1	0	1	0	N_1	-V
0	0	1	1	0	0	1	0	0	0	N_2	-2V
1	1	0	0	1	0	1	0	0	1	N_3	-3V
0	1	0	0	1	0	1	0	1	1	N_4	-4V
0	0	1	0	1	0	1	0	0	1	N_5	-5V
1	1	0	0	1	1	1	0	0	0	N_6	-6V
0	1	0	0	1	1	1	0	1	0	N_7	-7V
0	0	1	0	1	1	1	0	0	0	N_8	-8V

III. SKIPPED LEVEL OUTPUT AND ITS CONTROL STRATEGY

This section briefs the concept of skipped level output by considering a case study on seven-level MLI under different conditions, as shown in Fig. 2. Fig 2(a) corresponds to the output voltage of the inverter under healthy conditions. In this case, all seven voltage levels, such as $\pm 3\ V$, $\pm 2\ V$, $\pm V$, and 0 levels, are produced at the output. Fig. 2(b) and (c) shows the samples of inverter possible output voltage cases under faulty conditions. Here, if some voltage levels are unavailable at the output, it is referred to as skipped level output. In Fig. 2(b), the $2\ V$ voltage level is missed in both positive and negative half cycles of the output voltage, and it is referred to as symmetrical

TABLE IV
SWITCHING STATES FOR OC FAULT CONDITIONS IN ASYMMETRIC MODE

Faulty switches/sources	Voltage levels with state numbers																
	+8V	+7V	+6V	+5V	+4V	+3V	+2V	+V	0	-V	-2V	-3V	-4V	-5V	-6V	-7V	-8V
S_1	X	P_7	P_6	X	P_4	P_3	X	P_1	Z_1	N_1	N_2	X	N_4	N_5	X	N_7	N_8*
S_3	P_8*	P_7	X	P_5	P_4	X	P_2	P_1	Z_2	N_1	X	N_3	N_4	X	N_6	N_7	X
S_2	X	X	X	X	X	P_3	X	X	Z_1	X	N_2	X	X	N_5	X	X	N_8*
S_4	X	X	X	P_5	P_4	P_3	P_2	P_1	Z_1	X	X	N_3	N_4	N_5	N_6*	N_7*	N_8*
S_6	P_8*	P_7*	P_6*	P_5	P_4	P_3	X	X	Z_2	N_1	N_2	N_3	N_4	N_5	X	X	X
S_5	P_8*	P_7*	P_6	X	X	X	X	X	Z_2	N_1	N_2	X	X	X	X	X	X
S_7	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	Z_1	N_1	N_2	N_3	N_4	N_5	N_6	N_7	N_8
S_8	P_8	P_7	P_6	P_5	P_4	P_3	P_2	P_1	Z_1	N_1	N_2	N_3	N_4	N_5	N_6	N_7	N_8
S_9	P_8	X	P_6	P_5	X	P_3	P_2	X	Z_1	X	N_2	N_3	X	N_5	N_6	X	N_8
S_{10}	P_8	P_7	P_6	X	X	X	P_2	P_1	Z_2	N_1	N_2	X	X	X	N_6	N_7	N_8
V_1V_2	X	X	P_6	X	X	P_3	X	X	Z_1	X	X	N_3	X	X	N_6	X	X
V_3V_4	X	X	X	X	X	X	P_2	P_1	Z_2	N_1	N_2	X	X	X	X	X	X
V_1V_3	X	X	X	X	X	P_3	X	X	Z_1	X	X	N_3	X	X	X	X	X
V_2V_4	X	X	X	X	X	X	X	P_1	Z_2	X	X	N_3	X	X	X	X	X

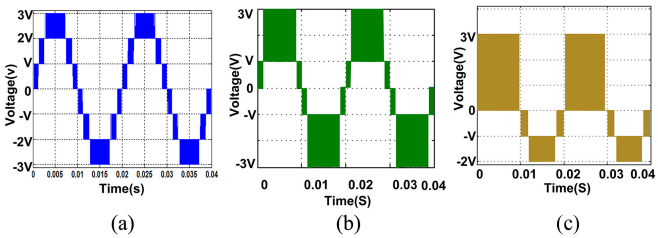

Fig. 2. (a) Seven-level output. (b) Symmetric skipped level output. (c) Asymmetric skipped level output.

skipped level output, whereas in Fig. 2(c), $+V$, $+2$ V, and -3 V levels are missed at the output waveform. This type of output waveform is called an asymmetric skipped level output. The unequal voltage levels in the positive and negative half cycle produce dc offset at the output, which is undesirable. Thus, the authors in the literature did not utilize the above-skipped level output and made the inverter unavailable for service. Recently, an interesting work [29] addressed the above problem with the appropriate modifications in carrier dispositions and modulation index (m_a) value in the PWM control technique. Application of the same technique is explored for the proposed converter in utilizing the converter at post fault conditions and is discussed below.

In generating the PWM pulses for MLI, the position of the carriers and reference sine wave for healthy and skipped level cases are shown in Fig. 3. Here, V_{c1}, V_{c2}, V_{c3}, V_{c-1}, V_{c-2}, and V_{c-3} are the carriers required to generate $+V$, $+2$ V, $+3$ V, $-V$, -2 V, and -3 V voltage levels, respectively. From the figure, it can be observed that the carrier positions corresponding to ± 3 V levels in symmetric skipped level case and carrier position of $+3$ V level in asymmetric skipped level are modified as compared to healthy case. In Fig. 2(b), the maximum available positive and negative voltage levels are equal to 3 V, and hence the reference sine magnitude remains unchanged, as shown in Fig. 3(b), whereas, in Fig. 2(c), the peak available voltage in positive and negative is 3 V and 2 V, respectively. In this case, to avoid dc offset, the peak value of the reference sine wave is fixed to two (or <2). Hence, the maximum possible modulation index ($m_{a\_\max}$) value for

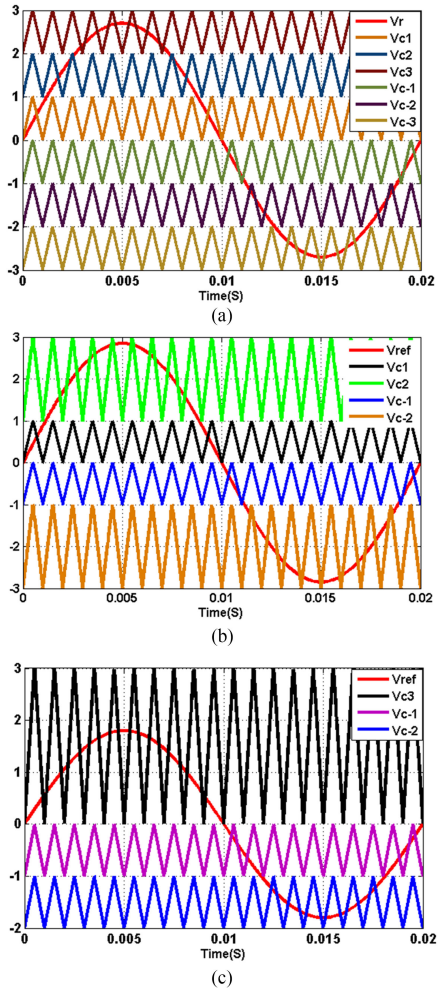

Fig. 3. Carrier positions in PWM technique for (a) healthy case (HC) and (b) symmetric skipped level case (SSLC). (c) Asymmetric skipped level case (ASLC).

the asymmetric skipped level output is 0.67. Furthermore, the harmonic analysis for the seven-level and skipped level outputs shown in Fig. 2 is performed with level shifted carrier PWM (LSCPWM) at different switching frequencies and modulation

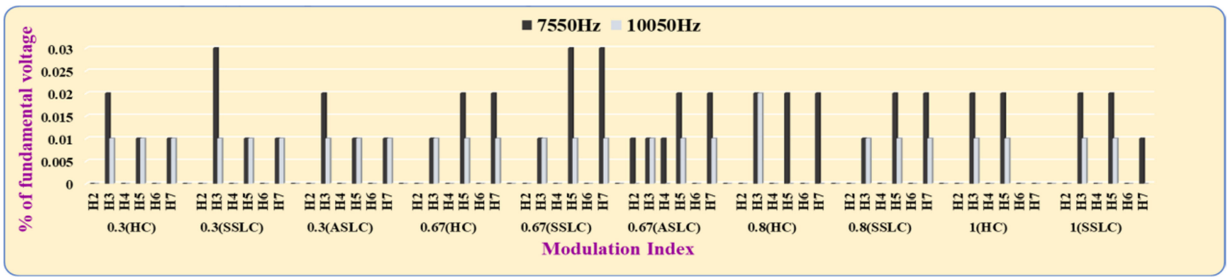

Fig. 4. Voltage harmonics for HC, SSLC, and ASLC.

TABLE V
LIST OF SIMULATION AND EXPERIMENTAL PARAMETERS

Input DC Voltage Sources	Symmetric Mode: $V_1 = V_2 = V_3 = V_4 = 30$ V Asymmetric Mode: $V_1 = V_2 = 10$V; $V_3 = V_4 = 30$V
Reference frequency	50 Hz
Carrier frequency	10 kHz
Load Resistance	R= 50 Ω
Load Inductance	L= 50 mH

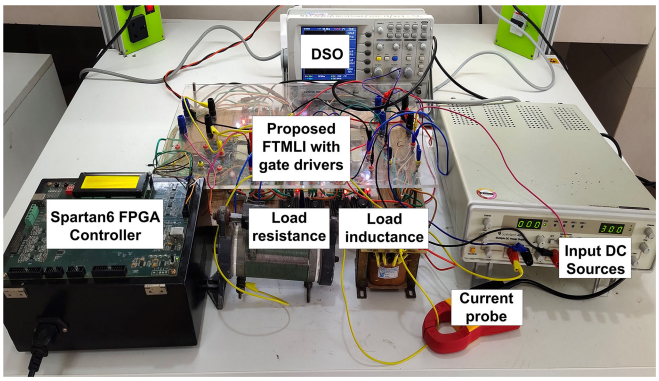

Fig. 5. Prototype of the proposed FTMLI topology.

indexes, and the corresponding lower order voltage harmonics are depicted in Fig. 4. It can be observed that the magnitudes of the individual lower order harmonics for skipped level output voltages are insignificant as per IEEE-519 rules.

IV. SIMULATION AND EXPERIMENTAL RESULTS

Numerous simulation and experimental studies are performed to demonstrate the proposed MLI functioning under healthy and faulty conditions. The different parameters considered for both the study are given in Table V. The prototype model of the proposed topology is depicted in Fig. 5. Here, the SPARTAN6 field-programmable gate array controller is used to obtain the gate pulses using the LSCPWM control technique for healthy and faulty modes as per the flowchart given in Fig. 6. Once the fault detection algorithm [30] identifies the fault on the switch, the controller generates the switching pulses according to Table II for SM or Table IV for ASM. From Tables II and IV, the unavailable switching states limit the operating range of the proposed FTMLI in four quadrants under fault conditions, which is based on the inverter's highest available voltage level at the output.

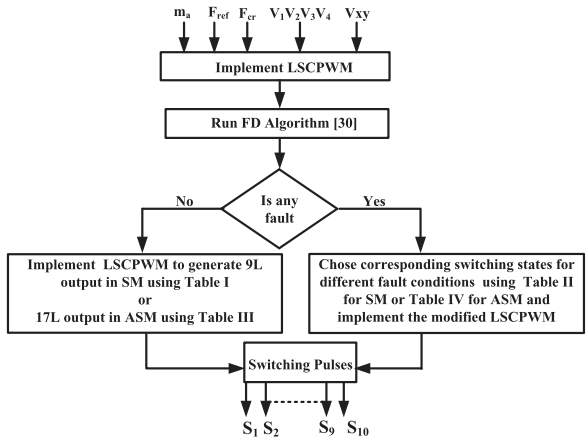

Fig. 6. Flowchart for implementation of control strategy under healthy and fault conditions.

A. Symmetric Mode (SM)

The simulation and experimentation for symmetric mode are performed under fault-free conditions and the corresponding results are shown in Figs. 7(a) and 8(a), respectively. It can be observed that the nine-level voltage waveform with the near sinusoidal current is produced at the output. The FT capability of the proposed MLI for one case from each group depicted in Table II is presented in the following.

1) Fault on S_1 (Group1): The simulation and experimental results of the output voltage and current for S_1 failure are shown in Figs. 7(b) and 8(b). The OC fault on S_1 causes the loss of $+2$ *V* and $+4$ *V* voltage levels at the output. However, during the reconfiguration, the $+2$ *V* voltage level is produced by considering the switching state (P_{21}) mentioned in Table II, whereas the $+4$ *V* level is not possible to generate as it does not contain any redundant switching states. The possible voltage levels under this fault condition are 0, $\pm V$, ± 2 *V*, and ± 3 *V*. So, to generate the seven-level output voltage waveform, the maximum modulation index value ($m_{a\_\max}$) is updated to 0.75. The OC fault on the remaining group1 switches would exhibit similar results.

2) Fault on S_2 (Group2): During the S_2 OC fault condition, the voltage levels 3 *V* and 4 *V* in the positive half cycle and V level in the negative half cycle are not possible to generate, as given in Table II. The topology is now reconfigured to avoid dc offset

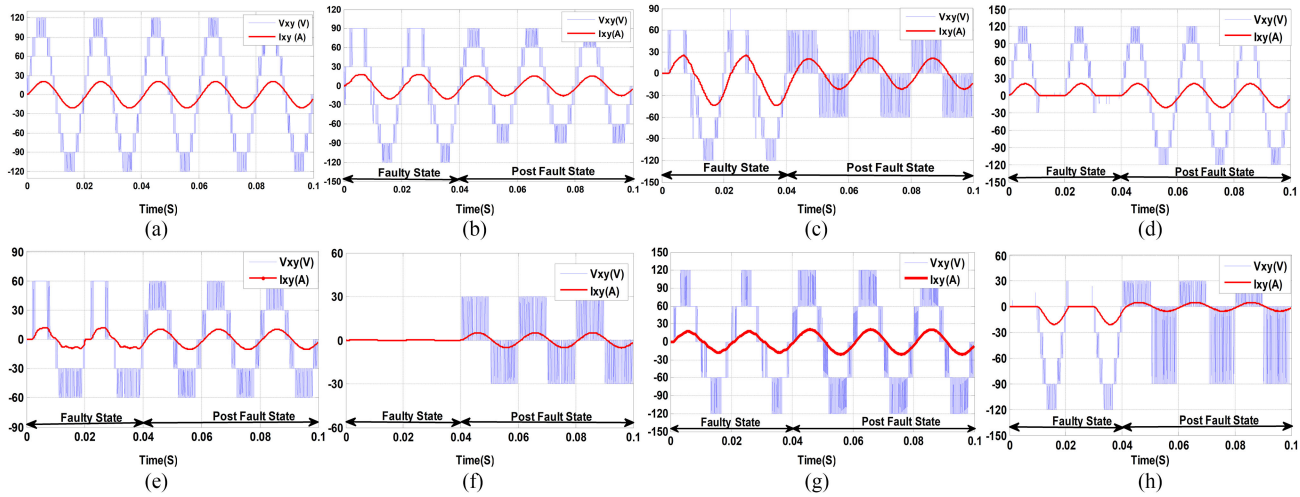

Fig. 7. Simulation results in SM during (a) healthy condition, (b) S_1 fault, (c) S_2 fault, (d) S_7 fault, (e) V_1V_2 fault, (f) V_1V_3 fault, (g) S_9S_{10} fault, and (h) S_2S_4 fault.

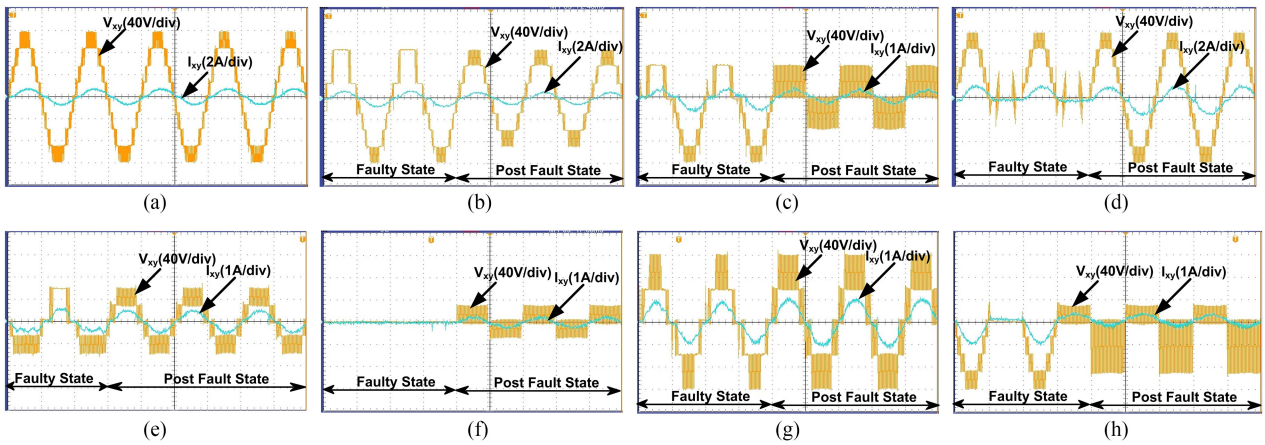

Fig. 8. Experimental results in SM during (a) healthy condition, (b) S_1 fault, (c) S_2 fault, (d) S_7 fault, (e) V_1V_2 fault, (f) V_1V_3 fault, (g) S_9S_{10} fault, and (h) S_2S_4 fault.

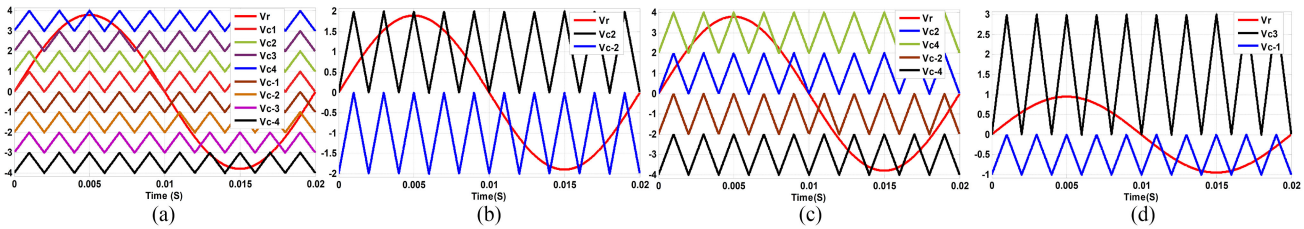

Fig. 9. Position of the carriers in SM during (a) healthy condition, (b) S_2 fault, (c) S_9S_{10} fault, and (d) S_2S_4 fault.

by changing carrier positions and $m_{a\_\max}$ value to 0.5 in the LSCPWM technique. Here, the carrier positions under healthy and post fault states are shown in Fig. 9(a) and (b), respectively. In this figure, V_{c2} and $V_{c\text{-}2}$ represent the carriers required to generate the $+2$ V and -2 V levels, respectively. The simulation and experimental results of the proposed MLI under the S_2 fault condition are shown in Fig. 7(c) and 8(c). The remaining switch failure cases belong to group2 show similar results as that of S_2 failure.

3) Fault on S_7 (Group3): The OC fault of the S_7 switch will not produce any voltage levels during the negative half cycle. Under this situation, the redundant switch $\overline{S_7}$ is operated to get all the voltage levels at the output. Figs. 7(d) and 8(d) depict the simulation and experimental results for S_7 fault. It can be noticed that the proposed topology under S_7 fault condition produces the same number of voltage levels as that of a healthy condition. Similarly, the fault on the remaining switches of the group3 generates the nine-level output waveform.

4) Simultaneous Fault on Sources V_1 and V_2 (Group4): The simultaneous OC fault on sources V_1 and V_2 results in a loss of ± 4 *V* and ± 3 *V* voltage levels, as shown in Table II. So, the proposed MLI generates the five-level output waveform consisting of ± 2 *V*, $\pm V$, and 0 voltage levels; here, the maximum modulation index value ($m_{a\_\max}$) is limited to 0.5. Figs. 7(e) and 8(e) demonstrate the simulation and experimental results for V_1V_2 fault conditions. Similar results are obtained when both the sources V_3 and V_4 undergone OC fault.

5) Simultaneous Fault on Sources V_1 and V_3 (Group5): Figs. 7(f) and 8(f) show the simulation and experimental results of the proposed topology under V_1 and V_3 OC fault conditions. Table II presents that the voltage levels such as 4 *V*, 3 *V*, and 2 *V* in both positive and negative half cycles cannot be generated during the simultaneous OC fault on the V_1 and V_3 sources. Hence, the resultant three-level output voltage waveform consisting of $+V$, 0, and $-V$ levels can be produced by changing the $m_{a\_\max}$ value to 0.25. The simultaneous OC fault on V_2 and V_4 exhibit similar results as that of V_1 and V_3 failure.

6) Simultaneous Fault on S_9S_{10} (Group6): When a simultaneous fault occurs on the switches S_9 and S_{10}, the proposed MLI generates the symmetrical skipped output waveform with ± 4 *V*, ± 2 *V*, and 0 voltage levels, as depicted in Table II. The remaining voltage levels ± 3 *V* and $\pm V$ are not possible to generate at this fault condition due to the absence of current paths. Due to this, the positions of the carriers are changed in comparison with the healthy conditions, and are shown in Fig. 9(c). In this figure, V_{c2} and V_{c4} represent the carriers required to generate the $+2$ *V* and $+4$ *V* voltage levels, and $V_{c\text{-}2}$ and $V_{c\text{-}4}$ correspond to the -2 *V* and -4 *V* levels, respectively. With the above modifications, the proposed MLI generates the symmetrical skipped output waveform shown in Figs. 7(g) and 8(g).

7) Simultaneous Fault on S_2S_4 (Group7): Table II indicates that only $+4$ *V*, $+3$ *V*, 0, and $-V$ voltage levels are possible when an OC fault occurs on the switches S_2 and S_4 simultaneously. A dc offset has appeared at the output because of these unequal voltage levels in positive and negative half cycles. None of the authors in the literature did not consider the above voltage levels and made the system into a nonoperative mode. However, with the appropriate modifications in the LSCPWM technique, the dc offset can be eliminated, and thus the inverter shutdown can be prevented. The modifications required in the LSCPWM technique are 1) change the carrier's positions and 2) update the $m_{a\_\max}$ value. Here, the positive half cycle must be clamped to $+V$ to make the dc offset zero. But this level is not present in the positive half cycle, and hence the next highest possible voltage level $+3$ *V* is emulated as $+V$ by changing the carrier position, which is shown in Fig. 9(d). It can be observed that the carrier position corresponding to $+3$ *V* level and reference peak are modified. These modifications in the LSCPWM technique eliminates the dc offset present in the output. The simulation and experimental results of the load voltage and current for S_2 and S_4 fault conditions are presented in Figs. 7(h) and 8(h). A similar procedure can be adopted for OC fault on S_3 and S_5.

B. Asymmetric Mode (ASM)

Figs. 10(a) and 11(a) show the simulation and experimental results for the proposed MLI working under ASM mode. It can be seen that the proposed topology under fault-free conditions generates the 17-level output voltage waveform with the sinusoidal current. The proposed MLI fault-tolerant capability in ASM mode is described in the following.

1) Fault on S_1: The possible voltage levels under the S_1 OC fault condition are *V*, 3 *V*, 4 *V*, 6 *V*, and 7 *V* in the positive half cycle and *V*, 2 *V*, 4 *V*, 5 *V*, 7 *V*, and 8 *V* in the negative half cycle, as given in Table IV. The dc offset at the output resulting from these levels can be eliminated by clamping the negative cycle to the peak value of 7 *V* with the change of m_a value. Under this fault condition also, the position of the carriers in the LSCPWM technique is changed, as shown in Fig. 12(b). With these modifications, the proposed MLI under the S_1 OC fault condition generates the output waveform shown in Figs. 10(b) and 11(b). The OC fault on S_3 shows results that are similar to the S_1 fault.

2) Fault on S_2: Table IV presents when an OC fault occurs on S_2, the voltage levels such as $+3$ *V*, $+6$ *V*, 0, -2 *V*, -5 *V*, and -8 *V* are possible at the output. In this fault scenario also, the LSCPWM requires changes in the carrier position and m_a value shown in Fig. 12(c). From the figure, it can be observed that the carrier positions and peak reference wave are changed compared to that of healthy conditions. These modifications ensure zero dc offset at the output. Figs. 10(c) and 11(c) display the output voltage and current waveforms obtained in simulation and experimental studies for the S_2 fault in ASM.

3) Fault on S_4: During the S_4 OC fault condition, the voltage levels $+6$ *V*, $+7$ *V*, $+8$ *V*, $-V$, and -2 *V* are not possible to generate, which is given in Table IV. These unequal of voltage levels introduce a dc offset in the output. The voltage levels -6 *V*, -7 *V*, and -8 *V* are not considered to eliminate the dc offset, and the m_a value is changed corresponding to ± 5 *V* voltage levels. Besides, the carrier ($V_{c\text{-}3}$) position corresponding to the -3 *V* voltage level is changed, as shown in Fig. 12(d). Figs. 10(d) and 11(d) demonstrate the simulation and experimental results of the proposed MLI under S_4 fault condition in ASM. Similar results are obtained when S_6 undergone OC fault.

4) Fault on S_5: The simulated and experimental output voltage and current waveforms for the S_5 fault condition under ASM are shown in Figs. 10(e) and 11(e). Table IV indicates that, when S_5 undertakes OC fault, only $+6$ *V*, $+7$ *V*, $+8$ *V*, 0, $-V$, and -2 *V* voltage levels are possible to generate at the output. The modified control strategy, as shown in Fig. 12(e), eliminates the dc offset that appeared at the output. From the figure, it can be observed that the only 6 *V* voltage level in positive half cycle is considered and the carrier position corresponding to this level and m_a values is changed.

5) Fault on S_7: The OC fault of the S_7 switch will not produce any voltage levels during the negative half cycle. Under this situation, the redundant switch is operated to get all the voltage levels at the output. Figs. 10(f) and 11(f) depict the simulation and experimental results for S_7 fault in ASM. It can be noticed that the proposed topology under the S_7 fault condition

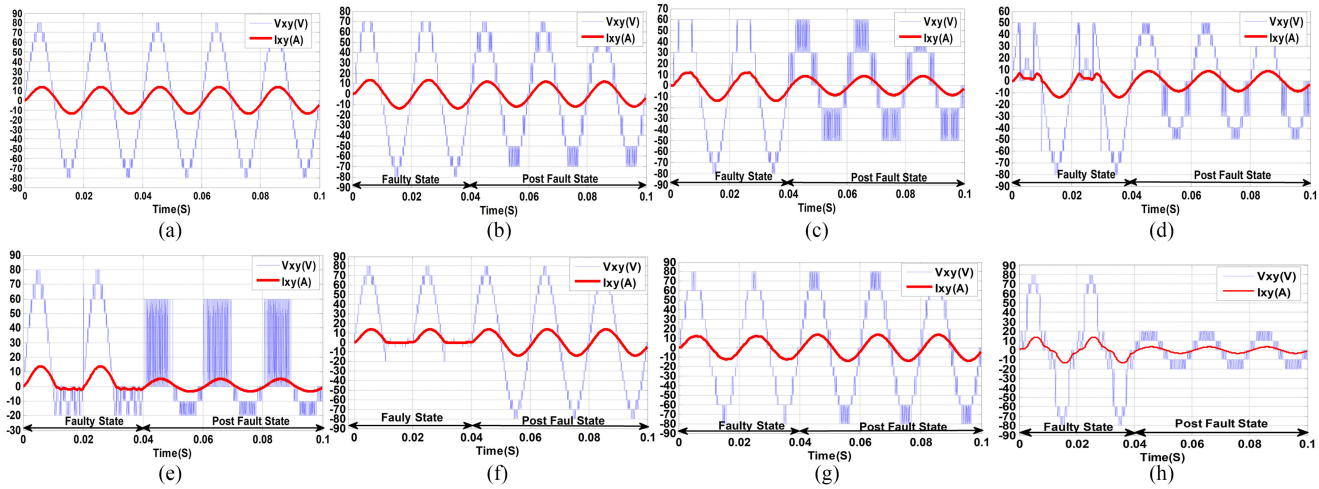

Fig. 10. Simulation results in ASM during (a) healthy condition, (b) S_1 fault, (c) S_2 fault, (d) S_4 fault, (e) S_5 fault, (f) S_7 fault, (g) S_9 fault, and (h) V_3V_4 fail.

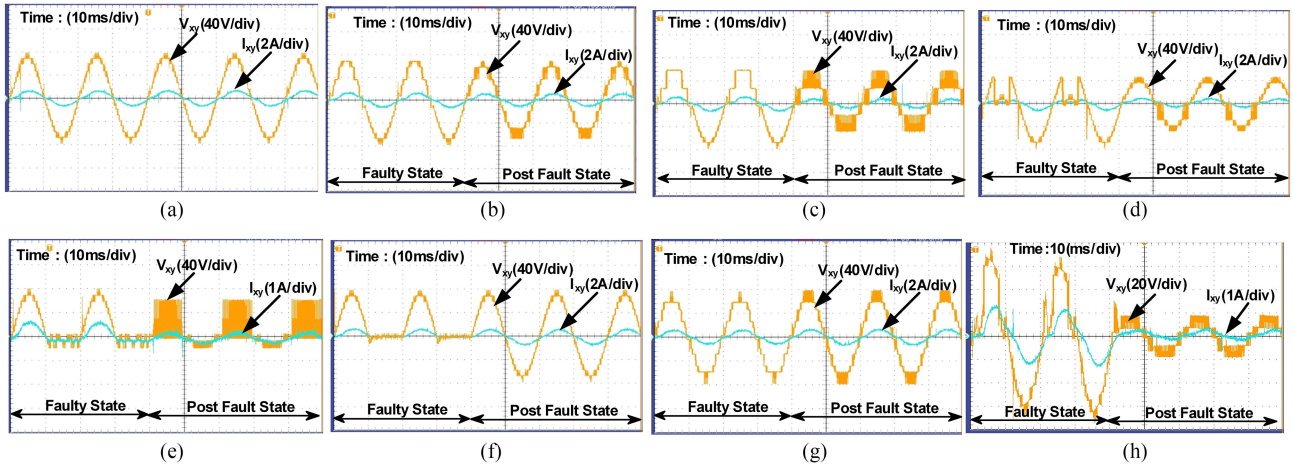

Fig. 11. Experimental results in ASM during (a) healthy condition, (b) S_1 fault, (c) S_2 fault, (d) S_4 fault, (e) S_5 fault, (f) S_7 fault, (g) S_9 fault, and (h) V_3V_4 fail.

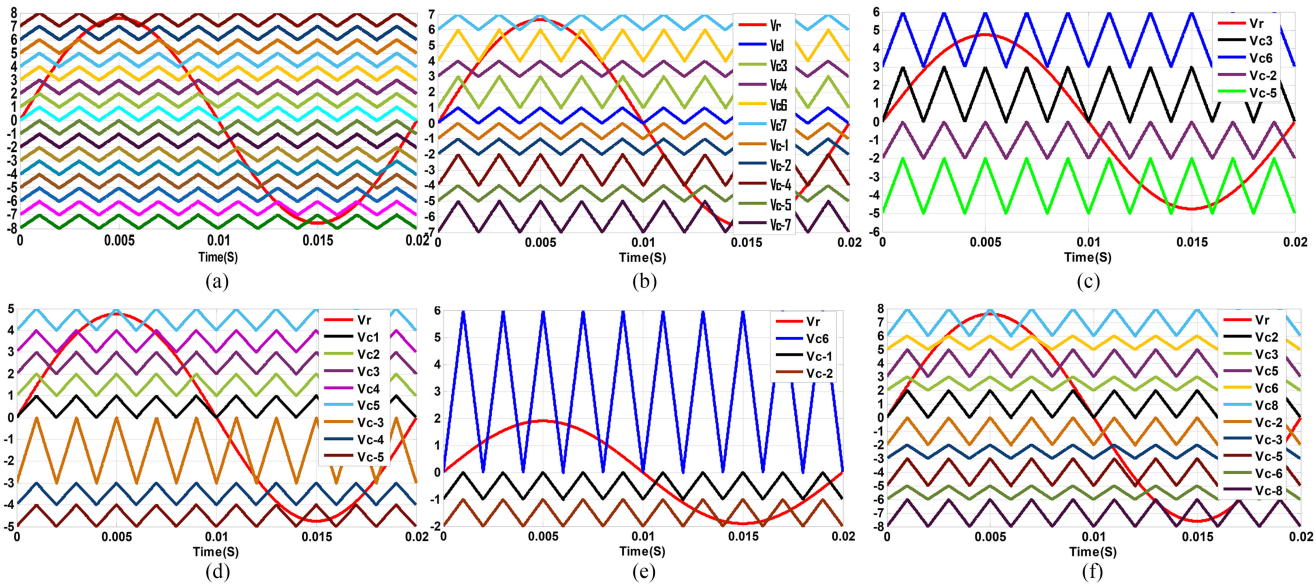

Fig. 12. Position of the carriers in ASM during (a) healthy condition, (b) S_1 fault, (c) S_2 fault, (d) S_4 fault, (e) S_5 fault, and (f) S_9 fault.

produces the same number of voltage levels as that of a healthy condition. Similarly, the fault on the S_8 switch generates the 17-level output voltage waveform with the help of the switch.

6) Fault on S_9: Under the S_9 OC fault, the voltage levels $\pm V$, $\pm 4\ V$, and $\pm 7\ V$ are not possible to generate, as given in Table IV. However, the proposed MLI with a modified PWM technique generates the symmetric skipped level waveform consisting $\pm 2\ V$, $\pm 3\ V$, $\pm 5\ V$, $\pm 6\ V$, and $\pm 8\ V$ levels. Fig. 12(f) shows the position of the carriers under S_9 fault conditions. The carrier positions associated with the above voltage levels are changed to make dc offset zero. The corresponding output voltage and current waveforms for the S_9 fault condition in ASM are shown in Figs. 10(g) and 11(g). The OC fault on switch S_{10} has similar characteristics to the S_9 fault.

7) Simultaneous Fault on the Sources V_3 and V_4: The simultaneous OC fault on sources V_3 and V_4 results in a loss of $\pm 3\ V$, $\pm 4\ V$, $\pm 5\ V$, $\pm 6\ V$, $\pm 7\ V$, and $\pm 8\ V$ voltage levels, as shown in Table IV. So, the proposed MLI generates the five-level output waveform consisting of $\pm 2\ V$, $\pm V$, and 0 voltage levels. Figs. 10(h) and 11(h) demonstrate the simulation and experimental results for V_3V_4 fault conditions. Similar fault analysis can be applied for the remaining sources.

C. SC Fault Analysis

When compared to an OC fault, an SC fault causes severe damage to power semiconductor switches. The switch SC fault can lead to the SC of the input dc source when its complementary switch is turned ON and draws a higher magnitude of the current from it. If this current exceeds the rated thermal integral value, the protection fuse blows out, resulting in an OC [31]. One such case considered is the SC fault on the switch S_1. The input dc source V_2 gets short-circuited when the complementary switch of S_1 (i.e., S_9) is given a pulse to generate $+V$ and $+3\ V$ levels. The simulation and experimental results of switch S_1 under SC fault are shown in Fig. 13. From the figure, it can be noticed that a large current is flowing through the switch S_1 due to the SC of the source V_2 at the fault instant. The fuse blows out due to the high current, and thereby the SC fault is changed to OC fault. During the reconfiguration, the proposed FTMLI generates the symmetric load voltage waveform with $+2\ V$, 0, and $-2\ V$ levels by changing the carrier positions similar to S_2 OC fault conditions. The SC fault on S_6, S_9, and S_{10} would exhibit similar results as that of the S_1 SC fault for symmetric and asymmetric modes. However, the proposed topology is unable to tolerate the SC fault on the remaining switches.

V. Comprehensive Evaluation and Comparisons With Recent Works

A. Efficiency Analysis

The conduction and switching losses are the main parameters that decide the efficiency of any power electronic converter. Moreover, the conduction losses significantly affect the efficiency and are highly reliant on the number of conducting devices. From Table I, it can be noticed that at each level, a maximum of five switches are conducted in the proposed

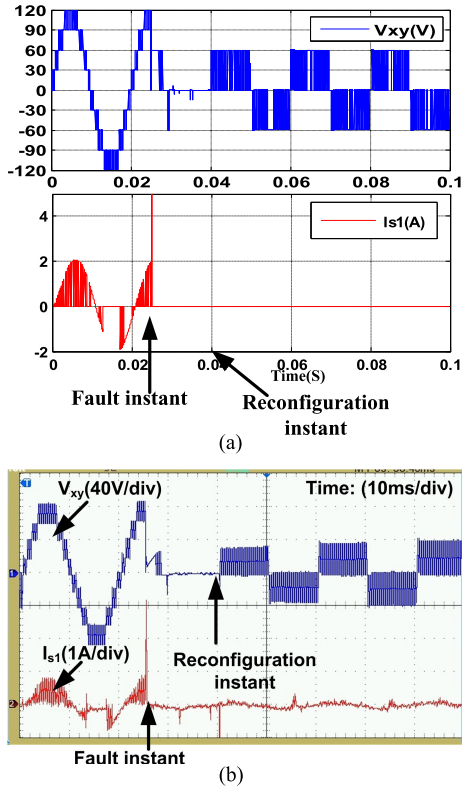

Fig. 13. (a) Simulation and (b) experimental results of output voltage (V_{xy}) and S_1 switch current (I_{s1}) under SC fault condition.

FTMLI. The average conduction and switching losses for each switch and diode are given as

$$P_{sL} = P_{\mathrm{con}L} + P_{\mathrm{sw}L} = \left\{\frac{1}{T_s}\int_0^{T_s}[V_t * i(t) + i(t)^2 * R_{\mathrm{ON}}]dt\right\} + \left\{C_{ds} f_s V_{ds}^2\right\} \quad (2)$$

$$P_{dL} = P_{\mathrm{con}L} = \left\{\frac{1}{T_s}\int_0^{T_s}[V_t * i(t) + i(t)^2 * R_{\mathrm{ON}}]dt\right\} \quad (3)$$

where V_t and $i(t)$ are the forward voltage drop and the current flowing through the devices, respectively, and R_{ON} is the internal resistance of the devices. C_{ds}, f_s, and V_{ds} are the drain–source capacitance, switching frequency, and drain–source voltage of the switch. With the parameters given in Table V, the simulated and experimental efficiency curves shown in Figs. 14 and 15, respectively, are obtained for the proposed FTMLI under healthy and different fault conditions. From the figures, it can be understood that at higher values of m_a, the proposed topology's efficiency is the same for healthy and faulty conditions, whereas at lower values of m_a, its value is slightly less for fault conditions. The slight deviation in the simulation efficiency curves from the experimental ones is due to nonconsideration of contact and solder resistance.

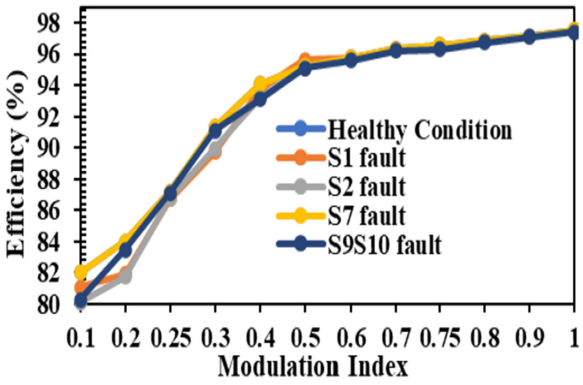

Fig. 14. Simulated efficiency curves of the proposed FTMLI for healthy and different fault scenarios.

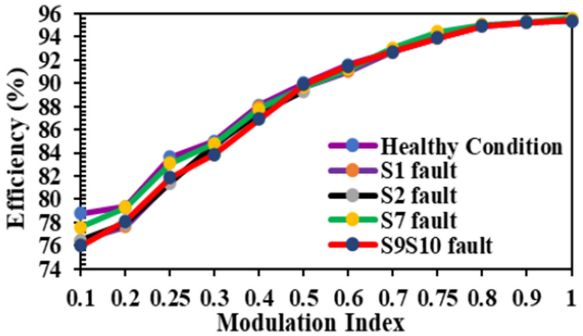

Fig. 15. Experimental efficiency curves of the proposed FTMLI for healthy and different fault scenarios.

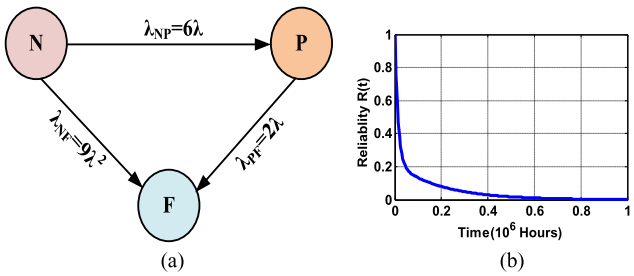

Fig. 16. (a) Markov chain diagram. (b) Reliability curve of the proposed topology.

B. Reliability Evaluation

Reliability evaluation is needed to assess the performance of the FTMLIs. The proposed FTMLI's reliability is assessed using the most widely used Markov chain reliability method. The Markov state transition chain for the proposed topology is shown in Fig. 16(a). The Markov state transition chain with transition rates ($\lambda_{\rm NP}$, $\lambda_{\rm NF}$, and $\lambda_{\rm PF}$) for the proposed topology is shown in Fig. 15. In state N, all the devices are working at fault-free mode, and the inverter delivers the full-rated power. States P and F are related to the inverter's states that deliver reduced power and no power, respectively. The failure rate λ, which is assumed to be the same for all the switches considering severe operating conditions, is obtained by using Military Reliability Handbook (MIL-HNDBK-217F), and the detailed procedure is given in [20]. The reliability function for the proposed topology is given as

$$\begin{aligned} R(t) &= \left(\frac{\lambda_{\rm NP}}{\lambda_{\rm NP}+\lambda_{\rm NF}-\lambda_{\rm PF}}\right)\mathrm{e}^{-\lambda_{\rm PF}t} \\ &\quad + \left(\frac{\lambda_{\rm NF}-\lambda_{\rm PF}}{\lambda_{\rm NP}+\lambda_{\rm NF}-\lambda_{\rm PF}}\right)\mathrm{e}^{-(\lambda_{\rm PF}+\lambda_{\rm NF})t} \\ &= 0.22\mathrm{e}^{-5.04t}+0.78\mathrm{e}^{-72.28t}. \end{aligned} \tag{4}$$

With the above equation, the reliability curve for the proposed topology shown in Fig. 16(b) is obtained.

The mean time to failure, one of the significant reliability performance indices, is obtained for the proposed MLI using the procedure given in [20], and it is found to be 73 500 h.

C. Comparative Study

Table VI indicates the comparison of the proposed nine-level FT topology with other topologies in terms of performance parameters. This table reveals that compared to all other topologies, the proposed FTMLI incorporates fewer switching devices. Furthermore, the topologies in [21] and [22] used extra diodes, whereas the proposed MLI did not use any diodes. The other benefit of the proposed topology is the absence of relays over the topology shown in [21], where two relays are used. Lower TSV is another significant merit of the proposed FTMLI than all other topologies mentioned in Table VI, except for [24] and [31]. However, topologies in [24] and [31] utilized more switching devices than the proposed topology. Also, the proposed FTMLI tolerates the various faults on the sources and single and multiple switches.

The power loss and efficiency of the topologies presented in Table VI are obtained with the help of the PLECS simulation tool by considering the thermal model of the switching device (IKW30N60H3-IGBT). The simulations are performed by considering the IKW30N60H3-IGBT switch model with thermal resistances of 0.8 K/W (junction case) and parameters given in Table V at an ambient temperature of 25 °C. Table VI reveals that the proposed MLI has lower power loss than the remaining topologies, and hence its efficiency is as high as 97.53%. Another important parameter that decides the cost of the inverter is the switching device power (SDP) rating [32]. It is obtained by the product of maximum voltage stress and peak current flowing through each switch. The proposed MLI has a lower SDP rating of 1750 compared to the topologies [18], [21], [22], [26], and [33]. Although the proposed FTMLI and the topology presented in [29] employ an equal number of components, it has a higher TSV and SDP rating than the proposed FTMLI. A lower SDP rating indicates that the proposed FTMLI is cost-effective.

Reliability is another key characteristic of the FTMLI and depends mainly on the number of power semiconductor devices, the availability of redundant states, and the thermal stress of the switching devices [34]. The proposed FTMLI ensures high reliability because of the lower number of switches and low power loss, as shown in Table VI.

From the comparative study and Table VI, the proposed topology is more competitive than other FT topologies in terms

TABLE VI
COMPARISON OF DIFFERENT NINE-LEVEL FTMLI TOPOLOGIES

Parameter	[21]	[24]	[18]	[22]	[26]	[33]	[29]	[31]	Proposed
1	4	2	4	2	4	2	4	2	4
2	0	2	0	2	0	2	0	2	0
3	12	24	20	16	12	6	12	16	12
4	2	0	0	6	4	3	0	0	0
5	4	0	0	4	0	0	0	0	0
6	2	0	0	0	0	0	0	0	0
7	22	16	20	32	24	25	20	16	18
8	4750	1600	2000	4050	2400	2575	1850	1750	1750
9	40.98	37.97	49.31	40.98	33.28	31.62	28.5	30.3	25.31
10	96.06	96.34	95.3	96.06	96.78	96.93	97.22	97.05	97.53
11	Medium	Low	Low	Medium	High	High	High	High	High
12	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
13	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

1- No of DC sources
2- No of flying capacitors
3- No of unidirectional switches
4- No of bidirectional switches
5- No of clamping diodes
6- No of relays
7- TSV(*V)
8-SDP rating in terms of VA
9- Power loss in watts
10-%Efficiency at 1KW
11-Reliability
12- Single switch fault tolerance
13- Multi switch fault tolerance

of component count and functionalities, such as single and multiple switch fault tolerance, but it requires four separate dc sources. However, the proposed topology is best suited for the applications supporting multiple source interfaces.

VI. CONCLUSION

A novel FTMLI topology with a fewer number of power semiconductor switches is presented in this article. The normal and FT operation of the proposed MLI for both symmetric and asymmetric modes is tested through simulation and experimentation. Both the simulation and experimental studies reveal the proposed FTMLI capability in tolerating the faults on the single, multiple switches and sources. The concept of skipped level output voltage and its associated modified PWM control strategy under faulty scenarios is presented and validated for the proposed FTMLI. This feature makes the proposed MLI suitable for driving emergency/critical loads. The comparative study indicates the superiority of the proposed FTMLI in terms of various parameters, such as the number of components, TSV, SDP rating, and efficiency over other recent topologies.

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