A High-Power-Density High-Efficiency Soft-Switched Single-Phase Universal Input to 28-V Isolated AC–DC Converter Module Designed for Paralleled Operation

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***Abstract*—This article presents a high-power-density high-efficiency soft-switched single-phase universal input to 28-V isolated ac–dc converter module designed for parallel operation. The proposed two-stage converter utilizes a totem-pole bridgeless boost power factor correction (PFC) ac–dc converter stage followed by an isolated *LLC* resonant dc–dc converter stage. A comprehensive design and optimization methodology is presented that compares various designs and operating modes for the converter's power stages and selects the optimal design based on overall power density and efficiency. Additionally, a control scheme is presented for the PFC stage to minimize current distortion by accounting for various sensor, control, and gate-drive delays while ensuring zero-voltage switching (ZVS) of the transistors. Moreover, a new droop control strategy is presented, which utilizes the input current of the *LLC* dc–dc stage to ensure equal output current distribution between paralleled modules powering a common output load. To validate the proposed design and control strategy, two 1-kW universal input to 28-V isolated ac–dc converter modules are built and tested. Each prototype converter module achieves a high power density of 84 W/in^3 and a peak efficiency of greater than 93% while ensuring a current distribution error of less than 0.3% when operating in parallel to deliver the maximum output power of 2kW.**

***Index Terms*—AC–DC power conversion, boundary conduction mode (BCM), bridgeless power factor correction (PFC), dc–dc power conversion, digital control, droop control, galvanic isolation, parallel operation, rectifier, soft-switching, zero-voltage switching (ZVS).**

I. Introduction

STEP-DOWN isolated ac–dc power converters are extensively utilized in several applications, including military, aerospace, medical, lighting, and data centers [1]. In such applications, an isolated ac–dc converter needs to satisfy multiple performance specifications, including stringent EMI requirements [2]. Additionally, ever-increasing space and energy utilization constraints in modern applications have made power density and efficiency a key performance requirement for such power converters [3], [4]. Existing state-of-the-art isolated ac–dc power converters can be broadly categorized into single-stage or two-stage architectures [5], [6]. Single-stage ac–dc converters typically utilize a line-frequency bridge rectifier followed by an isolated dc–dc converter, such as isolated pulsewidth modulated (PWM) converters [7]–[11] or isolated resonant converters [12]–[16]. In such architectures, the isolated dc–dc converter performs multiple functions including input power factor correction (PFC) and output dc voltage regulation. Single-stage low-output-voltage ac–dc converter architectures have potential for a lower component count and higher efficiencies but often suffer from lower power densities. The reason stems from the fact that in such architectures, the twice-line-frequency energy buffering capacitor is placed at the output of the converter. Thus, a very large output capacitor is required to keep the twice-line-frequency voltage ripple within the output voltage regulation requirements. On the contrary, in two-stage ac–dc converters, the PFC function is performed by a front-end ac–dc stage and the output voltage regulation function is accomplished by the isolated dc–dc stage [6]. An intermediate dc bus is utilized between the two conversion stages for twice-line-frequency energy buffering. This decouples the energy buffering and output voltage regulation functions, resulting in a reduction in overall capacitance requirement. As a result, the two-stage architectures can achieve high power densities exceeding 50 W/in^3 (3.1 W/cm^3) [17]–[22].

Extensive research has been reported in the literature to enhance the performance of two-stage ac–dc converters by proposing rigorous design and optimization methodologies in [19], [23], and [24], by devising new topological innovations in [25]–[29], and by utilizing new soft-switching techniques in [15]–[18], [20], and [22]–[33]. However, such performance benefits often come at the cost of higher overall switch count, which increases design complexity and/or requires complex control

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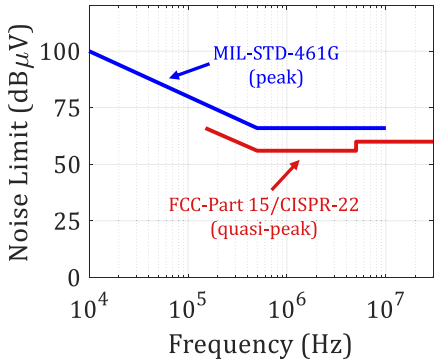

Fig. 1. EMI limits imposed on ac–dc converters by FCC-Part 15/CISPR-22 and MIL-STD 461G.

strategies. Additionally, limited research is available to evaluate the performance of two-stage architectures for compliance with the more stringent MIL-STD-461G EMI requirements, which impose regulations starting at a lower frequency (10 kHz) as compared to 150 kHz in FCC-Part 15 or CISPR regulations, as shown in Fig. 1 [34], [35].

Paralleled converter operation is also preferred in many high power applications as it enables modularity and improved fault tolerance and reliability due to redundancy [36], [37]. Recently, various paralleling strategies have been proposed that utilize either centralized or decentralized control architectures to enable equal load current distribution among paralleled converter modules [38]–[47]. Centralized (or master–slave) control architectures allow high conversion efficiency and tight output voltage regulation [38], [39]. However, they suffer from lower overall system reliability due to a single master controller which in case of a fault acts as a single point of failure hence rendering the whole system inoperable. On the contrary, decentralized architectures utilize multiple autonomous power converter modules to ensure equal load current distribution. Such system architectures are beneficial as they do not result in full system failure in the case of a single fault in an individual module. Popular decentralized control architectures for power conversion systems utilizing multiple paralleled modules mainly comprise of a droop controller which varies the output voltage of a converter module based on the magnitude of its output current. Several output current-based droop control strategies are presented in the literature, which ensures equal output load current distribution while maintaining a stable output dc voltage [40]–[47]. However, these control strategies require output current sensing, which is challenging in isolated low-output-voltage high-power converters where large magnitudes of output currents are involved. Furthermore, limited research is available to evaluate the performance of droop controllers in two-stage isolated ac–dc conversion architectures, especially in low output voltage (under 48 V) applications.

This article presents a high-power-density high-efficiency soft-switched single-phase universal-input to 28-V isolated ac–dc converter module designed for parallel operation. The proposed two-stage converter utilizes a totem-pole bridgeless boost PFC converter stage followed by an isolated *LLC* resonant

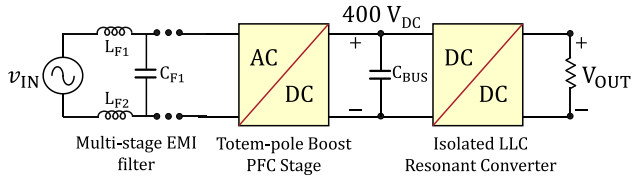

Fig. 2. Power conversion architectures considered in the design of the proposed two-stage ac–dc converter comprising a totem-pole bridgeless boost converter and an *LLC* resonant converter.

dc–dc converter stage and is designed to meet MIL-STD-461G EMI specifications. A comprehensive design methodology is presented, which compares various designs and operating modes for the power stages of the converter module and selects the optimal design based on the overall efficiency and power density. For the selected design, a control scheme is presented for the PFC stage which accounts for various sensor, control, and gate-drive delays to minimize input current distortion and achieve a high input power factor while operating under soft-switched boundary-conduction mode. Additionally, a new droop control strategy is presented to enable equal output current distribution between paralleled modules when powering a common output load. The proposed droop control strategy employs the input current of the *LLC* dc–dc conversion stage along with a variable droop resistance to minimize sensing complexity associated with conventional output-current-based droop control strategies. To validate the proposed design and control strategy, two 1-kW universal-input to 28-V isolated ac–dc converter modules are built and tested. Each prototype converter module achieves a high power density of 84 W/in^3 (5.126 W/cm^3) and a peak efficiency of greater than 93% while ensuring a current distribution error of less than 0.3% when operating in parallel to deliver the maximum output power of 2 kW.

The rest of this article is organized as follows. Section II presents the system design and optimization to maximize the overall power density and efficiency of the proposed ac–dc converter. Control strategy for the PFC stage and the droop control strategy for the *LLC* dc–dc stage are presented in Sections III and IV, respectively. Experimental results validating the operation of individual isolated ac–dc converter modules as well as their operation in parallel mode are presented in Section V. Finally, Section VI concludes this article.

II. System Design and Optimization

The architecture of the proposed two-stage ac–dc converter is shown in Fig. 2. It comprises a front-end totem-pole PFC ac–dc stage that is followed by an isolated *LLC* dc–dc stage. To obtain a high-power-density and high-efficiency converter, a design and optimization methodology is presented. The design methodology co-optimizes the volume and efficiency of the ac–dc converter by optimally selecting the operating modes of the PFC stage, the number of EMI filter stages across various operating modes (continuous conduction and boundary conduction), and switching frequencies. Moreover, a design approach for the *LLC* dc–dc stage is presented to maximize its efficiency by considering various topologies for its inverter and rectifier. For

TABLE I
SPECIFICATIONS OF THE ISOLATED AC–DC CONVERTER

Input Voltage	85-260 V_{rms}
Line Frequency	47-63 Hz
Output Voltage	28 V_{DC}
Maximum Output Voltage Ripple	560 mV_{pk-pk}
Output Power	1 kW
EMI Compliance	MIL-STD-461G

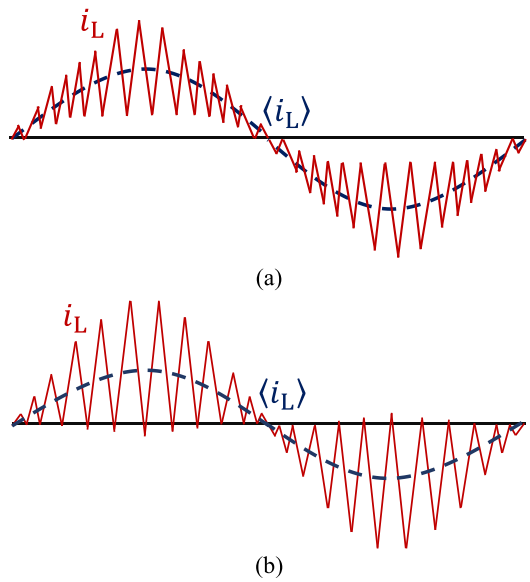

Fig. 3. Time exaggerated view of the instantaneous inductor current (solid red line) and average inductor current (dashed blue line) while the PFC stage is operating under (a) CCM and (b) BCM.

the overall ac–dc conversion system, all design optimizations are performed for the specifications listed in Table I.

A. Totem-Pole Boost PFC Stage Design

For the design of the totem-pole boost PFC stage, two operating modes are considered: continuous conduction mode (CCM) and boundary conduction mode (BCM). A time-exaggerated view of the inductor current in both these operating modes is shown in Fig. 3. During CCM operation, the inductor current has a smaller peak-peak ripple and rms value, but the PFC stage's switches would incur switching losses due to hard-switching. These switching losses include v–i overlap losses and output capacitance losses. In the case of BCM operation, the PFC stage switches will achieve zero-voltage switching (ZVS) resulting in negligible output capacitor losses and lower v-i overlap losses. However, the inductor current ripple and its rms value will be higher, which can lead to higher conduction losses in the switches and winding and core losses in the PFC inductor. Therefore, the PFC stage design strategy accounts for the tradeoffs

TABLE II
DESIGN SPACE FOR CCM PFC STAGE AND BCM PFC STAGE

CCM	Operating Frequency	100kHz -300kHz (increments of 5kHz)
	Peak Inductor Current Ripple	10% - 100% (increments of 5%)
	EMI Filter Stages	2, 3
	PFC Inductor Cores	RM14, PQ40/40, PQ50/50, PM50/39
BCM	Inductance	15µH - 50µH (increments of 1µH)
	EMI Filter Stages	2, 3
	PFC Inductor Cores	RM14, PQ40/40, PQ50/50, PM50/39

associated with both operating modes. Further details related to the loss model are presented in Appendix A.

The choice of PFC stage's operating mode also influences the required attenuation by the input EMI filter and affects its volume and efficiency. Therefore, the design strategy incorporates both the design of the input EMI filter and the PFC stage to achieve the overall optima in terms of efficiency and volume for the EMI filter and the PFC stage. As specified in Table I, the ac–dc converter needs to adhere to MIL-STD 461G EMI regulations. Therefore, the EMI filter design accounts for the noise limits specified by the solid-blue line in Fig. 1.

For the CCM operation, the optimization is performed across switching frequency and PFC inductor current ripple, which in turn determines the PFC inductance and the differential-mode (DM) EMI filtering requirements. For BCM operation, the optimization is performed across PFC inductance value, which in turn determines the operating frequency range of the PFC stage and the DM EMI filtering requirements. For the DM input EMI filter, multistage (2 and 3 stages) EMI filters are considered. For the efficiency estimation of the PFC stage, detailed loss models are developed, which estimate winding and core losses in the EMI filter and PFC inductors and switching and conduction losses in the PFC switches. Finally, a design space is defined for each of the above-mentioned operating modes and is shown in Table II. To only consider a design with inductor volume below a maximum limit, the minimum CCM operating frequency is kept at 100 kHz and the maximum PFC inductance for the BCM operation is kept at 50 μH. Several inductor cores are considered for both BCM and CCM designs including RM14, PQ40/40, PQ50/50, and PM50/39. The design space is constrained to only these cores to keep the maximum inductor temperature under 125 °C (setting a limit on the smallest core size) and to limit the occupied board area to 24 cm^2 (setting a limit on the largest core size). Furthermore, to limit the switching losses in the devices, the maximum CCM operating frequency is limited to 300 kHz. Moreover, owing to the limitation of

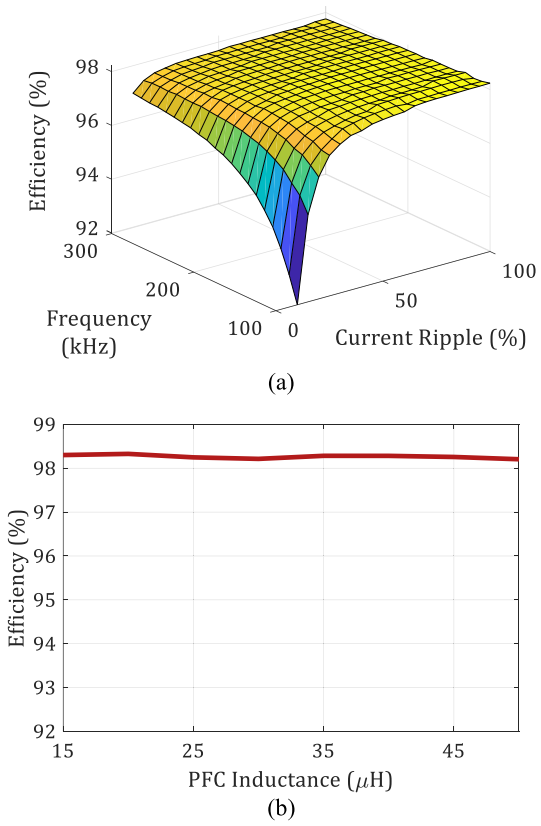

Fig. 4. Predicted efficiencies of the PFC stage and EMI filter under (a) CCM operation and (b) BCM operation.

sensing circuitry and digital controller, the maximum operating frequency for BCM operation is limited to 1 MHz (at high-line input voltage), and therefore the minimum inductance in the soft-switched design is kept at 15 μH.

The results of the optimization are shown in Fig. 4. Fig. 4(a) shows the estimated efficiency of the converter for the CCM design across the range of switching frequency and inductor current ripple specified in Table II. As can be seen from Fig. 4(a), the CCM designs with lower peak current ripple and operating frequencies have lower efficiencies. This is due to the higher PFC inductance requirement for such low current ripple values, which leads to higher winding losses for a given maximum volume limit on the PFC inductor. Fig. 4(b) shows the efficiency for the BCM design across the PFC inductance range specified in Table II. The efficiency of the PFC stage remains relatively flat as a function of PFC inductance. This is due to the reason that the optimization process selects a different inductor core for each of the designed inductances while still ensuring that the height of the PFC stage and EMI filter does not exceed the maximum limit (to preserve a high power density).

The volume (of the EMI filter and PFC inductor) and efficiency for each of the considered BCM and CCM design is computed and displayed in Fig. 5(a) and (b), respectively. As can be seen from the figures, the efficiency tends to increase as the volume of the PFC stage increases. The Pareto optimal designs (i.e., the designs that provide the best achievable tradeoff between efficiency and volume) are extracted from Fig. 5(a) and

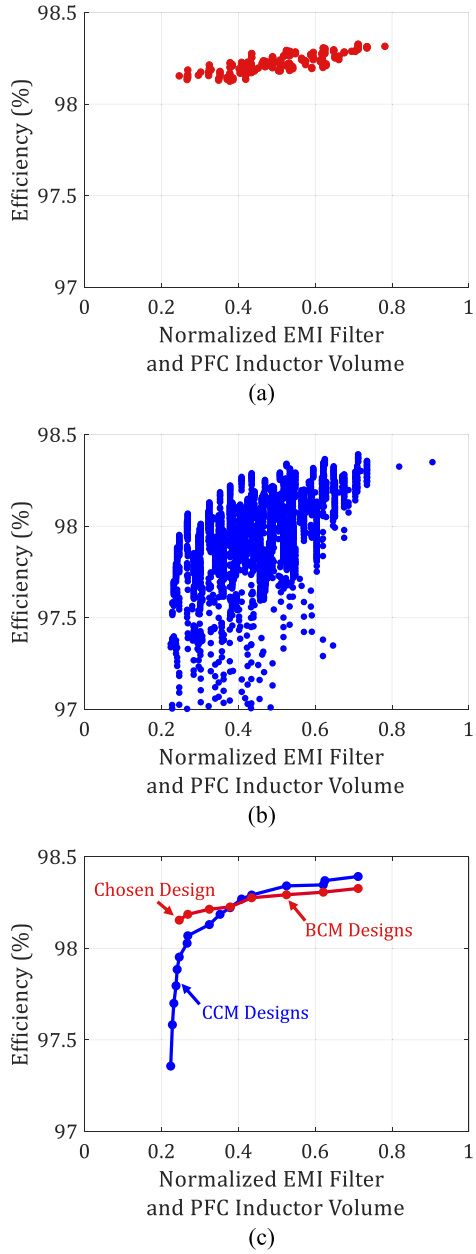

Fig. 5. Efficiencies and normalized volumes of designs evaluated for isolated ac–dc converter. (a) Designs considered for BCM operation. (b) Designs considered for CCM operation. (c) Pareto optimal designs for BCM and CCM operations.

(b) and are shown in Fig. 5(c) for both BCM and CCM designs. As can be seen from Fig. 5(c), BCM designs are superior to CCM designs in terms of efficiency at small volumes, whereas CCM designs are superior to BCM designs in terms of efficiency at larger volumes. From the Pareto optimal designs shown in Fig. 5(c), the design with the smallest volume and efficiency greater than 98% is chosen for the final prototype as indicated in Fig. 5(c). The selected design utilizes a 15 μH PFC inductance, has a three-stage EMI filter, and operates under BCM.

For the chosen design of the PFC stage, the switching frequency range is also computed and is given in Fig. 6. The switching frequency of the BCM controlled PFC stage is a

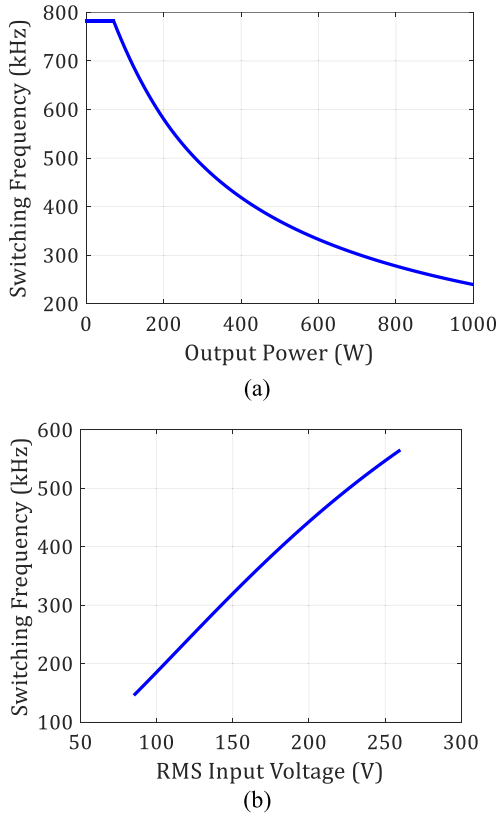

Fig. 6. Maximum switching frequency of the PFC stage with an inductance of 15 μH while operating under BCM (a) as a function of output power when a 120-V_{rms} input voltage is applied and (b) as a function of rms input voltage when powering a 1-kW load.

function of the input voltage and output power. Fig. 6(a) shows the maximum switching frequency of the PFC stage as a function of output power when it is powered from a 120-V_{rms} input ac line. As can be seen, the switching frequency falls as the load is increased. Moreover, for loads below 70 W, the switching frequency of the converter is clamped at 780 kHz and below this power level, the PFC stage is designed to operate in burst mode. Fig. 6(b) shows the maximum switching frequency of the PFC stage as a function of rms input voltage when powering a 1-kW load. As can be seen, the switching frequency of the PFC stage increases with the input voltage. The reason is the lower average (and peak) inductor currents and higher volt–seconds applied across the PFC inductor at higher input voltages. Both these effects result in a lower ON-time for the PFC stage at the higher input voltages. The OFF-time also reduces as the inductor current takes less time to discharge to zero. This results in a decrease in the switching period (ON-time + OFF-time) and an increase in switching frequency of the PFC stage as the input voltage increases.

To understand the impact of MIL-STD EMI regulations, relative to FCC and CISPR regulations, on the volume and efficiency of the PFC stage and the EMI filter, we have also utilized our optimization methodology to determine Pareto optimal designs that target FCC and CISPR EMI regulations. The Pareto optimal designs for totem-pole bridgeless boost PFC operating under

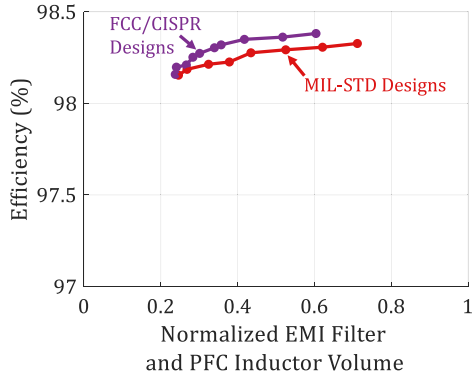

Fig. 7. Comparison of Pareto optimal designs of totem-pole boost PFC ac–dc converters operating in BCM targeting either FCC/CISPR or MIL-STD EMI regulations.

BCM and targeting either FCC/CISPR or MIL-STD EMI regulations are shown in Fig. 7. As can be seen from this figure, it is easier to meet FCC/CISPR EMI regulations than MIL-STD EMI regulations, as the FCC/CISPR compliant Pareto optimal designs have a smaller volume and/or higher efficiency than the MIL-STD compliant designs. It is interesting to note, that all the FCC/CISPR compliant Pareto optimal designs shown in Fig. 7 operate at switching frequencies under 150 kHz, whereas most of the MIL-STD compliant Pareto optimal designs have switching frequencies that exceed 150 kHz. This is understandable, as FCC/CISPR regulations impose no restrictions on emissions below 150 kHz.

B. LLC DC–DC Stage Design

The dc–dc stage of the isolated ac–dc converter needs to step down the 400-V dc bus voltage to 28 V required by the load. For the *LLC* dc–dc stage optimization, various inverter and rectifier topologies are considered as shown in Figs. 8 and 9, respectively. For each of these inverter and rectifier combinations, the resonant tank is designed based on the optimization methodology presented in [48]. During the design process, only GaN transistors are considered for the inverter switches owing to their lower output capacitance compared to Si-MOSFETs. This facilitates ZVS with minimal circulating currents, thereby reducing conduction losses in the inverter switches and winding losses in the *LLC* transformer and resonant inductor. Moreover, this enables higher switching frequency operation of the *LLC* dc–dc stage, and, therefore, the *LLC* dc–dc stage is designed to operate across a switching frequency range of 300 kHz to 1 MHz.

For the *LLC* inverter, three topologies were considered as shown in Fig. 8. A full-bridge inverter topology is shown in Fig. 8(a). Each half-bridge leg in this topology operates at 50% duty ratio and out of phase with each other. This produces a square wave at the input of the *LLC* resonant tank with voltage in the range of $+V_{BUS}$ and $-V_{BUS}$. For the converter specifications listed in Table I, a half-bridge inverter can also be utilized and is shown in Fig. 8(b). This inverter operates with a 50% duty ratio generating a square-wave voltage in the range of $+V_{BUS}$ and 0 at the input of the resonant tank. This results in

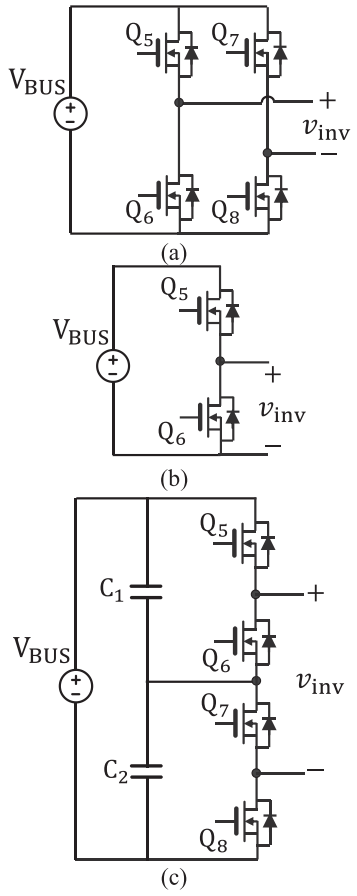

Fig. 8. Inverter circuit topologies considered for the design of the *LLC* dc–dc stage. (a) Full-bridge inverter. (b) Half-bridge inverter. (c) Variable frequency multiplier (VFX).

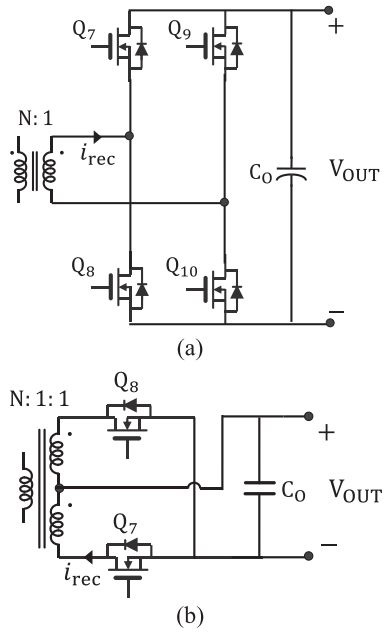

Fig. 9. Rectifier circuit topologies considered for the design of the *LLC* dc–dc stage. (a) Bridge rectifier. (b) Full-wave rectifier.

a natural step down of the dc bus voltage by a factor of two as compared to the full-bridge inverter and reduces the step-down burden on the *LLC* dc–dc stage. Moreover, this topology has one switch in series with the tank current, which can lead to a lower overall conduction loss in the *LLC* dc–dc stage. Fig. 8(c) shows a variable-frequency-multiplier (VFX) topology for *LLC* inverters [49], [50]. This topology utilizes two stacked capacitors at the input with a half-bridge connected across each capacitor. With appropriate control of the switches, the voltage across each half-bridge is reduced by a factor of two, thereby allowing low voltage rated switches to be used. The VFX also operates at half switching frequency as compared to the other two inverter topologies which reduces the turn-OFF losses associated with each inverter switch. Moreover, the inverter topology provides a step-down of the dc bus voltage by a factor of two as compared to the half-bridge inverter (factor of four if compared with a full-bridge inverter) which reduces the step-down burden on the *LLC* dc–dc stage and its transformer. However, the topology requires two switches to come in series with the resonant tank current which can increase the overall conduction loss. The choice of inverter topology also affects the voltage rating of the *LLC* resonant capacitor, where a full-bridge inverter will result in the lowest voltage rating and half-bridge inverter will require the highest voltage rating capacitor. However, the difference in the size of the resonant capacitor will have minimal impact on the volume of the overall converter and therefore this effect is considered negligible during the optimization of the *LLC* converter. To estimate the efficiency of the *LLC* dc–dc stage, conduction, turn-OFF, and gate-drive losses are computed for each of these inverter implementations and are summarized in Fig. 10(a) for the best-in-class commercially available GaN transistors. As can be seen from the figure, conduction loss is the most dominant loss mechanism in the *LLC* inverter topologies. Based on the loss calculations, the half-bridge inverter results in the lowest overall inverter loss. Therefore, the half-bridge inverter topology is chosen for the final *LLC* dc–dc stage implementation.

Similarly, two topologies are considered for the *LLC* rectifier as shown in Fig. 9. Fig. 9(a) shows a bridge rectifier comprising four switches with switches Q_8 and Q_9 operating in-phase and switches Q_7 and Q_{10} operating in-phase, depending on the direction of rectifier input current $i_{\rm rec}$. A full-wave rectifier topology is also considered for the proposed converter and is shown in Fig. 9(b). This topology utilizes two switches, each blocking twice the voltage as compared to the switches in a full-bridge rectifier. This type of rectifier also requires a dual-secondary center-tapped winding architecture of the *LLC* transformer where each secondary winding only conducts during a half switching period of the *LLC* dc–dc stage. An advantage of this topology is that the rectifier switches can be driven using two low-side gate drivers reducing gate drive complexity.

Based on the specifications of the *LLC* dc–dc stage, conduction and gate-drive losses for each of the two rectifier topologies are computed and compared. Moreover, while designing the rectifiers, several GaN transistors and Si-MOSFETs were considered and the type of device with the best overall performance was used for loss analysis. Based on this analysis, it is observed that even though Si-MOSFETs have higher gate-drive

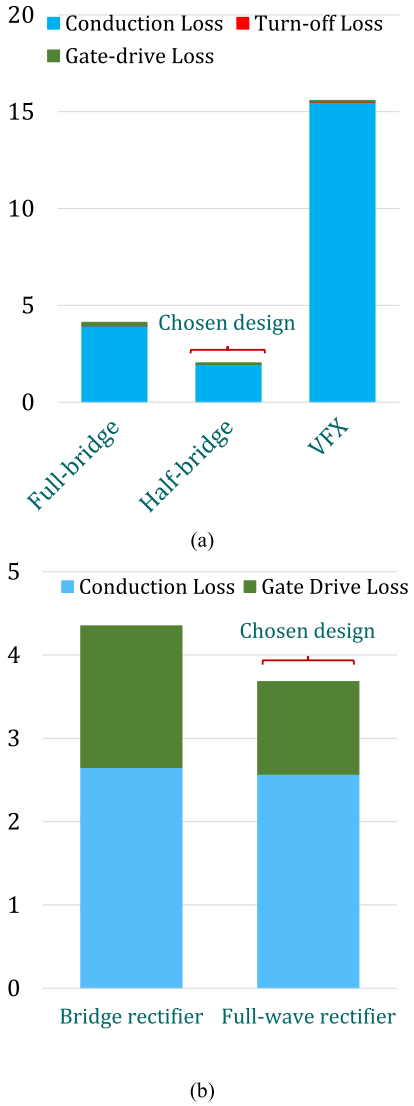

Fig. 10. Losses in the *LLC* resonant dc–dc converter while converting a 400-V dc bus voltage to 28-V output voltage to power a 1-kW load. (a) Inverter losses. (b) Rectifier losses.

losses, they result in better performance because of their lower ON-state resistance, lower source–drain forward voltage drop (0.9 V versus 1.5 V), and better thermal characteristics for both rectifier topologies. A summary of the losses in both rectifier topologies is shown in Fig. 10(b). As can be seen from the figure, the gate-drive losses account for a substantial portion of the overall rectifier losses. Based on the computations, the full-wave rectifier implementation shown in Fig. 9(b) is found to be the most efficient among the two rectifier topologies and is therefore chosen for final *LLC* implementation. The optimal *LLC* implementation comprises a half-bridge inverter and a full-wave rectifier.

The final topology of the end-to-end isolated ac–dc converter is shown in Fig. 11. In this design, a three-stage DM EMI filter is utilized (with $L_1 = L_2 = L_3 = 11\ \mu$H and $C_1 = C_2 = C_3 = 1\ \mu$F) to attenuate the input current noise.

III. PFC Controller Implementation

A digital controller based BCM control is utilized for the soft-switched totem-pole boost PFC stage. To ensure BCM operation of the PFC stage, a zero-current detection (ZCD) circuit is utilized, which generates a trigger when the inductor current crosses the zero-current mark. The trigger is sensed by the controller to turn-OFF the synchronous switch (Q_2 when the input voltage is positive, and Q_1 when the input voltage is negative, according to the circuit illustrated in Fig. 11) and start the next switching cycle. In an ideal case, when ZCD sensor, control, and gate drive delays are negligible, the inductor current resembles a waveshape as shown in Fig. 3(b). In this case, the PFC stage's high-frequency switches (Q_1 and Q_2) naturally achieve ZVS when the inductor current is brought to zero at the end of the switching period and input voltage v_{IN} satisfies $v_{IN} < V_{BUS}/2$. However, for input voltages greater than $V_{BUS}/2$, the synchronous switch (Q_2 when input voltage is positive and Q_1 when input voltage is negative) needs to be kept on for an additional duration of time beyond the zero crossing of the instantaneous inductor current to allow inductor current to build to a minimum value given by

$$i_{ZVS} \leq -\sqrt{\frac{2C_{OSS}}{L_{PFC}} V_{BUS} \left(2\left|v_{IN}\right| - V_{BUS}\right)} \tag{1}$$

where C_{OSS} is the output capacitance of the boost switches, L_{PFC} is the PFC inductance, V_{BUS} is the instantaneous dc bus voltage, and v_{IN} is the instantaneous input voltage [51], [52]. Given this constraint, the ZCD circuit trigger is set such that the boost switches achieve full ZVS across the entire input voltage line cycle.

In practice, a delay is also present in the ZCD sensing circuit, digital controller, and gate drive. This delay results in an extra build-up of reverse current flowing through the inductor than is required to achieve ZVS. This extra inductor current is given by

$$i_{extra} = -\frac{V_{BUS} - |V_{IN}|}{L_{PFC}} T_{delay} \tag{2}$$

where T_{delay} is the cumulative sensor, control, and gate drive delay. As is evident from (2), the effect of this delay is most prominent when the input voltage is low since the voltage across the PFC inductor is highest. If this delay is ignored during the design of the BCM controller, it causes the average inductor current to fall, as illustrated in Fig. 12(a) [53]. As can be seen from the figure, at instantaneous input voltage magnitudes below a certain value, the product of input voltage v_{IN} and input current $\langle i_L \rangle$ is negative and the instantaneous input power is being transferred back toward the input voltage source increasing circulating currents and causing higher conduction losses. To mitigate this effect, the PFC converter is generally switched-OFF at such low input voltages introducing dead bands in the inductor current. Fig. 12(b) shows the inductor current i_L and its average value $\langle i_L \rangle$ in the presence of such dead bands. As can be seen, these dead bands introduce distortion in the input current waveshape and consequently affect the input current total harmonic distortion (THD) and power factor.

To preserve a good input current waveshape and to improve the input power factor in the presence of sensor, control, and

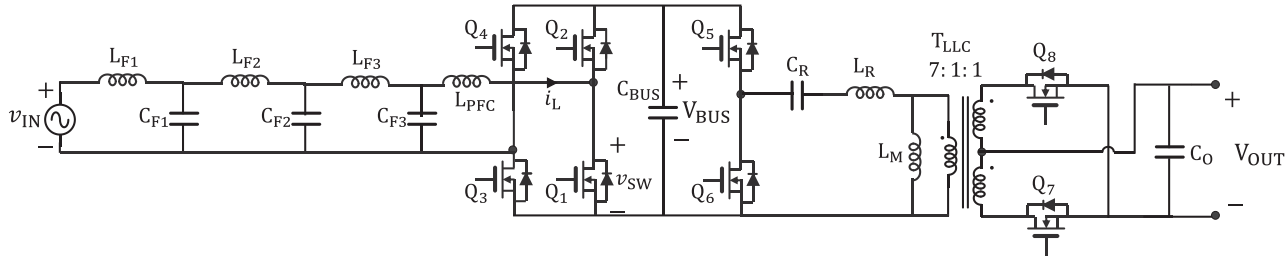

Fig. 11. Final topology of the isolated ac–dc converter.

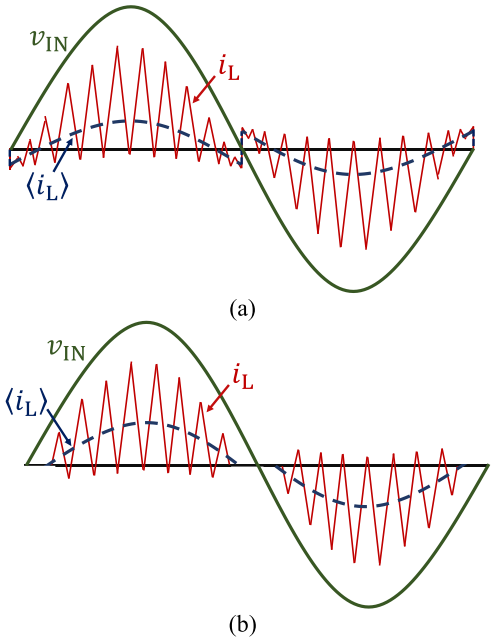

Fig. 12. Time exaggerated view of PFC stage's inductor current i_L and its average value $\langle i_L \rangle$ while it is operating under BCM (a) in the presence of sensor, control, and gate drive delays, and (b) when dead bands are introduced at low input voltages causing distortion in the input current waveshape.

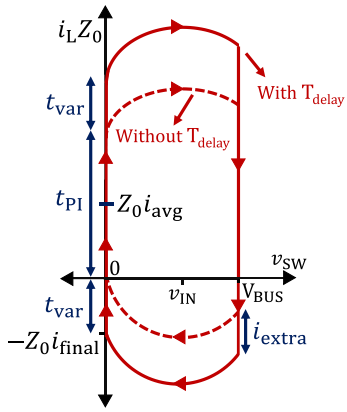

Fig. 13. State-plane diagram of a boost converter without any delays T_{delay} (dotted red line) and in the presence of delays T_{delay} with the proposed PFC control strategy (solid red line). Here, Z_0 is given by $\sqrt{\frac{L_{PFC}}{2C_{OSS}}}$ and i_L and v_{SW} are state parameters.

gate drive delays, a new PFC control strategy is also presented in this article. The new PFC control strategy considers the delays and the resultant extra inductor current in the PFC inductance i_{extra} and based on this information, computes the ON-time for the boost main switch (Q_1 when the input voltage is positive and Q_2 when the input voltage is negative). Fig. 13 shows the state plane diagram of the inductor current and the switch-node voltage for a boost converter. As can be seen, in the presence of delays T_{delay}, an additional ON-time given by $t_{ON,extra} = 2t_{var}$ is needed to maintain the average inductor current at its required value. This additional time ($t_{ON,extra}$) is a function of input and dc bus voltages as well as PFC circuit resonant parameters and is given by

$$t_{ON,extra} = \frac{2\sqrt{2L_{PFC}C_{OSS}}}{|v_{IN}|}\sqrt{V_{BUS}^2 - 2V_{BUS}|v_{IN}| + \frac{i_{min,B}^2 L_{PFC}}{2C_{OSS}}} \quad (3)$$

where $i_{min,B}$ is given by

$$i_{min,B} = |i_{extra}| + |i_{ZCD}| \quad (4)$$

where i_{ZCD} is the current level at which the ZCD circuit is configured to generate a trigger. Fig. 14(a) shows the extra ON-time $t_{ON,extra}$ required to maintain the input current waveshape while the PFC stage is operating at $120V_{rms}$, and the dc bus is regulated at 400 V. As can be seen from the figure, $t_{ON,extra}$ varies inversely with the input voltage. Accurately computing this additional ON-time $t_{ON,extra}$ based on (3) will substantially increase the controller computational overhead, which will affect the control complexity.

To overcome this hurdle, this article proposes a simpler implementation for this additional ON-time based on a curve fit approximation. The curve fit utilized is of the form $t_{ON,extra} \approx \alpha/v_{IN} + \beta$, where the constants α and β can be found by curve fitting the ON-time plot of Fig. 14(a). Fig. 14(b) shows the error between the actual and curve-fitted $t_{ON,extra}$ values. As can be seen, the percentage error remains below 8.5% across the full input voltage line cycle. Also, the error remains below 1% at low voltage values (near zero crossing of the input voltage where the effect of delay T_{delay} is most prominent), resulting in a negligible difference between actual and curve-fitted $t_{ON,extra}$ values. The overall control architecture of the PFC stage is summarized in Fig. 15. As can be seen, the effective ON-time of the main switch is given by $t_{ON} = t_{PI} + t_{ON,extra}$. Here, t_{PI} regulates the output power of the PFC stage and is generated by a low-bandwidth dc bus voltage control loop and $t_{ON,extra}$ helps maintain the

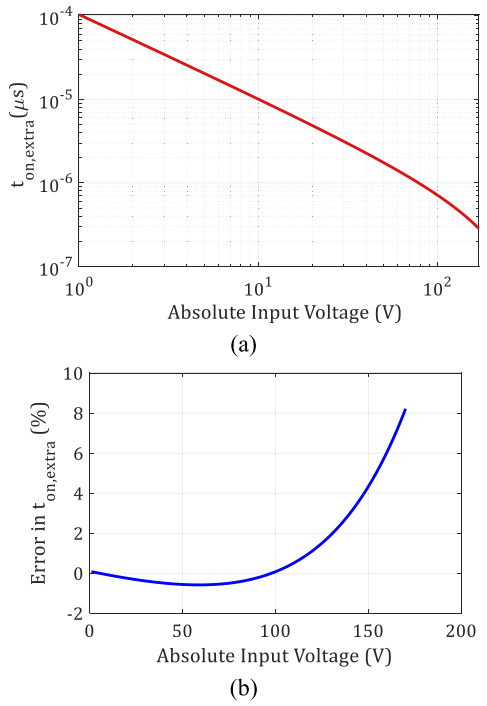

Fig. 14. Compensation needed to mitigate the effect of sensor, control, and gate drive delay, T_{delay}, when operating at an input voltage of 120V_{rms} and a dc bus voltage of 400 V. (a) Extra ON-time required to restore input current waveshape. (b) Percentage error between the exact and curve-fitted extra ON-time for the PFC stage for $\alpha = 104\ \mu\text{Vs}$ and $\beta = 327$ ns.

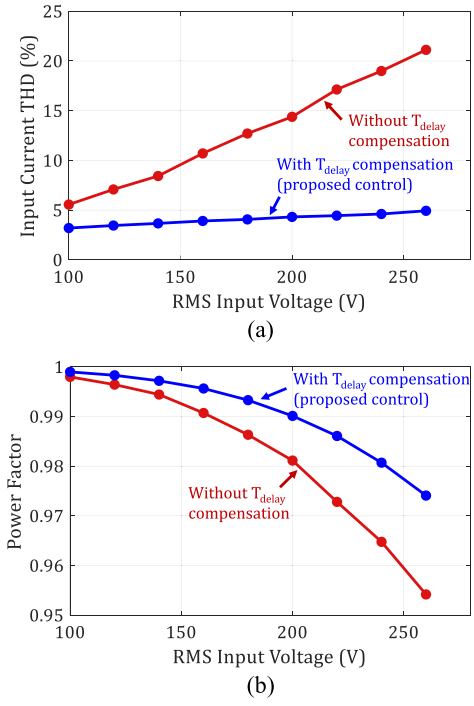

Fig. 16. Performance of the BCM totem-pole boost PFC stage operating at 1-kW output power as a function of input voltage in the presence of sensing, control, and gate-drive delay T_{delay} with and without delay compensation in the PFC control loop. (a) Input current THD. (b) Input power factor.

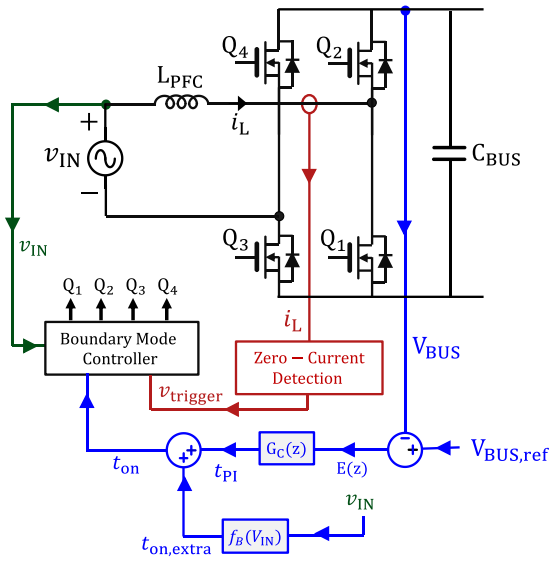

Fig. 15. Proposed control architecture for the totem-pole boost PFC stage.

waveshape of the average input current by compensating for sensor, control, and gate drive delay (T_{delay}).

The proposed PFC control strategy is simulated in PLECS to investigate the effect of T_{delay} on the input current THD and the input power factor. Fig. 16 shows the input current THD and input power factor as a function of rms input voltage in the presence of T_{delay} while the converter is powering a 1-kW load. As can be seen, the performance of the PFC stage improves considerably with the proposed control (with the T_{delay} compensation) and the converter maintains an input current THD of less than 5% and an input power factor of greater than 0.97 across the entire input voltage range. Based on the collected data, a THD reduction of at least 42% can be achieved if the proposed T_{delay} compensation is incorporated in the control of the PFC stage.

The EMI compliance of the proposed ac–dc converter is also evaluated while utilizing the proposed PFC control strategy in the optimized ac–dc converter design of Section II. The MIL-STD-461G EMI compliance is typically evaluated at 115V_{rms} line voltage with noise limits shown in solid-blue line on Fig. 17(a). Moreover, at the high-line (260V_{rms} input voltage) the noise limits are relaxed by 9 dBμV as indicated by dotted red line in Fig. 17(b). As can be seen from the figures, the proposed ac–dc converter design meets the MIL-STD-461G noise limits while utilizing the optimized DM EMI filter of the PFC stage for both nominal (115V_{rms}) and high-line (260V_{rms}) ac input voltages.

IV. *LLC* Input Current Based Droop Controller

The *LLC* dc–dc converter stage provides galvanic isolation and regulates the output voltage of the proposed ac–dc converter at 28V. Therefore, the *LLC* controller must comprise an output voltage controller similar to those discussed in [54] and [55]. Additionally, the proposed ac–dc converter also needs to operate in parallel with multiple other similar modules to accommodate a higher output power than the maximum rating of each individual module. While several off-the-shelf *LLC* controller ICs exist which can provide output voltage regulation in *LLC* converters,

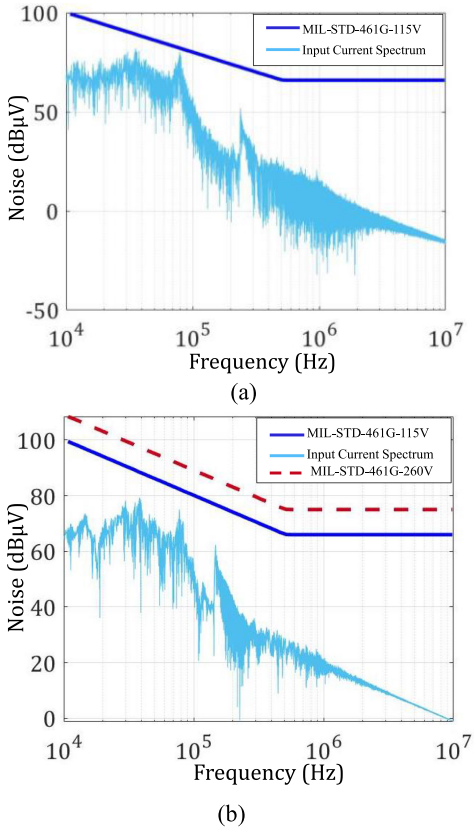

Fig. 17. Input current harmonic spectrum with the MIL-STD-461G requirements at (a) 115V_{rms} and (b) 260V_{rms} input ac voltages.

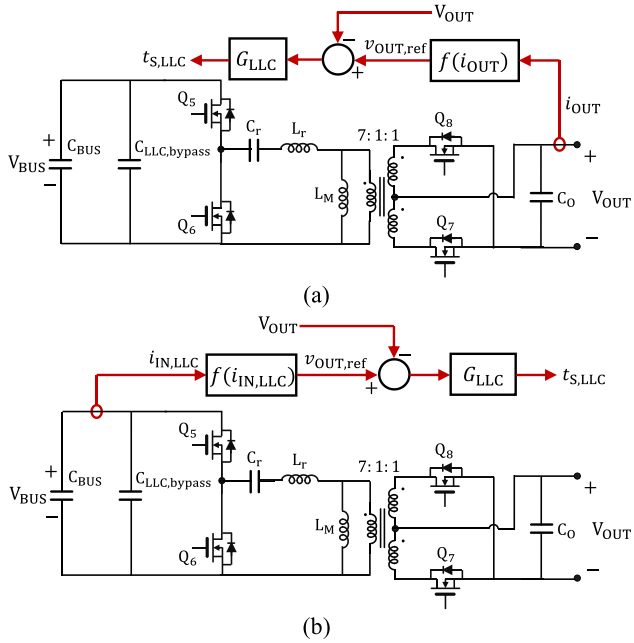

Fig. 18. Droop control architecture for *LLC* dc–dc stage. (a) Conventional output current based droop control. (b) Proposed input current based droop control strategy.

at the time of this research, none of the *LLC* controllers support parallel operation of *LLC* converters. Therefore, this article also presents a new droop control strategy to achieve parallel operation of multiple *LLC* dc–dc (and hence isolated ac–dc) converters. The proposed droop control strategy varies the output voltage of the *LLC* dc–dc stage based on its output power.

A control architecture for a conventional output-current based droop controller is shown in Fig. 18(a). In the conventional droop control strategy, the output current is sensed by the controller and the reference for the output voltage $v_{\text{OUT,ref}}$ is computed based on the following control law:

$$v_{\text{OUT,ref}}\ (t) = V_{\text{OUT,max}} - i_{\text{OUT}}\,(t)\,R_{\text{droop}} \tag{5}$$

where $V_{\text{OUT,max}}$ is the maximum output voltage corresponding to no-load at the output port, $i_{\text{OUT}}(t)$ is the instantaneous output current, and R_{droop} is the virtual droop resistance given by

$$R_{\text{droop}} = \Delta V_{\text{OUT}}/\Delta I_{\text{OUT}} \tag{6}$$

where ΔV_{OUT} is the maximum allowable variation in the output voltage, and ΔI_{OUT} is the maximum variation in output current across the full output power range of the converter. As can be seen from (5), if a module is delivering higher output current i_{OUT} than other modules in its parallel, its droop controller will reduce the voltage reference $v_{\text{OUT,ref}}$ to its voltage control loop thereby limiting the amount of power being processed by the module. This shifts the power delivery burden to other parallel modules, which increase their output current eventually enabling equal current (and output power) distribution in the system. To implement this control strategy, an additional output current sensor is required for the conventional droop control strategy. In high-power step-down isolated ac–dc power converters, the high output current is often challenging to sense. This is because of the power losses in the sensing circuitry, e.g., sensing resistor used in current-shunt monitors or primary conductor present in hall effect sensors. To reduce these power losses, the resistance of the current sense resistor or primary conductor is kept low, which impacts the sensitivity of the sensor (in mV/A) [56]. Several techniques are employed to restore the sensitivity of the sensor while incurring low power losses, however, such techniques require additional amplification circuitry which increases the cost of the sensor and its circuit complexity [56]–[59]. Moreover, to implement an output current based droop control using a digital controller on the primary side of the *LLC* transformer, the sensed output current information needs to be conveyed to the primary side. Therefore, an isolated current sensor is required which needs to meet the same isolation rating as the *LLC* transformer. This is especially pertinent if the isolated ac–dc converter is being designed for certain military or medical applications which require reinforced isolation, e.g., up to $5000\text{V}_{\text{rms}}$ in UL 1577. Therefore, the use of an isolated current sensor for output-current-based droop control in such applications further introduces implementation challenges and cost concerns for high-volume design.

To overcome these challenges, a new *LLC* input current based droop control strategy is proposed in this article which estimates the magnitude of the output current of the *LLC* dc–dc stage by instead sensing its input current. This is beneficial as the input current is much lower in magnitude than the output current and therefore simpler current sensing techniques can be leveraged

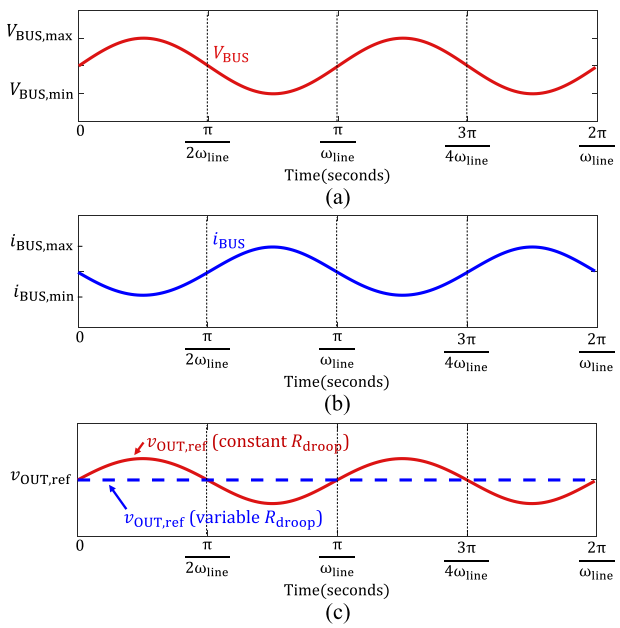

Fig. 19. Effect of twice-line-frequency dc bus voltage ripple on the output voltage reference of the *LLC* dc–dc stage's input current based droop controller: (a) dc bus voltage, (b) second-stage input current, and (c) output voltage reference with constant droop resistance (solid red line) and with the proposed variable droop resistance (dotted blue line).

[56]. Also, the input current of the *LLC* dc–dc stage can be sensed with respect to the controller ground (located at the primary side of the *LLC* isolation transformer) by either using a simple current shunt sensor or low current hall effect sensor. Therefore, it does not interfere with the above-specified isolation constraints. The control architecture for the proposed *LLC* input current based droop control strategy is shown in Fig. 18(b). Based on this architecture, the output current of the *LLC* dc–dc stage is given by

$$i_{\text{OUT}}(t) = \frac{i_{\text{IN},LLC}(t)\,\eta_{LLC}}{H_{LLC}} \tag{7}$$

where $i_{\text{IN},LLC}(t)$ is the instantaneous input current, η_{LLC} is the efficiency, and H_{LLC} is the conversion ratio of the *LLC* dc–dc stage given by $V_{\text{OUT,nominal}}/V_{\text{BUS,nominal}}$. The control law for the input current based droop controller is given by

$$v_{\text{OUT,ref}}(t) = V_{\text{OUT,max}} - \frac{i_{\text{IN},LLC}(t)\,\eta_{LLC}}{H_{LLC}}.R_{\text{droop}}. \tag{8}$$

The above-mentioned control law is adequate if the *LLC* dc–dc stage exhibits a constant conversion ratio, i.e., if *LLC* is connected to a constant dc bus voltage. However, in two-stage ac–dc converters, a twice-line-frequency voltage ripple appears across the dc bus due to the PFC operation performed by the front-end PFC stage, as shown in Fig. 19(a). Since the *LLC* dc–dc stage is regulating its output voltage, its output power and hence its input power will be constant given the load impedance is unchanged. Consequently, any increase (or decrease) in the *LLC* dc–dc stage's input voltage (i.e., the dc bus voltage v_{BUS}) will result in a decrease (or increase) in the input current of the *LLC* dc–dc stage ($i_{\text{IN},LLC}$), as shown in Fig. 19(b). Since the output voltage reference $v_{\text{OUT,ref}}$, as given in (8), depends on the instantaneous value of the *LLC* input current $i_{\text{IN},LLC}$, any variation in $i_{\text{IN},LLC}$ will cause a similar variation in $v_{\text{OUT,ref}}$. This phenomenon is shown in Fig. 19(c) in solid red line. The ripple in $v_{\text{OUT,ref}}$ observed in Fig. 19(c) will also appear in the output dc voltage V_{OUT}. Such a ripple is unacceptable in many point-of-load converters as most applications demand a stable output dc voltage with a very small steady-state ripple. Moreover, in parallel operation, such a ripple in the output voltage can cause currents to flow between modules resulting in increased circulating currents and related losses. To overcome this constraint, a variable droop resistance is utilized which varies in magnitude based on the instantaneous conversion ratio of the *LLC* dc–dc stage ($v_{\text{OUT}}/v_{\text{BUS}}$). This compensates for the twice-line-frequency ripple in the input current of the *LLC* dc–dc stage and helps ensure a stable output dc-voltage. The variable droop resistance is given as follows:

$$r_{\text{d,control}}(t) = \frac{\eta_{LLC} R_{\text{droop}} v_{\text{BUS}}(t)}{v_{\text{OUT}}(t)} \tag{9}$$

and the control law for the proposed droop control method is given as follows:

$$v_{\text{OUT,ref}}(t) = V_{\text{OUT,max}} - i_{\text{IN},LLC}(t).r_{\text{d,control}}(t). \tag{10}$$

With the *LLC* dc–dc stage regulating the dc output voltage, any increase in the instantaneous dc bus voltage will result in a decrease in the instantaneous input current of the *LLC* dc–dc stage. In such a case, with the proposed control law, the variable droop resistance will be increased by the same factor to cancel the effect of the reduced input current and result in a constant output voltage reference for the *LLC* output voltage control loop. On the contrary, a decrease in the dc bus voltage will increase the input current of the *LLC* dc–dc stage and a decrease in the variable droop resistance again leading to a constant output voltage reference. The dotted blue line in Fig. 19(c) shows the output voltage reference of the *LLC* dc–dc stage with the proposed variable droop resistance based control in the presence of the twice-line-frequency ripple in the dc bus voltage. As can be seen from Fig. 19(c), the proposed control strategy results in a constant voltage reference for the *LLC* output voltage control loop and hence eliminates the effect of the twice-line-frequency dc bus voltage ripple to ensure a stable output voltage across the load.

To evaluate the stability criteria of the proposed input current based droop control, an analytical model is also developed. Based on the analysis, the proposed droop controller is stable if R_{droop} is smaller than the load resistance. Therefore, this constraint needs to be considered when designing the droop resistance. The detailed analysis and derivation of the stability criteria are provided in Appendix B.

V. Prototype Design and Experimental Results

A 1-kW prototype ac–dc converter, based on the specifications of Table I , utilizing the optimized design and proposed control schemes is built and tested. A photograph of the prototype is

Fig. 20. Photograph of the prototype 1-kW universal input to 28-V isolated soft-switched ac–dc converter, which achieves a power density of 84 W/in^3 (5.13 mW/mm^3).

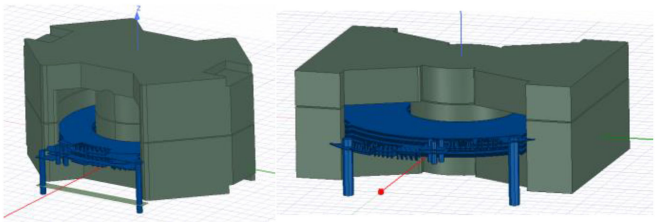

Fig. 21. 3-D images of magnetics used in the proposed ac–dc converter: (a) PFC inductor utilizing a planar RM core. (b) *LLC* transformer utilizing a modified PQ core.

shown in Fig. 20. The prototype converter achieves an overall power density of 84 W/in^3 (5.13 W/cm^3). The converter utilizes low-profile magnetic cores with planar winding to implement the PFC inductor and *LLC* transformer as shown in Fig. 21. The magnetics design is optimized in a 3-D finite-element-modeling software (Ansys HFSS) to maximize efficiency. The PCB stack-up for the planar magnetics is shown in Fig. 21. A 4 oz. copper eight-layer PCB is utilized to implement seven turns of the PFC inductor and two 4 oz. copper eight-layer PCBs are used to implement the interleaved primary and secondary turns of the *LLC* transformer as shown in Fig 22(a) and (b), respectively. A 200-MHz 32-bit digital controller is utilized to implement the closed-loop control in the PFC and the *LLC* dc–dc stage of the converter. The ZCD circuitry used to ensure BCM operation in the PFC controller is shown in Fig. 23. The circuit utilizes a current sense resistor in series with the PFC inductor. The voltage drop across this resistor is amplified using a high-bandwidth voltage amplifier circuit and the output of the amplifier is fed to high-speed comparators to generate two triggers when the inductor current crosses zero. Each trigger is utilized in either the positive or negative half-line cycle of the input ac voltage and resets the PWM counter in the digital controller. For sensing the input current of the *LLC* dc–dc stage, a hall effect sensor is connected between positive terminal of the dc bus capacitor and the *LLC* inverter switch Q_5. Further details about the components used in the prototype ac–dc converter are listed in Table III.

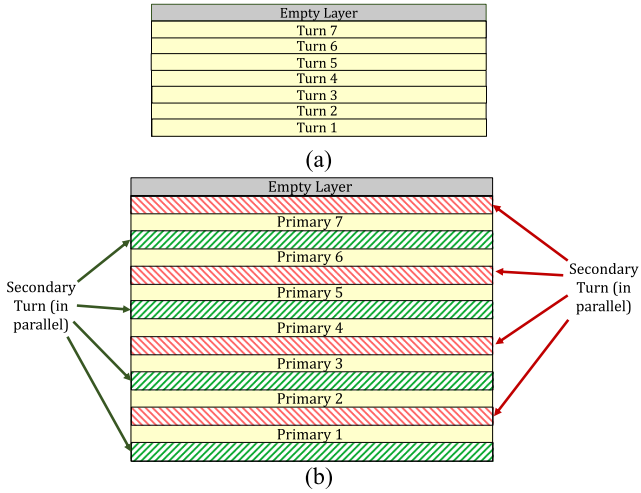

Fig. 22. PCB stack-up for the planar magnetics. (a) Planar PCB to implement seven turns of PFC inductor. (b) Planar PCB to implement 7:1:1 turns ratio in *LLC* transformer.

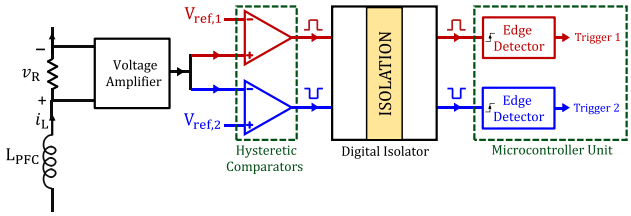

Fig. 23. ZCD circuit used to ensure BCM operation of the PFC stage.

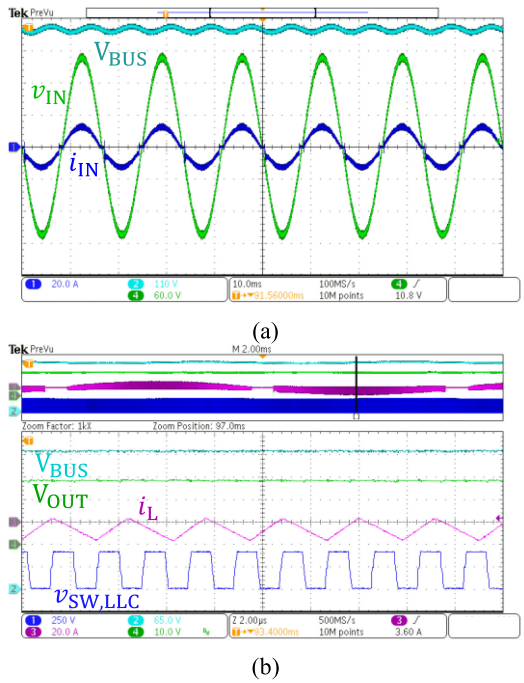

Fig. 24. Experimentally measured steady-state waveforms of the converter. (a) Input voltage (60 V/div), input current (20 A/div), and dc bus voltage of the PFC stage (110 V/div). (b) DC bus voltage (65 V/div), PFC inductor current (20 A/div), *LLC* switch-node voltage (250 V/div), and *LLC* output voltage (10 V/div), when a 120V_{rms} ac voltage is applied to the input of the converter.

TABLE III
COMPONENTS USED IN THE PROTOTYPE ISOLATED AC–DC CONVERTERS

Component	Value	Description
C_{F1}, C_{F2}, C_{F3}	1μF	275-V Polypropylene X2 film capacitor
L_{F1}, L_{F2}, L_{F3}	11μH	Magnetics Inc. 125u core, 20 turns
S_1, S_2, S_5, S_6	–	650-V, 60-A GaN E-HEMT
S_3, S_4	–	600-V, 75-A Si MOSFET
S_7, S_8	–	80-V, 300-A Si MOSFET
L_{PFC}	15μH	RM-14 EPCOS N49 (7 turns)
L_R	3.1μH	RM-10 EPCOS N49 (3 turns)
L_{LLC}	31μH	LLC transformer magnetizing inductance (T_{LLC})
T_{LLC}	7:1:1	PQ-32/20 EPCOS N49
C_{BUS}	390μF	450-V Aluminum electrolytic capacitor
C_R	33nF	630-V C0G/NP0 Ceramic capacitor
C_{OUT}	220μF	50-V Aluminum electrolytic capacitor

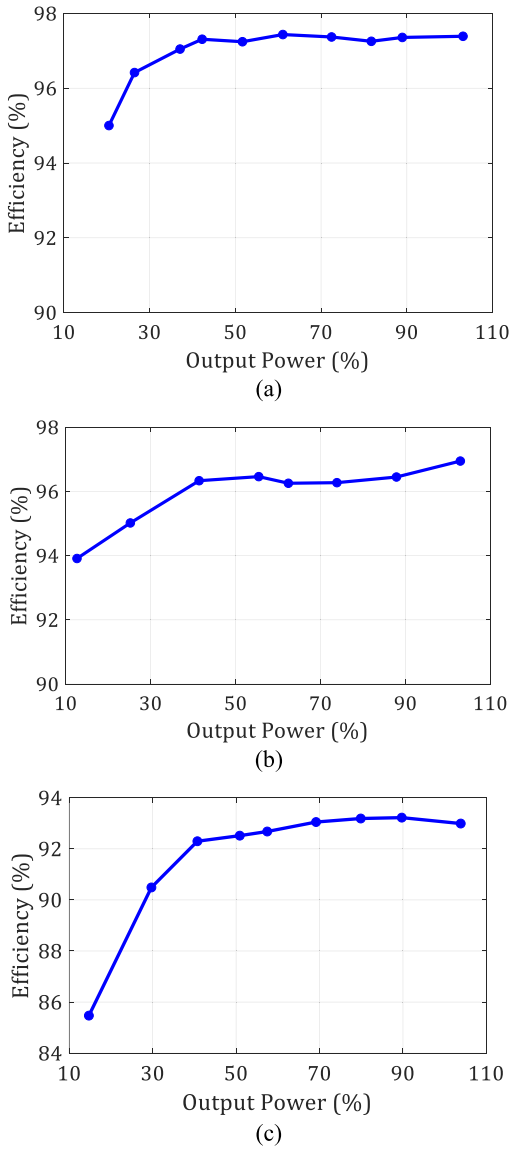

Fig. 25. Experimentally measured efficiencies of the proposed ac–dc converter as a function of output load. (a) PFC stage converting 120-V_{rms}, 60-Hz ac input voltage to a 400-V dc bus voltage across capacitor C_{BUS}, (b) *LLC* dc–dc stage converting the 400-V dc bus voltage to 28-V output voltage across the output load. (c) Full end-to-end isolated ac–dc converter converting the 120-V_{rms}, 60-Hz ac input voltage to a 28-V output voltage across the output load.

Fig. 24 shows the experimentally measured steady-state waveforms of the ac–dc converter. As can be seen from Fig. 24(a), the input current is sinusoidal and in-phase with the input voltage and dc bus voltage is regulated at 400 V validating the operation of the PFC controller. The slight distortion in the input current near the zero crossing is caused by the converter being turned OFF near the line voltage zero crossings to prevent an uncontrolled rise in the PFC inductor current due to any error in the polarity of the sensed input voltage. This distortion is more pronounced in the negative half cycle due to an offset in the sensed input voltage which causes the converter to stay OFF for a longer period during the negative half cycle than the positive half cycle. However, this slight distortion does not materially affect the sinusoidal waveshape and phase of the input current and the PFC stage achieves a high input power factor as is shown later in this section.

Fig. 24(b) shows the zoomed-in steady-state waveform of the ac–dc converter. As can be seen in the figure, the inductor current crosses zero in each switching cycle verifying BCM operation of the PFC stage. Moreover, the output voltage of the *LLC* dc–dc stage is regulated at 28 V validating the end-to-end operation of the ac–dc converter.

Fig. 25 shows the experimentally measured efficiencies of the proposed ac–dc converter as a function of output power. Fig. 25(a) shows the efficiency of the PFC stage when it is converting a 120-V_{rms}, 60-Hz input ac voltage to a 400-V dc bus voltage across the dc bus capacitor while utilizing the proposed PFC control strategy. As can be seen, the PFC stage maintains a high conversion efficiency of greater than 97% across a wide output power range and achieves a peak efficiency 97.4%. Fig. 25(b) shows the efficiency of the *LLC* dc–dc stage while it is converting a 400-V dc bus voltage to a 28-V output voltage.

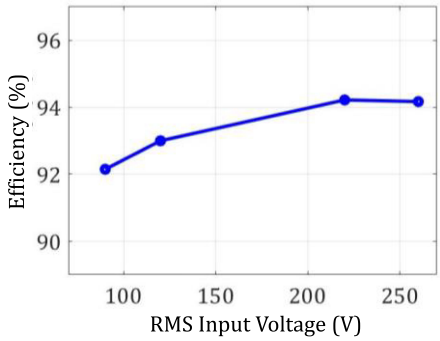

Fig. 26. Experimentally measured efficiency of the prototype isolated ac–dc converter as a function of input voltage while powering a 1-kW load.

The *LLC* dc–dc stage maintains an efficiency of greater than 96% across the majority of output power range and achieves a peak efficiency of 97%. The end-to-end efficiency of the proposed ac–dc converter is given in Fig. 25(c). As can be seen from the figure, the prototype converter maintains a high conversion efficiency of greater than 90% across 3:1 output power range and achieves a high peak efficiency of 93.3%.

Furthermore, the performance of the two-stage ac–dc converter is also evaluated across the entire input range. The end-to-end measured efficiency of the prototype converter when powering a 1-kW load is shown in Fig. 26. It can be seen that the efficiency remains greater than 92% across the entire input voltage range, with a peak efficiency of 94.3%.

The power loss distribution based on the theoretical loss models of the PFC stage and *LLC* dc–dc stage while the proposed ac–dc converter is operating at an input ac voltage of $120V_{rms}$, nominal dc bus voltage of 400 V, output dc voltage of 28 V, and output power of 1 kW, is shown in Fig. 27(a) and (b), respectively. As can be seen, the dominant loss mechanism of PFC stage operating in BCM is the device conduction loss in switches Q_1-Q_4. The other dominant loss mechanisms are winding and core losses in PFC inductor, losses in the EMI filter, and equivalent series resistance (ESR) losses in the dc bus capacitor, in decreasing order. There is also a slight turn-OFF loss in the PFC stage switches, which results in some device switching loss. In the *LLC* dc–dc stage, the dominant loss mechanisms are the winding and core losses in the transformer. This is followed by the losses in rectifier switches Q_7-Q_8, and inverter switches Q_5-Q_6, winding and core losses in the resonant inductor, and losses in planar PCB interconnects, PCB traces, and the resonant capacitor, in decreasing order.

The input power factor of the ac–dc converter is also measured experimentally and is shown in Fig. 28. The converter maintains a high input power factor above 0.98 across 4:1 output power range and achieves a near-unity input power factor of 0.997 at the rated output power of 1 kW. Hence, the experimental data validates the efficacy of the proposed control strategy and verifies the PFC operation of the ac–dc converter. The power factor as the function of input voltage is also measured while the prototype converter is powering a 1-kW load, as shown in Fig. 29. As can be seen from the figure, the power factor remains greater than 0.95 across a wide range of input voltage.

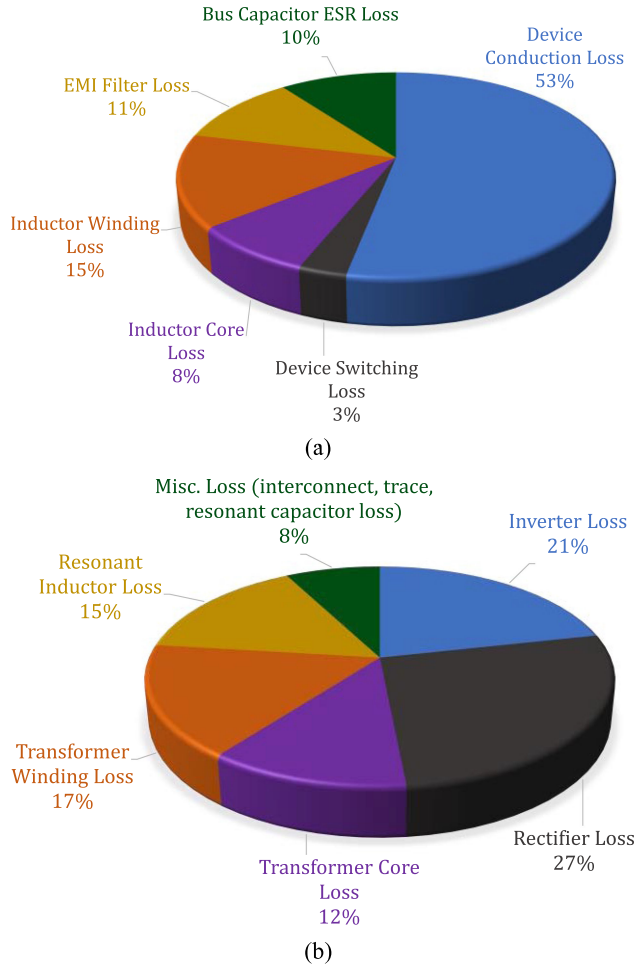

Fig. 27. Detailed loss breakdowns of (a) PFC stage and (b) *LLC* dc–dc stage based on the theoretical loss models when the proposed ac–dc converter is operating at an input ac voltage of $120V_{rms}$, nominal dc bus voltage of 400 V, output dc voltage of 28 V, and output power of 1 kW.

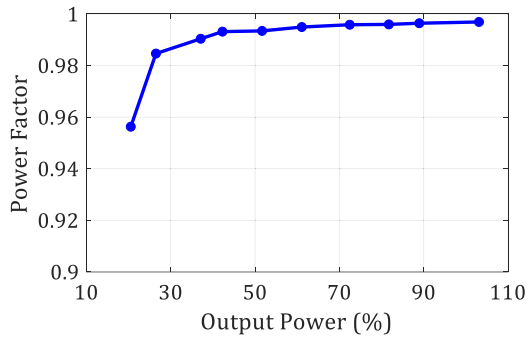

Fig. 28. Experimentally measured input power factor of the proposed ac–dc converter as a function of output power when a 120-V_{rms} 60-Hz ac input voltage is converted to a 28-V dc output voltage.

Fig. 30 shows the experimentally measured steady-state waveforms of two ac–dc converters operating in parallel. Fig. 30(a) shows the output voltage (across the shared load) and output currents of both ac–dc converters with the voltage control loop active and with the current sharing controller deactivated (without any droop control). It can be seen that with just the voltage

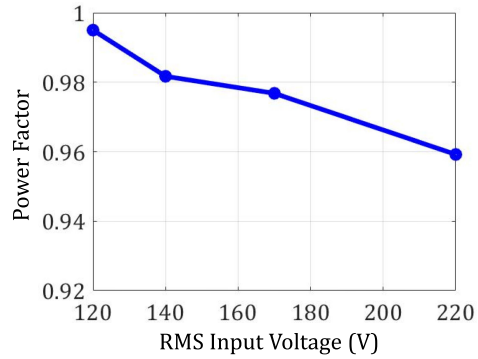

Fig. 29. Experimentally measured input power factor of the prototype isolated ac–dc converter as a function of input voltage while powering a 1-kW load.

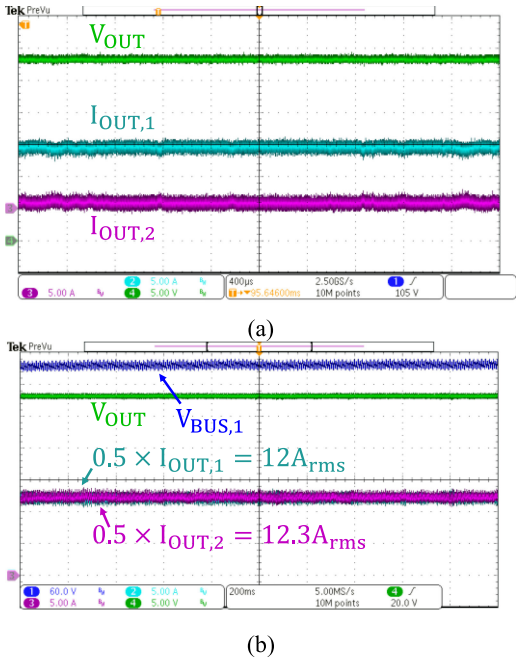

Fig. 30. Experimentally measured steady-state waveforms of two converters connected in parallel. (a) Output currents of converters 1 and 2 (5 A/div), and output voltage across the load with the current-sharing controller turned-OFF (5 V/div). (b) Output currents of converters 1 and 2 (5 A/div), dc bus voltage of converter 1 (60 V/div), and output voltage across the load with the proposed current sharing controller turned-ON (5 V/div).

control loop operating in each converter, the output currents are highly imbalanced with the converter 1 delivering the entire load current, and the two converters do not naturally share any output current. Fig. 30(b) shows the output voltage (across the shared load), output current of both converters, and dc bus voltage of converter 1 with the proposed *LLC* input current based droop control active. As can be seen, the output currents of both converter modules are well balanced, while the output voltage is regulated at 28 V and dc bus voltage of the converter 1 is regulated at 400 V.

Fig. 31 shows the experimentally measured output voltage as a function of output power when two 1-kW rated ac–dc converters are connected in parallel. It can be seen that the output voltage drops with output load. Based on this drop in output voltage, the

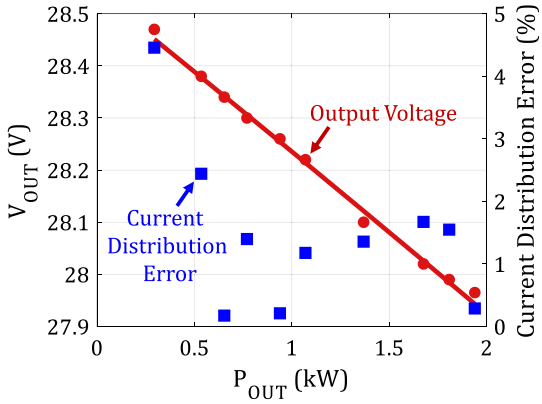

Fig. 31. Experimentally measured output voltage and current distribution error of the paralleled converter modules powering a common output load while utilizing the proposed droop control strategy. Here, 1 kW represents 100% load, which is the maximum power rating of a single ac–dc converter module.

virtual droop resistance R_{droop} is measured to be 8.6 m Ω. Fig. 30 also shows the percentage current distribution error (CDE) between the two ac–dc converter modules connected in parallel. The CDE is defined as $\max(|\frac{I_{OUT1}-I_{OUT,ideal}}{I_{OUT,ideal}}|, |\frac{I_{OUT2}-I_{OUT,ideal}}{I_{OUT,ideal}}|)$ and is the deviation of output current of each parallel-connected module (i.e., $I_{OUT,1}$ and $I_{OUT,2}$) from the nominal output current of each module (under perfect current distribution) $I_{OUT,ideal}$. As can be seen from Fig. 31, the CDE remains below 5% for the entire test range and below 2% for power levels exceeding 650 W. Moreover, the measured CDE is below 0.3% near the maximum total output power of 2 kW thereby validating the efficacy of the proposed *LLC* input current based droop controller.

VI. Conclusion

This article presents a high-power-density high-efficiency soft-switched single-phase universal-input to 28-V isolated ac–dc converter module designed for parallel operation. The proposed two-stage converter utilizes a totem-pole bridgeless boost PFC stage followed by an isolated *LLC* resonant dc–dc stage. A new comprehensive design methodology is presented, which compares various designs and operating modes for the converter modules' power stage and selects the optimal design based on overall power density and efficiency. For the selected design, a control scheme is presented for the PFC stage to minimize current distortion by accounting for various sensor, control, and gate-drive delays while ensuring ZVS of the transistors. Additionally, a new droop control strategy is presented, which employs the input current of the secondary dc–dc conversion stage to enable equal output current distribution between paralleled modules when powering a common output load. To validate the proposed design and control strategy, two 1-kW universal-input to 28-V isolated ac–dc converter modules are built and tested. Each prototype converter module achieves a high power density of 84 W/in^3 (5.13 W/cm^3) and a peak efficiency of greater than 93% while ensuring a current distribution error of less than 0.3% when operating in parallel to deliver the maximum output power of 2 kW.

APPENDIX A

LOSS CALCULATION AND DEVICE SELECTION METHODOLOGY USED IN THE DESIGN OF THE PROPOSED ISOLATED AC–DC CONVERTER MODULES

This appendix provides the loss calculations and device selection methodology used in the design of the proposed isolated ac–dc converter. The loss calculations estimate the efficiency and loss breakdown by accounting for various losses in transistors, magnetics (inductor and transformer), and capacitors as highlighted in the following.

1) Device Selection

To select transistors for use in the isolated ac–dc converter, several commercial GaN and Si transistors are compared for each of the following set of switches:

1) boost high-frequency switches;
2) boost low-frequency switches;
3) *LLC* inverter switches;
4) *LLC* rectifier switches.

For boost and *LLC* high-frequency switches Q_1 , Q_2, Q_5, and Q_6, a figure of merit based on transistor ON-resistance and output capacitance ($R_{\mathrm{DS,ON}} \times C_{\mathrm{OSS}}$) is used to compare the best-in-class transistors in the voltage range of 500 to 650 V, reducing conduction and switching losses. For boost low-frequency switches (Q_3 and Q_4) lowest $R_{\mathrm{DS,ON}}$ transistor is chosen between a voltage range of 500 to 650 V, reducing conduction losses, and for *LLC* high-frequency rectifier switches (Q_7 and Q_8) a figure of merit based on transistor ON-resistance and gate charge ($R_{\mathrm{DS,ON}} \times \mathrm{Q}_{\mathrm{gate}}$) is used to compare the best-in-class transistors in the voltage range of 80–100 V reducing conduction and gate-drive losses.

a) Transistor Selection and Loss Computation: Once the appropriate devices are selected, an analytical loss model is used to estimate conduction, switching, and gate-drive losses for both stages of the proposed isolated ac–dc converter. For the PFC stage, the current in each transistor is computed (across a line cycle) for the entire design space associated with the CCM and BCM operation of the converter. For the *LLC* stage, fundamental harmonic approximation is utilized to obtain the resonant tank current for the various considered inverter and rectifier topologies. The transistor forward conduction losses are computed using

$$P_{\mathrm{t,fc}} = I_{\mathrm{t,rms}}^2 \, R_{\mathrm{DS,ON}} \tag{11}$$

where $I_{\mathrm{t,rms}}$ is the rms current through the transistor and $R_{\mathrm{DS,ON}}$ is the ON-state resistance of the transistor. Transistor reverse conduction losses (during the deadtime) are also computed as

$$P_{\mathrm{t,dt}} = I_{\mathrm{t,d,avg}} \, V_{\mathrm{SD}} t_{\mathrm{dt}} f_{\mathrm{s}} \tag{12}$$

where $I_{\mathrm{t,d,avg}}$ is the average current through the switch during the deadtime t_{dt}, f_{s} is the switching frequency, and V_{SD} is the source-to-drain voltage drop obtained from the transistor's datasheet.

For transistor switching losses, three loss mechanisms are considered: turn-ON overlap loss, turn-OFF overlap loss, and output capacitor loss. The turn-ON v-i overlap loss is given by

$$P_{\mathrm{t,ON}} = f_{\mathrm{s}} \times \int_0^{t_{\mathrm{ON}}} v_{\mathrm{DS}}(t) \times i_{\mathrm{DS}}(t) \, dt \tag{13}$$

where v_{DS} and i_{DS} are the transistor drain-to-source voltage and current during the switching event and t_{ON} is the time taken from the transistor gate voltage rising to threshold to the transistor drain voltage falling to zero. This t_{ON} is obtained by simulating transistor SPICE model provided by the manufacturer for a given gate turn-ON resistance.

Similarly, the transistor turn-OFF losses are estimated by calculating the v–i overlap losses during the turn-OFF transition using the following equation:

$$P_{\mathrm{t,OFF}} = f_{\mathrm{s}} \times \int_0^{t_{\mathrm{OFF}}} v_{\mathrm{DS}}(t) \times i_{\mathrm{DS}}(t) \, dt \tag{14}$$

where t_{OFF} is the time taken from the transistor drain voltage rising above zero to the transistor gate voltage falling below the threshold voltage. This t_{OFF} is obtained by simulating the transistor SPICE model provided by the manufacturer for a given gate turn-OFF resistance. During the turn-OFF process, the current is assumed to fall linearly to zero with time. As the transistor current is falling, the inductor current (for PFC stage) or resonant tank current (for *LLC*) flows into the transistor output capacitance resulting in a quadratic rise in drain-to-source voltage (v_{DS}). For this case, (14) is given as

$$\mathrm{P_{t,OFF}} = \frac{i_{\mathrm{OFF}}^2 t_{\mathrm{OFF}}^2 \mathrm{f_s}}{48 \mathrm{C_{OSS}}} \tag{15}$$

where i_{OFF} is the transistor current at the turn-OFF instant and C_{OSS} is the output capacitance of the transistor. For C_{OSS}, the charge-related output capacitance value given in transistor data sheet is used.

Transistor output capacitance losses are also a significant loss mechanism in CCM designs of the PFC stage where the transistors Q_1 (when input voltage is positive) or Q_2 (when input voltage is negative) are turning ON under hard-switching. These losses can be computed using the following expression:

$$P_{\mathrm{t,OSS}} = C_{\mathrm{OSS}} V_{\mathrm{BUS}}^2 f_{\mathrm{s}}. \tag{16}$$

Based on the three switching loss mechanisms given in (13), (15), and (16), the total transistors switching losses are calculated by the following equation:

$$P_{\mathrm{t,s}} = P_{\mathrm{t,ON}} + P_{\mathrm{t,OFF}} + P_{\mathrm{t,OSS}}. \tag{17}$$

The transistors' gate drive losses are also computed in the loss model using the following equation:

$$P_{\mathrm{t,g}} = Q_{\mathrm{G}} \, V_{\mathrm{GS}} f_{\mathrm{s}} \tag{18}$$

where Q_{G} is the total gate charge of the transistor (obtained from transistors' data sheet) and V_{GS} is the gate-to-source voltage of the transistors. The total transistor losses can be computed by adding (11), (12), (17), and (18) and are given by

$$P_{\mathrm{t,s}} = P_{\mathrm{t,fc}} + P_{\mathrm{t,dt}} + P_{\mathrm{t,s}} + P_{\mathrm{t,g}}. \tag{19}$$

b) Magnetic Losses: Two loss mechanisms are considered for estimating magnetic (inductor and transformer) losses: winding losses and core losses. Winding losses are computed using

the following equation:

$$P_{\text{winding}} = \sum I_{\text{rms,i}}^2 R_{\text{AC},i} \tag{20}$$

where $I_{\text{rms},i}$ is the rms value of the ith harmonic of the winding current and $R_{\text{AC},i}$ is the ac resistance of the winding at the ith harmonic frequency. During the optimization of the PFC stage, Litz-wire based nonplanar designs are considered for the inductor. For such designs, ac resistance is calculated based on (2) presented in Section II of [60], which accounts for both skin and proximity losses. However, for hardware prototype, planar implementation of the magnetics is chosen to reduce the height of the inductor and transformers, and the ac resistance is then recomputed by exporting the 3-D model of the magnetic and planar PCB structures into a 3-D finite element analysis software Ansys HFSS.

The core losses in the magnetics are calculated using (9) (improved generalized Steinmetz equation—IGSE) given in Section II of [61]. Ferrite material parameters are required to solve the IGSE which are obtained by curve fitting the core loss density curves given in the ferrite material's datasheet using the basic Steinmetz equation $P_{\text{core,basic}} = k \times f^{\alpha} \times B_{\text{pk}}^{\beta}$, where B_{pk} is the peak value of the sinusoidal flux density excitation, f is the frequency of the excitation, and k, α, and β are the core material parameters.

c) Capacitor Losses: Capacitor losses are computed using the following equation:

$$P_{\text{cap, ESR}} = I_{\text{cap,rms}}^2 \, R_{\text{ESR}} \tag{21}$$

where $I_{\text{cap,ESR}}$ is the rms current flowing through the capacitor and R_{ESR} is the equivalent series resistance of the capacitor obtained from the capacitor's datasheet.

Appendix B

Analytical Model to Derive the Stability Limits for the Proposed Input Current Based Droop Control Strategy

This appendix presents an analytical model to determine the stability criteria for the *LLC* converter under the proposed input current based droop controller. For the proposed droop control, the underlying control law is given by

$$v_{\text{OUT,ref}}\ (t) = \text{V}_{\text{OUT,max}} \ - i_{\text{IN},LLC}\ (t) \,.r_{\text{d,control}}\,(t) \tag{22}$$

where $r_{\text{d,control}}\ (t) = \frac{\eta_{LLC} R_{\text{droop}} v_{\text{BUS}}(t)}{v_{\text{OUT}}(t)}$. Since the control law is nonlinear, it can be linearized around the nominal operating point to obtain a small-signal model, as given in the following equation:

$$\hat{v}_{\text{OUT,ref}} = \frac{\partial v_{\text{OUT,ref}}}{\partial i_{\text{IN},LLC}}\ \hat{i}_{\text{IN},LLC} + \frac{\partial v_{\text{OUT,ref}}}{\partial v_{\text{OUT}}} \hat{v}_{\text{OUT}}$$

$$+ \frac{\partial v_{\text{OUT,ref}}}{\partial v_{\text{BUS}}} \hat{v}_{\text{BUS}}. \tag{23}$$

These partial derivatives in (23) are defined and evaluated as follows:

$$-\frac{\partial v_{\text{OUT,ref}}}{\partial i_{\text{IN},LLC}} \equiv f_1 = \frac{\eta_{LLC} R_{\text{droop}} V_{\text{BUS}}}{V_{\text{OUT}}} \tag{24}$$

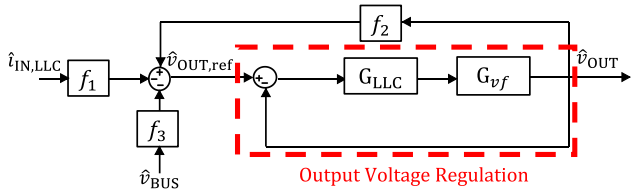

Fig. 32. Small-signal model of the droop control and the output voltage regulation loop.

$$\frac{\partial v_{\text{OUT,ref}}}{\partial v_{\text{OUT}}} \equiv f_2 = \frac{\eta_{LLC} R_{\text{droop}} V_{\text{BUS}} I_{\text{IN},LLC}}{{V_{\text{OUT}}}^2} \tag{25}$$

$$-\frac{\partial v_{\text{OUT,ref}}}{\partial v_{\text{BUS}}} \equiv f_3 = \frac{\eta_{LLC} R_{\text{droop}} I_{\text{IN},LLC}}{V_{\text{OUT}}}\ . \tag{26}$$

The small-signal model of the *LLC* converter with output voltage regulation under droop control is shown in Fig. 32.

Under output voltage regulation, the output voltage is related to the reference voltage by

$$\hat{v}_{\text{OUT}} = \frac{\text{T}}{1+\text{T}}\ \hat{v}_{\text{OUT,ref}} \tag{27}$$

where $T\ = \text{G}_{LLC}\ \text{G}_{vf}$ is the loop gain of the output voltage regulation loop. Since the output voltage regulation loop's bandwidth is kept significantly higher than the bandwidth of the droop controller (at least an order of magnitude), the loop gain of output voltage regulation loop is high at the frequencies of interest for droop control. This ensures accurate output voltage reference tracking, and hence $\hat{v}_{\text{OUT}} = \hat{v}_{\text{OUT,ref}}$ holds for the analysis of droop control. With this simplification (23) reduces to

$$\hat{v}_{\text{OUT,ref}} = \frac{-K}{1-f_2}\ \left(V_{\text{BUS}} \hat{i}_{\text{IN},LLC} + I_{\text{IN},LLC} \hat{v}_{\text{BUS}}\right) \tag{28}$$

where $K\ = \frac{\eta_{LLC} R_{\text{droop}}}{V_{\text{OUT}}}$. Hence, the proposed droop control remains in negative feedback (and stable) if $\frac{K}{1-f_2}$ is positive. This imposes an upper limit on f_2 according to the following:

$$f_2 < 1. \tag{29}$$

This bound translates to an upper limit on droop resistance. This upper limit is evaluated by substituting (25) into (29) and is given by

$$R_{\text{droop}} < R_{\text{LOAD}}. \tag{30}$$

Therefore, the *LLC* converter under the proposed droop control is stable if the droop resistance selected is smaller than the load resistance.

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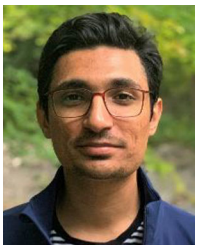

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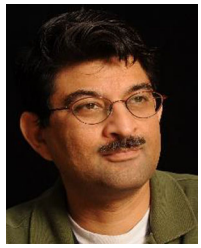

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