A Graph-Modeling Approach to Topology Simplification in Power Converters

Guidong Zhang, *Member, IEEE*, Yukai Liao, Samson Shenglong Yu, *Member, IEEE*, and Yun Zhang

***Abstract*—In this article, we propose a topology simplification method (TSM) for power converters, based on graph theory, to improve the converter design. In the proposed method, a directed graph is first established to model a converter circuits, from which the conceptually new converter adjacency matrix (CAM) is derived. Combined with the electrical features of power converters, a rule for electronics current paths is presented. Then, the redundant components are eliminated based on the proposed TSM and a new CAM is obtained, which is converted to a new directed graph and thus a new converter topology with reduced components. In the process, the integrity of the current paths is preserved and the new topology contains all the current paths of the original converter. With the proposed TSM, the derivations of the existing single-ended primary-inductor converter and current-fed dual active bridge converters are employed for theoretical verification. A novel single-phase boost push–pull converter topology is designed, which is validated by experiments.**

***Index Terms*—Boost push–pull converter, current-fed dual active bridge (CF-DAB), graph theory, power converters, single-ended primary-inductor converter (SEPIC), topology simplification.**

I. Introduction

POWER electronics devices play an indispensable role in modern energy systems [1], [2]. Research articles of power electronics can be classified into three categories: converter topology, power conversion control, and semiconductors. Among them, converter topology research is the backbone of power electronics, since studies of power conversion control and power semiconductors are all based on specific converter circuits [3].

Power converters are required to have high-efficiency, low economic cost, and high stability to meet the requirements of today's power industry [4]. To realize this, many topologies have been proposed. For instance, high-gain dc–dc converters are proposed for the application of high transmission ratio of voltage in distributed power generation systems, aerospace, and electric vehicles [5], [6]. *LLC*-resonant converters are proposed to realize full load range soft switching of switching devices. Power factor correction (PFC) converters are developed to reduce power pollution in the power system [7] to list just one among many advantages.

However, most power converter topologies are normally designed from researchers' experience or inspirations. To achieve systematic converter topology design, a few researchers have developed a range of methods. Axelrod *et al.* [8] proposed the switched-capacitor/switched-inductor structures, aiming at structuring transformerless hybrid dc–dc converters. Li *et al.* [9] proposed a systematic method for deriving high-gain dc converters based on the geometric structure. Zhang *et al.* [10] proposed a generalized additional voltage pumping solution to realize high-gain dc–dc converters based on the existing high-step-up converters.

The single-ended primary-inductor converter (SEPIC) converter is the simplest structure of cascading a boost and buck–boost converter. It is well known that the SEPIC converter is composed of cascaded boost and buck–boost converters but with single switch. That is to say, SEPIC converter is the simplest topology of boost cascaded with buck–boost. Another typical example is the double-switches *LLC*-resonant ac–dc converter [11], [12], which is the simplest topology of the boost PFC converter cascaded with a half-bridge *LLC*-resonant converter and has four diodes and two switch. Emadi *et al.* [13] coined out all the boost-type integrated topologies, buck-type integrated topologies, and buck–boost-type integrated topologies. They made an excellent summary of common simplified topologies, but did not further propose a generalized integrated topology method.

Therefore, a systematic method of simplifying electronics components in a power converter is greatly needed. This can help improve the converter design efficiency and reduce procurement and manufacturing cost of power converters.

Many researchers began to study the general methods of integrated topology since 1990s. Madigan *et al.* [14] proposed a family of integrated converters and a derivation method. However, the application conditions of this method are too constricted and thus have limited applicability. Redl *et al.* [15] proposed the method of integrating two synchronous switches with a common node and their integrated cell, but they only studied a few of switch connection types. Wu and Yu [16] established a general method for integrating switches in multistage converter. Four fundamental types of synchronous switches were proposed and

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relevant control methods were devised. Wu and Liang [17] further applied this method to develop soft-switching pulse width modulation (PWM) converters. This general method can derive all the topologies in [13]. However, this method requires manual manipulations of circuits and choose the methodology on a case-by-case basis, which is deemed of having low efficiency. Chen *et al.* [18] proposed an ingenious method to use three switches to generate two sets of complementary duty cycles that were traditionally generated by four switches and integrated switches by computers. However, this method requires a large amount of computations.

To achieve this, a generalized analytical method for converter topology is needed. It is found that the converter topology can be modeled as a graph by using graph theory [19], [20]. It is found that the converter topology can be abstracted into a graph by using graph theory, which can be modeled as an adjacency matrix or an incidence matrix according to the research in [21], [22]. For example, Maksimovic and Cuk [23] used graph theory to analyze the properties of the converters. Zhang and Qiu [24] proposed a sneak circuit analysis method, where all paths of the topology are calculated by graph theory to analyze the sneak circuits. Ogata and Nishi [25] employed graph theory for the design of dc–dc converters and averaged state-space model is combined with graph theory. Mo *et al.* [26] derived multiport converters with reduced switches and used graph theory to model the converters.

Inspired by this, in this article, we propose a systematic topology components simplification method for power converters, which uses graph theory as the mathematical foundation. The topology simplification method (TSM) can be summarized as follows. First, a directed graph is established from a converter topology, from which the converter adjacency matrix (CAM) is obtained. Then, electronics components with the same electrical features are removed, with a new CAM established, which leads to a simplified converter topology. Finally, the integrity of the current paths is verified by ensuring that new topology contains all current paths of the removed electronics components in the original circuit.

Compared with existing TSMs, we establish the mathematical model of the converters using graph theory, which enables computer-aided converter topology design with high applicability, scalability, and design efficiency. In this way, a large number of topology simplifications can be achieved by computer, not manual observations and design. Moreover, the method we proposed can verify the effectiveness of the new topology obtained by the simplification method through mathematical calculations. Existing methods still require simulation or experimental verification.

The rest of this article is organized as follows. In Section II, the directed graph of power electronics topology, the definition of its CAM, and the physical meaning of cofactors are presented. In Section III, four steps of the TSM are presented in detail. In Sections IV and V, the derivations of the SEPIC and current-fed dual active bridge (CF-DAB) are presented based on the TSM, respectively. In Section V, the derivations of CF-DAB converters are presented based on the TSM. In Section VI, a new single-phase boost push–pull converter is designed based on the proposed method. In Section VII, simulation and experiment studies are conducted for the new converter topology, with results presented and analyzed. Finally, Section VIII concludes this article.

II. Preliminaries

A. Directed Graph

A converter topology can be modeled as a directed graph. A directed graph $\mathcal{G}(V, E)$ consists of two finite sets V and E, where $V = \{V_1, V_2, \ldots, V_N\}$ is the set of nodes and $E = \{E_1, E_2, \ldots, E_N\}$ is the set of edges connecting all nodes, and the directions of the edges depend on the electrical feature of a particular component [27], [28]. A component whose current only flows in one direction is an unidirectional component, such as diodes; while a component whose current can flow in both directions is a bidirectional component, i.e., a bidirectional edge.

B. Converter Adjacency Matrix

Any graph has a unique adjacency matrix corresponding to it, and a CAM corresponds to a unique graph. The conventional adjacency matrix comprises Boolean values "0" and "1," representing whether there are edges between two nodes, where $a_{ij} = 1$ indicates that node i and node j are connected through the edge, and $a_{ij} = 0$ means no connection between two nodes.

$$a_{ij} = \begin{cases} 1 & \text{if } i = j \\ 0 & \text{if } i \neq j \text{ and no edges between node } i \text{ and node } j \\ \sum_{i,j=1}^{K} (k/\overline{k}) e_{ij} & K \text{ is the maximum number of nodes} \\ & e_{ij} \text{ is the component connecting nodes } i \text{ and } j \\ & k \text{ and } \overline{k} \text{ are the control elements.} \end{cases} \tag{1}$$

Deriving from the conventional adjacency matrix, we propose a novel CAM to represent the directed graph in the form of matrix to model the converter topology. CAM A is a matrix of $N \times N$ (N is the number of nodes), where the matrix elements a_{ij} are defined [29] as (1).

It can be seen that the difference between the traditional adjacency matrix and the CAM is that, the components on the edge of a directed graph is the value of the edge in CAM. For example, if there is an inductor between node i and node j, then $a_{ij} = a_{ji} = L$.

In addition, k and $\overline{k}$ are the control elements, and they only exist in front of switch (S) and diode (D). The value of k is 1 or 0, and $\overline{k} = 1 - k$. We put k in front of the merged switches. Then, according to whether the remaining diodes and switches have the same conduction sequence as the merged switches, k or $\overline{k}$ is placed in front of them. Components with k and components with $\overline{k}$ do not conduct at the same time.

Notably, the diode is an unidirectional component. Thus, if $a_{ij} = kD$, then $a_{ji} = 0$, and vice versa. Except for the components in which current cannot flow in the reverse direction such as diodes, unidirectional thyristors, and reverse-blocking insulated gate bipolar transistor (IGBTs), the remaining components are

TABLE I
PHYSICAL MEANINGS OF SYMBOLS

Symbol	Meaning in CAM	Meaning in converter cofactor
$\times_s$	Components are connected in series	The same as in CAM
$+_s$	Components are connected in parallel	Direction of current path
$-_s$	/	Direction of current path, it is opposite to $+_s$
1_s	When node i = node j	There is a wire between two nodes
0_s	There is no component between two nodes	The same as in CAM
$k/\bar{k}$	Components current conduction	kk and $\bar{k}\bar{k}$ mean that the current path can be conducted, i.e., kk=1, $\bar{k}\bar{k}$=1. $k\bar{k}$ means that the current path cannot be conducted, i.e., $k\bar{k}$=0
a_{ij}^2	/	If a component in a current path contains a square term and there is a negative sign in front of the current path, it means that the current flows through the component from one node to another, and then returns to the original point, e.g., $-S^2$=1

$a_{ij} = a_{ji}$ in the CAM. Each symbol in the CAM is interpreted with physical meanings in Table I.

C. Cofactor of a Converter Topology

The determinant of an $N \times N$ matrix is the algebraic sum of the products of all n elements taken from different rows and columns, with a total of (n factorial) products. Different from the traditional determinant, the traditional determinant is a value and the determinant of CAM is all current paths of the circuit. The elements in CAM are components in the circuit, so the product of n elements taken from different rows and columns in CAM is an algebra. This algebra represents a current path since it is equivalent to a connection of these n elements. When there is no current path between n elements, at least two of the n elements are not connected, the element at the corresponding position in the CAM is "0," and the product of these n elements is 0. Here, all products represent the circuit of all current paths.

The remaining $(N-1) \times (N-1)$ determinant is called the cofactor of a_{ij} after the row i and column j are deleted, which is denoted by M_{ij}. Combining the property of determinant, all current paths of a component in the circuit are equal to $a_{ij}M_{ij}$ + a_{ji} M_{ji} since M_{ij} and M_{ji} are all the connection between the (i, j) component and other components in the topology. a_{ij} M_{ij} represents the current paths flowing from node i to node j while a_{ji} M_{ji} represents the current paths flowing from node j to node i.

Notably, in a converter's cofactor, the negative sign "−" in front of the current path only indicates the direction of current of the component. For bidirectional components, there is no difference between the positive sign "−" and the negative sign "+". Each symbol has a physical meaning in a cofactor, as shown in Table I.

D. Proposed TSM Rules

Based on directed graph, the CAM, and cofactor, three TSM rules are proposed, i.e., the graph theory abstraction rule, node merging rule, and current path reduction rule, which lays the foundation of the TSM.

1) Graph Theory Abstraction Rule: A node connecting two components in the topology is regarded as a node of a corresponding directed graph. The component is regarded as the edge of the directed graph, while its direction of the edge is represented by an arrow.

2) Node-Merging Rule: If node i and node j are merged, row j is added to row i (it is equivalent to the positive connection where the current direction is positive between node j and other nodes being added to node i), and column j is added to column i in the CAM (it is equivalent to the negative connection in which the current direction is positive between node j and other nodes being added to node i). Then, row j and column j are deleted.

3) Current Path Reduction Rule: In all current paths, if one of the current paths contains another current path, for instance, current path 1 is RC_2 and current path 2 is RC_2 D_2L_2 in Fig. 2, path 1 + path 2 = $RC_2(1 + D_2L_2) = RC_2$. The physical meaning is that D_2 L_2 is in parallel with a wire and thus D_2 L_2 is short-circuited, i.e., path 1 $\supseteq$ path 2. Then, path 1 can be ignored. In addition, components with k and components with $\bar{k}$ do not conduct at the same time. Thus, if a current path contains both k and $\bar{k}$, the current path can be ignored.

III. PROPOSED TOPOLOGICAL SIMPLIFICATION METHOD

The proposed TSM is achieved by the following four steps, i.e., modeling, simplification, objectification, and verification, as shown in Fig. 1. As an example, Fig. 2 is the derivation of the SEPIC using the TSM.

A. Modeling: Circuit → Directed Graph → CAM

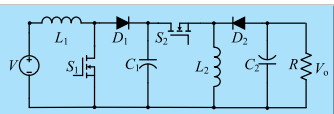
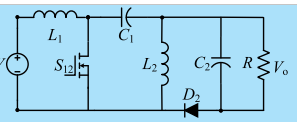
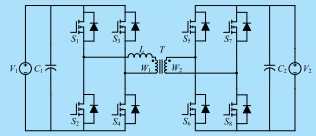
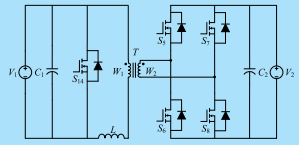
According to the definition and approach mentioned in Section II, a converter topology is modeled as a directed graph using the graph theory abstraction rule. Then, a CAM is obtained from the directed graph. We brand this step as *Modeling* in the TSM.

B. Simplification: Reducing the CAM Dimension

First, we introduce the definition of components of having the same electrical features. Having the same electrical features refers to the state in which the same types of components operate synchronously. For instance, as shown in Fig. 3, switches S_1 and S_2 operate synchronously at the same frequency and duty cycle, i.e., their conduction sequences are the same, and they have the same electrical features.

Components that have the same electrical features and do not affect the integrity of the current paths after merging can be

TABLE II
EXAMPLES OF CURRENT PATH INTEGRITY VERIFICATION

	Original circuit	Components with same electrical feature	Old paths	New circuit	New paths
Example 1 (can be simplified)		S_1 and S_2	S_1L_1V $S_2C_1L_2$		$S_{12}L_1V$ $S_{12}C_1L_2$
Example 2 (cannot be simplified)		S_1 and S_4	$S_1C_1LS_4W_1$ $S_1V_1LS_4W_1$		V_1S_{14} C_1S_{14} LW_1S_{14}

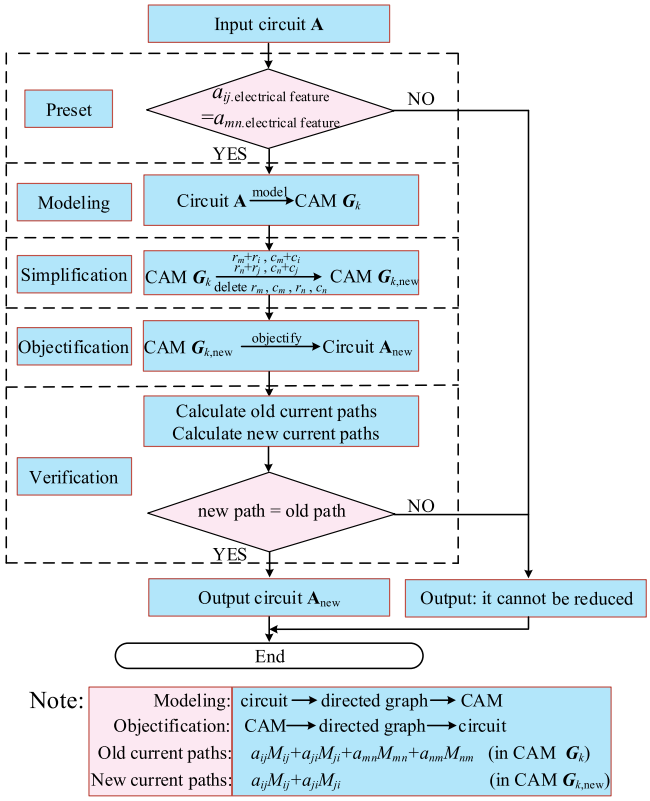


Fig. 1. Flowchart of the TSM.

merged. Whether the integrity of the path is destroyed will be verified in the *Verification* step.

Merging the components also means merging nodes connected to the components in the graph using the node-merging rule.

In this step, the components with the same electrical features are combined and a new CAM is obtained, with topology simplified.

C. Objectification: CAM → Directed Graph → Circuit

This step is the inverse process of *Modeling*. The new CAM is objectified to a directed graph, and then, a new converter topology is obtained from the directed graph. We name this step as *Objectification* in the TSM.

D. Verification: Checking the Integrity of Current Paths

In this step, we need to verify the functionality of the new circuit. First, all the current paths are calculated in the combined components in both new and old topologies. If the current paths are intact in the new circuit, this means that we have successfully simplified the converter topology without altering the functionality of the original converter. However, if the current paths of the simplified converter are different than the original converter, it means that the simplification process destroys the current paths or creates new current paths. Then, the combined component is not a redundant component and should be retained and restored.

Relevant details are illustrated in Table II for the SEPIC converter. To well explain this step, two examples are presented in Table II.

Example 1 is a successful example, and Example 2 is a failed example.

In Example 1, S_1 and S_2 have the same conduction sequence, so we consider their electrical features are the same. Their current paths in the original circuit are $S_1\ L_1V$ and $S_2\ C_1L_2$. S_{12} represents a switch after merging S_1 and S_2. Its current paths in the new circuit are $S_{12}\ L_1V$ and $S_{12}\ C_1L_2$. The new current paths are the same as the old current paths, so there are no current paths that have been destroyed, i.e., the integrity of the current paths is retained.

In Example 2, S_1 and S_4 have the same conduction sequence, i.e., with the same electrical feature. Their current paths in the original circuit are $S_1\ C_1LS_4\ W_1$ and $S_1\ V_1LS_4\ W_1$. S_{14} is the combined switches S_1 and S_2. Its current paths in the new circuit are $V_1\ S_{14}$, $C_1\ S_{14}$ and $LW_1\ S_{14}$. There are some current paths that have been destroyed and thus the removal is reverted and the simplification for this part is not feasible.

E. Potential Adjustment

Sometimes the diode and transformer windings can be connected in parallel in the new converter topology. We know that the diode has the clamping effect and can affect the winding, so we need to add a diode in the new converter topology. In detail, the node connected with the original diode anode moves to have a new node, and then the anode of the new diode is connected to the new node, and the cathode is connected to the original

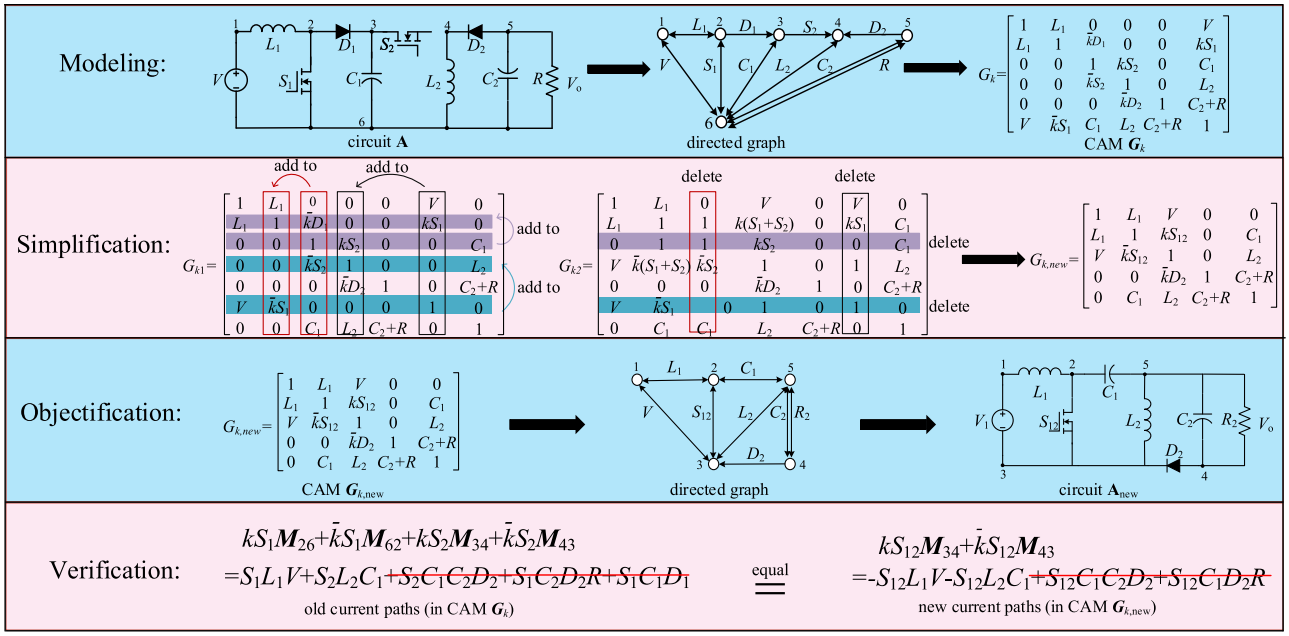


Fig. 2. Derivation of the SEPIC using the TSM: An example.

node. This ensures that the winding is not affected by diodes clamping characteristics. The direction of the node movement should be the same as the direction of the diode current to ensure that the additional diode does not affect other current paths. Note that because in the graph theory modeling approach and mathematical expressions of converters, transformer windings are represented mathematically, the proposed TSM can detect this situation and add the required diode. This step is therefore a systematic, not manual, step. This process will be implemented in Section V-C with a particular example.

We have included two more examples to illustrate the working principle of the proposed graph-modeling-based TSM in Appendix A.

IV. Case Study: Derivation of the CF-DAB Converter Using the Proposed TSM

The existing voltage-fed dual active bridge (VF-DAB) converter [see Fig. 4(a)] has the problem of large current fluctuations [30]. Therefore, the CF-DAB converter [Fig. 4(b)] was proposed. Since the output end of CF-DAB converter has inductors, the output current is continuous and the current ripple is small [31]. In fact, the CF-DAB converter comes from the VF-DAB converter cascading with the interleaved bidirectional buck converter and simplify topology. In this section, we show this process by the proposed TSM.

A. Modeling

The topology of VF-DAB converter cascaded with the interleaved bidirectional buck converter is shown in Fig. 5(a).

As shown in Fig. 5(b), the topology can be modeled as a directed graph. Then, according to (1), its CAM can be obtained as

$$\boldsymbol{G}=\begin{bmatrix} 1 & L_2 & L_3 & 0 & 0 & 0 & V_2 \\ L_2 & 1 & 0 & S_9 & 0 & 0 & S_{10} \\ L_3 & 0 & 1 & S_{11} & 0 & 0 & S_{12} \\ 0 & S_9 & S_{11} & 1 & S_5 & S_7 & C_2 \\ 0 & 0 & 0 & S_5 & 1 & W_2 & S_6 \\ 0 & 0 & 0 & S_7 & W_2 & 1 & S_8 \\ V_2 & S_{10} & S_{12} & C_2 & S_6 & S_8 & 1 \end{bmatrix}. \quad (2)$$

S_5 and S_9 have the same conduction sequence, so k_1 is added in front of them. The conduction sequences of S_6 and S_{10} are opposite to those of S_5 and S_9, respectively, so $\overline{k_1}$ is added in front of them. S_7 and S_9 have the same conduction sequence, so k_2 is added in front of them. The conduction sequences of S_8 and S_{12} are opposite to those of S_7 and S_{11}, respectively, so $\overline{k_2}$ is added in front of them. Now, we have

$$\boldsymbol{G}_k=\begin{bmatrix} 1 & L_2 & L_3 & 0 & 0 & 0 & V_2 \\ L_2 & 1 & 0 & \overline{k_1}S_9 & 0 & 0 & \overline{k_1}S_{10} \\ L_3 & 0 & 1 & \overline{k_2}S_{11} & 0 & 0 & \overline{k_2}S_{12} \\ 0 & k_1S_9 & k_2S_{11} & 1 & k_1S_5 & k_2S_7 & C_2 \\ 0 & 0 & 0 & \overline{k_1}S_5 & 1 & W_2 & \overline{k_1}S_6 \\ 0 & 0 & 0 & \overline{k_2}S_7 & W_2 & 1 & \overline{k_2}S_8 \\ V_2 & k_1S_{10} & k_2S_{12} & C_2 & k_1S_6 & k_2S_8 & 1 \end{bmatrix}. \quad (3)$$

B. Simplification and Objectification

S_5 and S_9 have the same conduction sequence, so we consider their electrical features are the same and they can be merged.

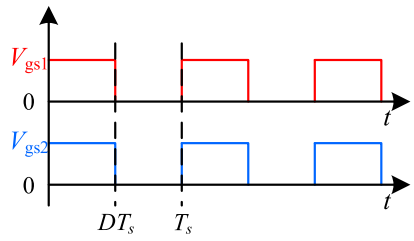


Fig. 3. Waveforms of V_{gs1} and V_{gs2} when the electrical features of S_1 and S_2 are the same.

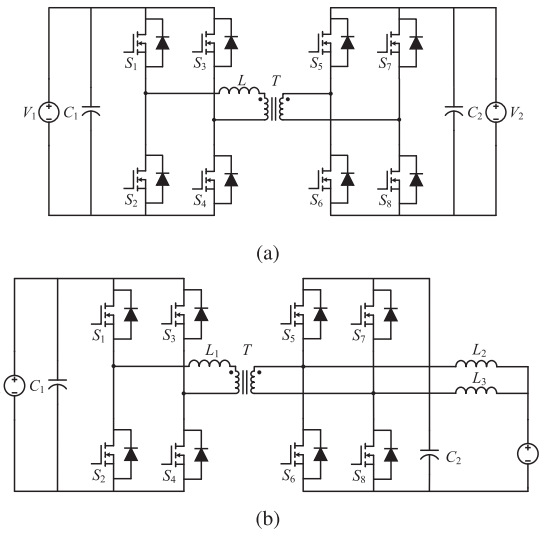


Fig. 4. (a) VF-DAB bidirectional DC–DC converter. (b) CF-DAB bidirectional DC–DC converter.

Similarly, according to the conduction sequence of the remaining switches, S_6 and S_{10} can be merged, S_7 and S_{11} can be merged, and S_8 and S_{12} can be merged. Thus, node 2 and node 5 are merged, and node 3 is merged with node 6. Then, a new CAM is obtained as (4) shown at the bottom of this page.

S_5+S_9 represents switch S_5 parallel switch S_9, so it can be replaced by switch S_{13}. Similarly, $S_6 + S_{10}$ is replaced by S_{14}, $S_7 + S_{11}$ is replaced by S_{15}, and $S_8 + S_{12}$ is replaced by S_{16}.

Subsequently, the new CAM (4) is objectified into Fig. 6 and then into Fig. 4(b) accordingly. This further verifies the proposed TSM.

C. Verification

The integrity of the current paths should be verified. In this example, we should calculate and compare whether all current

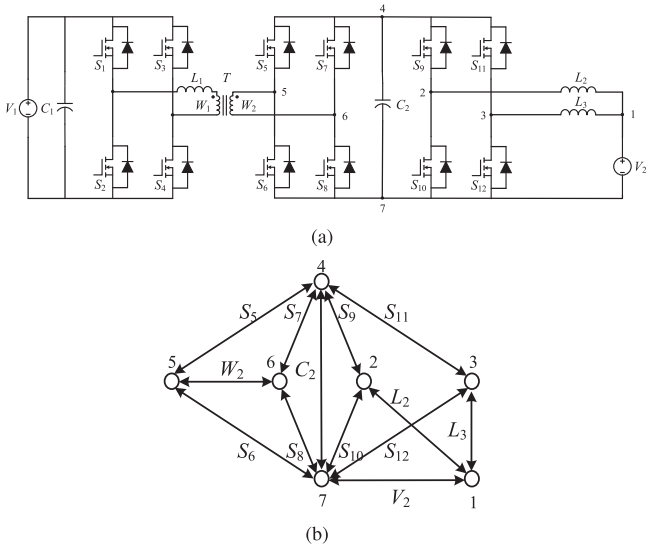


Fig. 5. VF-DAB cascaded with interleaved bidirectional buck. (a) Topology. (b) Directed graph.

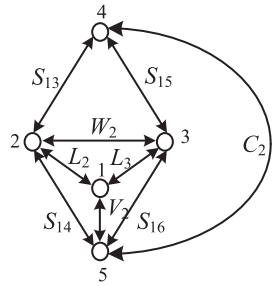


Fig. 6. Directed topology graph after merging selected nodes.

paths of S_5, S_9, S_6, S_{10}, S_7, S_{11}, S_8, and S_{12} in the original topology [see Fig. 5(a)] are intact in the current paths of S_{13}, S_{14}, S_{15}, and S_{16} in the new topology [see Fig. 4(b)].

All current paths of the merged switches in the original topology [see Fig. 5(a)] can be calculated. By simplifying them through the current paths reduction rule and removing the current paths which do not comply with the electrical laws, we have

$$\begin{aligned}&k_1S_5\boldsymbol{M}_{45}+\overline{k_1}S_5\boldsymbol{M}_{54}+k_1S_6\boldsymbol{M}_{75}+\overline{k_1}S_6\boldsymbol{M}_{57}\\&+k_2S_7\boldsymbol{M}_{46}+\overline{k_2}S_7\boldsymbol{M}_{64}+k_2S_8\boldsymbol{M}_{76}+\overline{k_2}S_8\boldsymbol{M}_{67}\\&+k_1S_9\boldsymbol{M}_{42}+\overline{k_1}S_9\boldsymbol{M}_{24}+k_1S_{10}\boldsymbol{M}_{72}+\overline{k_1}S_{10}\boldsymbol{M}_{27}\\&+k_2S_{11}\boldsymbol{M}_{43}+\overline{k_2}S_{11}\boldsymbol{M}_{34}+k_2S_{12}\boldsymbol{M}_{73}+\overline{k_2}S_{12}\boldsymbol{M}_{37}\end{aligned}$$

$$\boldsymbol{G}_{k,\text{new}}=\begin{bmatrix}1 & L_2 & L_3 & 0 & V_2\\ L_2 & 1 & W_2 & \overline{k_1}(S_5+S_9) & \overline{k_1}(S_6+S_{10})\\ L_3 & W_3 & 1 & \overline{k_2}(S_7+S_{11}) & \overline{k_2}(S_8+S_{12})\\ 0 & k_1(S_5+S_9) & k_2(S_7+S_{11}) & 1 & C_2\\ V_2 & k_1(S_6+S_{10}) & k_2(S_8+S_{12}) & C_2 & 1\end{bmatrix} \tag{4}$$

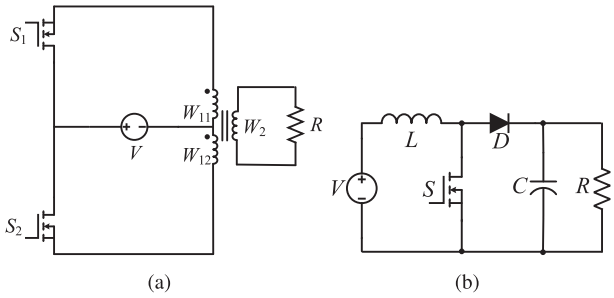


Fig. 7. (a) Single-phase push–pull converter. (b) Boost converter.

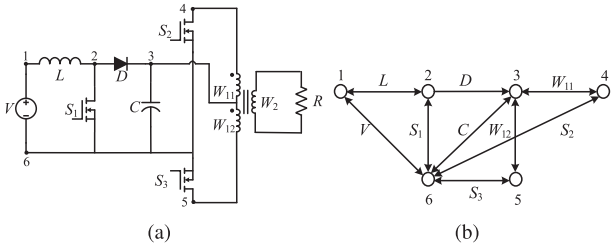


Fig. 8. Traditional single-phase boost push–pull converter circuit. (a) Topology. (b) Directed graph of the topology.

$$= S_{10}S_{12}L_2L_3 + S_6S_8W_2 + S_5S_8C_2W_2 + S_9S_{12}C_2L_2L_3 + S_9S_{11}L_2L_3 + S_{11}C_2L_3V_2 + S_{12}L_3V_2 + S_5S_7W_2 - S_{10}L_2V_2 - S_9C_2L_2V_2 - S_{10}S_{11}C_2L_2L_3 - S_6S_7C_2W_2. \tag{5}$$

Similarly, all current paths of S_{13}, S_{14}, S_{15}, and S_{16} in the new topology [see Fig. 4(b)] can be calculated. By simplifying them through the current paths reduction rule, we get

$$k_1S_{13}\boldsymbol{M}_{42} + \overline{k_1}S_{13}\boldsymbol{M}_{24} + k_1S_{14}\boldsymbol{M}_{52} + \overline{k_1}S_{14}\boldsymbol{M}_{25} + k_2S_{15}\boldsymbol{M}_{43} + \overline{k_2}S_{15}\boldsymbol{M}_{34} + k_2S_{16}\boldsymbol{M}_{53} + \overline{k_2}S_{16}\boldsymbol{M}_{35} = S_{10}S_{12}L_2L_3 + S_6S_8W_2 + S_5S_8C_2W_2 + S_9S_{12}C_2L_2L_3 + S_9S_{11}L_2L_3 + S_{11}C_2L_3V_2 + S_{12}L_3V_2 + S_5S_7W_2 - S_{10}L_2V_2 - S_9C_2L_2V_2 - S_{10}S_{11}C_2L_2L_3 - S_6S_7C_2W_2. \tag{6}$$

We can see that all current paths of S_5, S_9, S_6, S_{10}, S_7, S_{11}, S_8, and S_{12} in the original topology [see Fig. 5(a)] are included in the current paths of S_{13}, S_{14}, S_{15}, and S_{16} in the new topology [see Fig. 4(b)]. Thus, merging switches has not destroyed the current paths, and the topology simplification of the cascaded topology is successful.

V. A Novel Single-Phase Boost Push–Pull Converter With the TSM

The existing single-phase push–pull converter [see Fig. 7(a)] has a low output voltage amplitude. The traditional method to increase its voltage gain is to cascade the boost converter [see Fig. 7(b)] in the front stage, as shown in Fig. 8(a) [32]. However, it adds a switch and increases the loss. To here, we have designed a new topology by the TSM.

A. Modeling

As shown in Fig. 8(b), the topology can be modeled as a directed graph. Then, according to (1), its CAM is obtained as

$$\boldsymbol{G} = \begin{bmatrix} 1 & L & 0 & 0 & 0 & V \\ L & 1 & D & 0 & 0 & S_1 \\ 0 & 0 & 1 & W_{11} & W_{12} & C \\ 0 & 0 & W_{11} & 1 & 0 & S_2 \\ 0 & 0 & W_{12} & 0 & 1 & S_3 \\ V & S_1 & C & S_2 & S_3 & 1 \end{bmatrix}. \tag{7}$$

The conduction sequences of S_1 and S_2 are the same, so k is added in front of them. S_1 in the sixth column of the second row and S_2 in the sixth column of the fourth row represent the reverse conduction of S_1 and S_2, respectively. Therefore, $\overline{k}$ is added in front of them. The conduction sequences of diode D and switch S_3 are opposite to S_1 and S_2. Hence, $\overline{k}$ is added in front of them. S_3 in the fifth column of the sixth row represents the reverse conduction of S_3. k is added in front of them. Then, we can get

$$\boldsymbol{G}_k = \begin{bmatrix} 1 & L & 0 & 0 & 0 & V \\ L & 1 & D & 0 & 0 & kS_1 \\ 0 & 0 & 1 & W_{11} & W_{12} & C \\ 0 & 0 & W_{11} & 1 & 0 & kS_2 \\ 0 & 0 & W_{12} & 0 & 1 & kS_3 \\ V & \overline{k}S_1 & C & \overline{k}S_2 & \overline{k}S_3 & 1 \end{bmatrix}. \tag{8}$$

B. Simplification and Objectification

S_1 and S_2 have the same conduction sequence, so we can consider their electrical features are the same and they can be merged. Node 2 and node 4 are merged, and we can obtain a new CAM as follows:

$$\boldsymbol{G}_{k,\text{new}} = \begin{bmatrix} 1 & L & 0 & 0 & V \\ L & 1 & W_{11}+D & 0 & k(S_1+S_2) \\ 0 & W_{11} & 1 & W_{12} & C \\ 0 & 0 & W_{12} & 1 & kS_3 \\ V & \overline{k}(S_1+S_2) & C & \overline{k}S_3 & 1 \end{bmatrix}. \tag{9}$$

S_1+S_2 represents switch S_1 parallel switch S_1, so it can be replaced by switch S_{12}. Subsequently, the new CAM (9) is objectified into Fig. 9(a) and (b).

C. Verification

We need to check if current paths of S_1 and S_2 in the original topology [see Fig. 8(a)] are included in the current paths of S_{12} in the new topology [see Fig. 9(b)].

S_1 in (8) has two cofactors $\boldsymbol{M}_{26}$ and $\boldsymbol{M}_{62}$. kS_1 $\boldsymbol{M}_{26}$ represents the paths of the forward current, and $\overline{k}S_1$ $\boldsymbol{M}_{62}$ represents the paths of reverse current. Similarly, switch S_2 in (9) has two cofactors $\boldsymbol{M}_{46}$ and $\boldsymbol{M}_{64}$. kS_2 $\boldsymbol{M}_{46}$ represents the paths of forward current and $\overline{k}S_2$ $\boldsymbol{M}_{64}$ represents the paths of reverse current.

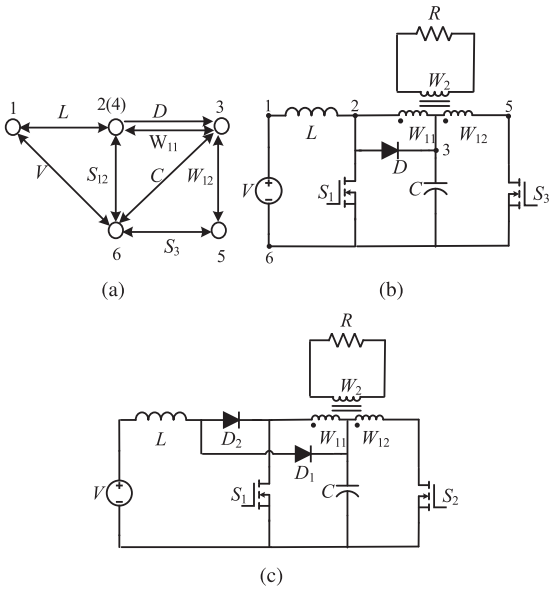


Fig. 9. Novel single-phase boost push–pull converter circuit evolution diagram. (a) Directed graph of topology after merging the nodes. (b) Topology obtained by the directed graph. (c) Adjusted topology.

All current paths of S_1 and S_2 in the original topology [see Fig. 8(a)] can be calculated. By simplifying them through the current paths reduction rule, we get

$$\begin{aligned}
&kS_1\boldsymbol{M}_{26} + \bar{k}S_1\boldsymbol{M}_{62} + kS_2\boldsymbol{M}_{46} + \bar{k}S_2\boldsymbol{M}_{64}\\
&= kS_1LV - k\bar{k}S_1^2 + \bar{k}S_1LV - k\bar{k}S_1^2 + \bar{k}S_1CD\\
&- k\bar{k}S_1S_2W_{11}D - k\bar{k}S_1S_3DW_{12}\\
&+ kS_2CW_{11} - k\bar{k}S_2^2 + kS_2DLVW_{11}\\
&- k\bar{k}S_1S_2DW_{11} - k\bar{k}S_2S_3W_{11}W_{12} + \bar{k}S_2CW_{11}\\
&= kS_1LV + \bar{k}S_1LV + \bar{k}S_1CD + kS_2CW_{11}\\
&+ kS_2DLVW_{11} + \bar{k}S_2CW_{11}\\
&= S_1LV + S_1CD + S_2CW_{11} + S_2DLVW_{11}. \qquad (10)
\end{aligned}$$

Since current paths S_2DLVW_{11} and S_1CD do not comply with the electrical laws and does not actually exist, thus, all current paths of S_1 and S_2 are S_1LV and S_2CW_{11}.

Similarly, switch S_{12} in (9) has two cofactors $\boldsymbol{M}_{25}$ and $\boldsymbol{M}_{52}$. $kS_{12}\ \boldsymbol{M}_{25}$ represents the path of forward current, and $\bar{k}S_{12}\boldsymbol{M}_{52}$ represents the current reverse flow path. Thus, all current paths of S_{12} in the new topology [see Fig. 9(b)] can be calculated. By simplifying them through the current paths reduction rule, we get

$$\begin{aligned}
&kS_{12}\boldsymbol{M}_{25} + \bar{k}S_{12}\boldsymbol{M}_{52}\\
&= k\bar{k}S_{12}^2 - kS_{12}LV - kS_{12}CW_{11} - \bar{k}\bar{k}S_{12}S_3W_{11}W_{12}\\
&- \bar{k}S_{12}LV - \bar{k}S_{12}CD - \bar{k}S_{12}CW_{11} + k\bar{k}S_{12}S_3DW_{12}\\
&= -kS_{12}LV - kS_{12}CW_{11} - \bar{k}S_{12}CD\\
&- \bar{k}S_{12}LV - \bar{k}S_{12}CW_{11}\\
&= -S_{12}LV - S_{12}CW_{11} + S_{12}CD. \qquad (11)
\end{aligned}$$

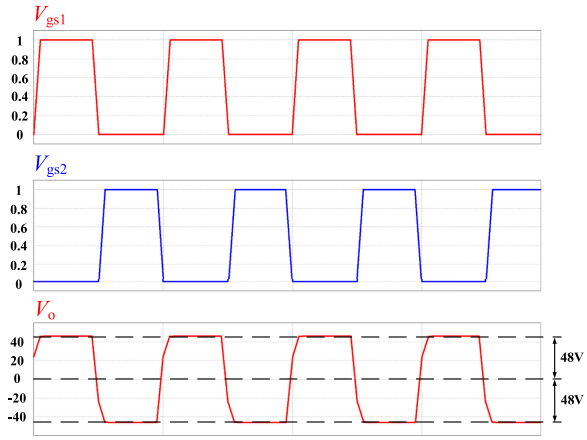


Fig. 10. Simulation results: Waveforms of $V_{\mathrm{gs1}}, V_{\mathrm{gs2}}, V_{\mathrm{o}}$.

Since current path S_1CD does not satisfy Kirchhoff's laws and does not actually exist. All current paths of S_{12} are S_{12}LV and S_{12}CW$_{11}$, which are the same as the current paths of S_1 and S_2. It means that all current paths of S_1 and S_2 in the original topology [see Fig. 8(a)] are retained in the new topology [see Fig. 9(b)], meaning that the construction of the new topology is successful.

In the new topology, the diode is parallel to the transformer winding, and a new diode should be added to the circuit. As shown in Fig. 9(c), the anode of the diode is moved to the edge of the inductor to ensure that the new diode does not affect the current path of the topology. The new diode anode is connected to the original diode anode, and the cathode is connected to the original node to ensure that the transformer is not affected by diode clamping.

It is noteworthy that the proposed TSM is designed only for the switches with the same conduction sequence in the boost push–pull converter. It is a subset of multiple working states of the traditional single-phase boost push–pull converter. Compared to this subset, the new circuit has the same topology. If the switches of the converter do not have the same conduction sequence, the new circuit is not equivalent to the original converter. This has been discussed in Section III, which is the main limitation of the work, which varies with different converter topologies. In Appendix A, we have included two more examples of applying the proposed TSM, which do not have this limitation.

VI. Simulation and Experiment

A. Simulation Verification

In order to verify the functionality of the new single-phase boost push–pull converter with the proposed TSM, simulations are conducted in PSIM™. The simulation parameters are shown in Table III.

The simulation results are shown in Fig. 10. According to Fig. 10, we can see that the control signals of S_1 and S_2 are out of phase by 180 degrees and their duty cycles are both 0.5. The output voltage V_{o} is an ac square wave with an amplitude of 48 V. Note that this circuit realizes the function of the traditional single-phase boost push–pull converter when switch S_1 and

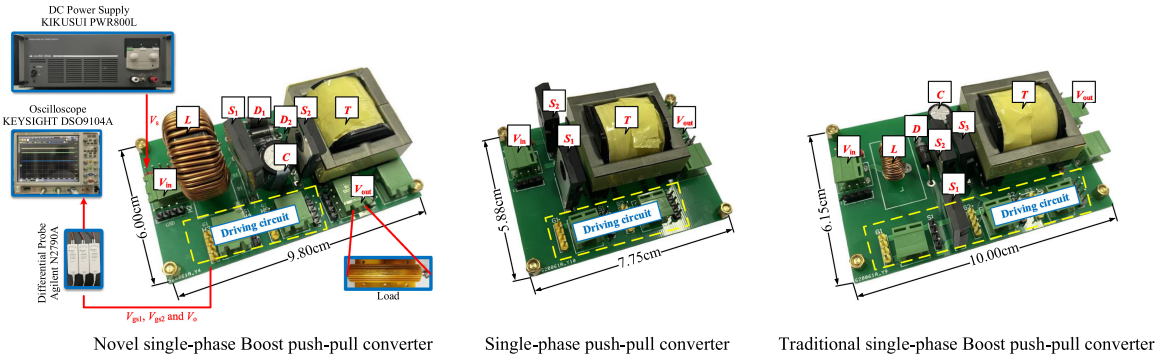


Fig. 11. Prototypes and experimental platform.

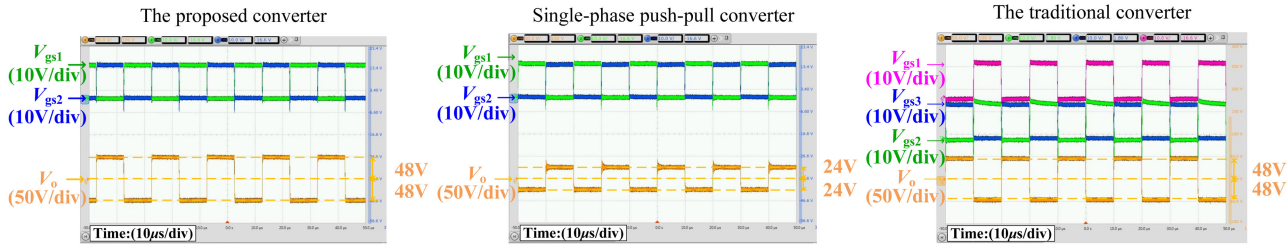


Fig. 12. Experimental results—output voltage and control signals. (a) V_{gs1}, V_{gs2}, and V_{o} of the novel single-phase boost push–pull converter prototype. (b) V_{gs1}, V_{gs2}, and V_{o} of the single-phase push–pull converter prototype. (c) V_{gs1}, V_{gs2}, V_{gs3}, and V_{o} of the traditional single-phase boost push–pull converter prototype.

TABLE III
SIMULATION AND EXPERIMENTAL PARAMETERS

Parameters	Value
Input voltage (V_{s})	24V
Inductance (L)	330μH
Capacitance (C)	47μF
Output load (R)	100Ω
Duty Cycle (d)	0.5
Switching frequency (f_{s})	50kHz
Ratio of transformer (n)	1:1:1

TABLE IV
EXPERIMENTAL PLATFORM

Equipment	Type
DC Power Supply	KIKUSUI PWR800L
Oscilloscope	KEYSIGHT DSO9104A
Differential Probe	Agilent N2790A

switch S_2 have the same conduction sequence with a simplified topology, indicating that the proposed TSM is feasible.

B. Experimental Verification

In order to further verify the effectiveness of the new designed push–pull converter circuit, as shown in Fig. 11, we have manufactured three prototypes and conducted experiments on them. Three prototypes are based on the novel single-phase boost push–pull converter, the single-phase push–pull converter, and the traditional single-phase boost push–pull converter. Experimental parameters are shown in Table III and the experimental environment is shown in Table IV and Fig. 11. In addition, the MOSFETs (S_1, S_2 and S_3) model is IRFP250 M, the diodes model (D_1 and D_2) is SR5100, and the driving IC is TLP250.

The measured waveforms of the control signals V_{gs1} and V_{gs2} of the novel single-phase boost push–pull converter are shown in Fig. 12(a). They are out of phase by 180 degrees and duty cycles are both 0.5. We can see the output voltage V_{o} is 48 V. The measured waveforms of the control signals V_{gs1} and V_{gs2} of the single-phase push–pull converter are shown in Fig. 12(b). They have the same control signals as the novel single-phase boost push–pull converter. We can see that when the input voltage is 24 V, the novel single-phase boost push–pull converter has the same output voltage. Fig. 12(c) shows the measured waveforms of the traditional single-phase push–pull converter. We can see that the control signals V_{gs1} and V_{gs2} are the same. Their phases are 180 degrees apart from that of the control signal V_{gs3}. The output voltage is 48 V.

When the electrical features of S_1 and S_2 are the same, the voltage gain of the novel single-phase boost push–pull converter is the same as that of the traditional single-phase boost push–pull converter. But the novel single-phase boost push–pull converter

TABLE V
COMPARISON OF LOSS BETWEEN THE TRADITIONAL CONVERTER AND THE PROPOSED CONVERTER

Loss of the traditional converter			vs.	Loss of the proposed converter		
P_L	$I^2_{L(\mathrm{RMS})}R_L$	0.64W	=	0.64W	$I^2_{L(\mathrm{RMS})}R_L$	P_L
P_D	$V_\mathrm{F}I_{D(\mathrm{avg})} + I^2_{D(\mathrm{RMS})}R_\mathrm{F}$	10.48W	>	8.97W	$V_\mathrm{F}I_{D_1(\mathrm{avg})} + I^2_{D_1(\mathrm{RMS})}R_\mathrm{F}$ $V_\mathrm{F}I_{D_2(\mathrm{avg})} + I^2_{D_2(\mathrm{RMS})}R_\mathrm{F}$	P_D
P_S	$I^2_{S_1(\mathrm{RMS})}R_{S_1} + \frac{V_{DS_1(\mathrm{off})}I_{S_1(\mathrm{on})}(t_\mathrm{on}+t_\mathrm{off})f_S}{6}$ $I^2_{S_2(\mathrm{RMS})}R_{S_2} + \frac{V_{DS_2(\mathrm{off})}I_{S_2(\mathrm{on})}(t_\mathrm{on}+t_\mathrm{off})f_S}{6}$ $I^2_{S_3(\mathrm{RMS})}R_{S_3} + \frac{V_{DS_3(\mathrm{off})}I_{S_3(\mathrm{on})}(t_\mathrm{on}+t_\mathrm{off})f_S}{6}$				$I^2_{S_1(\mathrm{RMS})}R_{S_1} + \frac{V_{DS_1(\mathrm{off})}I_{S_1(\mathrm{on})}(t_\mathrm{on}+t_\mathrm{off})f_S}{6}$ $I^2_{S_2(\mathrm{RMS})}R_{S_2} + \frac{V_{DS_2(\mathrm{off})}I_{S_2(\mathrm{on})}(t_\mathrm{on}+t_\mathrm{off})f_S}{6}$	P_S
P_C	$I^2_{C(\mathrm{RMS})}R_C$	0.63W	=	0.63W	$I^2_{C(\mathrm{RMS})}R_C$	P_C
P_T	$I^2_{W_{11}(\mathrm{RMS})}R_{W_{11}} + I^2_{W_{12}(\mathrm{RMS})}R_{W_{12}}$ $+I^2_{W_2(\mathrm{RMS})}R_{W_2} + P_\mathrm{V}V_\mathrm{e}$	3.51W	=	3.51W	$I^2_{W_{11}(\mathrm{RMS})}R_{W_{11}} + I^2_{W_{12}(\mathrm{RMS})}R_{W_{12}}$ $+I^2_{W_2(\mathrm{RMS})}R_{W_2} + P_\mathrm{V}V_\mathrm{e}$	P_T
P_{loss}	$P_L + P_D + P_S + P_C + P_T$	15.26W	=	13.75W	$P_L + P_D + P_S + P_C + P_T$	P_{loss}

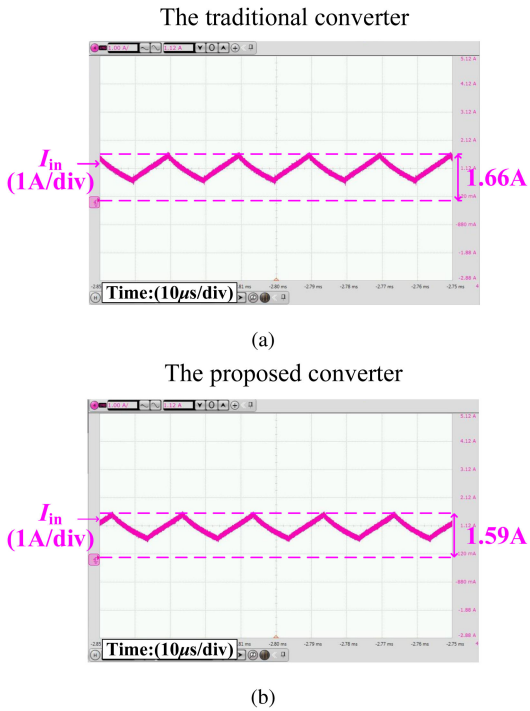


Fig. 13. Experimental results—input current. (a) I_in of the traditional single-phase boost push–pull converter prototype. (b) I_in of the novel single-phase boost push–pull converter prototype.

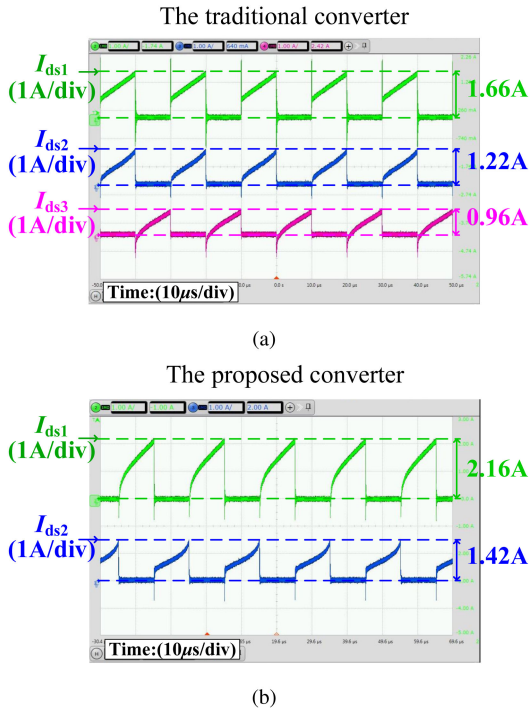


Fig. 14. Experimental results of switches' voltage stresses. (a) $V_{\mathrm{ds}1}$, $V_{\mathrm{ds}2}$, and $V_{\mathrm{ds}3}$ of the traditional single-phase boost push–pull converter prototype. (b) $V_{\mathrm{ds}1}$ and $V_{\mathrm{ds}2}$ of the novel single-phase boost push–pull converter prototype.

has one less switch than the traditional single-phase boost push–pull converter.

Fig. 13(a) and (b) shows the input current of the traditional single-phase boost push–pull converter and the novel single-phase boost push–pull converter, respectively. Its input current is slightly smaller than that of the traditional single-phase boost push–pull converter, which also substantiated our previous observation that the novel single-phase boost push–pull converter has higher efficiency.

Fig. 14(a) and (b) depicts the voltage stresses of switches in the traditional single-phase boost push–pull converter and the novel single-phase boost push–pull converter. It can be seen that

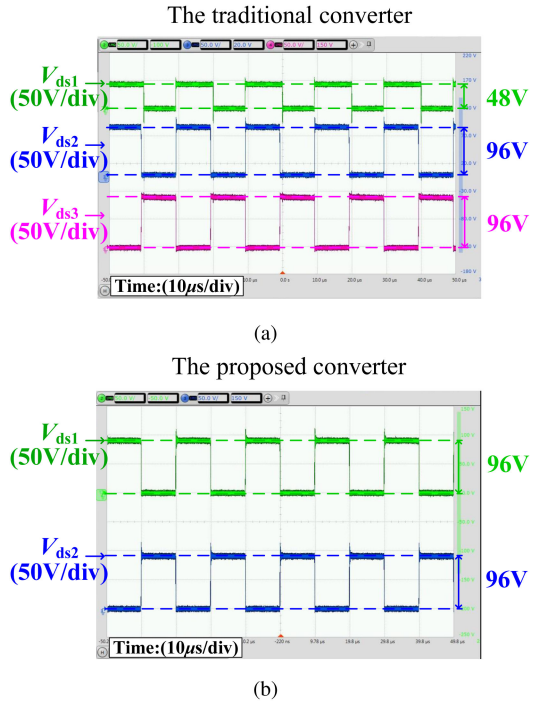


Fig. 15. Experimental results of switches current stress. (a) I_{ds1}, I_{ds2}, and I_{ds3} of the traditional single-phase boost push–pull converter prototype. (b) I_{ds1} and I_{ds2} of the novel single-phase boost push–pull converter prototype.

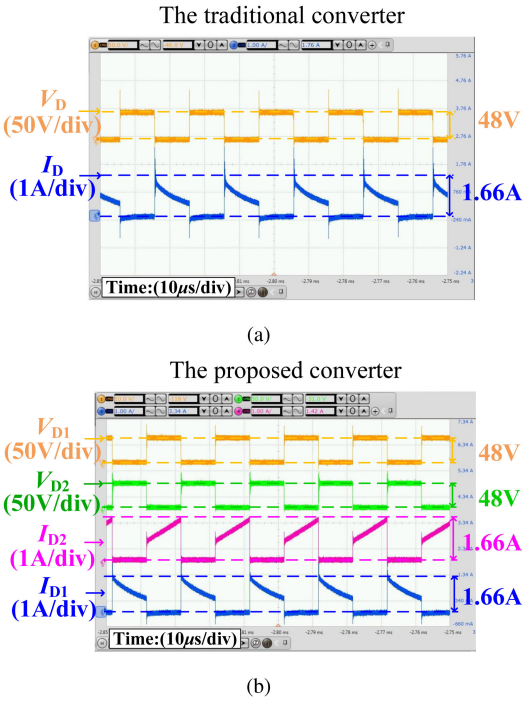


Fig. 16. Experimental results of diodes' voltage and current stresses. (a) V_D and I_D of the traditional single-phase boost push–pull converter prototype. (b) V_{D_1}, I_{D_1}, V_{D_2}, and I_{D_2} of the novel single-phase boost push–pull converter prototype.

the switches in the novel single-phase boost push–pull converter have the same voltage stress as the switches in the traditional single-phase boost push–pull converter.

Fig. 15(a) and (b) describes the current stresses of switches in the traditional single-phase boost push–pull converter and the novel single-phase boost push–pull converter. It can be seen that due to the reduction of a switch, the current stresses of the switches in the novel single-phase boost push–pull converter increases. Fig. 16(a) and (b) depicts the current stresses of diodes in the traditional single-phase boost push–pull converter and the novel single-phase boost push–pull converter.

The efficiency curves of the traditional single-phase boost push–pull converter and the novel single-phase boost push–pull converter are shown in Fig. 17. It can be seen that the power loss is reduced due to the reduction of a switch. Therefore, the novel single-phase boost push–pull converter has higher efficiency. In addition, when the output power is 100 W, the efficiency of the traditional single-phase boost push–pull converter prototype and the novel boost single-phase push–pull converter reach their maximum values, i.e., 86.76% and 87.91%, respectively. The breakdown of power loss and comparison of loss analysis between the traditional converter and the proposed converter are shown in Fig. 18 and Table V.

The above experimental results prove that the output of the traditional single-phase boost push–pull converter is the same as that of the novel single-phase boost push–pull converter, provided S_1 and S_2 have the same conduction sequence. Furthermore, the novel single-phase boost push–pull converter also reduces the number of switches. This proves that the proposed

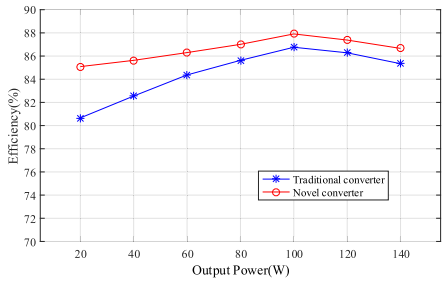


Fig. 17. Efficiency curves.

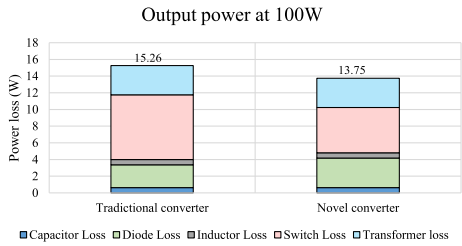


Fig. 18. Power loss breakdown at 100-W output power.

method can simplify converter topologies without affecting its essential functions. The limitation of the proposed TSM for the boost push–pull converter lies in that the switches must have the same conduction sequence; otherwise, the topology of the single-phase boost push–pull cannot be simplified. In practice,

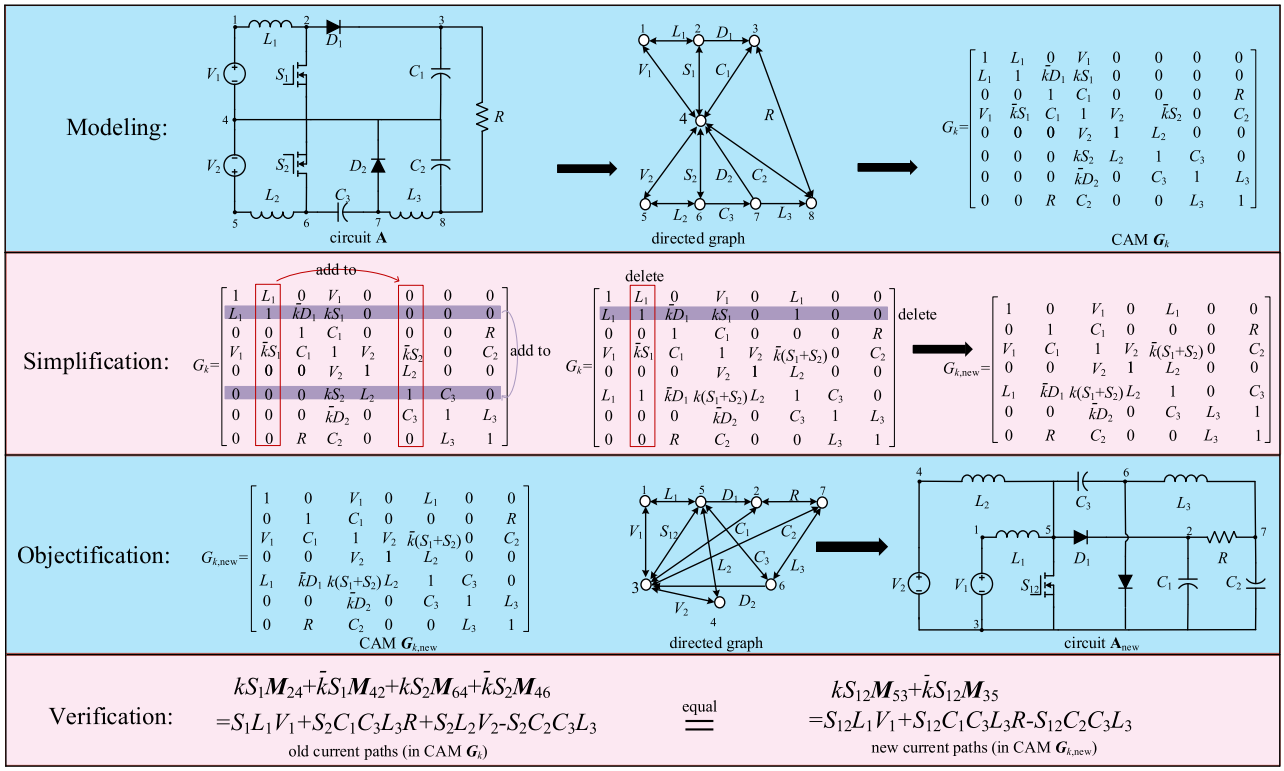


Fig. A1. Derivation of the single-switch adder converter using the proposed TSM.

converters only need to achieve specific functions, and the conduction sequence of switches is relatively fixed. Therefore, the proposed TSM, though moderately limited, can still be applied to various cases where switches switching sequences are fixed.

VII. Conclusion

In this article, we have presented a graph theory-based systematic approach to simplify the topology of power converters. Four steps of modeling, simplification, objectification, and verification constitute the TSM. A graph theory abstraction rule, node-merging rule, and current path reduction rule have been proposed and employed for modeling, simplification, and verification. The derivations of the popular SEPIC and CF-DAB converters have successfully verified the TSM and also proved that these two popular converters cannot be further simplified. A novel single-phase boost push–pull converter is proposed using the TSM. Simulations and experiments show that the novel single-phase boost push–pull converter can reduce the number of switches, while retaining the voltage gain of the traditional single-phase boost push–pull converter. The proposed TSM can be further used for other industrial application for topology simplification to improve the efficiency and reduce costs of power converters.

Limitation of the Work: This article aims to propose a systematic method of simplifying converters by proposing a graph-theory modeling approach. The novel boost single-phase push–pull converter is used as an example of this approach, with additional two examples supplemented in the Appendix. There are other obvious examples, such as the SEPIC and CF-DAB. The proposed converter TSM reduces the number of switches and some other components, which saves costs and reduces product sizes. On the other hand, this method may sometimes lower the versatility of converters for certain topologies. It is noted that power electronics design always targets certain applications, and there are many practical applications for power converters that do not require the most versatile control mechanism to produce the desired output voltage with high efficiency and low cost. As long as controlling the remaining components of the converter can achieve the desired converter function, this limitation is considered acceptable.

Appendix A
Two Examples to Illustrate the Proposed Graph-Modeling-Based TSM

To better illustrate the working principle of the proposed graph-modeling-based TSM, we give two other examples here, which do not have the limitation of switches having the same switching sequence. Fig. A1 shows the process of deriving the single-switch adder converter using the TSM, and Fig. A2 describes the process of deriving the single-switch subtracter converter using the TSM.

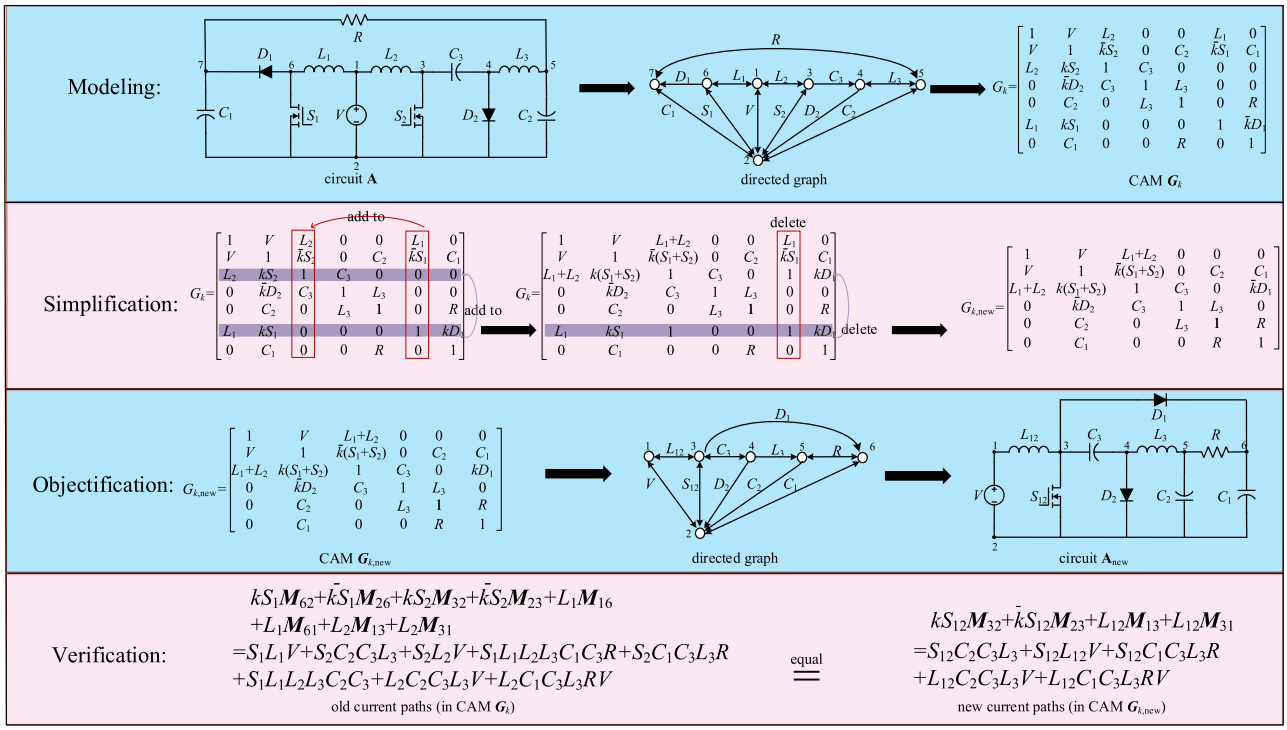


Fig. A2. Derivation of the single-switch subtracter converter using the proposed TSM.

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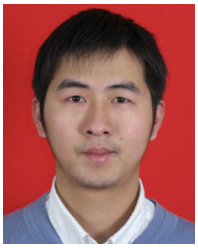

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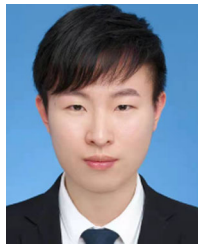

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