# Letters

## Two-Step Robust Design of *LLC* Converter With Corner Judgment and Greedy Algorithm

Xueyi Wang, *Student Member, IEEE*, Guiping Du, Mingtao Wu, Qingliang Song, and Yu Chen

***Abstract*—Negative effects caused by parameter fluctuation (PF) of resonant elements have not been thoroughly considered in the current design methodologies of *LLC* converters. In this letter, typical negative PF effects are revealed as restriction violation and optimization degradation. Then, a novel two-step robust design methodology is proposed for *LLC* converters. The first step is to effectively establish more reliable solving domain considering PF effects on all the restrictions by the proposed corner judgment method. In the second step, the lowest fluctuation efficiency as the novel concept is proposed and taken as the global optimization goal of efficiency due to optimization degradation, with a greedy algorithm proposed for simplicity and effectiveness. Simulation and experimental results have proved the validity and superiority of the proposed design methodology.**

***Index Terms*—Design methodology, optimization methods, robustness.**

### NOMENCLATURE

| | |
|---|---|
| PO | Typical operation mode of *LLC* converter. |
| PODM | Traditional PO-mode-based design methodology. |
| POMS | PO-mode solver. |
| PF | Parameter fluctuation. |
| CJ | Corner judgment. |
| MB | Monotonous boundary. |
| NMB | Nonmonotonous boundary. |
| LFE | Lowest fluctuation efficiency. |
| HG | Highest gain. |
| FL | Full load. |
| ML | Minimal load. |
| *SS* | Loose solving domain regardless of PF effects. |
| *S* | Final solving domain considering PF effects. |
| $\eta_{\mathrm{LFE\_}GB}$ | Globally highest LFE. |
| $\eta_{\mathrm{LFE\_}C}$ | LFE of the current design candidate. |
| $\eta_{N\_CB}$ | Currently highest nominal efficiency. |
| $L_m$ | Real magnetic inductance considering PF. |
| $L_r$ | Real resonant inductance considering PF. |
| *K* | Real inductor ratio considering PF. |
| $C_r$ | Real resonant capacitance considering PF. |
| $L_{mN}$ | Designed nominal magnetic inductance. |
| $L_{rN}$ | Designed resonant inductance. |
| $K_N$ | Designed nominal inductor ratio. |
| $C_{rN}$ | Designed nominal resonant capacitance. |
| $\alpha$, $\beta$, and $\gamma$ | Fluctuation percentages referring to designed nominal values. |

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### I. INTRODUCTION

SINCE the fundamental *LLC* converter was proposed in [1], it has been emerged and widely applied to many industrial applications [2]–[4] due to simple topology, zero-voltage switching (ZVS) capability within the whole load range, high efficiency, and so on. In view of convenience and cost, the most classical pulse frequency modulation (PFM) is still adopted in most *LLC* converters. Fig. 1(a) shows the common framework of designing PFM-based *LLC* converters [5]–[8], which mainly suffers two challenges.

The first one is that conflicts exist between the simplicity and accuracy for establishing the model solver of *LLC* converters: for simplest fundamental harmonic analysis [5], serious accuracy drop occurs when operating frequency is far from the series resonant frequency; time-domain analysis [6], [7] is of the highest accuracy but it also suffers complex design procedures and heavy computational burden. Recently, a PO-mode-based design methodology (PODM) was proposed in [8]. Instead of multiple modes of *LLC* converters, only PO mode [9] is adopted when operating frequency deviates from the resonant frequency, which leads to effective PO-mode solver (POMS) with satisfying accuracy and less decision parameters. Moreover, restrictions are only required to be checked at the worst case of PO modes, i.e., highest gain (HG) and full load (FL). Overall, PODM realizes nice tradeoff between the conflicts and, thus, is adopted in this letter. In other words, the *LLC* converter in this letter

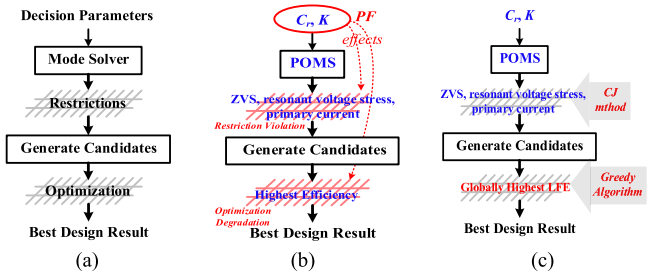


Fig. 1. Frameworks of designing PFM-based *LLC* converter. (a) Common framework. (b) Specific framework of PODM with negative PF effects. (c) Specific framework of the proposed robust design methodology.

only operates in PO mode. A specific framework of PODM is presented in Fig. 1(b).

The second one is that resonant elements all have parameter fluctuation (PF) due to various temperatures, frequencies, and so on [10], [11], whose negative effects are ambiguous in the conventional design methodologies [5]–[8]. Analysis of negative PF effects on the voltage-conversion ratio (VCR) of resonant dc transformers (DCTs) was first presented in [11]. Since open-loop control with a fixed frequency that is equal to the designed resonant frequency is applied to DCTs, PF will incur fluctuation of nominal VCR, which should be maintained by robust design procedures. However, PF may also affect other restrictions, such as ZVS realization, resonant voltage stress, and so on, while these effects were not considered by the robust design procedures in [11]. For example, it is not clear whether ZVS realization can be guaranteed when risking PF. In other words, PF may cause restriction violation when applying conventional design methods. In addition, although optimal nominal parameters that result in globally highest nominal efficiency are obtained in current design methodologies of resonant converters [6]–[8], [11]–[13], PF may unexpectedly incur practical efficiency that is lower than the designed optimal nominal efficiency, leading to optimization degradation.

Typically, negative PF effects on the traditional design methodologies are summarized as restriction violation and optimization degradation. In particular, negative PF effects on the conventional PODM are visualized in Fig. 1(b).

In order to further strengthen design robustness for *LLC* converters, a two-step robust design methodology derived from PODM is proposed. The first step is to establish the solving domain that only contains design candidates of resonant parameters that meet with all the restrictions robustly when suffering PF, with an effective corner judgment (CJ) method proposed. In the second step, a novel concept called lowest fluctuation efficiency (LFE) is proposed and taken as the global optimization goal of efficiency due to optimization degradation, with a greedy algorithm specifically targeted at LFE optimization proposed. The framework of the proposed design methodology is shown in Fig. 1(c).

The rest of this letter is organized as follows. Section II provides the definitions of PF and its negative effects on restrictions and optimization, with the novel concept LFE proposed.

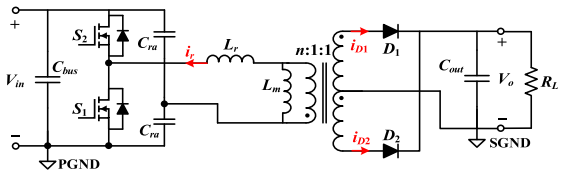


Fig. 2. Structure of the SHB *LLC* converter.

Section III provides the procedures of the proposed design methodology in detail. Section IV provides the simulation and experimental results to verify the validity of theories with comparative analysis. Finally, Section V concludes this letter.

## II. Basic Theory of PF

The structure of the symmetrical half-bridge (SHB) *LLC* converter is shown in Fig. 2, where resonant components include magnetic inductor $L_m$, resonant inductor $L_r$, and two resonant capacitors with equivalent resonant capacitance $C_r = 2C_{ra}$ [14]. It is noted that the *LLC* converter, as shown in Fig. 2, is just an example for the implementation of the proposed design methodology that is also applicable for asymmetrical half-bridge and full-bridge *LLC* topologies [8], [15].

### A. Definition of PF

Definitions for PF of resonant parameters are given as

$$\begin{cases} L_m \in [1-\alpha, 1+\alpha]\, L_{mN} = [L_{mN-}, L_{mN+}] \\ L_r \in [1-\beta, 1+\beta]\, L_{rN} = [L_{rN-}, L_{rN+}] \\ C_r \in [1-\gamma, 1+\gamma]\, C_{rN} = [C_{rN-}, C_{rN+}] \end{cases} \tag{1}$$

where $L_{mN}$, $L_{rN}$, and $C_{rN}$ are the nominal resonant parameters; $\alpha$, $\beta$, and $\gamma$ are the fluctuation percentages referring to the nominal values. Then, PF of inductor ratio *K* is derived as

$$K = \frac{L_m}{L_r} \in \left[\frac{1-\alpha}{1+\beta}, \frac{1+\alpha}{1-\beta}\right] K_N = [K_{N-}, K_{N+}] \tag{2}$$

where $K_N = L_{mN}/L_{rN}$ is the nominal inductor ratio.

### B. Effects of PF on Boundary Restrictions

Boundary restrictions, such as ZVS restriction, voltage stress restriction, magnetic saturation restriction, and so on, are essential for designing *LLC* converters. In the conventional PODM, all the boundary restrictions can be turned into lines in the $C_r - K$ plane. Derived from PODM, $(C_{rN}, K_N)$ is, thus, adopted as the decision parameter group of the proposed design methodology, as shown in Fig. 1(c).

To simplify the analysis, the monotonous boundary (MB) is primarily taken as an example. As for conventional PODM regardless of PF, it is just guaranteed that the single nominal point $N(C_{rN}, K_N)$ is located in the area permitted by the MB restriction, as shown in Fig. 3(a). However, due to PF, the nominal point is expanded into an adjacent area, i.e.,

$$\Omega\left(C_{rN}, K_N\right) = \left\{\left(C_r, K\right) \middle| C_r \in \left[C_{rN-}, C_{rN+}\right], K \in \left[K_{N-}, K_{N+}\right]\right\} \tag{3}$$

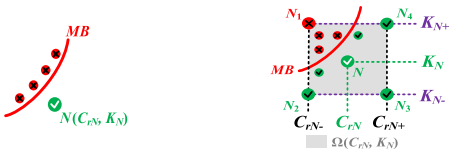


Fig. 3. PF effects on restrictions in the case of MB. (a) Conventional design without considering PF. (b) Failure in the MB restriction caused by PF.

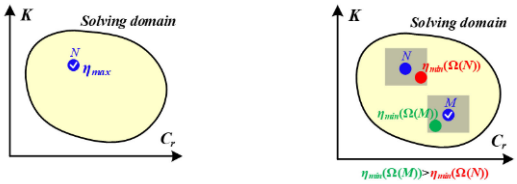


Fig. 4. PF effects on optimization of efficiency. (a) Conventional design without considering PF. (b) Optimization degradation caused by PF.

where the MB restriction should be permanently satisfied with. By contrasting Fig. 3(a) and (b), it can be seen that restriction violation may occur due to the potential failure region containing the point $N_1$ when suffering PF.

### C. Effects of PF on Efficiency Optimization

Based on the boundary restrictions, the solving domain can be established in the $C_r - K$ plane. For the conventional PODM regardless of PF, only the point *N* in the solving domain that realizes globally highest efficiency $\eta_{\max}$ is taken as the optimal design result, as shown in Fig. 4(a). However, as shown in Fig. 4(b), although point *N* is capable of optimal efficiency, real efficiency risks reaching the lowest efficiency generated from parameter groups that belong to the adjacent area of *N*, i.e., $\eta_{\min}(\Omega(N))$. In other words, point *N* is not the best solution in aspect of PF. If point *M* whose $\eta_{\min}(\Omega(M))$ is higher than $\eta_{\min}(\Omega(N))$ exists in the solving domain, *M* will replace *N* as the optimal design result, which means optimization degradation for conventional design.

In consequence, the lowest efficiency generated from parameter groups in the adjacent area of a nominal parameter group is defined as LFE of it. In other words, LFE represents the lowest practical efficiency that PF is likely to result in. Therefore, instead of the common concept of efficiency, the novel optimization goal of efficiency is aimed at the globally highest LFE to restrain optimization degradation caused by PF.

## III. Two-Step Robust Design of *LLC* Converter

To intensify design robustness, a two-step robust design methodology originated from PODM is proposed in this letter. Since POMS based on time-domain analysis and relevant restrictions for *LLC* converters have been thoroughly presented in [8], they are directly applied in this letter. Design indices of a typical *LLC* converter application are listed in Table I. Turn ratio *n* is set as 4 to ensure near resonance for *LLC* converter with maximal input voltage.

TABLE I
Design Requirements of *LLC* Converter

| Parameter | Description |
|---|---|
| Input voltage | 320-380V |
| Output voltage | 48V |
| Output power | 48W-240W |
| Minimal switching frequency | 100kHz |

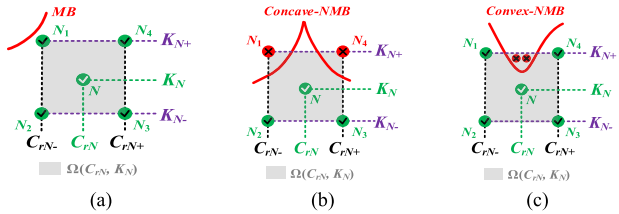


Fig. 5. Illustration of four CJ methods. (a) MB case. (b) Concave NMB case. (c) Convex NMB case.

*Step 1. Set up the solving domain considering PF by the proposed CJ method.*

In general, as shown in Fig. 1(c), the first step is to establish the solving domain that meets all the restrictions robustly. In order to prevent restriction violation effectively, the CJ method is proposed. As shown in Figs. 5(a) and 3(b), if the four corner points ($N_1$–$N_4$) are all permitted by an MB restriction, the whole adjacent area will also meet with it; otherwise, at least one corner point fails because the MB line intersects with two edges of the adjacent area. In other words, only the four corner points are required to be checked, which displays the convenience of the proposed method. Moreover, the cases of nonmonotonous boundaries (NMBs) are also presented in Fig. 5(b) and (c). As for a concave NMB line referring to the nominal point *N*, it interacts with at least two edges and, thus, the CJ method is still effective. However, the CJ method is invalid for the case of a convex NMB line that interacts with only one edge of the adjacent area.

Therefore, above all, the loose domain *SS* generated by natural restrictions without considering PF should be checked for its boundary shape in the $C_r - K$ plane, and *SS* is formed by POMS for the worst case of *LLC* converter according to PODM, i.e., minimal input voltage with HG, and minimal operating frequency and largest derivation from resonance with FL. Actually, $C_r$ varies discontinuously and its iteration step is decided by commercial capacitance values. Also, small variation of $C_r$ or *K* will cause negligible effects on guaranteeing restrictions and total efficiency, whereas it will be unrealistic with heavy computational burden. The solving domain *SS* is, thus, visualized by infinite grid points. Iteration ranges of $C_r$ and *K* can be gradually enlarged to cover the loose domain with enough margin. The fluctuation percentages are set as $\alpha = \beta = \gamma = 10\%$. As shown in Fig. 6, all the boundary lines of *SS* are monotonous, and concave nonmonotonous shapes referring to inner nominal points exist at line crossovers, which prove the validity of the proposed CJ method. Based on the *SS* domain, the real solving domain *S* considering PF is then picked out by applying the CJ method.

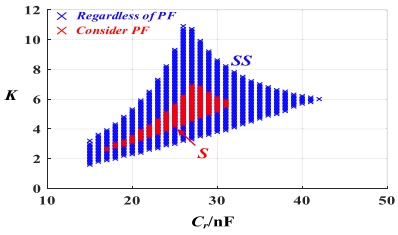


Fig. 6. Visualization of loose domain *SS* and real solving domain *S* by grid points based on the worst case, i.e., HG and FL.

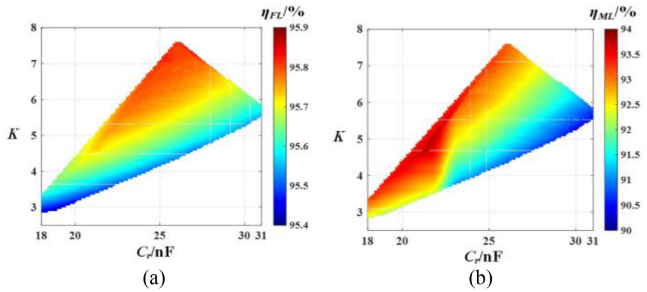


Fig. 7. Calculated efficiencies for design candidates derived from the *S* domain under HG and various load conditions. (a) With FL. (b) With ML.

*Step 2. Global optimization of LFE based on the proposed greedy algorithm.*

In general, as shown in Fig. 1(c), the second step is to obtain the best design candidate from the *S* domain for the optimization goal stated in Section II-C, i.e., globally highest LFE. However, it should be discussed what the worst condition is in aspect of LFE for better optimization value.

In the conventional PODM, efficiency optimization is aimed at the worst condition, taken as HG and FL. Nevertheless, it is noted that FL just extremely obstacles realization of the restrictions, which cannot represent the worst load level in view of efficiency or LFE. Specifically, a grid point $(C_{rN}, K_N)$ in the *S* domain determines corresponding $L_{mN}$ and $L_{rN}$ based on HG and FL by POMS, which generates a design candidate $(C_{rN}, L_{mN}, L_{rN})$ that meets with all the restrictions at the worst case and, thus, passes through them permanently in other cases. However, the efficiency performances of these design candidates should be evaluated within the whole load range. A thorough power loss model of *LLC* converter in [15] is adopted in this letter for efficiency calculation. As shown in Fig. 7(a), efficiencies vary with maximum 0.38% under HG and FL conditions with various design candidates, which restrain the value of optimization among them. In contrast, efficiencies vary with maximum 3.3% under HG and minimal load (ML) conditions, as shown in Fig. 7(b), where obtaining the optimal candidate is more valuable. Moreover, fluctuation of nominal efficiencies becomes more serious at HG and ML when suffering PF. Therefore, the optimization process of LFE is conducted under the worst HG and ML conditions.

Moreover, the core of LFE optimization is to earn the optimal adjacent area that results in globally highest LFE in the *S* domain, which represents PF ranges of the final optimal solution. It is noted that only the optimal point of the solving domain is obtained in common optimization processes [8], [11], [12], whereas the optimal adjacent area with globally highest LFE of the solving domain is obtained in the proposed methodology aiming for more robust design.

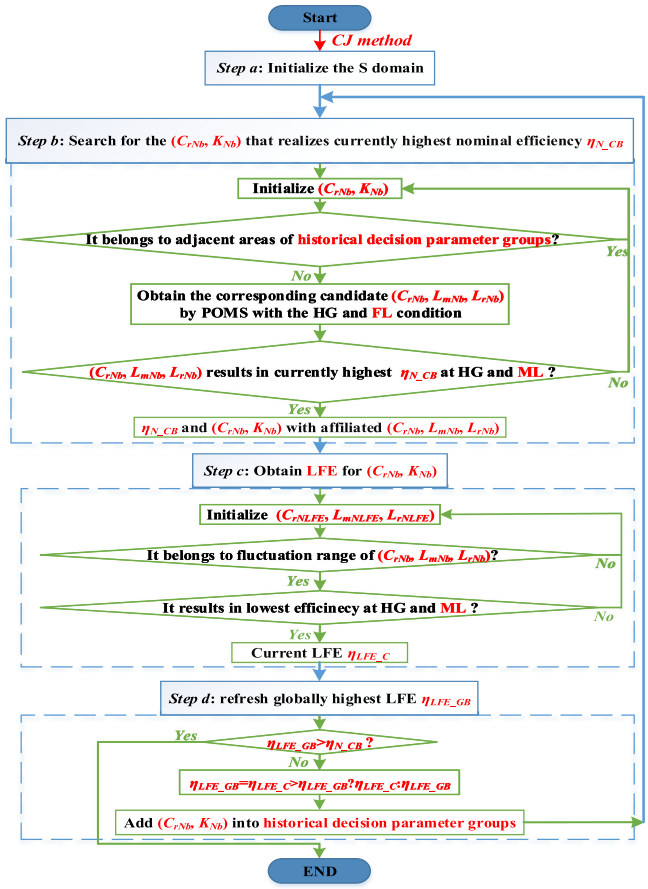


Fig. 8. Flowchart of the proposed greedy algorithm.

As a result, due to the particularity of LFE optimization, the conventional traversal search algorithm [8], [11] will suffer heavy computational burden for searching the optimal adjacent area. Although artificial intelligence (AI) algorithms [12] may be suitable for LFE optimization, they are very complicated to be applied, and they risk trapping into local optimization and slow convergence speed due to bad settings. Most importantly, the feature of LFE is not fully utilized to develop more simple and comprehensive algorithms. Therefore, a greedy algorithm is proposed for LFE optimization in this letter, with the flowchart of it, as shown in Fig. 8. Illustrations are made as follows.

*Step a*: At the beginning, establish the initial *S* domain in the $C_r - K$ plane by the CJ method.

*Step b*: Search for the decision parameter group $(C_{rNb}, K_{Nb})$ in the *S* domain that does not fall in adjacent areas of historical decision parameter groups and results in the affiliated candidate $(C_{rN}, L_{mN}, L_{rN})$ that realizes currently highest nominal efficiency $\eta_{N\_CB}$ with the worst HG and ML conditions. The affiliated candidate $(C_{rN}, L_{mN}, L_{rN})$ is obtained with the HG and FL conditions by POMS according to PODM.

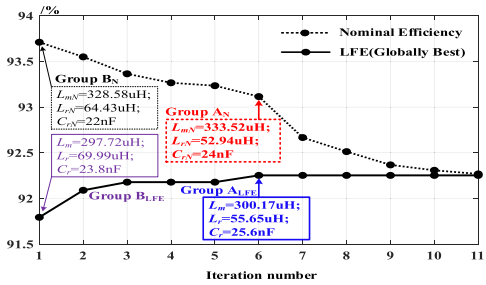


Fig. 9. Iteration process of the greedy algorithm with variation of nominal efficiency and globally highest LFE under the HG and ML conditions.

*Step c*: Search for the grid point $(C_{r\mathrm{LFE}}, L_{m\mathrm{LFE}}, L_{r\mathrm{LFE}})$ in the fluctuation range of $(C_{rNb}, L_{mNb}, L_{rNb})$ that leads to the lowest efficiency under the HG and ML conditions, and thus, LFE of the decision parameter group $(C_{rNb}, K_{Nb})$ obtained in *Step b* is figured out, denoted as $\eta_{\mathrm{LFE\_}C}$.

*Step d*: If globally highest LFE $\eta_{\mathrm{LFE\_}GB}$ is larger than $\eta_{N\_CB}$, quit the algorithm. Otherwise, refresh $\eta_{\mathrm{LFE\_}GB}$ referring to $\eta_{\mathrm{LFE\_}C}$ obtained in *Step c*; add $(C_{rNb}, K_{Nb})$ into historical decision parameter groups, and then return to *Step b*.

The core of the proposed algorithm is to obey the greedy strategy that globally highest LFE is more likely to belong to a design candidate performing higher nominal efficiency, which fully utilizes the definition of LFE and simplifies the optimization process. Besides, it is quit when globally optimal LFE $\eta_{\mathrm{LFE\_}GB}$ exceeds currently highest nominal efficiency $\eta_{\mathrm{LFE\_}C}$ obtained among all the residual candidates, which guarantees convergence of the proposed algorithm.

The iteration process of the proposed algorithm is shown in Fig. 9. Although the candidate $B_N$ (at iteration number $= 1$) reaches the globally highest nominal efficiency of 93.71%, it risks unsatisfying LFE of 91.76% for the group $B_{\mathrm{LFE}}$. By the iteration process, globally highest LFE is refreshed continuously. Eventually, the candidate $A_N$ (at iteration number $= 6$) is taken as the optimal design of nominal resonant parameters, which has the globally highest LFE of 92.25% for the group $A_{\mathrm{LFE}}$ and acceptable nominal efficiency of 93.12%.

## IV. Simulation and Experimental Results

### A. Simulation and Experimental Verification

An experimental prototype was built with the characteristics listed in Table II to verify the validity of the proposed two-step design methodology.

First, for the final optimal design result, i.e., group $A_N$, as shown in Fig. 9, it should be checked that all the restrictions are permanently met with under the worst HG and FL conditions when suffering PF. Since it is very tough to realize all the PF values of resonant elements, in reality, it is strictly verified by the simulation software. The simulation *LLC* circuit is, respectively, set with $A_N$ and other eight extreme PF groups that are generated from $A_N$. All the simulation results are provided in the supplementary file, which confirms the robustness of satisfying all the restrictions for the optimal design result $A_N$. Besides, experimental waveforms of the prototype set with the group $A_N$

TABLE II
Specifications of the Prototype

| Parameters | Values | Item | Description |
|---|---|---|---|
| Turn ratio | 28:7:7 | Transformer | Winding-type<br>Core: PQ3230<br>Material: PC47<br>Turns: 28:7:7 |
| $L_{mN}$ | 333.52uH | | |
| $L_{rN}$ | 52.94uH | Resonant inductor | Winding-type<br>Core: PQ2020<br>Material: PC47<br>Turns:33 |
| $C_{rN}$ | 24nF | Resonant capacitor | TDK, 450V, C0G |
| *Switches $S_1$, $S_2$: FCH104N60F; Diodes $D_1$, $D_2$: MBR20200 | | | |

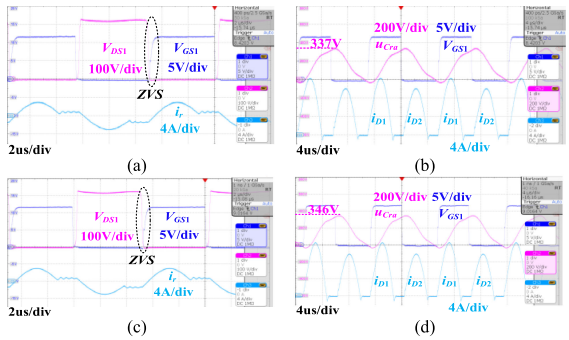


Fig. 10. Experimental waveforms under HG and FL conditions. (a) ZVS with $C_{rN}$. (b) $u_{Cra}$ with $C_{rN}$. (c) ZVS with $C_{rN-}$. (d) $u_{Cra}$ with $C_{rN-}$.

TABLE III
Comparisons Between the Simulation and Experimental Results

| Parameters | Index | Simulation | Experiment |
|---|---|---|---|
| $(C_{rN}, L_{mN}, L_{rN})$ | ZVS realization | YES | YES |
| | Resonant voltage stress | 334.2V | 337V |
| | Primary current stress | 2.95A | 3.05A |
| $(C_{rN-}, L_{mN}, L_{rN})$ | ZVS realization | YES | YES |
| | Resonant voltage stress | 341.1V | 346V |
| | Primary current stress | 2.94A | 3.05A |

under the HG and FL conditions are shown in Fig. 10(a) and (b), where ZVS, acceptable resonant voltage stress, and primary current stress are realized. In contrast, the resonant capacitance is changed from $C_{rN}$ of the group $A_N$ to $C_{rN-}$ for extreme PF, and all the restrictions are still satisfied, as shown in Fig. 10(c) and (d). What is more, comparisons between the simulation and experimental results about restrictions are displayed in Table III, which proves the acceptable accuracy of the simulation results and validity of simulation verification.

Second, the validity of the proposed greedy algorithm should also be verified briefly due to the impossible realization of all the PF values in reality. It is noted that if the converter is set with the parameter group $B_N$, it will certainly suffer the worst parameter group $B_{\mathrm{LFE}}$ that leads to LFE in the PF range of $B_N$. In other words, if it is proved by experiment that the efficiency level for $B_{\mathrm{LFE}}$ is lower than its counterpart of $A_{\mathrm{LFE}}$ that also reaches LFE for $A_N$, the core of the algorithm is, thus, verified. Therefore, efficiency curves of various prototypes set with group $A_N$, $A_{\mathrm{LFE}}$, and $B_{\mathrm{LFE}}$, as shown in Fig. 9, respectively, are measured with HG and various load levels, as shown in Fig. 11. The order of whole levels of efficiency curves within the whole load range for the three groups is $A_N$>$A_{\mathrm{LFE}}$>$B_{\mathrm{LFE}}$ and the experimental

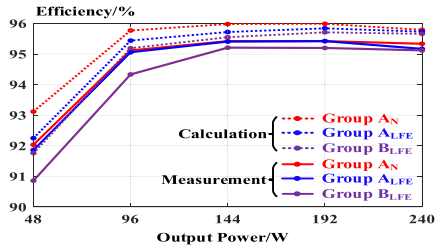


Fig. 11. Efficiency curves corresponding to various prototypes set with different groups of resonant parameters under HG and various output powers.

TABLE IV
COMPARISONS IN ASPECT OF ALGORITHM

| Reference | [5]-[8] | [12] | Our work |
|---|---|---|---|
| Algorithm | Traversal Method | AI-based Algorithm | Greedy Algorithm |
| Complexity | Low | High | Low |
| Calculation time of being applied for LFE optimization | 2000ms | Highest 160ms (highly depend on initial settings) | 170ms |
| Risk trapping into local optimization | No | Yes | No |

result at ML for group $A_{\mathrm{LFE}}$ approximates the calculated result that is theoretical LFE for $A_N$, which confirm the validity of the proposed algorithm. It is mentioned that $A_{\mathrm{LFE}}$ also matches with the globally highest LFE, whereas $B_{\mathrm{LFE}}$ matches with a lower LFE, which is generated by $B_N$ that realizes globally highest nominal efficiency.

### B. Comparative Analysis and Expectation

Comparative analysis to previous work is mainly conducted in the following two aspects.

1) *In aspect of the algorithm:* Table IV lists comparisons between applying traditional algorithms and the proposed algorithm in the second step, which confirms the specific superiority of the proposed algorithm for LFE optimization. Moreover, only the four corner points are required to be checked in the proposed CJ method, showing its effectiveness.
2) *In aspect of PF:* It can be inferred that both restriction violation and optimization degradation caused by PF have not been paid any attention in common design methodologies of *LLC* converter [5]–[8]. Besides, in [11], only the restriction of VCR is considered with PF effects on other restrictions ignored, and optimization degradation is also ignored.

As a result, it is highlighted that negative PF effects are thoroughly addressed in the proposed design methodology derived from PODM, whose framework, as shown in Fig. 1(c), can be converted and applied for other design methodologies and applications. In this regard, the proposed CJ method in the first step can be further improved to deal with multiple decision parameters; in the second step, the proposed concept of LFE with the greedy algorithm may be applied to deal with other issues, such as output ripple, which deserves to be further studied in the future work.

## V. CONCLUSION

In this letter, a two-step robust design methodology derived from PODM is proposed for *LLC* converters for defending typical negative PF effects that are revealed as restriction violation and optimization degradation. More reliable solving domain considering PF is effectively obtained by the proposed CJ method. Also, the novel concept called LFE is proposed and taken as the novel optimization goal of efficiency for restraining optimization degradation, with LFE optimization effectively conducted by the proposed greedy algorithm. Simulation and experimental results have proved the validity of the proposed design methodology. What is more, the framework of the proposed methodology can be applied for other design methodologies and applications for intensifying design robustness.

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