Thermal Mitigation and Optimization Via Multitier Bond Wire Layout for IGBT Modules Considering Multicellular Electro-Thermal Effect

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***Abstract*—The stitch wire configuration is widely adopted for large-area IGBT chips. However, an inhomogeneous wire current density introduces uneven self-heating and nonuniform chip heating, which exacerbates the chip thermal stress. In this article, a multicellular electro-thermal model considering the stitch-bonding wires is derived to optimize the wire layout parameters. Furthermore, the current density alleviation of wire bonds is investigated to be the most sensitive and effective method to comprehensively mitigate the thermal nonequilibrium and local overheating. Consequently, an improved multitier layout is proposed to further achieve thermal stress suppression without any additional components and advanced materials. Finally, a triple-tier-bonded IGBT module with optimal design parameters is fabricated to validate the thermal mitigation performance. The prototype experimental results demonstrate that the modeling error is less than 3.0%. The multitier layout decreases the current density by 57.6%, hence, the maximum and average chip temperature are reduced by 21.8% and 12.4%, respectively.**

***Index Terms*—Electro-thermal coupling, Fourier series, multitier layout, physics-based IGBT model, stitch-bonding wire, three-dimensional (3-D) multicellular equivalent circuit, wire layout optimization.**

I. Introduction

IGBT modules are prevailing devices for high power applications including EV motor drives, renewable energy inverters, and solid-state transformers. The high power is achieved by the parallel connection of IGBT chips [1]. The emitter pad on the chip surface is connected to the substrate via wedge wire bonding. However, the bonding wires deliver an equal amount of current as the chips, the power dissipation causes expansion of the materials. Because of the coefficient of thermal expansion (CTE) mismatches among IGBT die (2.6 ppm/K) and aluminum wires (23.5 ppm/K), wire bond contacts are subjected to severe thermo-mechanical stress and regarded as the weakest parts in the wire-bonded modules [2]. The weakest bonding contact lifts off and the remaining wires conduct higher current, which eventually results in a cascading failure for the IGBT module [3]. Hence, how to suppress the thermo-mechanical stress and enhance the reliability level for the bonding contact becomes an urgent problem to the module design.

There have been several approaches to improve the bonding contact against thermo-mechanical stress, mainly from three aspects: material, structure, and wire layout. The material-related methods are to replace the aluminum (Al) wire with materials close to the CTE value of silicon, represented by copper (Cu), Al-clad Cu, and novel Al-alloys. The structure-associated methods focus on reshaping the connection parts or inserting external components, symbolized by direct lead bonding, flexible circuit board sintering, molybdenum-based strain buffer soldering [4], and flip-chip bonding [5]. However, the aforementioned methods require expensive preparation and complex plating processes, which are not practical in applications.

To effectively mitigate the thermal stress of bonding contact, diversified wire layout patterns were implemented to minimize the chip temperature distribution [6]–[11]. Among these patterns, stitch wire is recognized as the most compelling, which can be defined as one wire with more than one bonding contact on chip. The comparison between stitch wire and conventional wire is shown in Fig. 1. The increased number of bonding contacts is beneficial to current density reduction around the bond feet in chip metallization. In [6], the maximum current density of the chip metallization is reduced by 20% when one more bonding contact is simply introduced, which results in a four-fold improved power cycling performance. Hence, the stitch-bonding pattern is widely adopted in large-area chips [12].

However, as the chip current rating continues to increase, the stitch-bonding contact number is boosting, the current density induced by the ohmic self-heating effect cannot be ignored [13].

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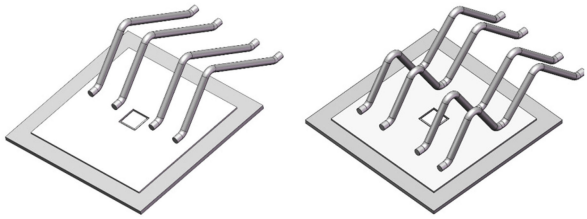

Fig. 1. (a) Conventional wire. (b) Stitch wire.

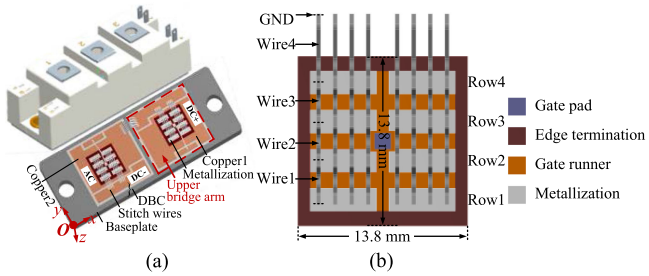

Fig. 2. Schematic of the baseline IGBT module. (a) Package outline and configuration. (b) Diagram of stitch-wire-bonded chip.

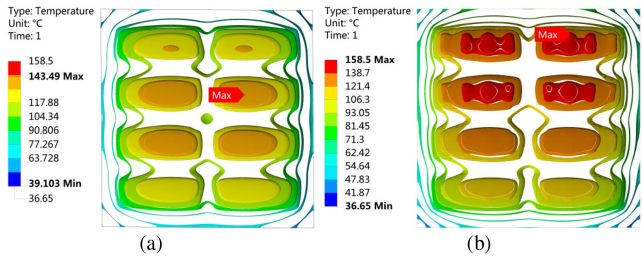

Fig. 3. Comparison of temperature distribution on chip. (a) Discounting the current flow of wires. (b) Considering the current flow of wires. ($I_{\rm chip} = 250$ A).

Furthermore, due to the electrical connection characteristics, an inhomogeneous current density would flow through the stitch wires and introduce uneven self-heating to the chip. This uneven self-heating effect will cause chip local overheating, which accelerates the degradation of bonding contacts. So far, the aforementioned models considering the stitch wire do not take the uneven self-heating effect into account. Moreover, few existing studies have focused on the electro-thermal distribution caused by the stitch-configuration influence. Therefore, the formation mechanism of chip temperature has not been comprehensively understood.

In this article, a high-accuracy three-dimensional (3-D) multicellular electro-thermal model for the stitch-wire-bonded IGBT module is proposed, which takes into account the comprehensive contribution of bonding wires to the voltage potential and temperature rise of chip. Thereafter, the principle of bonding contact number on the chip temperature is profoundly revealed, and the optimal contact number is uncovered for the local overheating suppression and thermal equilibrium improvement, which is expected to be developed into the guideline for the layout design of bonding wires. On this basis, a novel multitier bonding layout pattern is proposed to supplementarily achieve thermal stress suppression without any additional components and advanced materials, which can be an excellent candidate for industrial applications.

The rest of this article is organized as follows. The stitch-bonding property induced local overheating problem is illustrated and the impact mechanism is preliminarily analyzed in Section II. The contribution of bonding wires to the chip is completely modeled by the 3-D multicellular electro-thermal coupling process in Section III. Based on these, a two-step thermal mitigation method by bonding contact optimizing and wire current mitigation is proposed in Section IV. The experimental validation results are provided in Section V. Finally, Section VI concludes this article.

II. Problem Description: Stitch-Bonding Property Exacerbates Thermal Stress in IGBT Modules

A. Configuration of Stitch-Wire-Bonded IGBT Modules

The configuration of baseline stitch-wire-bonded IGBT module is displayed in Fig. 2, where the well-known 34 mm packaging platform is selected. As shown in Fig. 2(a), a half-bridge power module is designed to place a single IGBT chip for each bridge arm. Considering the symmetry of overall layout and avoiding the thermal coupling effect, it is feasible to investigate and evaluate the electro-thermal performance of the upper bridge arm, which is marked by red lines.

The diagram of stitch-wire-bonded IGBT is depicted in Fig. 2(b). The active area is established by excluding the gate pad and edge termination. According to the predesigned bonding contact number N, the active area is further divided into N parts, separated by the gate runner [14]. The active area turns bondable after covered with metallization. As shown in Fig. 2(b), the active area of the selected 1200 V/200 A IGBT chip is preliminarily divided into four rows of cells by the crossed gate runners. The stitch-bonding wires are split into four wire arches accordingly. The numbering rule is based on the current flow direction from the chip on Copper 1 to Copper 2.

B. Characteristics of Stitch-Bonding Wires on Chip

To analyze the self-heating effect of stitch-bonding wires on the chip, a 3-D IGBT module is imported into Ansys thermal-electric model and is simulated with finite element method (FEM). The current source with 250 A is set at Copper 1 (see Fig. 2). The eight metallization layers are set as the ground when overlooking the wires, while Copper 2 is set as the ground when considering the wires. The simulation results when the current flow of stitch-bonding wires is discounted or considered are displayed in Fig. 3. It is exhibited that the chip temperature is symmetrically distributed when discounting the wires, where $T_{\rm row2}$ (143.5 °C) $= T_{\rm row3} > T_{\rm row1}$ (131.9 °C) $= T_{\rm row4}$. The highest temperature is located in the second or third row of cells, owing to the transverse heat conduction effect with the soldered direct bonding copper (DBC). While when considering the wires, the heat is generated in the chip and wires at the

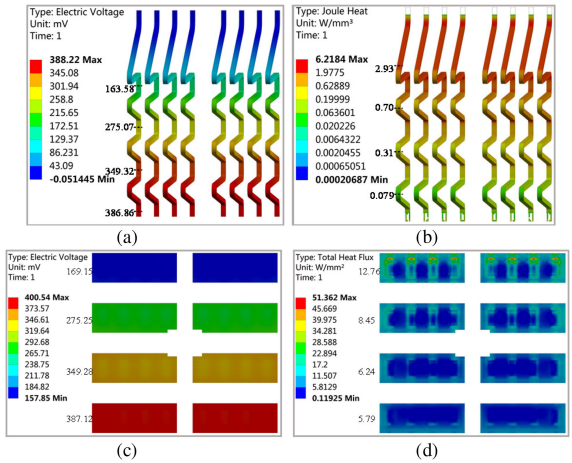

Fig. 4. (a) Electric potential distribution of wires. (b) Joule heat distribution of wires. (c) Electric potential distribution of active region in chip. (d) Power dissipation distribution of active region in chip. ($I_{\rm chip} = 250$ A).

same time. The self-heating caused by wire current introduces a temperature rise of up to 15.01 °C (12.4%). Note that the introduced temperature rise is uneven among different rows of chip cells, where $T_{\rm row4}$ (158.5 °C) $> T_{\rm row3}$ (151.54 °C) $> T_{\rm row2}$ (130.49 °C) $> T_{\rm row1}$ (108.82 °C) specifically.

To further interpret the mechanism of chip temperature formation, the related electrical parameter distribution of wires and chip is displayed in Fig. 4. It is revealed that the electric potential of wire decreases nonuniformly along the current direction, where $\triangle V_{12} = 37.54$ mV, $\triangle V_{23} = 74.25$ mV, $\triangle V_{34} = 111.49$ mV, and $\triangle V_{4G} = 163.58$ mV. Since the length of wire arch is equal, it indicates that the wire arch current is unbalanced. The uneven ohmic Joule self-heating power distribution of wire can further verify it, which is shown in Fig. 4(b). The extremely unbalanced wire self-heating introduces uneven temperature rise on chip, which directly causes $T_{\rm row4} > T_{\rm row2} > T_{\rm row1}$. Simultaneously, the stitch-bonding configuration also makes the chip emitter surface potential present an inhomogeneous distribution characteristic, where the potential value is in conformity to that of wires. The inhomogeneous emitter potential results in non-uniform cell current, which is intuitively expressed by heat flux in Fig. 4(d). The shown cell heat flux value of a row has been averaged, where the maximum imbalance degree between row4 and row1 is up to 54.6%. Consequently, the severely unbalanced cell current further exacerbates local overheating on chip, which additionally motivates $T_{\rm row4} > T_{\rm row3}$.

Thus, the local overtemperature field formation of the stitch-wire-bonded chip is summarized as induced by the following.

1) Unbalanced wire current brought uneven wire self-heating.
2) Inhomogeneous electric potential introduced nonuniform cell heat flux.

III. Multicellular Electro-Thermal Modeling of Stitch-Wire-Bonded IGBT Module

In order to avoid the potential overheating effect, the stitch wires should be delicately designed. The fundamental design parameters include wire number, bonding contact number, arc height, arc angle, and diameter. However, existing FEM commercial software demands redrawing the geometric diagram and redividing the element when adjusting the design parameters. A proposed modeling method in this section, whose results can be obtained directly corresponding to numerous combinations of wire design parameters, can remarkably speed up the design iteration and validation for bonding wire layout.

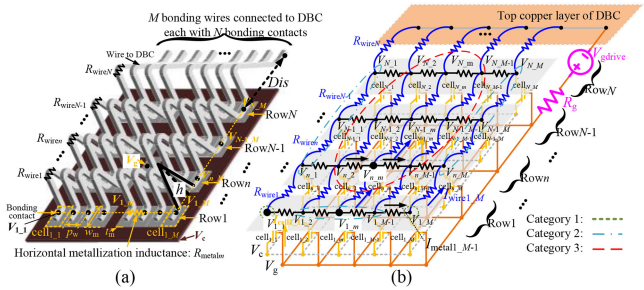

Fig. 5. (a) General geometry structure of chip with stitch-bonding wires. (b) Three-dimensional multicellular circuit with resistances of wires and metallizations.

A. Three-Dimensional Multicellular Circuit With Stitch-Bonding Wire

A proposed 3-D multicellular circuit with wire resistance and metallization resistance is employed to describe the imbalance in current and voltage between chip cells. The general geometry structure of M stitch-bonding wires each with N bonding contacts is illustrated in Fig. 5(a). The fifth to $(m-1)$th bonding wire, second to $(n-1)$th, and $(n+1)$th to $(N-2)$th chip metallization are not drawn in the figure. The active region beneath the metallization layer can be divided into $N \times M$ cells in accordance with the contact number N and wire number M. Each IGBT cell model is scaled with a physics-based IGBT model. The bonding contact potential is consistent with the cell emitter terminal potential, which is marked with V_{n_m}. The subscript is successively defined by the serial number of bonding contacts and bonding wires. The wire arch is treated as two intersecting line elements, which form an equivalent isosceles triangle structure, as marked in Fig. 5(a). The wire arch length is determined by the arc height h, contact number N, and chip width $W_{\rm chip}$. The $(M-1)$ horizontal metallization resistance $R_{{\rm metal}\,m}$ is determined by the thickness of metallization layer $t_{\rm m}$, wire number M, chip length $L_{\rm chip}$, metallization width $w_{\rm m}$, and electrical conductivity $\rho_{\rm metal}$; while the longitudinal metallization resistance in parallel with wire can be ignored since it is about ten times larger than wire arch resistance $R_{{\rm wire}\,n}$, owing to the relatively smaller cross-sectional area of metallization layer [15]. The wire arch resistance and horizontal metallization resistance can be expressed as

$$\begin{cases} R_{{\rm wire}n} = 2\rho_{\rm Al}\dfrac{\sqrt{(W_{\rm chip}/2N)^2+h^2}}{\pi(d/2)^2}, 1 \le n \le N-1 \\ R_{{\rm wire}N} = 2\rho_{\rm Al}\dfrac{\sqrt{(Dis/2)^2+h^2}}{\pi(d/2)^2}, R_{{\rm metal}m} = \rho_{\rm metal}\dfrac{L_{\rm chip}}{Mt_{\rm m}w_{\rm m}} \end{cases} \quad (1)$$

where ρ_{Al} represents the electrical conductivity of aluminum wire, d represents the wire diameter, Dis represents the distance between the Nth-row bonding contact and DBC bonding contact.

The corresponding 3-D multicellular circuit with resistances of wires and metallizations is shown in Fig. 5(b). All collector terminals of chip cells are shared on the surface of solder, which can be uniformly represented by V_{c}. The electric potential of nodes connected to the top copper layer of DBC is set as zero, which serves as the current-collection sink. The relationship between the voltage of all bonding contacts and the branch current can be expressed as

$$\begin{cases} V_{\mathrm{c}} - V_{n\_m} = I_{\mathrm{cell}n\_m} R_{\mathrm{cell}n\_m} \\ V_{n\_m} - V_{n\_m+1} = I_{\mathrm{metal}n\_m} R_{\mathrm{metal}m} \\ V_{n\_m} - V_{n+1\_m} = I_{\mathrm{wire}n\_m} R_{\mathrm{wire}n} \\ V_{N\_1} + \cdots + V_{N\_m} + \cdots + V_{N\_M} = I_{\mathrm{chip}} R_{\mathrm{wire}N} \end{cases} \tag{2}$$

where M, N represents the number of bonding wire and bonding contact, respectively, m, n represents the serial number of bonding wire and bonding contact, respectively, $R_{\mathrm{cell}\,n\_m}$ represents the equivalent conductive resistance of IGBT cell, which is discussed in Section III-B.

According to the number of included branches, the cells can be classified into three categories. The circuit equation of category 1 node with three branches included (e.g., V_{1_1}) can be written as

$$\begin{aligned} &(V_{\mathrm{c}} - V_{1\_1})/R_{\mathrm{cell}1\_1} = (V_{1\_1} - V_{2\_1})/R_{\mathrm{wire}1} \\ &+ (V_{1\_1} - V_{1\_2})/R_{\mathrm{metal}1}. \end{aligned} \tag{3}$$

The circuit equation of category two node with four current branches included (e.g., V_{1_m}) can be represented by

$$\begin{aligned} &(V_{\mathrm{c}} - V_{1\_m})/R_{\mathrm{cell}1\_m} + (V_{1\_m-1} - V_{1\_m})/R_{\mathrm{metal}m-1} \\ &= (V_{1\_m} - V_{2\_m})/R_{\mathrm{wire}1} + (V_{1\_m} - V_{1\_m+1})/R_{\mathrm{metal}m}. \end{aligned} \tag{4}$$

The circuit equation of category three node with five current branches included (e.g., V_{n_m}) can be expressed as

$$\begin{aligned} &(V_{\mathrm{c}} - V_{n\_m})/R_{\mathrm{cell}n\_m} + (V_{n-1\_m} - V_{n\_m})/R_{\mathrm{wire}n-1} \\ &+ (V_{n\_m-1} - V_{n\_m})/R_{\mathrm{metal}m-1} = (V_{n\_m} - V_{n+1\_m})/R_{\mathrm{wire}n} \\ &+ (V_{n\_m} - V_{n\_m+1})/R_{\mathrm{metal}m}. \end{aligned} \tag{5}$$

According to (3)–(5), the similar $N\times M$ equations for an arbitrary number of bonding contacts and bonding wires can be automatically written and solved by "eval", "strcat", and "solve" function of the numerical calculation software MATLAB. Based on the solution, the cell current I_{cell}, wire current I_{wire}, node voltage V_{n_m}, and collector voltage V_{c} can be obtained. The proposed 3-D multicellular circuit model demonstrates an improved accuracy and comparable calculation speed than the widely used classical model (e.g., PSpice, Saber).

B. Physics-Based IGBT Cell Model Decoupling Bonding Wires

The *V–I* curve of the IGBT module datasheet consists of semiconductor and bonding wires [16]. Therefore, the chip

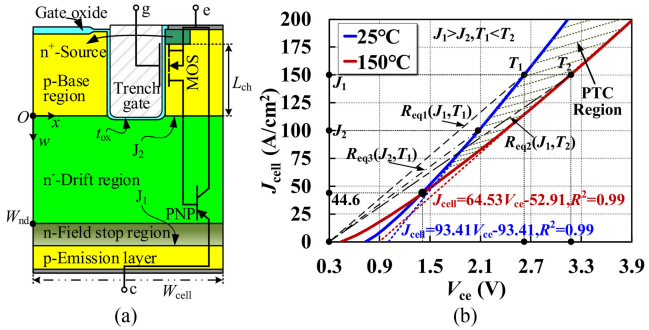

Fig. 6. (a) Schematic diagram and equivalent circuit of IGBT cell. (b) Modeled voltage-current density curve and extracted equivalent resistance ($V_{\mathrm{GE}} = 15$ V).

conduction characteristic is required to be achieved through physics-based modeling. The schematic diagram and equivalent circuit of IGBT cell are shown in Fig. 6(a), where the p-n junction formed by p emitter region and n field stop region, and the PN junction formed by n drift region and p base region are marked as J_1 and J_2, respectively, V_{J1}, V_{J2}, V_{nd}, and V_{ch} are the voltage drop of J_1 junction, J_2 junction, n^- drift region and channel, respectively, W_{nd} is the width of n^- drift region, L_{ch} is the channel length, t_{ox} is the oxide thickness, W_{cell} is the cell pitch. The ON-state cell voltage drop is represented as

$$\begin{cases} V_{\mathrm{ce}}(J_{\mathrm{cell}}, T_{\mathrm{j}}) = V_{\mathrm{J1}} + V_{\mathrm{nd}} + V_{\mathrm{J2}} + V_{\mathrm{ch}} \\ V_{\mathrm{J1}} = \frac{kT_{\mathrm{j}}}{q} \ln\left(\frac{p_2 N_{\mathrm{fs}}}{{n_{\mathrm{i}}}^2}\right),\ V_{\mathrm{J2}} = \frac{kT_{\mathrm{j}}}{q} \ln\left(\frac{p_1 N_{\mathrm{nd}}}{{n_{\mathrm{i}}}^2}\right) \\ V_{\mathrm{nd}} = \frac{J_{\mathrm{n\_drift}}}{s_0 q \mu_{\mathrm{n}}} \ln\frac{p_2 + s_0 W_{\mathrm{nd}}}{p_2},\ V_{\mathrm{ch}} = \frac{J_{\mathrm{cell}} L_{\mathrm{ch}} W_{\mathrm{cell}} t_{\mathrm{ox}}}{2\mu_{\mathrm{ni}} \varepsilon_{\mathrm{ox}} (V_{\mathrm{GE}} - V_{\mathrm{GEth}})} \\ J_{\mathrm{n\_drift}} = \frac{1}{\mu_{\mathrm{n}} + \mu_{\mathrm{p}}} \left[\mu_{\mathrm{n}} J_{\mathrm{cell}} - (\mu_{\mathrm{n}} - \mu_{\mathrm{p}}) q D_{\mathrm{n}} s_0\right] \end{cases} \tag{6}$$

where T_{j} is the local junction temperature whose unit is °C, J_{cell} is the cell current density, p_1, p_2 is the carrier concentration near $w = 0$ and at $w = W_{\mathrm{nd}}$, respectively, k is Boltzmann's constant, q is the charge coefficient, N_{fs} and N_{nd} are the doping concentration of field stop layer and n^- drift region, respectively, n_{i} is the intrinsic carrier concentration, μ_{ni} is the electron mobility of the channel, $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the gate oxidation layer, V_{GE} is the gate voltage, V_{GEth} is the gate threshold voltage, $J_{\mathrm{n\_drift}}$ is the electron drift current density in the n^- drift region, and s_0 is the approximate slope absolute value of the carrier concentration distribution in the n^- drift region, $s_0 \approx (p_1 - p_2) / W_{\mathrm{nd}}$, μ_{n}, and μ_{p} are the mobility of electrons and holes, respectively, D_{n} is the diffusion coefficient of electrons.

The doping concentration, geometry parameters, and temperature-sensitive parameters are shown in Table I. The parameter extraction procedure is introduced as follows. The geometry parameters are provided by the chip supplier. Due to the process deviation, the doping concentration parameters are estimated from [17] and corrected according to [18] and [19]. The temperature-sensitive parameters are the intrinsic physical parameters of silicon semiconductors, which are taken from [20].

Therefore, the modeled voltage-current density *(V–J)* curve by (6) at $V_{\mathrm{GE}} = 15$ V is depicted in Fig. 6(b). The strong temperature effect for the chip conduction is demonstrated, where the voltage increases with the increase of temperature when the current

TABLE I
DOPING CONCENTRATION, GEOMETRY PARAMETERS, AND TEMPERATURE-SENSITIVE PARAMETERS

Type	Parameters	Value
Doping concentration	N_{nd}	7×10^{13} cm^{-3}
	N_{fs}	1×10^{16} cm^{-3}
Geometry parameters	t_{ox}	94 nm
	W_{nd}	160 μm
	L_{ch}	2.7 μm
	W_{cell}	40 μm
Temperature -sensitive parameters	n_i	$3.88\times10^{16}T_j^{1.5}/\exp(7000/T_j)$
	μ_{ni}	$400(300/T_j)^{2.5}$
	μ_n	$1500(300/T_j)^{2.5}$
	μ_p	$450(300/T_j)^{2.5}$
	D_n	$\mu_n(kT_j/q)$

density is greater than 44.6 A/cm^2, which is specified as positive temperature characteristics (PTC). The voltage and current density at a certain temperature meet a perfect linear relationship in the PTC region, where the calculated 0.99 R-square fitness is shown.

However, the required cell equivalent resistance $R_{\text{cell}n\_m}$ in (2) literally refers to R_{eq} marked in Fig. 6(b), which conforms to the proportional relationship of Ohm's law. The diverse values of equivalent resistances at different temperatures T_1, T_2 and current density J_1, J_2 indicate that the cell equivalent resistance is not purely resistive, but current and temperature simultaneously dependent.

According to [3], dV_{ce}/dJ_{cell} and temperature T_j meet a strong linear relationship in the PTC region, that is

$$\frac{dV_{\text{ce}}}{dJ_{\text{cell}}}(T_j) = kT_j + b \tag{7}$$

where k and b are the fitting coefficients, respectively.

From (7), the linearized *V–J* relationship at different temperature can be rewritten as

$$\begin{aligned} V_{\text{ce}}(J_{\text{cell}}, T_j) &= \int \frac{dV_{\text{ce}}}{dJ_{\text{cell}}}(T_j)\, dJ_{\text{cell}} = \int (kT_j + b)\, dJ_{\text{cell}} \\ &= (kT_j + b) J_{\text{cell}} + B \Rightarrow \left(3.06 \times 10^{-5} T_j + 0.01\right) J_{\text{cell}} + 0.91 \end{aligned} \tag{8}$$

where B is the fitting coefficient.

The final part of (8) is obtained by fitting multiple sets of modeled results via (6) whose temperature range is 25 to 175 °C and current density range is 0 to 200 A/cm^2. The fit surface plot is illustrated in Fig. 7, where the R-square fitness is 0.98.

Thus, the cell equivalent resistance is determined as

$$\begin{aligned} R_{\text{cell}n\_m}(T_j, I_{\text{cell}}) &= \frac{V_{\text{ce}}(T_j, J_{\text{cell}})MN}{J_{\text{cell}} L_{\text{chip}} W_{\text{chip}}} \\ &= (kT_j + b) \frac{MN}{L_{\text{chip}} W_{\text{chip}}} + \frac{B}{I_{\text{cell}}} \end{aligned} \tag{9}$$

where L_{chip}, W_{chip} are the length and width of chip, M, N is the number of bonding wires and bonding contacts, I_{cell} is the cell current.

By now, the physics-based cell equivalent resistance $R_{\text{cell}n\_m}$ decoupling bonding wires is obtained, which can be adopted as the basis for solving (2).

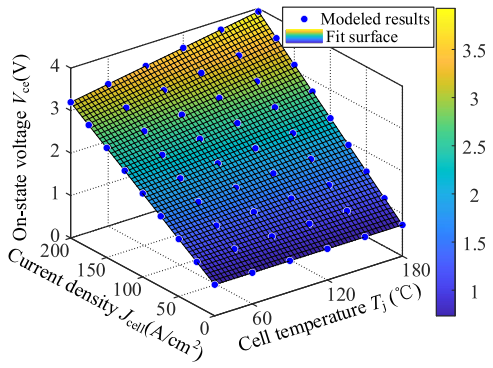

Fig. 7. Two-dimensional surface plot of the voltage-current-temperature fitting function.

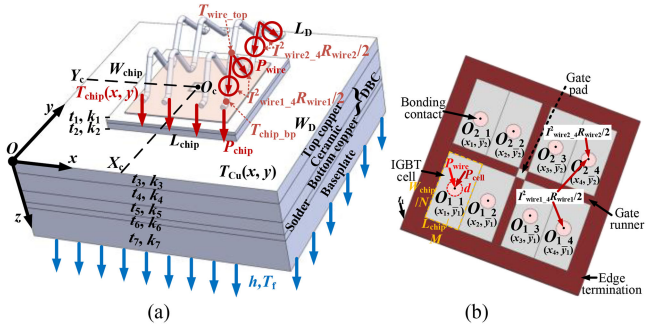

Fig. 8. (a) Package parameters and boundary conditions of a stitch-wire-bonded IGBT module. (b) Multicellular chip with distributed heating power of bonding wires.

C. Three-Dimensional Fourier Series Based Thermal Field Modeling

Due to the nonuniform heating effect introduced by stitch-bonding wires, there is a high lateral temperature gradient on the chip surface [21], [22], which cannot be reflected by the conventional lumped-based thermal model (e.g., Foster, Cauer). In this article, Fourier series based physical thermal modeling is introduced, which solves 3-D Laplace's equation by Fourier series and determines Fourier coefficient by package parameters and boundary conditions. Compared with FEM, the distinguished advantage of the Fourier method is its fast calculation speed, strong convergence, and geometric drawing unnecessity.

The package parameter and boundary condition of a stitch-wire-bonded IGBT module is shown in Fig. 8(a). The chip with bonding wires is soldered on the surface of top copper layer. The chip position is given by its center coordinate O_c (X_c, Y_c). The thickness and thermal conductivity of the jth layer from the chip to the baseplate are t_j and k_j, respectively. The power generated by chip P_{chip} and wire P_{wire} penetrates through multilayers to the bottom of the baseplate. The bottom surface of the baseplate is cooled by forced convection (liquid or forced air) of uniform temperature T_f with convection coefficient h_{conv}. The sidewall surface of the power module is cooled by natural convection, which is far less than forced convection. Thus, the adiabatic boundary conditions are assumed on the sidewall faces [23]. The temperature distribution on the chip surface $T_{\text{chip}}(x,y)$ and the copper surface $T_{\text{Cu}}(x,y)$ is brought

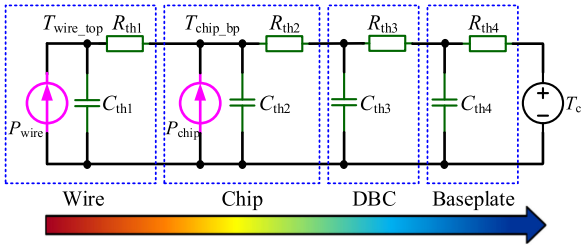

Fig. 9. Cauer-type thermal network of power module with heat generation in bonding wire and chip.

about by the above-mentioned boundary conditions, which are mathematically expressed as

$$\begin{cases} -k_7 \partial T(x,y,t_7)/\partial z = h_{\text{conv}}\left[T(x,y,t_7) - T_{\text{f}}\right] \\ -k_3 \partial T(x,y,0)/\partial z = \sum P/(L_{\text{chip}} W_{\text{chip}}) \\ \partial T(0,y,z)/\partial x = 0, \partial T(L_{\text{D}},y,z)/\partial x = 0 \\ \partial T(x,0,z)/\partial y = 0, \partial T(x,W_{\text{D}},z)/\partial y = 0. \end{cases} \tag{10}$$

According to the heat transfer theory, the temperature $T(x, y, z)$ in a 3-D solid with isotropic materials is governed by Laplace's equation, which is

$$\nabla^2 T(x,y,z) = \frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} = 0. \tag{11}$$

Using the separation of variables, the eigenvalue λ_u, δ_v, and corresponding Fourier coefficients can be solved by (10). The detailed derivation process is introduced in [23]. The formed temperature rises distribution of top copper surface introduced by a uniform 1 W rectangular heat source with length L_{hs}, width W_{hs}, and center coordinate $(x_{\text{hs}}, y_{\text{hs}})$ is of the form

$$\begin{aligned} &\Delta T_{\text{Cu\_perwatt}}(x,y) @ (x_{\text{hs}}, y_{\text{hs}}, L_{\text{hs}}, W_{\text{hs}}) \\ &= A_0 + \sum_{u=1}^{\infty} A_1 \cos(\lambda_u x) \\ &+ \sum_{v=1}^{\infty} A_2 \cos(\delta_v y) + \sum_{u=1}^{\infty}\sum_{v=1}^{\infty} A_3 \cos(\lambda_u x)\cos(\delta_v y) \end{aligned} \tag{12}$$

where $\lambda_u = u\pi/L_{\text{D}}$, $\delta_v = v\pi/W_{\text{D}}$, and $u, v = 1, 2, \ldots$; A_0, A_1, A_2, A_3 are the Fourier coefficients regarding the eigenvalues λ_u, δ_v.

The thermal coupling relationship between cells and wires can be briefly illustrated in Fig. 9. Where $T_{\text{wire\_top}}$ and $T_{\text{chip\_bp}}$ represent the top position of bonding wire arch and the bonding position on chip, respectively, marked in Fig. 8(a). R_{th1} (C_{th1}), R_{th2} (C_{th2}), R_{th3} (C_{th3}), and R_{th4} (C_{th4}) represent the thermal resistance (capacitance) of wire, chip layer, DBC layer, and baseplate layer, respectively. According to the boundary conditions in (10), the power module presents a single heat transfer path. Therefore, the bonding wire has a coupling effect on the heat generation in chip and, thus, affects $T_{\text{chip\_bp}}$, while the chip has no coupling effect on the heat generation in bonding wire and will not affect $T_{\text{wire\_top}}$. In order to study $T_{\text{chip\_bp}}$, the wire power and chip power are both considered in the following.

The multicell with distributed wire heating power is displayed in Fig. 8(b). The cell heating power is described as the volume heat source with the cell length L_{chip}/M, width W_{chip}/N and thickness t_1. According to the heat transfer theory of semi-infinite heat flux media, rectangular heat source and circular heat source with the identical area will produce similar temperature gradient [24], [25]. Thus the circular heat source of bonding wire is described as the square heat source with the identical cross-sectional area and sharing the corresponding cell coordinate (x_m, y_n).

Based on (12), the temperature rise of top copper surface is formed by the linear superposition of temperature rise individually introduced by cell power and wire power. Thus, there is where m, n represents the serial number of bonding wire and bonding contact, respectively; the heating powers are calculated by

$$\begin{cases} P_{\text{wire}n\_m} = I^2_{\text{wire}n-1\_m} R_{\text{wire}n-1}/2 \\ +I^2_{\text{wire}n\_m} R_{\text{wire}n}/2, n \geq 2 \\ P_{\text{wire1}\_m} = I^2_{\text{wire1}\_m} R_{\text{wire1}}/2 \\ P_{\text{cell}n\_m} = I^2_{\text{cell}n\_m} R_{\text{cell}n\_m} \end{cases} \tag{14}$$

where $P_{\text{wire}n\_m}$ represents the heating power injected into the cell number n_m with the centrally located wire arches. As shown in Fig. 8(a), the heating power generated by a bonding wire arch is injected into the chip through two bonding contacts, which are located on the chip layer. As shown in Fig. 9, the thermal impedance of the two bonding contacts is considered to be equal, thus, it can be considered that the heating power of a wire arch is divided into two and injected into the located cell, respectively. Therefore, $P_{\text{wire}n\_m}$ is obtained by summing half of the wire arch power in the previous $(n-1)$th row and half of the wire arch power in this nth row, where an example $P_{\text{wire2\_4}}$ is illustrated in Fig. 8(b).

Internal heat generation of cells in the chip is described by the 1-D heat conduction model with volume heat source, while the temperature rise through the chip introduced by wires is described by the 1-D heat conduction model with surface heat source, which is also applicable to the temperature rise through the chip solder. Therefore, it means that

Consequently, the chip temperature rise distribution $\triangle T_{\text{j}}(x, y)$ is the sum of the temperature rise formed in the top copper layer $\triangle T_{\text{Cu}}(x,y)$, the chip solder $\triangle T_{\text{cs}}$, and the chip $\triangle T_{\text{chip}}$. After this, the cell temperature $T_{\text{cell}n\_m}$ is represented by the temperature at the position (x_m, y_n). By (13) and (15) shown at the bottom of the next page, it can be concluded that

$$\begin{aligned} T_{\text{cell}n\_m} = T_{\text{j}}(x_m, y_n) &= \Delta T_{\text{Cu}}(x_m, y_n) \\ &+ \Delta T_{\text{chip}} + \Delta T_{\text{cs}} + T_{\text{f}}. \end{aligned} \tag{16}$$

Through the above-mentioned calculation process, the accurate chip thermal field considering the wire self-heating and nonuniform cell heat flux effect is obtained to comprehensively evaluate the temperature gradient and suppress the local overheating.

D. Bidirectional Electro-Thermal Coupling for Multicell

In the aforementioned three sections, the circuit equation solution, cell equivalent resistance extraction, and temperature field calculation are individually developed, which can be integrated to realize the bidirectional electro-thermal coupling for

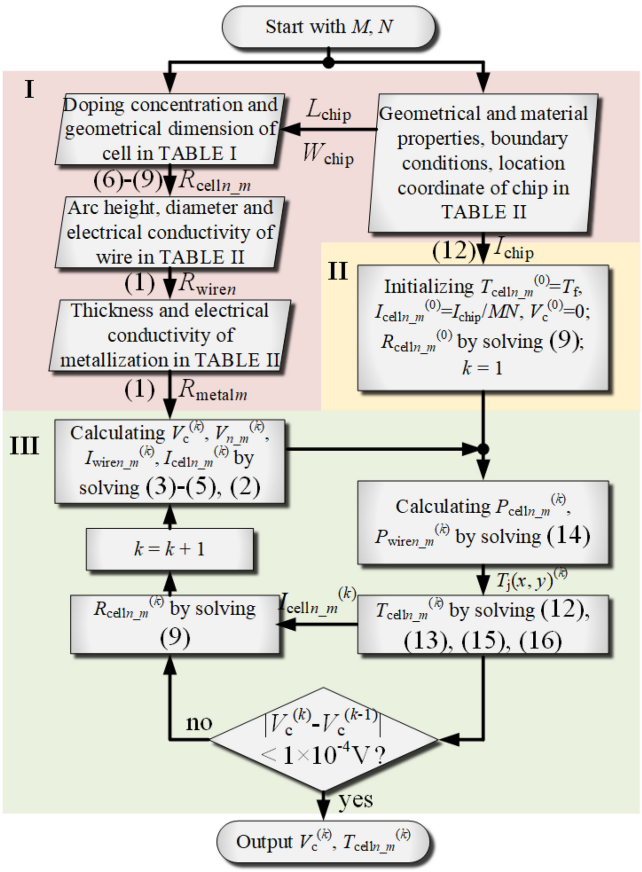

Fig. 10. Proposed flowchart of multicellular electro-thermal coupling process for the stitch-wire-bonded IGBT module.

multicell, which is shown in Fig. 10. The process is mainly divided into three parts: 1) parameters input, 2) initialization, 3) and electro-thermal iteration. The specific process under a certain value of wire number M, bonding contact number N, arc height h, and diameter d can be expressed as

(I-1) Inputting the geometrical and material properties k_1, …, k_7, t_1, …, t_7, t_m, L_{chip}, W_{chip}, L_D, W_D, boundary conditions h_{conv}, T_f, location coordinate of chip (X_c, Y_c) to obtain the function (12).

(I-2) Inputting the doping concentration, geometrical dimension, and temperature-sensitive parameters in Table I, such as N_{fs}, N_{nd}, t_{ox}, W_{nd}, and L_{ch}, for bipolar semiconductor, to obtain (9) by (6)–(8) with the chip length L_{chip} and width W_{chip} in (I-1).

(I-3) Inputting the arc height h, diameter d, and electrical conductivity ρ_{Al} of bonding wires to calculate the wire arch resistance R_{wiren} by (1) with the chip width W_{chip} in (I-1).

(I-4) Inputting the thickness t_m and electrical conductivity of chip metallization ρ_{metal} to calculate the resistance of horizontal metallization layer R_{metalm} by (1) with the chip length L_{chip} and metallization thickness t_m in (I-1).

(II) Initializing variables $T_{celln\_m}^{(0)}$, $I_{celln\_m}^{(0)}$ that affect cell equivalent resistance, assuming that the initial chip temperature is evenly equal to the ambient or fluid temperature T_f, the initial chip current I_{chip} is evenly divided into $N\times M$ cell currents so that the initial $R_{celln\_m}^{(0)}$ can be preliminarily calculated by solving (9); the chip collector potential $V_c^{(0)}$ is set to zero to avoid the false end in the first iteration.

(III-1) *Circuit equation solving*: according to the calculated R_{wiren}, R_{metalm}, and $R_{celln\_m}^{(0)}$, the built-in MATLAB function "solve" is used to find the $V_c^{(1)}$, $V_{n\_m}^{(1)}$ by (3)–(5); then calculating $I_{wiren\_m}^{(1)}$, $I_{celln\_m}^{(1)}$ by (2) and $P_{celln\_m}^{(1)}$, $P_{wiren\_m}^{(1)}$ by (14).

(III-2) *Temperature field solving*: working out $T_{celln\_m}^{(1)}$ by solving (12), (13), (15), and (16).

(III-3) *Cell equivalent resistance solving and iteration*: judging whether $V_c^{(1)}$ converges. If yes, outputting the above calculated $V_c^{(1)}$, $T_{celln\_m}^{(1)}$; if not, continuing to update $R_{celln\_m}^{(1)}$ by solving (9) with $I_{celln\_m}^{(1)}$ and iterating to the second step, which starts from (III-1) again, repeats (III-2) and proceeds to the judgment in (III-3) until the kth step converges.

IV. Proposed Model Oriented Design and Multitier Layout Optimization for Stitch Wires

A. Simulation Verification and Case Analysis

The simulation of the baseline power module shown in Fig. 2 is conducted to verify the proposed model. The active area of the selected IGBT chip is divided into 4×8 cell structure by the stitch-bonding wires, whose numbering rules for each cell is illustrated in Fig. 5(a). The center coordinate of chip is (X_c,Y_c). The material characteristics, geometrical parameters, and position coordinates are listed in Table II.

The results of modeled cell temperature T_{celln_m}, cell emitter potential V_{n_m}, wire arch current I_{wiren_m}, cell current

$$\begin{aligned}\Delta T_{Cu}(x,y) &= \sum_{m=1}^{M}\sum_{n=1}^{N} P_{celln\_m}\Delta T_{Cu\_perwatt}(x,y)\,@\left(x_m, y_n, \frac{L_{chip}}{M}, \frac{W_{chip}}{N}\right)\\ &+ \sum_{m=1}^{M}\sum_{n=1}^{N} P_{wiren\_m}\Delta T_{Cu\_perwatt}(x,y)\,@\left(x_m, y_n, \sqrt{\frac{\pi d^2}{4}}, \sqrt{\frac{\pi d^2}{4}}\right)\end{aligned} \tag{13}$$

$$\begin{cases}\Delta T_{chip} = \displaystyle\sum_{m=1}^{M}\sum_{n=1}^{N} P_{celln\_m}\frac{t_1}{2k_1 L_{chip} W_{chip}} + \sum_{m=1}^{M}\sum_{n=1}^{N} P_{wiren\_m}\frac{t_1}{k_1 L_{chip} W_{chip}}\\ \Delta T_{cs} = \left(\displaystyle\sum_{m=1}^{M}\sum_{n=1}^{N} P_{celln\_m} + \sum_{m=1}^{M}\sum_{n=1}^{N} P_{wiren\_m}\right)\frac{t_2}{k_2 L_{chip} W_{chip}}\end{cases} \tag{15}$$

TABLE II
MATERIAL AND GEOMETRICAL PARAMETERS OF POWER MODULE

Parameter	Value	Parameter	Value
k_1	98.9 W/(m·°C)	t_4	0.32 mm
k_2, k_6	55 W/(m·°C)	t_7	3 mm
k_3, k_5, k_7	380 W/(m·°C)	L_{chip}	13.8 mm
k_4	24 W/(m·°C)	W_{chip}	13.8 mm
ρ_{Al}	4×10^{-8}(Ω·m)	L_D	91.9 mm
ρ_{metal}	4×10^{-8}(Ω·m)	W_D	31.8 mm
t_m	3.2 μm	(X_c, Y_c)	(64.4, 15.8) mm
t_1	0.12 mm	h	3.5 mm
t_2	0.12 mm	d	0.4 mm
t_3, t_5, t_6	0.3 mm	Dis	5.1 mm

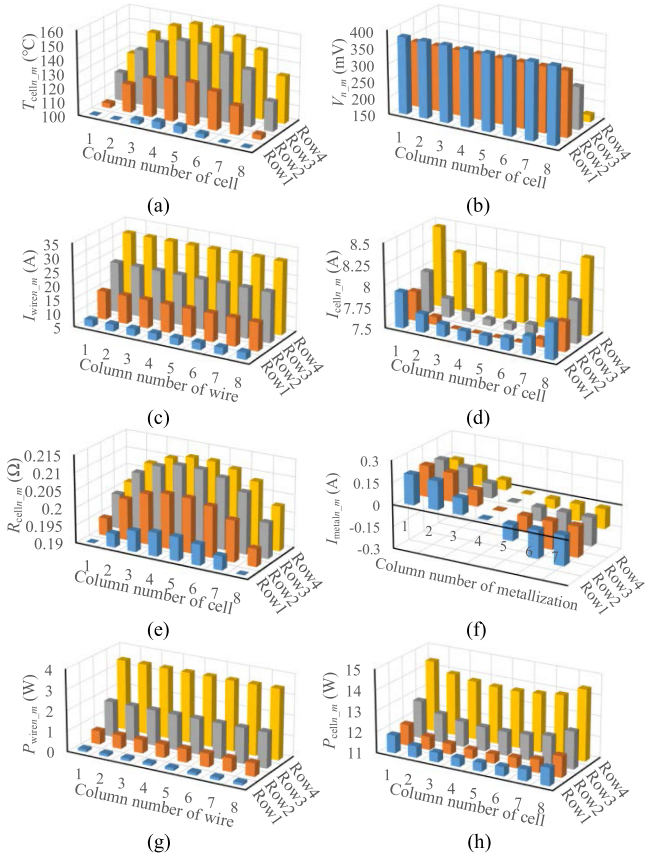

Fig. 11. Modeled results of (a) cell temperature, (b) cell emitter potential, (c) wire current, (d) cell current, (e) cell equivalent resistance, (f) metallization current, (g) joule heat of wires, and (h) heat power of cells. (I_{chip} = 250 A).

$I_{cell\,n\_m}$, cell equivalent resistance $R_{cell\,n\_m}$, metallization current $I_{metal\,n\_m}$, wire arch power $P_{wire\,n\_m}$, and cell power $P_{cell\,n\_m}$ are successively shown in Fig. 11. The maximum cell temperature, cell potential, wire current, maximum cell current, wire power, and maximum cell power in each row are summarized in Table III. Owing to the nonuniform self-heating of wires and cells, the cell temperature between different rows presents the same principle as Fig. 3(b), where T_{cell4_5} (158.52 °C) > T_{cell3_5} (151.29 °C) > T_{cell2_5} (129.92 °C) > T_{cell1_5} (105.09 °C) specifically. The largest modeling error occurs in the first row, which is 3.43% (T_{cell1_5}). Due to the transverse heat conduction effect with the soldered DBC, the cell temperature in a row

TABLE III
MODELED RESULTS SUMMARY OF MAXIMUM CELL TEMPERATURE, CELL POTENTIAL, WIRE CURRENT, MAXIMUM CELL CURRENT, WIRE POWER, AND MAXIMUM CELL POWER (I_{CHIP} = 250 A)

Row number n	T_{cell} (°C)	V (mV)	I_{wire} (A)	I_{cell} (A)	P_{wire} (W)	P_{cell} (W)
4	158.52	171.53	31.47	8.46	3.45	14.42
3	151.29	276.51	23.16	8.00	1.75	12.80
2	129.92	345.62	15.36	7.85	0.67	12.01
1	105.09	379.97	7.72	7.93	0.13	11.85

presents a decreasing trend from the center to surrounding, where the maximum cell temperature in the fourth row T_{cell4_5} (158.52 °C) is 22.9% higher than the minimum cell temperature in the fourth row T_{cell4_1} (128.98 °C).

As shown in Fig. 11(b), the potential difference between cells in adjacent rows exhibits inhomogeneous characteristics, where $\triangle V_{12}$ = 34.35 mV, $\triangle V_{23}$ = 69.11 mV, $\triangle V_{34}$ = 104.98 mV, and $\triangle V_{4G}$ = 171.53 mV. The maximum emitter potential modeling error appears in the fourth row, which is 4.86% (V_{4_1}). The maximum emitter potential is 379.98 mV, which contributes 16.96% to V_c (2.24 V). As shown in Fig. 11(c), the wire arch current in the second row, third row, and fourth row is successively increased by 7.62 A, 7.86 A, and 8.29 A, respectively, compared to that in its previous row, which verifies the imbalance of stitch-bonding wire current.

In Fig. 11(d), the cell current between neighboring rows demonstrates incremental tendency as the row number increases due to the inhomogeneous cell emitter potential, where I_{cell2_m} < I_{cell3_m} < I_{cell4_m}, except I_{cell1_m} exceeds I_{cell2_m}. It can be explained by the PTC induced cell equivalent resistance distribution, which is shown in Fig. 11(e). There are

$$\begin{cases} I_{cell\,n\_m} = (V_c - V_{n\_m})/R_{cell\,n\_m}(T_{cell\,n\_m}) \\ V_{1\_m} > V_{2\_m} \Rightarrow I_{cell1\_m} < I_{cell2\_m} \\ T_{cell1\_m} < T_{cell2\_m}, R_{cell1\_m} < R_{cell2\_m} \\ \Rightarrow I_{cell1\_m} > I_{cell2\_m}. \end{cases} \tag{17}$$

The stitch-bonding configuration leads to $V_{1\_m} > V_{2\_m}$ so that there is a tendency that $I_{cell1\_m} < I_{cell2\_m}$, while the PTC of semiconductor results in $R_{cell1\_m} < R_{cell2\_m}$, causing the tendency that $I_{cell1\_m} > I_{cell2\_m}$. According to the results that $I_{cell1\_m} > I_{cell2\_m}$, it indicates that the PTC outweighs the stitch-bonding effect on the cell current distribution in the first and second rows. Furthermore, the cell current in a row performs PTC induced lateral unevenness, where the maximum cell current in the fourth row I_{cell4_1} (8.48 A) is 6.0% larger than the minimum cell current in the fourth row I_{cell4_5} (8.01 A). The results displayed in Fig. 11(f) further illustrates that the horizontal metallization resistor provides a path for the unbalanced cell current. The abovementioned results verify the necessity and effectiveness of considering the semiconductor temperature effect [26].

The modeled wire power and cell power are depicted in Fig. 11(g) and (h). The calculated volume of a wire arch is 1.2 mm^3. The calculated cell area is 1 mm^2. Thus, the maximum power modeling error is 5.36% (P_{wire1_8}) and 3.19% (P_{cell1_1}) compared with the simulation results in Fig. 4, indicating that

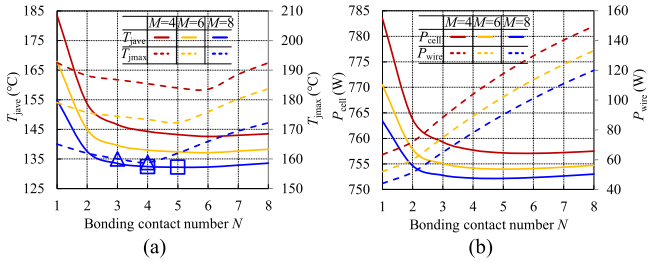

Fig. 12. (a) Impact of wire number and contact number on the maximum and average chip temperature. (b) Impact of wire number and contact number on the total heating power of multicell and wires. ($I_{\rm chip} = 250$ A).

the model can accurately reflect the effect of uneven wire self-heating and nonuniform cell heat flux. All results in this section validate that the proposed model can be adopted in the thermal stress evaluation and optimization for the stitch-wire-bonded IGBT module.

B. Indices for Thermal Stress Evaluation and Optimization of Bonding Contact Number

To comprehensively evaluate the thermal stress, two indexes are, respectively, defined to describe the local overheating ($T_{\rm jmax}$) and the thermal equilibrium ($T_{\rm jave}$) for the chip. The selected indices can be specifically expressed as

$$\begin{cases} T_{\rm jmax} = \max\left(T_{{\rm cell}n\_m}\right) \\ T_{\rm jave} = \frac{1}{MN}\sum\limits_{m=1}^{M}\sum\limits_{n=1}^{N} T_{{\rm cell}n\_m} \end{cases} \tag{18}$$

where $T_{\rm jmax}$ and $T_{\rm jave}$ represent the maximum chip temperature and average chip temperature, respectively.

According to the previous introduction, the design parameters of stitch-bonding wire include wire number M, bonding contact number N, arc height h, arc angle α, and diameter d. Determined by the thickness of chip metallization layer, the maximum diameter d of commercial bonding wires is less than 500 μm [27], [28]. Due to the head width limitation of wedge bonding tool, the allowed minimum pitch for adjacent bonding wire is set as 1.5 mm [28], resulting in the maximum wire number M. In order to avoid the infant failures of wires (e.g., heel crack, lift-off), the arc angle α is customarily arranged between 30° and 60° [29]. Based on this, the maximum number of bondable contacts N in constant loop angle bonding mode depends on the minimum arc height h, which is subjected to the head depth of bonding head and the minimum wire pulling height of bonding machine. Consequently, the design constraints can be concluded as follows:

$$\begin{cases} M : 4 \sim 8 \\ N : 2 \sim 8 \\ d : 0.5{\rm mm} \\ \alpha : 45°. \end{cases} \tag{19}$$

Oriented with (18), the results are fast obtained through the proposed multicellular electro-thermal model under the conditions of (19). The impact of the wire number M and bonding contact number N on $T_{\rm jmax}$ and $T_{\rm jave}$ is concluded in Fig. 12(a).

TABLE IV
IMPACT ANALYSIS OF BONDING CONTACT NUMBER ON HEATING POWER AND CHIP TEMPERATURE ($M = 8$)

	Bonding contact number N		
	rare (1~2)	medium (3~5)	sufficient (6~8)
$P_{\rm cell}$	**plummet** ↓	**slowly decline** ↘	constant →
$P_{\rm wire}$	linearly rise ↗	**linearly rise** ↗	**linearly rise** ↗
$T_{\rm jave}$ / $T_{\rm jmax}$	**$P_{\rm cell}$ dominance**	depends on $P_{\rm cell}$ **vs.** $P_{\rm wire}$	**$P_{\rm wire}$ dominance**

$N = 1$ refers to the conventional wire configuration in Fig. 1(a), while others represent the stitch-bonding configuration. It is shown that $T_{\rm jmax}$ of stitch-bonding configuration ($N = 2$) is decreased by 2.3%, 1.9%, and 1.9%, respectively, compared to the conventional wire configuration when $M = 4$, 6, 8; while $T_{\rm jave}$ of stitch-bonding configuration ($N = 2$) is decreased by 19.6%, 15.9%, and 12.6%, respectively, compared to the conventional wire configuration when $M = 4$, 6, 8. The impact of M and N on the total chip power $P_{\rm cell}$ and total wire power $P_{\rm wire}$ extracted from (14) is shown in Fig. 12(b). It is indicated that the stitch-bonding configuration is distinctively beneficial to the mitigation of $P_{\rm cell}$ (2.5%↓), which significantly affects $T_{\rm jave}$ reduction when $N \le 2$, despite there is a slight 13.7% increase in $P_{\rm wire}$.

Back to Fig. 12(a), it is indicated that as the wire number M increases, both the average temperature $T_{\rm jave}$ and maximum temperature $T_{\rm jmax}$ under certain contact number N are lower. To be specific, as the wire number is increased from 4 to 6 and 6 to 8, the maximum temperature is decreased by 8.1% and 9.9% ($N =$ 2), and the average temperature is decreased by 7.1% and 6.4% ($N = 2$). Thus, the maximum bondable number of bonding wires is beneficial to the chip thermal mitigation. As for the bonding contact number, it is revealed that there is an optimal value under a certain wire number for both the maximum temperature and average temperature. For example, when M is set as 8, the lowest $T_{\rm jmax}$ under the optimal contact number ($N = 4$) is 10.0% lower than the highest $T_{\rm jmax}$ under $N = 8$; while the lowest $T_{\rm jave}$ under the optimal contact number ($N = 5$) is 4.9% lower than the highest $T_{\rm jave}$ under $N = 2$. Therefore, for $M = 8$, when $T_{\rm jmax}$ is evaluated individually, $N = 3$ or 4 is preferred; while when $T_{\rm jave}$ is evaluated individually, $N = 4$ or 5 is preferred. In summary, the layout for stitch-bonding wires with $M = 8$, $N = 4$ can be selected as the optimum scheme, which has been preliminarily designed in Fig. 2.

As exhibited in Fig. 12(b), the formation mechanism of optimal bonding contact number can be attributed to that the increased N has quite limited contribution to $P_{\rm cell}$ mitigation but contrary to a more severe self-heating power of wires $P_{\rm wire}$ after $N \ge 3$. Taking $M = 8$ as an example, from $N = 3$ to $N = 8$, $P_{\rm wire}$ is increased by 84.5%, while $P_{\rm cell}$ is only varied 0.03%. This is because that as the contact number increases, the overall length of wire arch continues to extend, while the effect of stitch-bonding on chip current density reduction has achieved its limitation [6].

Therefore, the impact of bonding contact number on the heating power and chip temperature can be concluded in Table IV. It is shown that with the increase of contact number from 1 to 8,

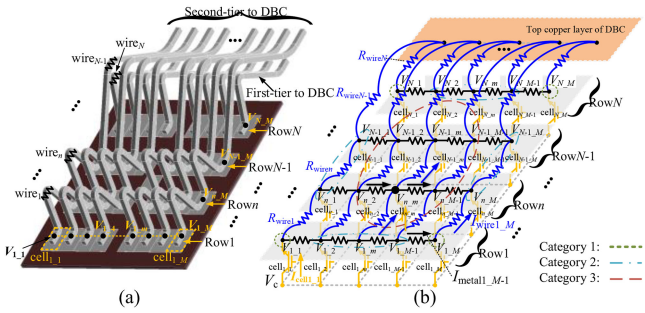

Fig. 13. (a) Geometry structure of proposed multitier layout. (b) Three-dimensional multicellular circuit of the proposed multitier layout.

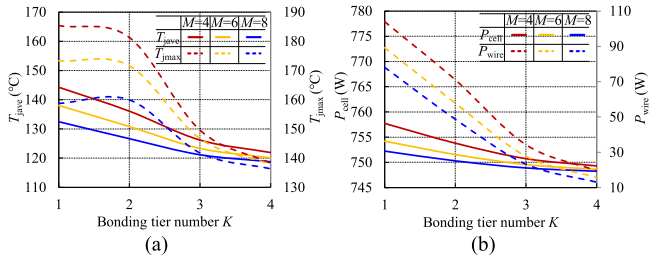

Fig. 14. (a) Impact of wire number and bonding tier number on the average and maximum temperature of chip. (b) Impact of the wire number and tier number on the total heating power of multicell and wires. ($N = 4$ and $I_{\mathrm{chip}} = 250$ A).

the total cell power presents a rapid decrease initially (1–2), slow decline subsequently (3–5), and almost unchanged finally (6–8), while the total wire power exhibits an approximately linear rise on the whole. With regard to the thermal evaluation indexes, the T_{jave} embodied thermal equilibrium performance is primarily determined by P_{cell}, which presents a slight optimal value ($N = 4$). While the T_{jmax} reflected local overheating performance experienced a shift from P_{cell} dominance to P_{wire} dominance with the increasing N. When the contact number is rare (1–2), the dramatically reduced P_{cell} plays the dominant role in the T_{jmax} mitigation. When the contact number is medium (3–5), the moderately reduced P_{cell} and perpetually increased P_{wire} are matched in strength, which results in the optimal contact number ($N = 4$). When the contact number is relatively great (6–8), the continuously enlarged P_{wire} prevails over the nearly constant P_{cell}, leading to progressively rising T_{jmax}.

C. Advanced Optimization With Multitier Bonding Layout

The aforementioned wire number and contact number optimization is employed to establish a baseline scheme for the metallization layer division and corresponding wire layout. According to the previous conclusion that the wire power has a superior influence on chip temperature when $N = 4$, further optimization for wire power mitigation is required consequently.

To this end, a novel wire-bonding layout, which is entitled as multitier bonding, is proposed to alleviate the wire current. Taking the bonding tier number $K = 2$ as an example, which is shown in Fig. 13(a), the first-tier stitch wire is directly connected to the DBC after bonded to the ($N-1$)th-row metallization layer. Simultaneously, there is an additional second-tier wire connecting the Nth-row metallization layer and DBC, which forms the dual-tier bonding configuration with the abovementioned wires.

For generality, the 3-D multicellular circuit of multi-tier layout with the tier number K is built, which is shown in Fig. 13(b). For a certain arc angle, the length of each tiered wire varies proportionally with the row number. Based on (1), the tiered wire arch resistance can be consequently calculated by

$$\begin{cases} R_{\mathrm{wire}N} = 8\rho_{\mathrm{Al}}\dfrac{\sqrt{(Dis/2)^2+h^2}}{\pi d^2} \\ R'_{\mathrm{wire}N-1} = 3R_{\mathrm{wire}N} \\ \quad \cdots \\ R'_{\mathrm{wire}N-K+1} = (2K-1)R_{\mathrm{wire}N} \end{cases} \tag{20}$$

where $R'_{\mathrm{wire}N-1}$, $R'_{\mathrm{wire}N-K+1}$ are the tiered wire arch resistance in the ($N-1$)th and ($N-K+1$)th row, respectively.

Correspondingly, the circuit equation of nodes involved in tiered wires should be rewritten. By (20), (3), (4), and (5) are rewritten as represented by V'_{N_1}, V'_{N-1_1}, and V'_{N-1_m}, respectively, as

$$\begin{aligned} &(V_{\mathrm{C}} - V'_{N\_1})/R_{\mathrm{cell}N\_1} = V'_{N\_1}/R_{\mathrm{wire}N} \\ &+(V'_{N\_1} - V'_{N\_2})/R_{\mathrm{metal1}} \end{aligned} \tag{21}$$

$$\begin{aligned} &(V_{\mathrm{c}} - V'_{N-1\_1})/R_{\mathrm{cell}N-1\_m} \\ &+(V'_{N-2\_1} - V'_{N-1\_1})/R'_{\mathrm{wire}N-2} \\ &= V'_{N-1\_1}/R'_{\mathrm{wire}N-1} + (V'_{N-1\_1} - V'_{N-1\_2})/R_{\mathrm{metal1}} \end{aligned} \tag{22}$$

$$\begin{aligned} &(V_{\mathrm{c}} - V'_{N-1\_m})/R_{\mathrm{cell}N-1\_m} + (V'_{N-2\_m} - V'_{N-1\_m})/ \\ &R'_{\mathrm{wire}N-2} + (V'_{N-1\_m-1} - V'_{N-1\_m}) \\ &/R_{\mathrm{metal}m-1} = V'_{N-1\_m} \\ &/R'_{\mathrm{wire}N-1} + (V'_{N-1\_m} - V'_{N-1\_m+1})/R_{\mathrm{metal}m}. \end{aligned} \tag{23}$$

The current and heating power of tier wire is rewritten as

$$\begin{cases} I_{\mathrm{chip}} = \sum_{m=1}^{M}(I'_{\mathrm{wireN\_m}} + \cdots + I'_{\mathrm{wireN-K+1\_m}}) \\ P'_{\mathrm{wireN\_m}} = I'^2_{\mathrm{wireN\_m}}R'_{\mathrm{wireN}/2} \\ \quad \cdots \\ P'_{\mathrm{wireN-K+2\_m}} = I'^2_{\mathrm{wireN-K+2\_m}}R'_{\mathrm{wireN-K+2}}/2 \\ P'_{\mathrm{wireN-K+1\_m}} = I'^2_{\mathrm{wireN-K\_m}}R_{\mathrm{wireN-K}}/2+ \\ \qquad I'^2_{\mathrm{wireN-K+1\_m}}R'_{\mathrm{wireN-K+1}}/2. \end{cases} \tag{24}$$

Likewise, the average and maximum chip temperature from (18) can be derived by the revised multicellular electro-thermal model with multitier layout under the conditions of (19). The impact of the wire number M and bonding tier number K on the average and maximum chip temperature is concluded in Fig. 14(a). $K = 1$ refers to the optimal baseline wire configuration ($N = 4$) in Fig. 12, while others represent the K-tier configuration with $N = 4$. It is indicated repeatedly that the increased wire number has a mitigative effect on both T_{jave} and T_{jmax}. As for the bonding tier number, it is revealed that there is an overall decreasing trend for both the maximum and average chip temperature. For example, when M is set as 4, as the tier number is increased from 2 to 4, the average chip temperature is decreased by 6.7%, 14.8%, and 18.3%, respectively, while the maximum chip temperature is decreased by 2.5%, 21.9%,

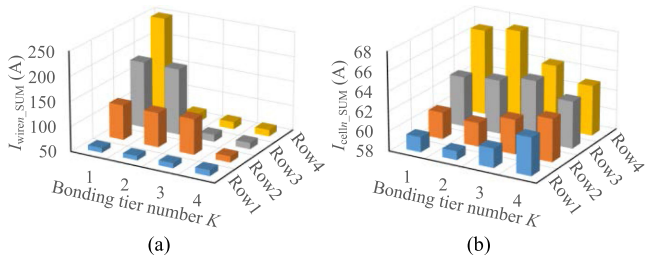

Fig. 15. (a) Impact of tier number on the sum of *n*th-row wire current with the proposed multitier layout. (b) Impact of tier number on the sum of *n*th-row cell current with the proposed multitier layout. ($N = 4$, $M = 8$, and $I_{\text{chip}} = 250$ A).

and 28.9%, respectively. When M is set as the abovementioned optimal value ($M = 8$), with the increase of tier number from 1 to 4, the maximum temperature even increases slightly (1–2), then decreases rapidly (2–3), and finally decreases slowly (3–4).

In the meanwhile, the impact of the wire number M and bonding tier number K on the total heating power of multicell and wires is concluded in Fig. 14(b). When M is set as 4, as the tier number is increased from 2 to 4, P_{cell} is decreased by 0.5%, 0.9%, and 1.1%, respectively, while P_{wire} is decreased by 31.7%, 67.0%, and 81.2%, respectively. It is indicated that the multitier configuration is distinctively beneficial to the mitigation of P_{wire}, accompanied by the reduction of P_{cell}. The decreasing tendency of average temperature is attributed to the reduction of P_{cell}, while the formation of maximum temperature is not only determined by P_{wire}.

To explore the mechanism of maximum chip temperature, the sum of *n*th-row cell current $I_{\text{cell}n\_\text{SUM}}$ and *n*th-row wire arch current $I_{\text{wire}n\_\text{SUM}}$ are, respectively, defined as

$$\begin{cases} I_{\text{cell}n\_\text{SUM}} = \sum_{m=1}^{M} I_{\text{cell}n\_m} \\ I_{\text{wire}n\_\text{SUM}} = \sum_{m=1}^{M} I_{\text{wire}n\_m}. \end{cases} \tag{25}$$

The impact of tier number on $I_{\text{cell}n\_\text{SUM}}$ and $I_{\text{wire}n\_\text{SUM}}$ is illustrated in Fig. 15. It is demonstrated that as the bonding tier number K increases, the wire current will extremely decrease, while not all cell current decreases simultaneously. It can be explained with an example when $K = 2$. There are

$$\begin{cases} I_{\text{cell}N\_m} = \frac{V_c - I_{\text{wire}N\_m} R_{\text{wire}N}}{R_{\text{cell}N\_m}} \\ I'_{\text{cell}N\_m} = \frac{V_c - I'_{\text{wire}N\_m} R_{\text{wire}N}}{R_{\text{cell}N\_m}} \\ I_{\text{wire}N\_m} > I'_{\text{wire}N\_m} \Rightarrow I_{\text{cell}N\_m} < I'_{\text{cell}N\_m} \end{cases} \tag{26}$$

where $I_{\text{wire}N\_m}$, $I'_{\text{wire}n\_m}$ are the *N*th-row wire arch current with the baseline and with the dual-tier layout respectively, $I_{\text{cell}n\_m}$, $I'_{\text{cell}N\_m}$ are the *N*th-row cell current with the baseline and with the dual-tier layout, respectively. Due to the multitier configuration, $I_{\text{wire}N\_m}$ is reduced to $I'_{\text{wire}N\_m}$, where the value is reduced from the chip current I_{chip} to about a quarter of the chip current I_{chip}. This leads to $V'_{N\_m} < V_{N\_m}$, which results in $I'_{\text{cell}N\_m} > I_{\text{cell}N\_m}$.

It can be seen that the reduction in the self-heating of tiered wires has the possibility of increasing the heat generation of chip, which is reflected in the rise of maximum temperature T_{jmax}. To

TABLE V
MODELED IMBALANCE RATIO OF CELL CURRENT WITH INCREASING TIER NUMBER AND WIRE NUMBER ($N = 4$ AND $I_{\text{CHIP}} = 250$A)

Imbalance ratio δ_{I} (%)		Tier number K			
		1	2	3	4
Wire number M	4	15.3	19.6	10.5	2.9
	6	13.1	16.0	8.5	2.4
	8	11.5	13.5	7.2	2.0

TABLE VI
IMPACT ANALYSIS OF BONDING TIER NUMBER ON HEATING POWER, IMBALANCE RATIO, AND CHIP TEMPERATURE ($M = 8$)

	Variation interval of bonding tier number K		
	[1,2]	[2,3]	[3,4]
P_{cell}	linearly decline		
P_{wire}	linearly decline		slowly decline
δ_I	slightly increase	rapidly decrease	slowly decrease
T_{jave}	depends on P_{cell}, linearly decline		
T_{jmax}	unchanged	rapidly decrease	slowly decrease

evaluate the interaction and avoid this risk, the imbalance ratio of the cell current δ_{I} is determined by

$$\begin{cases} \Delta I_{\text{cellSUM\_max}} \\ \quad = \max \left[\sum_{i=1}^{N-1} \sum_{j=i+1}^{N} \left(|I_{\text{cell}i\_\text{SUM}} - I_{\text{cell}j\_\text{SUM}}| \right) \right] \\ I_{\text{cellSUM\_mean}} = \left(\sum_{i=1}^{N} I_{\text{cell}i\_\text{SUM}} \right) / N \\ \delta_{\text{I}} = \frac{\Delta I_{\text{cellSUM\_max}}}{I_{\text{cellSUM\_mean}}} \times 100\% \end{cases} \tag{27}$$

where $\triangle I_{\text{cellSUM\_max}}$ represents the maximum difference of cell current in different rows, and $I_{\text{cellSUM\_mean}}$ represents the average value of cell current in all rows.

The imbalance ratio of cell current according to Fig. 15(b) is calculated in Table V. It can be found that when M is set as 8, as the tier number is increased from 1 to 2, the imbalance ratio is slightly increased by 2.0%, which prevents the decline of T_{jmax}, as shown in Fig. 14(a). As the tier number is increased from 2 to 4, the imbalance ratio is rapidly decreased by 6.3% and 5.2% successively, which promotes the decline of T_{jmax}.

In conclusion, the reduction of P_{wire} constitutes a necessary condition for T_{jmax} mitigation, while the reduction of δ_{I} ensures the T_{jmax} mitigation with the multitier layout configuration, which is concluded in Table VI.

V. EXPERIMENTAL EVALUATION

A. Introduction of Experimental Samples and Objectives

According to the introduction in the previous section, a two-step thermal mitigation and optimization technique for stitch-wire-bonded IGBT module is summarized as optimal bonding contact number exploration and wire current alleviation with the multitier layout. Hence four IGBT modules with eight wire numbers are fabricated, which are shown in Fig. 16. The doping concentration, geometry parameters, and temperature-sensitive parameters of the adopted chip are matched with Table I. The material characteristics, geometrical parameters, and chip position coordinates of the fabricated power module are consistent

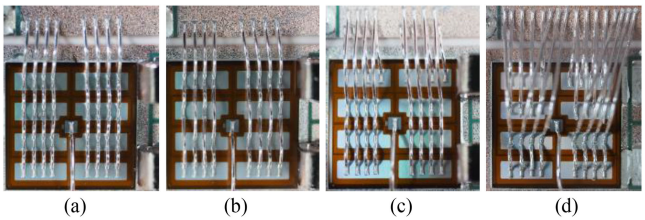

Fig. 16. Overview of (a) Sample A: baseline layout with four bonding contacts, (b) Sample B: baseline layout with three bonding contacts, (c) Sample C: proposed dual-tier layout with four bonding contacts, and (d) Sample D: proposed triple-tier layout with four bonding contacts.

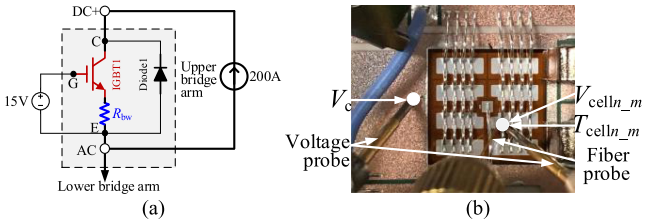

Fig. 17. (a) Electrical schematic diagram. (b) Top view of the experimental test rig for the verification of cell potential and cell temperature.

with Table II. The layout with four bonding contacts shown in Fig. 2 is picked out as the baseline scheme (sample A), which is employed to verify the proposed multicellular electro-thermal model. The baseline layout with three bonding contacts (sample B) is prepared to compare with sample A for the validation of bonding contact number effect. The dual-tier layout with four bonding contacts (sample C) is prepared to compare with sample A for the validation of wire current alleviation optimization. The triple-tier layout with four bonding contacts (sample D) is prepared to compare with sample C for the validation of bonding tier number effect. The IGBT module does not contain silica gel in order to detect the electric potential and temperature.

B. Proposed Model Verification

The proposed model is verified by comparing cell emitter potential and cell temperature with experiments. The baseline sample A is installed on the cooling coldplate. The temperature of liquid oil inside the cooling coldplate is controlled by Julabo PRESTO A80, which is controlled at 20 °C. The cooling capability is up to 1.2 kW. The electrical schematic diagram is shown in Fig. 17(a). The upper bridge arm is selected to be heated with a dc power current source by connecting the power terminals dc+ and ac. The provided +15 V driving voltage $V_{\rm GE}$ is consistent with the model setting in Fig. 6(b).

The top view of experimental test rig is shown in Fig. 17(b). The electric potential is detected by a self-developed voltage probe connected with an 18-bit voltmeter. The probe is placed on the metallization layer surface [30]. The potential of each node V_{n_m} is measured relative to the reference voltage point on the top copper layer of DBC. Since the infrared radiation (IR) thermal imaging required black coatings will insulate the voltage probe, the Opsens contact-type optical fiber probe OTG-F-10 is employed on the corresponding cell to monitor the local temperature, where the maximum temperature measurement error is ±0.8 °C and the resolution is 0.05 °C.

Due to the symmetrical structure, the cell$_{n_1}$ and cell$_{n_4}$ on the left half of the chip are selected as the test objects. The measured cell temperature results and quantitative comparison with the model calculations are listed in Table VII. The measured cell potential results and quantitative comparison with the model calculations are listed in Table VIII. The modeling error relative to experimental results is displayed in Fig. 18. The error of modeled cell temperature is less than 2.5%, which verifies the effectiveness and accuracy of the proposed temperature modeling. The maximum error of modeled cell potential is no more than 3.0%, which verifies the effectiveness and accuracy of the proposed electrical modeling. Furthermore, the formed voltage drop from the chip collector pad to the ground is modeled as 1.80 V, 2.28 V under $I_{\rm chip}$ = 200 A, 250 A, respectively, where the error with the measured results is barely +1.1% (1.78 V), +2.0% (2.24 V). The result declares that the proposed theoretical modeling can meet the requirements of bonding wire design.

TABLE VII
MEASURED CELL TEMPERATURE UNDER VARIOUS CHIP CURRENTS

$I_{\rm chip}$ (A)	Row n	Cell$_{n_1}$ temperature (°C) Exp.	Model	Error	Cell$_{n_4}$ temperature (°C) Exp.	Model	Error
200	4	89.95	89.50	-0.5%	108.70	110.01	+1.2%
	3	84.15	82.97	-1.4%	103.95	105.41	+1.4%
	2	73.35	72.10	-1.7%	90.20	89.32	-1.0%
	1	62.05	60.50	-2.5%	74.40	72.99	-1.9%
250	4	128.95	127.92	-0.8%	158.35	161.99	+2.3%
	3	120.05	117.89	-1.8%	151.25	148.53	-1.8%
	2	103.30	101.34	-1.9%	129.90	127.29	-2.0%
	1	85.55	83.41	-2.5%	105.05	102.53	-2.4%

TABLE VIII
MEASURED CELL POTENTIAL UNDER VARIOUS CHIP CURRENTS

$I_{\rm chip}$ (A)	Row n	Cell$_{n_1}$ potential (mV) Exp.	Model	Error	Cell$_{n_4}$ potential (mV) Exp.	Model	Error
200	4	137.1	134.22	-2.1%	136.5	133.50	-2.2%
	3	222.1	227.54	+2.4%	220.2	223.13	+1.3%
	2	276.3	282.36	+2.1%	275.8	280.20	+1.6%
	1	305.3	311.25	+1.9%	301.1	307.20	+2.0%
250	4	171.5	166.87	-2.7%	171.1	169.22	-1.1%
	3	276.5	285.06	+3.1%	275.9	274.59	-0.4%
	2	345.6	356.28	+3.0%	345.0	355.15	+2.9%
	1	380.0	390.21	+2.6%	379.4	391.03	+3.0%

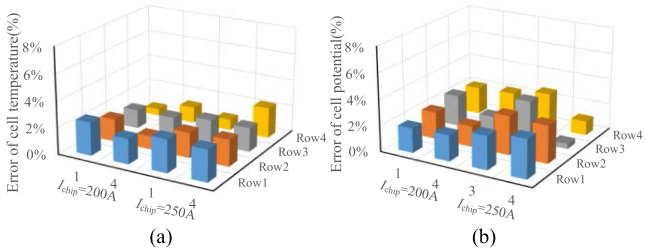

Fig. 18. (a) Error of modeled cell temperature compared with experiments. (b) Error of modeled cell emitter potential compared with experiments.

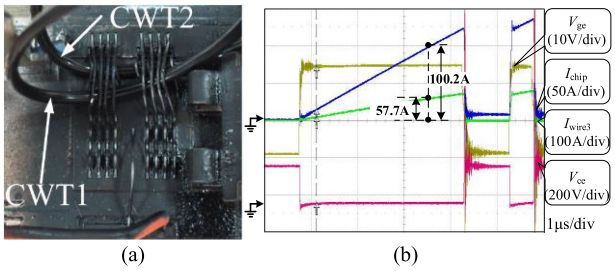

Fig. 19. (a) Double pulse test for the measurement of the wire current density, (b) Measured turn-ON trajectories of sample C (Test condition: 200V/100A).

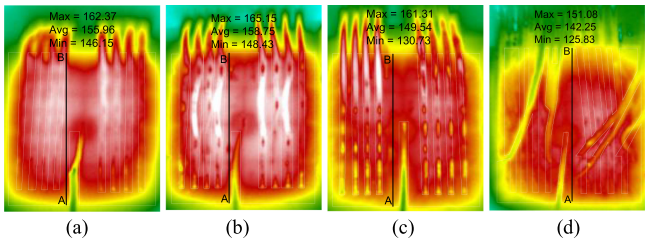

Fig. 20. IR thermal imaging graph of (a) Sample A: baseline layout with four bonding contacts, (b) Sample B: baseline layout with three bonding contacts, (c) Sample C: proposed dual-tier layout with four bonding contacts, and (d) Sample D: proposed triple-tier layout with four bonding contacts ($I_{\rm chip} = 250$ A).

TABLE IX
EXPERIMENTAL RESULTS SUMMARY OF MAXIMUM CHIP TEMPERATURE, AVERAGE CHIP TEMPERATURE, AND PERCENTAGE CHANGE TO SAMPLE A ($I_{\rm CHIP} = 250$ A AND $T_{\rm CASE} = 45$ °C)

Sample number n	M	N	K	$T_{\rm jmax}$ (°C)	% Change to Sample A	$T_{\rm jave}$ (°C)	% Change to Sample A
A	8	4	1	162.37	-	155.96	-
B	8	3	1	165.15	+2.4	158.75	+2.5
C	8	4	2	161.31	-0.9	149.54	-5.8
D	8	4	3	151.08	-9.6	142.25	-12.4

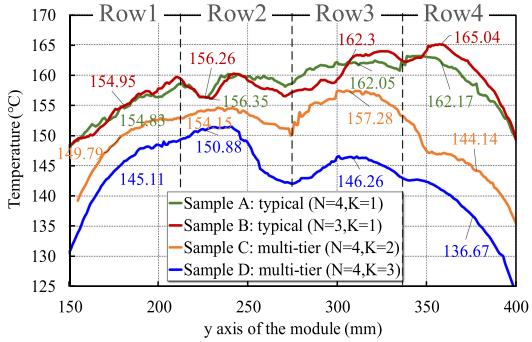

Fig. 21. Temperature in the chip of four samples along the line AB. ($I_{\rm chip} = 250$ A).

C. Optimization Method Verification

The optimization method verification is carried out from both electrical and thermal perspectives. The wire current alleviation benefited from the multitier configuration is first validated. The fourth-row wire current is measured and calculated by two Rogowski coils (30 MHz/300 A, CP9030S) from CYBERTEK, whose maximum error caused by undesired noises is 0.75 A. As shown in Fig. 19(a), CWT1 and CWT2 are employed to measure the third-row wire arches current and the chip current, respectively. Before the measurement, the consistency of the two Rogowski coils, CWT1 and CWT2, is verified by simultaneously measuring the current of terminal dc+. From the double pulse test results shown in Fig. 19(b), the fourth-row wire current can be calculated by

$$I_{\rm wire4} = I_{\rm chip} - I_{\rm wire3} = 100.2 - 57.7 = 42.5{\rm A}. \qquad (28)$$

Thus, the current density of the fourth-row wire arches is reduced from 100.2 A/8wires (sample A) to 42.5 A/8wires (−57.6%), which validates the effectiveness of the multitier layout.

For the sake of intuitively compare the four samples, the IR thermal imaging method is chosen. Based on the experimental setup shown in Fig. 17, the chip surface is coated with the high emissivity black paint, which can be seen in Fig. 19(a). The Fluke Ti450 thermal imager, whose temperature measurement error is within ±2 °C, is used. The tightening screw torque remains the same to control the TIM thermal resistance when comparison. The optical fiber probe is utilized to monitor the case temperature as the reference for temperature rise calculation.

As shown in Fig. 20, the chip temperature from IR thermal imaging graph is extracted by removing the undesired bonding wires [31]. Hence, the experimental results of maximum chip temperature, average chip temperature, and percentage change to sample A are summarized in Table IX. The case temperature is measured as 45 °C. The maximum and average chip temperature of sample A is 162.37 and 155.96 °C, while the maximum and average chip temperature of sample B is 165.15 °C (+2.4%) and 158.75 °C (+2.5%), which verifies that the bonding contact number affects the chip temperature. Furthermore, the maximum and average chip temperature of sample C is 161.31 °C (−0.9%) and 149.54 °C (−5.8%), while the maximum and average chip temperature of sample D is 151.08 °C (−9.6%) and 142.25 °C (−12.4%). The results indicate that the proposed triple-tier layout has a more distinguished effect on chip temperature mitigation than the dual-tier layout.

In order to investigate the chip temperature distribution, the longitudinal temperature results along the line AB of the four samples are summarized in Fig. 21. There is an increasing tendency of chip temperature along the line for sample A and sample B, where the maximum temperature is located in the fourth row. Compared with the baseline sample A, the temperature fluctuation ($T_{\rm row4} - T_{\rm row1}$) of sample B is more severe, where $\triangle T_{\rm sampleA} = 7.34$ °C and $\triangle T_{\rm sampleB} = 10.09$ °C. This result may be attributed to the nonaligned bonding when $N = 3$. Thanks to the wire current alleviation, the fourth-row temperature of sample C is significantly reduced by 15.4% compared to that of sample A, which eventually brings in a 5.8% reduction for the average chip temperature. Due to the cell current imbalance effect mentioned in Section IV-C, the maximum temperature occurs in the third row and is just decreased by 4.2%. The temperature alleviation in the first and second row is also ascribed to the cell current distribution variation of cell_{1_m} and cell_{2_m}, as shown

in Fig. 15. Similar to sample C, the third-row temperature of sample D continues to reduce drastically by 9.8%, which finally results in a 12.4% reduction for the average chip temperature. The maximum temperature is shifted to the second row, while it is still mitigated totally by 9.6% compared with that of sample A. The last row temperature of sample D is further mitigated by 21.8% compared with sample A because of the cell$_{4_m}$ current alleviation. The results validate the mitigation mechanism of chip temperature distribution with the multitier layout.

VI. Conclusion

The local overheating and thermal nonequilibrium of the stitch-wire-bonded IGBT chip was raised by the uneven wire self-heating and nonuniform cell heat flux. A high-accuracy multicellular electro-thermal model was derived to comprehensively evaluate the thermal stress and optimize the bonding parameters. Using the fast-iterative optimization, the 34 mm IGBT module was determined by wire number = 8, bonding contact number = 4, diameter = 0.5 mm, and arc angle = 45°. The improved multitier layout was proposed to further achieve thermal stress suppression. Finally, a 1200-V/200-A half-bridge prototype with the optimal design parameters and triple-tier bonding layout was fabricated and tested. The experimental results showed that the modeling error was less than 3.0%. The multitier layout reduced the current density by 57.6%. The maximum chip temperature and average chip temperature were reduced by 21.8% and 12.4%, respectively, which verified the effectiveness of the proposed optimization method. Therefore, the design methodology for stitch-bonding wire in this article is hopeful to be developed into the design rules for the large chip-area and high current rating power modules. The proposed multicellular electro-thermal modeling method can be adopted in the analysis of dynamic switching process as well. The detailed derivation process is described in the Appendix.

Appendix

The multicellular electro-thermal performance considering the dynamic switching process is modeled as follows.

During the switching process, the parasitism of bonding wires transforms from resistance to inductance due to the increase in frequency [32]. The wire arch inductance and horizontal metallization inductance can be expressed as [33]

$$\begin{cases} L_{\mathrm{wire}n} = \frac{\mu_0 l_{\mathrm{wire}n}}{2\pi}\left(\ln\frac{4l_{\mathrm{wire}n}}{d} - 1\right) \\ l_{\mathrm{wire}n}{=}2\sqrt{\left(W_{\mathrm{chip}}/2N\right)^2 + h^2}, l_{\mathrm{wire}N}{=}2\sqrt{\left(Dis/2\right)^2 + h^2} \\ L_{\mathrm{metal}m} = \frac{\mu_0 L_{\mathrm{chip}}}{2\pi M}\left(\ln\frac{2L_{\mathrm{chip}}}{M(W_{\mathrm{chip}}/N + t_{\mathrm{m}})} + 0.5\right) \end{cases} \tag{29}$$

where μ_0 represents the permeability of vacuum, $\mu_0 = 4\pi\times10^{-7}$ H/m, and l_{wire} represents the length of wire arch.

As shown in Fig. 5, all gate terminals of chip cells are shared with the gate pad and represented by V_{g}. The inductors of wires and metallizations are contained in the gate circuit loops of multicell, forming a network of common emitter stray inductors [11].

For the power module without Kelvin connection, the negative terminal of drive power supply V_{gdrive} and the Nth-row wires are both connected to the top copper layer of DBC, whose electric potential is set as zero.

For the power module with Kelvin emitter wire bonded on the cellx_y, $1 \le x \le N$, $1 \le y \le M$, the negative terminal of drive power supply V_{gdrive} is connected to cellx_y through the Kelvin wire, whose electric potential is identical with that of cell emitter V_{x_y}. The bonding contacts where Nth-row wires are bonded on the top copper layer of DBC are still set as the zero potential references.

The relationship between the cell emitter potential and the branch current can be uniformly expressed with the Laplace operator s

$$\begin{cases} V_{\mathrm{g}} - V_{n\_m} - V_{\mathrm{GEth}} = I_{\mathrm{cell}n\_m}/g_{\mathrm{cell}n\_m} \\ V_{n\_m} - V_{n\_m+1} = sI_{\mathrm{metal}n\_m}L_{\mathrm{metal}m} \\ V_{n\_m} - V_{n+1\_m} = sI_{\mathrm{wire}n\_m}L_{\mathrm{wire}n} \\ V_{N\_1} + \cdots + V_{N\_m} + \cdots + V_{N\_M} = sI_{\mathrm{chip}}L_{\mathrm{wire}N} \end{cases} \tag{30}$$

where

$$g_{\mathrm{cell}n\_m}\left(T_{\mathrm{cell}n\_m}\right) = \frac{A_{\mathrm{cell}}\mu_{\mathrm{ni}}\left(T_{\mathrm{cell}n\_m}\right)\varepsilon_{\mathrm{ox}}}{W_{\mathrm{cell}}L_{\mathrm{ch}}t_{\mathrm{ox}}(1-\alpha_{\mathrm{pnp}})} \tag{31}$$

where A_{cell} is the area of the divided cell, $A_{\mathrm{cell}} = (L_{\mathrm{chip}}W_{\mathrm{chip}})/(MN)$, L_{ch} is the channel length, W_{cell} is the cell pitch, t_{ox} is the oxide thickness, μ_{ni} is the temperature-dependent electron mobility of the channel, which is obtained from Table I, $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the gate oxidation layer, 3.41×10^{-13} F·cm^{-1}, and α_{pnp} is the bipolar current gain.

The circuit equations of three categories of cells represented by V_{1_1}, V_{1_m}, and V_{n_m} are expressed as

$$\begin{aligned} &g_{\mathrm{cell}1\_1}\left(V_{\mathrm{g}} - V_{1\_1} - V_{\mathrm{GEth}}\right) \\ &= \left(V_{1\_1} - V_{2\_1}\right)/\left(sL_{\mathrm{wire}1}\right) + \left(V_{1\_1} - V_{1\_2}\right)/\left(sL_{\mathrm{metal}1}\right) \end{aligned} \tag{32}$$

$$\begin{aligned} &g_{\mathrm{cell}1\_m}\left(V_{\mathrm{g}} - V_{1\_m} - V_{\mathrm{GEth}}\right) \\ &+\left(V_{1\_m-1} - V_{1\_m}\right)/\left(sL_{\mathrm{metal}m-1}\right) \\ &= \left(V_{1\_m} - V_{2\_m}\right)/\left(sL_{\mathrm{wire}1}\right) \\ &+ \left(V_{1\_m} - V_{1\_m+1}\right)/\left(sL_{\mathrm{metal}m}\right) \end{aligned} \tag{33}$$

$$\begin{aligned} &g_{\mathrm{cell}n\_m}\left(V_{\mathrm{g}} - V_{n\_m} - V_{\mathrm{GEth}}\right) \\ &+ \left(V_{n-1\_m} - V_{n\_m}\right)/\left(sL_{\mathrm{wire}n-1}\right) \\ &+\left(V_{n\_m-1} - V_{n\_m}\right)/\left(sL_{\mathrm{metal}m-1}\right) \\ &= \left(V_{n\_m} - V_{n+1\_m}\right)/(s \\ &L_{\mathrm{wire}n}) + \left(V_{n\_m} - V_{n\_m+1}\right)/\left(sL_{\mathrm{metal}m}\right). \end{aligned} \tag{34}$$

In addition, the circuit equation of the gate drive loop for the power module without Kelvin connection is calculated by

$$sR_{\mathrm{g}}C_{\mathrm{ies\_cell}}\sum_{m=1}^{M}\sum_{n=1}^{N}\left(V_{\mathrm{g}} - V_{n\_m}\right) + V_{\mathrm{g}} = V_{\mathrm{gdrive}}. \tag{35}$$

The circuit equation of the gate drive loop for the power module with Kelvin connection is calculated by

$$sR_{\mathrm{g}}C_{\mathrm{ies\_cell}}\sum_{m=1}^{M}\sum_{n=1}^{N}\left(V_{\mathrm{g}}-V_{n\_m}\right)+V_{\mathrm{g}}-V_{x\_y}=V_{\mathrm{gdrive}} \tag{36}$$

where R_{g} represents the gate resistance including the internal gate resistance, $C_{\mathrm{ies\_cell}}$ represents the cell input capacitance, V_{gdrive} represents the gate drive power supply voltage.

The equivalent frequency f is found as [34]

$$\begin{cases} f_{\mathrm{on}}=\frac{1}{\pi t_{\mathrm{r}}}\approx\frac{0.32}{t_{\mathrm{r}}} \\ f_{\mathrm{off}}=\frac{1}{\pi t_{\mathrm{f}}}\approx\frac{0.32}{t_{\mathrm{f}}} \end{cases} \tag{37}$$

where t_{r} and t_{f} represent the rise time and fall time, respectively.

Replacing s with j2πf and solving (30)–(37) for V_{n_m}, V_{g}, and $t_{\mathrm{r}}(t_{\mathrm{f}})$, the turn-ON/OFF energy loss per pulse of each cell $E_{\mathrm{cell}\,n\_m}$ and the turn-ON/OFF energy loss per pulse of each wire arch $E_{\mathrm{wire}\,n\_m}$ can be represented by

$$\begin{cases} E_{\mathrm{cellon}n\_m}\left(E_{\mathrm{celloff}n\_m}\right)=\frac{1}{2}\left(V_{\mathrm{c}}-V_{n\_m}\right)I_{\mathrm{cell}n\_m}t_{\mathrm{r}}\left(t_{\mathrm{f}}\right) \\ E_{\mathrm{wireon}n\_m}\left(E_{\mathrm{wireoff}n\_m}\right)=\frac{1}{6}I^2_{\mathrm{wire}n-1\_m}R_{\mathrm{wire}n-1}t_{\mathrm{r}}\left(t_{\mathrm{f}}\right) \\ \qquad\qquad +\frac{1}{6}I^2_{\mathrm{wire}n\_m}R_{\mathrm{wire}n}t_{\mathrm{r}}\left(t_{\mathrm{f}}\right),n\geq 2 \\ E_{\mathrm{wireon1}\_m}\left(E_{\mathrm{wireoff1}\_m}\right)=\frac{1}{6}I^2_{\mathrm{wire1}\_m}R_{\mathrm{wire1}}t_{\mathrm{r}}\left(t_{\mathrm{f}}\right). \end{cases} \tag{38}$$

Therefore, the switching power loss of each cell $P_{\mathrm{cell}\,n\_m}$ and bonding wire power $P_{\mathrm{wire}\,n\_m}$ is obtained when the load current is sinusoidal, which is

$$\begin{cases} P_{\mathrm{cell}n\_m}=f_{\mathrm{sw}}\left(E_{\mathrm{cellon}n\_m}+E_{\mathrm{celloff}n\_m}\right)/\pi \\ P_{\mathrm{wire}n\_m}=f_{\mathrm{sw}}\left(E_{\mathrm{wireon}n\_m}+E_{\mathrm{wireoff}n\_m}\right)/\pi \end{cases} \tag{39}$$

where f_{sw} is the switching frequency when applied to inverter.

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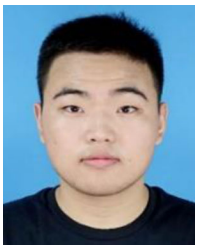

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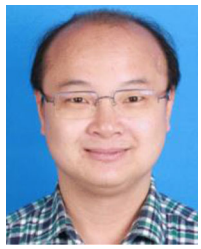

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