The Active Gate Drive Based on Negative Feedback Mechanism for Fast Switching and Crosstalk Suppression of SiC Devices

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***Abstract*—This article introduces the negative feedback into the gate drive. It proposes a negative feedback active gate drive (NFAGD) for silicon carbide devices to fully utilize their potential of high switching-speed capability in a phase-leg configuration. An auxiliary P-channel MOSFET is introduced to construct a negative feedback control mechanism. Due to the negative feedback mechanism, the proposed drive can automatically attenuate the disturbance from the complementary device of the phase-leg. Compared to conventional gate drives, the proposed drive can suppress the crosstalk without influencing the switching speed, thus enables coordinated optimization of gate voltage stability and switching behavior. This article analyzes the operation principle and then recommend the fundamental design principle for the proposed NFAGD. Finally, experiment results demonstrate the effectiveness of the proposed NFAGD.**

***Index Terms*—Active gate drive (AGD), crosstalk suppression, fast switching, gate drive, phase-leg configuration, silicon carbide (SiC).**

NOMENCLATURE

NFAGD	Negative feedback active gate drive.
v_{GS}*	Drive voltage.
v_{GS}	Gate voltage.
R	Drive resistance.
C	Auxiliary capacitor.
τ	Time constant.
Q_N	Controlled N-channel MOSFET.
Q_P	Auxiliary P-channel MOSFET.
R_g	Internal gate resistance of Q_N.
C_{iss}	Input capacitance of Q_N.
C_{gd}	Miller capacitance of Q_N.
$V_{GS,\mathrm{th}}$	Threshold voltage of Q_N.
$V_{GS,IL}$	Miller plateau voltage of Q_N.
g_m	Transconductance gain of Q_P.
V_{th}	Threshold voltage of Q_P.
K_v	Static velocity error constant.

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I. INTRODUCTION

THE EMERGENCE of silicon carbide (SiC) semiconductor devices promises to revolutionize next-generation power electronics converters [1]–[4]. Compared with Si devices, SiC devices featured with high breakdown electric field, low ON-state resistance, fast switching speed, and high junction temperature capability [5], [6]. These characteristics are beneficial for the efficiency, power density, and reliability of power electronics converters [7]–[9]. However, in a practical converter with a phase-leg configuration, the switching transient of one device will impact its complementary device, generating the crosstalk phenomenon [4], [10].

The crosstalk phenomenon is characterized by large high-frequency spikes and oscillations on the interfered device's gate voltage. The fast switching generates high *dv/dt* and *di/dt*, which would pass through the Miller capacitance, inducing high-frequency spikes and oscillations on the gate voltage [11], [12]. Severe spikes and oscillations may lead to false triggers and additional switching losses, even lead to shooting through [9]. Moreover, overshoot and undershoot of the gate voltage are critical parameters that influence the switching-induced drift of gate threshold voltage [13]–[15]. Crosstalk is the critical element for the switching behavior of SiC devices [16]–[18].

As the interface between power circuits and logic control circuits, gate drives significantly affect SiC devices' behavior, including the crosstalk phenomenon. However, the conventional gate drive with the fixed drive resistor must tradeoff between switching behaviors, such as switching speed, switching loss, switch stresses, and crosstalk suppression [19], [20]. For example, a false turn-ON phenomenon due to a significant positive *dv/dt* rating can also be limited by using a separate turn-OFF gate driving network or putting a small capacitor between the gate to source at the expense of reducing the efficiency improvement with higher switching losses [11]. Introducing only the auxiliary passive components for crosstalk suppression should tradeoff between switching behaviors to obtain superior performance

[19]. Induced Miller turn-ON effects and amplitude voltage glitches across the gate-source terminals may be slightly exacerbated due to the higher target commutation speed. Therefore, it is essential to establish proper driving conditions by preventing these anomalies with appropriate mitigation methods without overly compromising the device's switching performance. Hence, introducing auxiliary active devices into the gate drive circuit, researchers propose various active gate drives (AGDs) to suppress SiC MOSFET crosstalk. Naturally, AGD becomes one of the research focus.

As early as 1994, Italian scholars proposed an adaptive driving technique [21], which became one of the beginnings of AGD technology. In the early stage, AGD mainly serves Si-based MOSFETS and IGBTs [22]. By changing driving parameters in the switching transients, the active control is implemented on the transient switching behavior of the device. Hence, the gate drive can dynamically adjust the switching rate, providing additional freedom to balance the electromagnetic interference and switching speed. With the wide application of wide bandgap semiconductor devices, represented by SiC and gallium nitride (GaN), the crosstalk issue becomes one of the most critical elements for the switching behavior, especially in fast switching conditions [16], [23]. Hence, some researchers of the AGD technology paid close attention to the suppression of the crosstalk phenomenon.

An intelligent versatile model-based trajectory optimized AGD is proposed in [24]. Its various operation modes enable it to dynamically adjust the switching speed and be versatile for different scenarios, enabling a finetuned switching speed. Thus, the crosstalk can be suppressed by tuning switching speed by avoiding a too large *dv/dt*. Literature [25] proposed two kinds of AGDs, namely, gate impedance regulation (GIR) and gate voltage control (GVC). GIR predicts the variation trend of induced gate voltage and controls the auxiliary active device preemptively to reduce the gate impedance during the switching transients. Once its gate impedance becomes small during the switching transient, most displacement current will be bypassed by the gate loop, resulting in less current that would induce spurious gate voltage. Thus, crosstalk is mitigated. Similarly, GVC also predicts the variation trend of induced gate voltage. What is different is that GVC preemptively charges the gate–source capacitance before the switching transients to offset the induced voltage. In the follow-up research, literature [26] proposed the intelligent gate drive (IGD). IGD has a gate assist circuit consisting of two auxiliary transistors with two diodes. By predicting the switching behavior, the assist circuits preemptively control the gate voltage and gate loop impedances. However, the complex auxiliary logic circuits are needed for detecting the induced gate voltage, or for predicting the variation trend of the induced gate voltage, to take preemptive action. From the end-users' point of view, additional complexity is added, and the reliability concerns due to extra components. Thus, the acceptance and adoption of these advanced gate drive techniques are limited.

Active miller clamp (AMC) [11], [12], [27] is a typical AGD to attenuate crosstalk and is widely used in commercial gate drive chips with relatively simple components. The gate voltage is detected and the auxiliary clamp device is activated preemptively when the gate voltage drops below a threshold voltage, a value relative to the turn-OFF bias voltage. It is the detected gate voltage that is used to identify the existence of crosstalk. However, the detected gate voltage peaks are less than that across the internal gate–source terminals because of the relatively large internal gate resistance of SiC devices [25]. Moreover, due to the circuit propagation delay, the clamping bandwidth is not high enough for the crosstalk suppression [11], [25]. On the other hand, due to the high switching speed, the detected gate voltage is interfered with mainly by the common-source inductance between the drive loop and power loop, which is inevitable in practical situations [25]. AMC technique shows a significant crosstalk suppression with lower *dv/dt* ratings. However, some limitations and enlarged disturbance are visible at higher *dv/dt*, for example, higher than around 20 V/ns in the testbench used in the literature [11]. The AGD techniques mentioned above show significant crosstalk suppression at a relatively slow switching speed. However, those AGD techniques with a crosstalk suppression control that features a preemptive action, the crosstalk suppression is mainly based on the feedforward architecture [28], which shows significant drawbacks under fast switching speed conditions.

The AGD is based on the feedforward control architecture, and the gate voltage follows the drive's output in an open-loop way. It operates fixedly, pre-set based on switching behavior prediction. The prediction is not always accurate, especially in a fast switching condition, due to detection deviation, propagation delay, and parasitic inductances. The fixed operation cannot be self-adaptive following the increase of *dv/dt* ratings to ensure real-time control and robustness against parameter uncertainty. The AGD based on the feedback control architecture naturally attracts the attention of researchers in this area.

For the AGD techniques with a crosstalk suppression control featured with feedback control, the control method is inherited from the methods for switching slew rate control in the drive of Si-based devices [29]. The feedback control is implemented by high bandwidth analog circuits [30], [31] or digital approaches, such as field-programmable gate array with high-speed and high-resolution D/A and A/D conversion [32], [33]. Unlike the design criterion of AGD for Si power devices, crosstalk suppression for gate voltage stability is critical for SiC devices because of their low threshold voltage, considerable internal gate resistance, and fast switching speed. Several researchers have investigated the SiC-based switching transition negative feedback control by either the electrical approach [24], [34] or the optical approach [35], [36]. That research work enables flexible slew rate control under the maximum switching speed to avoid crosstalk but relatively slow switching speed. Limited feedback control works focus on crosstalk suppression, allowing an increased switching speed.

In summary, implementing negative feedback control in fast switching SiC devices for crosstalk suppression is challenging. First, considering the switching time for SiC devices is as short as tens of nanoseconds, the propagation delay of the feedback control is a concern since it may be comparable, even longer than the switching time. Second, fast switching is always associated with parasitic ringing so that sensors that attempt to identify different switching subintervals easily interfere, resulting in improper

operation. Generally, a high switching speed is desired due to the lower switching loss. However, coordinated optimization of gate voltage stability and switching speed is challenging.

This article proposes an NFAGD employing one auxiliary P-channel MOSFET and one auxiliary capacitor together with the drive resistor for fast switching and crosstalk suppression based on the negative feedback control mechanism. The combined operation mechanism based on negative feedback control in the drive-semiconductor system is given to show the basic operation principle of the proposed gate drive. This article then shows a design reference and experimental test results with commercial 1200V SiC MOSFETs to demonstrate the validity and effectiveness of the proposed methodology.

II. Combined Operation Mechanism Based on Negative Feedback Control in the Drive-Semiconductor System

The gate drive requirements of SiC MOSFETS are similar to its Si counterparts; however, the superior switching capability combined with the specific electrical characteristics of these power devices and parasitic elements requires special attention on the gate drive circuit and layout design to avoid the ringing and overshoot phenomena from becoming an issue. In the phase-leg configuration, the switching process of one device will disturb the gate voltage of the other device in the same phase-leg through the parasitic elements, which might worsen the switching performance and reliability. This interaction between the two devices is called crosstalk. In particular, induced Miller turn-ON effects and amplitude voltage glitches across the gate-source terminals may be slightly exacerbated due to the higher target commutation speed and because the negative gate voltage amplitude maximum rating is different from the positive one contrary to what is typically expected in Si devices. It is therefore very important to establish proper driving conditions by preventing these anomalies with appropriate mitigation methods, without overly compromising the device's switching performance.

This article introduces the negative feedback mechanism into the gate drive to shield interference and attenuate the disturbance generated on the gate voltage during fast switching. Based on the negative feedback control, the gate drive is proposed to suppress the crosstalk issue with a limited number of auxiliary components and a compact structure.

A. Negative Feedback Control Mechanism

The negative feedback mechanism is realized by taking the transconductance of the auxiliary MOSFET as the controller. As given in Fig. 1, the drive voltage $v_{GS}*$ presents as the drive reference, the control input of the whole feedback control system. Then the error between the drive reference and the gate voltage passes through the controller, which is realized by the transconductance gain of auxiliary MOSFET g_m, and controls the system's plant. The plant comprises the input capacitance (C_{iss}) and internal gate resistance (R_g) of the controlled SiC MOSFET. For simplification, the analysis at this section treats the input capacitance approximate linearly.

The disturbance denotes $d(s)$, here in Fig. 1. The object of the negative feedback control loop is to control the gate voltage

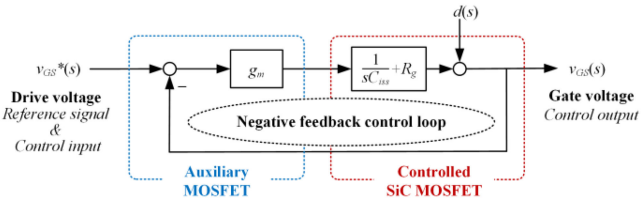

Fig. 1. Negative feedback control based on the transconductance gain in an SiC MOSFET drive-semiconductor system.

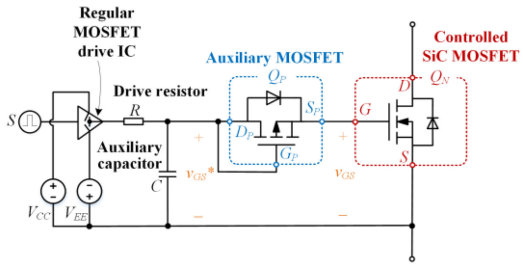

Fig. 2. Negative feedback active gate drive (NFAGD).

v_{GS} track the variation of drive reference $v_{GS}*$. In this way, the feedback loop would attenuate the disturbance from the complementary device of the phase-leg generated by the high switching slew rate.

B. Structure of the Active Gate Drive Based on the Negative Feedback Mechanism

The negative feedback diagram is given in Fig. 1. Based on the negative feedback mechanism, the AGB composes, as shown in Fig. 2. The output of a regular MOSFET drive integrated circuit (IC) is connected to a network, constituted by the drive resistor R and the auxiliary capacitor C. The output of the RC network is also regarded as the drive reference $v_{GS}*$ and presents as the drive reference. It then goes to the gate and source of controlled SiC MOSFET through the auxiliary MOSFET. In this article, v_{GS} represents the gate voltage of SiC MOSFET measured from the pins. For building the negative feedback, the controlled SiC MOSFET and auxiliary MOSFET should have a complementary channel characteristic. Usually, the controlled SiC MOSFET is N-channel. Hence, the auxiliary MOSFET is P-channel. Hereafter, this article denotes the controlled SiC MOSFET and the auxiliary MOSFET as Q_N and Q_P. Hereafter, the drain–source voltage and the drain current of Q_P would be represented as v_{DSP} and i_{DP}.

The RC network is responsible for tunning the speed of switching. The SiC MOSFET gate voltage would follow the drive reference $v_{GS}*$, owing to the negative feedback control. Hence, the speed of gate voltage v_{GS} is similar to that of the drive reference $v_{GS}*$. The proposed gate drive circuit can also be regarded as a compensator. At the same time, it is the feedback control that the compensators embedded to eliminate the steady-state error, as well as to attenuate the disturbance.

C. Mathematical Nature of NFAGD

The article makes two simplifications to explain the mathematical nature of NFAGD. First, the transconductance gain of the auxiliary MOSFET Q_P is treated as a non-time-varying constant g_m. The reverse transconductance gain of the parasitic body diode (the slope of the output characteristic curve) is also expressed by g_m. Second, the conducting threshold voltage of the parasitic body diode of the auxiliary MOSFET Q_P is equal to its forward conducting threshold voltage, and both are denoted V_{th}.

The close-loop transfer function of the NFAGD can be derived from the block diagram shown in Fig. 1, given as follows:

$$\Phi(s) = \frac{v_{GS}(s)}{v_{GS}*(s)} = \frac{G(s)}{1+G(s)} \tag{1}$$

where $G(s)$ is the open-loop transfer function of NFAGD, given as follows:

$$G(s) = g_m\left(\frac{1}{sC_{iss}} + R_g\right) = \frac{g_m}{C_{iss}}\frac{sR_gC_{iss}+1}{s}. \tag{2}$$

According to the system dynamic theory [37], the NFAGD is a unity-feedback type 1 control system. The open-loop gain is g_m/C_{iss}. Static velocity error constant can be expressed as follows:

$$K_v = \lim_{s\to 0} sG(s) = \frac{g_m}{C_{iss}}. \tag{3}$$

In general, the input capacitance of controlled SiC MOSFET (C_{iss}) is about several nano-farads. Simultaneously, the transconductance gain of the auxiliary MOSFET (g_m) is far larger than 1 Siemens, therefore under the international system of units, we can get $g_m >> C_{iss}$, so the static velocity error constant K_v is large enough. Therefore, when the gate voltage v_{GS} tracks the ramping drive reference $v_{GS}*$, the deviation between them is small enough and does not affect the turn-ON and turn-OFF of the controlled SiC MOSFET following the designer's request. Moreover, due to the large static velocity error constant K_v, the suppression ratio of the disturbance $d(s)$ is large enough to attenuate the induced spikes and oscillations on gate voltage $v_{GS}(s)$. Next, the working principle of the NFAGD based on transconductance gain will be expressed by substage analysis according to the theoretical waveform.

III. Operation Principle of the Negative Feedback Active Gate Drive

Fig. 3 shows the phase-leg circuit with NFAGD as the devices' driver. To facilitate the reader to understand the working principle, it demonstrates the controlled SiC MOSFETS (Q_H and Q_L) with the junction capacitors, representing the devices' dynamic characteristics. The meaning of each symbol in Fig. 3 is similar to that shown in Fig. 2. Only to distinguish upper and lower devices, adding marks "1" and "2" respectively, or marks "L" and "H." R_1 and R_2 represent the drive resistor of the upper and lower devices, respectively. C_1 and C_2 represent the auxiliary capacitor of the upper and lower devices, respectively. Q_{P1} and Q_{P2} represent the auxiliary MOSFET of the upper and lower devices, respectively. As the active device in the phase-leg, Q_H is turning ON and OFF under the control of signal S_1. Q_L is the nonactive device in the phase-leg, and its control signal S_2 is steady at a low level to keep the channel of Q_L turning OFF and only its parasitic body diode is used for freewheeling.

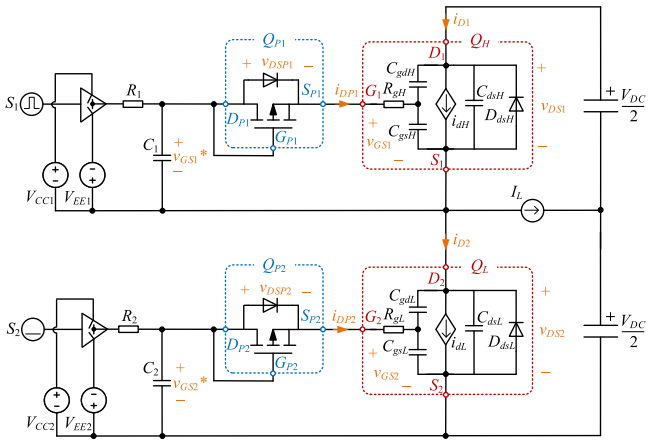

Fig. 3. NFAGD in a phase-leg configuration.

The miller capacitance C_{gdH} and C_{gdL} of the controlled SiC MOSFETS decrease with their drain voltage. This article introduces the piecewise linearization curve to approximate the actual curve for simplification. When the drain voltage is larger than the gate voltage, the value of miller capacitance is C_{gd1}. When the drain voltage is less than the gate voltage, the value of miller capacitance is C_{gd2}. The output current at the midpoint of the phase-leg is approximately constant during the switching process and represented by I_L. Fig. 4 shows the theoretical waveforms of the proposed NFAGD. The turn-ON and turn-OFF process of Q_H is given in Fig. 4(a) and (b), respectively. Four substages correspond to each subfigure. As the auxiliary MOSFETS operate under a low voltage range, usually smaller than the drive voltage. Compared with the power SiC MOSFETS, which have higher operating voltage, auxiliary MOSFETS have an ephemeral dynamic. The dynamic of auxiliary MOSFETS have a minor impact on the operation principle. Hence, the analysis below ignores the influence of the dynamic parameters of auxiliary MOSFETS for better understanding. The auxiliary MOSFET conductivity is nonlinear in practice. However, the nonlinearity shows a minor impact on the proposed gate drive. In fact, the auxiliary MOSFET has enough conductivity while conducting. Hence, the gate voltage tracks its drive reference signal without too large an error. For better understanding, the auxiliary MOSFET conductivity is simplified. Once the auxiliary MOSFET is turned ON, its ON-state resistance is treated as invariant; once the parasitic body diode is turned ON, it remains at the forward voltage.

A. Turn-ON Process of Q_H

Turn-ON substage 1: During the turn-ON delay time $t_{d(on)}$. Before $t = 0$ time point, S_1 changes from a low level to a high level. The driver IC charges C_1 through R_1. Hence, the drive voltage v^*_{GS1} increases, gradually rising from V_{EE1} to V_{CC1}.

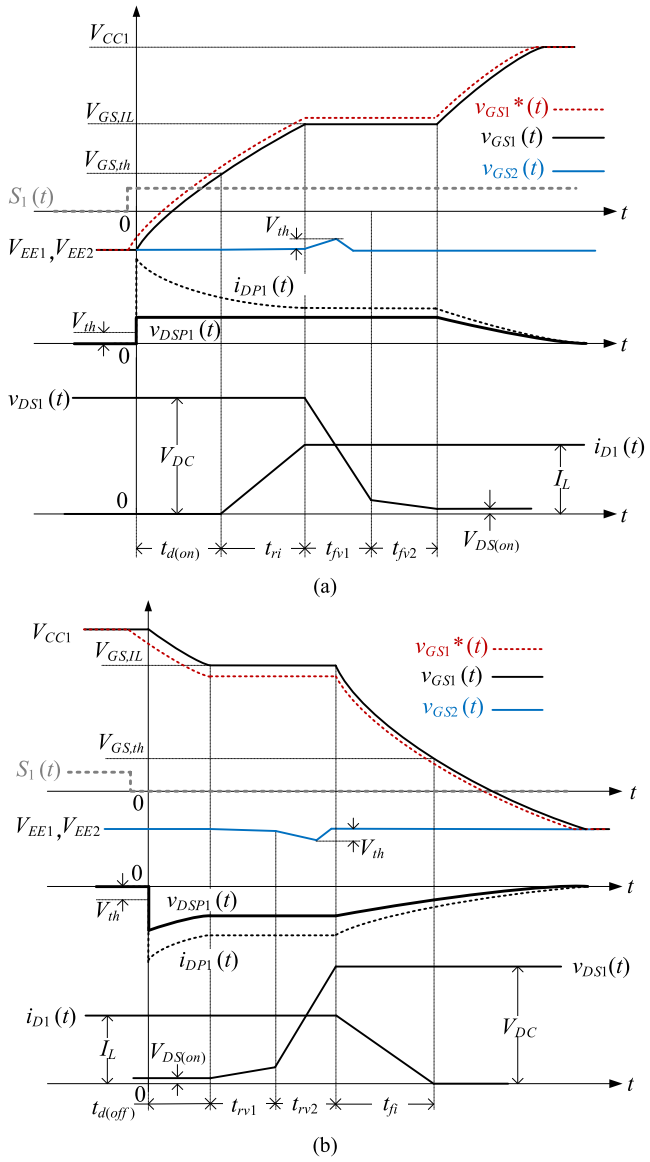

Fig. 4. Theoretical waveforms of the NFAGD. (a) Q_H turn-ON. (b) Q_H turn-OFF.

At $t = 0$ time point, the drain–source voltage of the auxiliary MOSFET v_{DSP1}, equal to the error between v_{GS1^*} and v_{GS1}, is larger than the conducting threshold voltage of the parasitic body diode of Q_{P1}. Hence, the parasitic body diode of Q_{P1} turns ON. v_{DSP1} remains at the forward voltage of the parasitic body diode of Q_{P1}. The forward voltage is small enough while the parasitic body diode is turned ON. Hence, the gate voltage v_{GS1} tracks its drive reference signal v_{GS1^*} without too large an error, which coincides with the mathematical analysis in the last section. The current of the auxiliary MOSFET i_{DP1} flows through the parasitic body diode and the internal gate resistance R_{gH} to charge the input capacitance of Q_H. Because of the negative feedback mechanism, the gate voltage v_{GS1} tracks v_{GS1^*} and also increases gradually. It should be noticed that, as mentioned above, the NFAGD system is a unity-feedback type 1 control system. There is some error in the tracking of the ramping drive reference v_{GS1^*}. The tracking error will not affect the regular operation due to the large value of the static velocity error constant. In this substage, since v_{GS1} is still less than the threshold voltage $V_{GS,\mathrm{th}}$, the channel of Q_H is in the OFF-state, $i_{D1} = 0$ can be got. V_{DS1} stands still at V_{DC}, and this substage ends when v_{GS1} reaches $V_{GS,\mathrm{th}}$.

Turn-ON substage 2: During the current rise time t_{ri}, V_{GS1} starts from the threshold voltage $V_{GS,\mathrm{th}}$, and rises to $V_{GS,IL}$, which indicates the value of v_{GS1} that can maintain channel current at I_L, i.e., the Miller plateau voltage. V_{DS1} stands still at V_{DC}. The current i_{D1} rises from 0 to I_L. During this process, due to the decrease of the passive device's current i_{D2}, the gate voltage of Q_L v_{GS2} increases slightly but is not large enough to trigger the conduction of Q_{P2}. The substage ends at the moment when the current i_{D1} rises to I_L.

Turn-ON substage 3: during the first voltage decrease time t_{fv1}, the gate voltage of Q_H (v_{GS1}) still tracks v_{GS1^*} as the negative feedback controls. Once the SiC MOSFET Q_H carries the full load current I_L, the gate voltage becomes temporarily clamped at $V_{GS,IL}$, which is the gate voltage needed to maintain channel current to be load current I_L. The entire gate charging current equals the current of the auxiliary MOSFET i_{DP1} and is given by the following:

$$i_{DP1} = \frac{C_{gsH}}{C_1 + C_{gsH}} \cdot \frac{V_{CC1} - V_{GS,IL}}{R_1}. \tag{4}$$

It flows through C_{gdH}, and this causes the drain voltage v_{DS1} to drop at a rate

$$\frac{dv_{DS1}}{dt} = \frac{dv_{DG1}}{dt} = \frac{i_{DP1}}{C_{gdH}} = \frac{C_{gsH}}{C_{gdH}} \cdot \frac{V_{CC1} - V_{GS,IL}}{R_1(C_1 + C_{gsH})}. \tag{5}$$

Recall that $v_{GS1} = V_{GS,IL}$ during this interval, so $dv_{GS1}/dt = 0$. The decrease in v_{DS1} occurs in two distinct time intervals t_{fv1} and t_{fv2}. In the first time interval, since the drain voltage is still larger than the gate voltage, the value of C_{gdH} is still relatively small (C_{gd1}). Therefore, v_{DS1} falls at a relatively fast rate at this stage. Q_L's drain voltage (v_{DS2}) rises rapidly, inducing Q_L's gate voltage (v_{GS2}) to rise significantly. Due to the negative feedback mechanism, when the electric potential of S_{P2} is higher than that of D_{P2} and the electric potential difference exceeds the threshold voltage V_{th}, leading to the conduct of Q_{P2}. Then, the drive IC discharges the input capacitance of Q_L (C_{issL}) through the channel of Q_{P2}. Hence, the Q_L's gate voltage v_{GS2} decreases, returning to V_{EE2} and the disturbance is suppressed. This substage ends when v_{DS1} falls to a value equal to v_{GS1}.

Turn-ON substage 4: During the second voltage decrease time t_{fv2}, the gate voltage v_{GS1} remains unchanged at $V_{GS,IL}$, v_{DS1} continues to fall. Since the drain voltage is less than the gate voltage, the value of C_{gdH} is relatively large (C_{gd2}), and the falling rate of v_{DS1} in this stage is relatively slow. This substage ends when v_{DS1} descends to $V_{DS(\mathrm{on})}$.

Once v_{DS1} has completed its drop to the ON-state value of $V_{DS(\mathrm{on})}$, the gate voltage v_{GS1} becomes unclamped and continues its growth to V_{CC1}, tracking its drive reference signal v_{GS1^*}. Simultaneously the current i_{DP1} decays toward zero. Due to the negative feedback mechanism, the error between v_{GS1^*} and v_{GS1} is getting smaller and v_{DP1} decays toward zero. The

turn-ON process is finally completed when v_{GS1} rises to the bias voltage V_{CC1}.

B. Turn-OFF Process of Q_H

Turn-OFF substage 1: During the turn-OFF delay time $t_{d(off)}$. Before $t = 0$ time point, S_1 changes from a high level to a low level. The driver IC discharges C_1 through R_1. Hence, the drive voltage v_{GS1^*} decreases, gradually falling from V_{CC1} to V_{EE1}. Because the gate of Q_{P1} connects to its drain, the drain–source voltage v_{DSP1} equals the error between v_{GS1^*} and v_{GS1}. At $t = 0$ time point, the drain–source voltage of the auxiliary MOSFET v_{DSP1} is smaller than its channel conducting threshold voltage. Hence, the auxiliary MOSFET Q_{P1} turns ON. Once turned ON, the auxiliary MOSFET can be regarded as an invariant ON-state resistance for simplification. The ON-state resistance is small enough while the auxiliary MOSFET is turned ON. Hence, the gate voltage v_{GS1} tracks its drive reference signal v_{GS1^*} without too large an error, which coincides with the mathematical analysis in the last section. The current of the auxiliary MOSFET i_{DP1} flows through its ON-state resistance, along with the internal gate resistance of Q_H (R_{gH}), to discharge the input capacitance of Q_H. Because of the negative feedback mechanism, the gate voltage v_{GS1} tracks v_{GS1^*} and also decreases gradually. It should be noticed that, as mentioned above, the NFAGD system is a unity-feedback type 1 control system. There is some error in the tracking of the ramping drive reference v_{GS1^*}. The tracking error will not affect the regular operation due to the large value of the static velocity error constant. In this substage, since v_{GS1} is still larger than the threshold voltage $V_{GS,\mathrm{th}}$, the channel of Q_H is in the ON-state, $i_{D1} = I_L$ can be got. V_{DS1} stands still at $V_{DS(\mathrm{on})}$, and this substage ends when v_{GS1} reaches $V_{GS,IL}$.

Turn-OFF substage 2: During the first voltage rise time t_{rv1}, the gate voltage of Q_H (v_{GS1}) still tracks v_{GS1^*} as the negative feedback controls. Once the SiC MOSFET Q_H carries the full load current I_L, the gate voltage becomes temporarily clamped at $V_{GS,IL}$, which is the gate voltage needed to maintain channel current to be load current I_L. The entire gate discharging current equals the current of the auxiliary MOSFET i_{DP1} and is given by the following:

$$i_{DP1} = \frac{C_{gsH}}{C_1 + C_{gsH}} \cdot \frac{V_{EE1} - V_{GS,IL}}{R_1}. \tag{6}$$

It flows through C_{gdH}, and this causes the drain voltage v_{DS1} to rise at a rate

$$\frac{dv_{DS1}}{dt} = \frac{dv_{DG1}}{dt} = \frac{i_{DP1}}{C_{gdH}} = \frac{C_{gsH}}{C_{gdH}} \cdot \frac{V_{EE1} - V_{GS,IL}}{R_1(C_1 + C_{gsH})}. \tag{7}$$

Recall that $v_{GS1} = V_{GS,IL}$ during this interval, so $dv_{GS1}/dt = 0$. The increase in v_{DS1} occurs in two distinct time intervals t_{rv1} and t_{rv2}. In the first time interval, since the drain voltage is still less than the gate voltage, the value of C_{gdH} is still relatively large (C_{gd2}). Therefore, v_{DS1} rises at a relatively slow rate at this stage. This substage ends when v_{DS1} rises to a value equal to v_{GS1}.

Turn-OFF substage 3: During the second voltage rise time t_{rv2}, the gate voltage v_{GS1} remains unchanged at $V_{GS,IL}$, v_{DS1} continues to increase. Since the drain voltage is larger than the gate voltage, the value of C_{gdH} is relatively small (C_{gd1}), and the rising rate of v_{DS1} in this stage is relatively fast. Q_L's drain voltage (v_{DS2}) falls rapidly, inducing Q_L's gate voltage (v_{GS2}) to fall significantly. Due to the negative feedback mechanism, when the electric potential of D_{P2} is higher than that of S_{P2} and the electric potential difference exceeds the threshold voltage of the parasitic body diode of Q_{P2}. The drive IC charges the input capacitance of Q_L (C_{issL}) through the parasitic body diode of Q_{P2}. Hence, the Q_L's gate voltage v_{GS2} increases, returning to V_{EE2} and the disturbance is suppressed. This substage ends when v_{DS1} rises to a value equal to V_{DC}.

Turn-OFF substage 4: During the current fall time t_{fi}, due to the negative feedback mechanism, the gate voltage v_{GS1} still falls along with v_{GS1^*}, until v_{GS1} reaches $V_{GS,\mathrm{th}}$. In this substage, v_{DS1} remains unchanged in V_{DC}.

Once v_{DS1} has completed its rise to the input dc voltage V_{DC}, the gate voltage v_{GS1} becomes unclamped and continues its decreasing to V_{EE1}, tracking its drive reference signal v_{GS1^*}. Simultaneously the current i_{DP1} reversely decays toward zero. Due to the negative feedback mechanism, the error between v_{GS1^*} and v_{GS1} is getting smaller and v_{DP1} also reversely decays toward zero.

IV. Principle of Design for the NFAGD

To better understand the combined operation mechanism based on negative feedback control in the drive-semiconductor system, this article would also show the design principle of the NFAGD.

A. Selection Principle for the Controlled SiC mosfet

When adopting the NFAGD, the controlled SiC MOSFET should be determined according to the converters' operation condition, like the conventional semiconductor power device driven by other circuits. In this article's experiment, the 1200 V SiC MOSFET IMZ120R030M1H with high commercialization degree in high power conditions is selected to demonstrate and verify the technical feasibility of the proposed method.

B. Drive IC Selection and Peripheral Circuit Design Principles

The proposed NFAGD has the effect of stabilizing the gate voltage, attenuating the interference effects from the pulse voltage and pulse current. However, it does not eliminate the gate instability problem once for all. Considering the low threshold voltage of the controlled SiC MOSFET (approximately 2–4V), the negative turn-OFF bias voltage is critical. While the turn-ON bias voltage usually relates to the ON-state resistance, whose design should refer to a typical suggestion from the datasheet. This article recommends the turn-ON bias voltage $V_{CC} = 15$–22 V and turn-OFF bias voltage $V_{EE} = -5$–0 V. Based on the above considerations, the bias voltages $V_{CC} = 15$ V and $V_{EE} = -5$ V are adopted in the subsequent design.

This article recommends that the drive IC's isolation part has a common mode transient immunity CMTI$\geq$100 V/ns (within the entire temperature range). The drive IC output current should

be no less than $(V_{CC}\text{-}V_{EE})/R_g$, where R_g is the internal gate resistance of the controlled SiC MOSFET. For example, the selected controlled SiC MOSFET (IMZ120R030M1H) internal gate resistance $R_g = 3\ \Omega$, the bias voltages $V_{CC} = 15$ V, and $V_{EE} = -5$ V is adopted, so drive IC output current should not be less than 6.7 A, subsequent experiments use drive IC IXDN614, which can provide an output current up to 14 A. 1EDI60H12AH is connected in series with IXDN614 for isolation.

C. Selection Principle for the Auxiliary mosfet

To ensure control accuracy, the auxiliary MOSFET's transconductance gain (g_m) should be more significant than 1 Siemens. Then, the threshold voltage ($V_{\rm th}$) should be designed as small as possible, further increasing the sensitivity of auxiliary MOSFET when stabilizing the gate voltage against disturbance.

The auxiliary MOSFET bears a certain current and voltage during the switching transients of the controlled SiC MOSFET. Hence, the auxiliary MOSFET's maximum current and voltage should be designed according to the bias voltages V_{CC} and V_{EE}. The maximum voltage and current of the auxiliary MOSFET should be designed according to the bias voltages V_{CC} and V_{EE}. We recommend that the maximum voltage be no less than $V_{CC}\text{-}V_{EE}$. The maximum current should be no less than $(V_{CC}\text{-}V_{EE})/R_g$.

A huge stray inductance introduced by the auxiliary MOSFET package should be avoided, as it would induce severe oscillation on SiC MOSFET's gate voltage. For example, PG-DSO-8 is recommended be the package of the auxiliary MOSFET. Other lead-less packages are also recommended, and there will be more and more package types to choose from, following the advance of the packaging technique.

Based on the above analysis, BSO201SP will be used as the auxiliary MOSFET in the subsequent experiments of this article. The maximum drain–source voltage is 20 (V), the sustained maximum drain current is 14.9 (A), and the typical value of transconductance gain is 71 (Siemens).

D. Design Principles for Auxiliary Capacitors and Drive Resistors

The design of auxiliary capacitors and drive resistors is based on the drive IC's load capability and switching speed choice.

The drive resistance R has the responsibility for limiting the output current of the driver IC. At the beginning of the switching action, the drive IC charges or discharges the auxiliary capacitor through the drive resistor, whose current reaches a peak valued $(V_{CC}\text{-}V_{EE})/R$. As the bias voltages $V_{CC} = 15$ V and $V_{EE} = -5$ V are adopted in the subsequent design, the drive IC IXDN614 can provide an output current up to 14 A. Hence, for the experimental verification of this article, we choose drive resistance valued at $R = 1.65\ \Omega$ for the drive IC's current limiting.

The auxiliary capacitor and drive resistor (refer to C and R in Fig. 2) determine the rising and falling speed of drive reference $v_{GS}*$ together. The product of auxiliary capacitance C and the drive resistance R is the time constant $\tau = RC$, a representative parameter for determining switching speed.

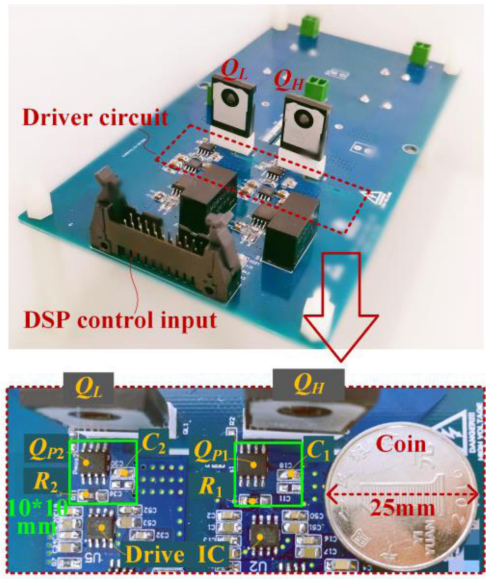

Fig. 5. Experimental hardware picture.

As analyzed in the above sections, the static velocity error constant is large enough. Therefore, the gate voltage v_{GS} tracks the ramping drive reference $v_{GS}*$ with a deviation small enough. Hence, the auxiliary capacitor and drive resistor also determine the rising and falling speed of v_{GS} together. The time constant τ is inversely proportional to the rising and falling rate of gate voltage $v_{GS}*$and v_{GS}. A large value of time constant τ would cause a slow rising and falling rate of gate voltage. Therefore, the switching speed of controlled SiC MOSFET will also be relatively slow. On the contrary, a small time constant τ would cause a fast rising and falling gate voltage rate. Therefore, the switching speed of controlled SiC MOSFET will also be relatively fast.

It should be noticed that, in industrial applications, the time constant τ of NFAGD can be flexibly adjusted according to the comprehensive requirements of efficiency, loss, electromagnetic compatibility.

V. Experimental Verification

This section shows the experimental results to verify the proposed NFAGD. It would provide the hardware parameters, operation principle, and comparison experimental results.

A. Hardware Setup

Fig. 5 shows the hardware setup with the proposed NFAGD. The phase-leg circuit experiment platform is built with the proposed active gate drive, refer to Fig. 3. The newly added components of the proposed gate drive, i.e., the auxiliary MOSFET, drive resistor, and the auxiliary capacitor, are limited to a 10 $*$ 10 mm square area, which realized a straightforward circuit configuration, and the drive circuit occupies not too much extra PCB space. The proposed NFAGD provides a simple and compact drive solution for end-users.

TABLE I
DEVICE PARAMETERS OF PHASE-LEG CIRCUIT EXPERIMENT PLATFORM

Parameters	Symbols	Values
Turn-on bias voltage	V_{CC1}, V_{CC2}	15V
Turn-off bias voltage	V_{EE1}, V_{EE2}	-5V
Auxiliary MOSFET	Q_{P1} Q_{P2}	BSO201SP
Controlled SiC MOSFET	Q_H, Q_L	IMZ120R030M1H

The parameters of the experimental platform are shown in Table I, which are obtained under the guidance of the design process given in the last section.

The digital signal processor (DSP) control board controls the active device Q_H with a double pulse signal and controls the passive device Q_L remains in the OFF-state. Voltage waveforms are measured by the 100 MHz differential probe Yokogawa 700924. The current waveforms are measured by the PEM CWT1 Rogowski current waveform transducer, with a peak current slew rate of 20 A/ns. It should be noticed that the bandwidth of the measurement equipment is high enough to ensure an accurate test of the operation principle and feasibility of the proposed gate driver. Although some research papers recommend higher bandwidth voltage probes and current measurement solutions, those solutions do not meet the needs for testing at both the upper and lower devices in this article. However, when it involves research about the accurate value, we still recommend higher bandwidth voltage and current probes, for example, the equipment in [4] and [10].

B. Verification for Operation Principle

This part of the experiment would investigate the feasibility of constructing a drive circuit based on negative feedback control. The waveforms are measured under input dc voltage $V_{\rm DC} = 800$ V and output current $I_L = 25$ A.

Fig. 6 shows the operation principle waveforms of the proposed NFAGD. Two sets of auxiliary capacitances are given as an example of tuning the switching time. The first one is drive resistance $R_1 = R_2 = 1.65\ \Omega$ and auxiliary capacitance $C_1 = C_2 = 10$ nF. The second one is drive resistance $R_1 = R_2 = 1.65\ \Omega$, auxiliary capacitance $C_1 = C_2 = 20$ nF.

In Fig. 6(a), the time constant is $\tau = 16.5$ ns. The gate voltage v_{GS1} tracked its ramping drive reference v_{GS1^*}. The deviation between them is small enough and does not affect the turn-ON and turn-OFF of the controlled SiC MOSFET following the designer's request. The zoomed-in figures show a transient time valued at about 50 ns, which coincides with the 3τ. In Fig. 6(b), the auxiliary capacitance increased twice as large, the time constant is $\tau = 33$ ns. The gate voltage v_{GS1} still tracked its ramping drive reference v_{GS1^*} with a small deviation. The transient time valued at about 100 ns accordingly, about twice the value in Fig. 6(a).

For further investigation, four sets of parameter cases are considered to measure the switching time. The measured switching time is illustrated in Fig. 7. The time constant $\tau = RC$ is taken

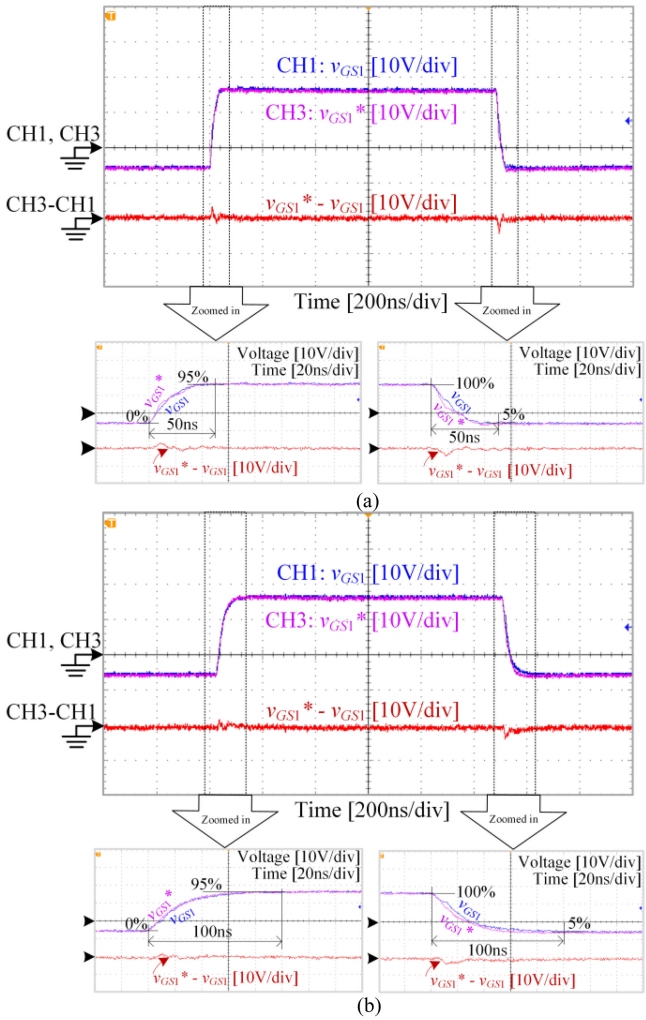

Fig. 6. Experimental waveforms of the proposed NFAGD $R_1 = R_2 = 1.65\ \Omega$ and (a) $C_1 = C_2 = 10$ nF and (b) $C_1 = C_2 = 20$ nF.

as the horizontal axis, the drive resistance is kept at 1.65 Ω, the auxiliary capacitance is chosen as $C_1 = C_2 = 10$, 14.7, 20, 24.7 nF, respectively, corresponding to time constant $\tau = 16.5$, 24.3, 33, 40.8 ns. The vertical axis is the switching time, denoted with each transient phase mentioned in the analysis above. As the major parameters denote the switching speed, the delay time and the voltage transient time are measured. $t_{d(\rm on)}+t_{ri}$ denotes the delay period from the gate voltage starts to rise to the drain voltage starts to fall significantly. t_{fv1} denotes the significantly falling period of drain voltage. $t_{d(\rm off)}+t_{rv1}$ denotes the delay period from the gate voltage starts to fall to the drain voltage starts to rise significantly. t_{rv2} denotes the rise significantly period of drain voltage. Fig. 7 shows that following the increase of time constant, the switching time increases accordingly. The larger the time constant, the longer the switching time.

As given in the last section, the drive resistance is designed to limit the current of drive ICs. Moreover, the time constant τ is designed to control the switching speed. The experimental trend coincides with the design objective. When driving different MOSFETS, the switching time would show different values, but

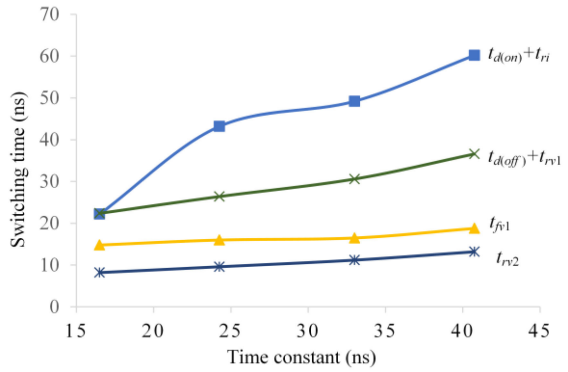

Fig. 7. Measured switching time under different time constants (SiC MOSFET IMZ120R030M1H at $V_{\rm DC} = 800$ V and $I_L = 25$ A).

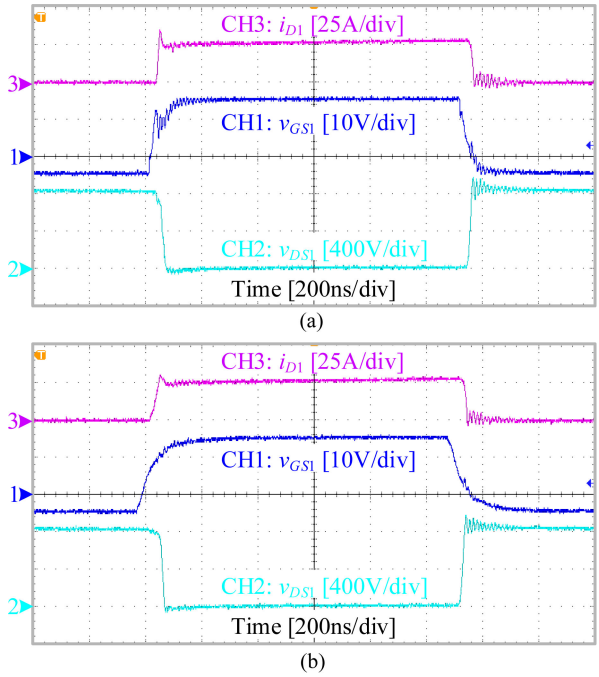

Fig. 8. Measured waveforms with different gate drives. (a) Conventional gate drive. (b) Proposed NFAGD.

the trend shown in Fig. 7 would provide a reference for NFAGD parameter design. In practice, the time constant τ of NFAGD can be flexibly adjusted according to the comprehensive efficiency, loss, and electromagnetic compatibility requirements.

Experimental waveforms of the proposed NFAGD in Figs. 6 and 7 verify that the negative feedback control loop, embedded in the gate drive, controls the gate voltage track the variation of the ramping drive reference. The deviation between them is small enough. It does not affect the turn-ON and turn-OFF of the controlled SiC MOSFET following the designer's request. Furthermore, the switching speed can flexibly change with the designed time constant, which increases the degree of freedom in application.

Fig. 8 is the experimental waveforms with different gate drives under the same operating point, $V_{\rm DC} = 800$ V and $I_L = 25$ A. Fig. 8(a) is the waveforms of the SiC MOSFET driven by the conventional gate drive circuit with only a drive resistor, while Fig. 8(b) is the waveforms under the proposed NFAGD. CH1 is the gate voltage of Q_H, CH2 is the drain voltage of Q_H, and CH3 is the drain current of Q_H. For better comparison, the drive parameters of both drive circuits are chosen to have a similar value of voltage slew rate, see to the waveforms of v_{DS1}. Both Fig. 8(a) and (b) show a similar pulse waveform in the gate voltage v_{GS1}. Waveforms in Fig. 8 also show that choosing an auxiliary MOSFET with a small value of package stray inductance, such as the PG-DSO-8 package in this experiment, the auxiliary MOSFET will not induce severe oscillation on the gate voltage.

Further investigation into the details can reveal that v_{GS1} in Fig. 8(b) shows a less disturbing noise than v_{GS1} in (a), during the rising and falling edges. This is owing to the proposed gate drive circuit, which can be regarded as a compensator, whose feedback control can attenuate the disturbance from the switching action. The experimental results in Fig. 8 coincide with the theoretical analysis in Section II.

Fig. 9 gives the accurate waveforms of controlled SiC MOSFET with the zoomed-in figures beneath the main figure. The simulation is carried out with the Allegro PSpice System Designer, which utilizes accurate internal models, hence taking full consideration for the parasitic parameters such as the parasitic capacitance of MOSFETS. The simulation and the experiment have the same operating point ($V_{\rm DC} = 800$ V and $I_L = 25$ A) and the same time constant τ, thus having similar switching conditions for better comparison.

The accurate waveform of the controlled SiC MOSFET is denoted as v_{GS1} in Fig. 9. The simulation and experimental waveforms of i_{D1}, v_{GS1} and v_{DS1} are given in Fig. 9(a) and (b). In the turn-ON process, v_{GS1} increased following the operation rule of NFAGD given in Section III. After v_{GS1} increased above the threshold voltage of the controlled SiC MOSFET, i_{D1} increased from zero to I_L, v_{DS1} decreased from $V_{\rm DC}$ to ON-state value. In the turn-off process, v_{GS1} decreased following the operation of NFAGD. After v_{GS1} decreased beneath the threshold voltage of the controlled SiC MOSFET, i_{D1} decreased from I_L to zero, v_{DS1} increased from ON-state value to V_{DC}. The experimental waveforms of i_{D1}, v_{GS1} and v_{DS1} in Fig. 9(b) coincide with their simulation counterparts in Fig. 9(a).

The simulation and experimental waveforms of i_{DP1}, v_{GS1} and v_{DSP1} are given in Fig. 9(c) and (d). In the turn-ON process, the parasitic body diode of auxiliary MOSFET turns ON. v_{DSP1} remains at the forward voltage of the parasitic body diode of the auxiliary MOSFET. The forward voltage is small enough while the parasitic body diode is turned ON. The current of the auxiliary MOSFET i_{DP1} flows through the parasitic body diode and the internal gate resistance to charge the input capacitance of the controlled SiC MOSFET. Gate voltage v_{GS1} gradually rises from V_{EE1} to V_{CC1}, following the operation rule of NFAGD given in Section III. In the turn-OFF process, once the drain–source voltage of the auxiliary MOSFET v_{DSP1} is smaller than its channel conducting threshold voltage, the auxiliary MOSFET turns ON. Once turned ON, the auxiliary MOSFET can be regarded as an invariant ON-state resistance for simplification. The ON-state resistance is small enough while the auxiliary MOSFET is turned

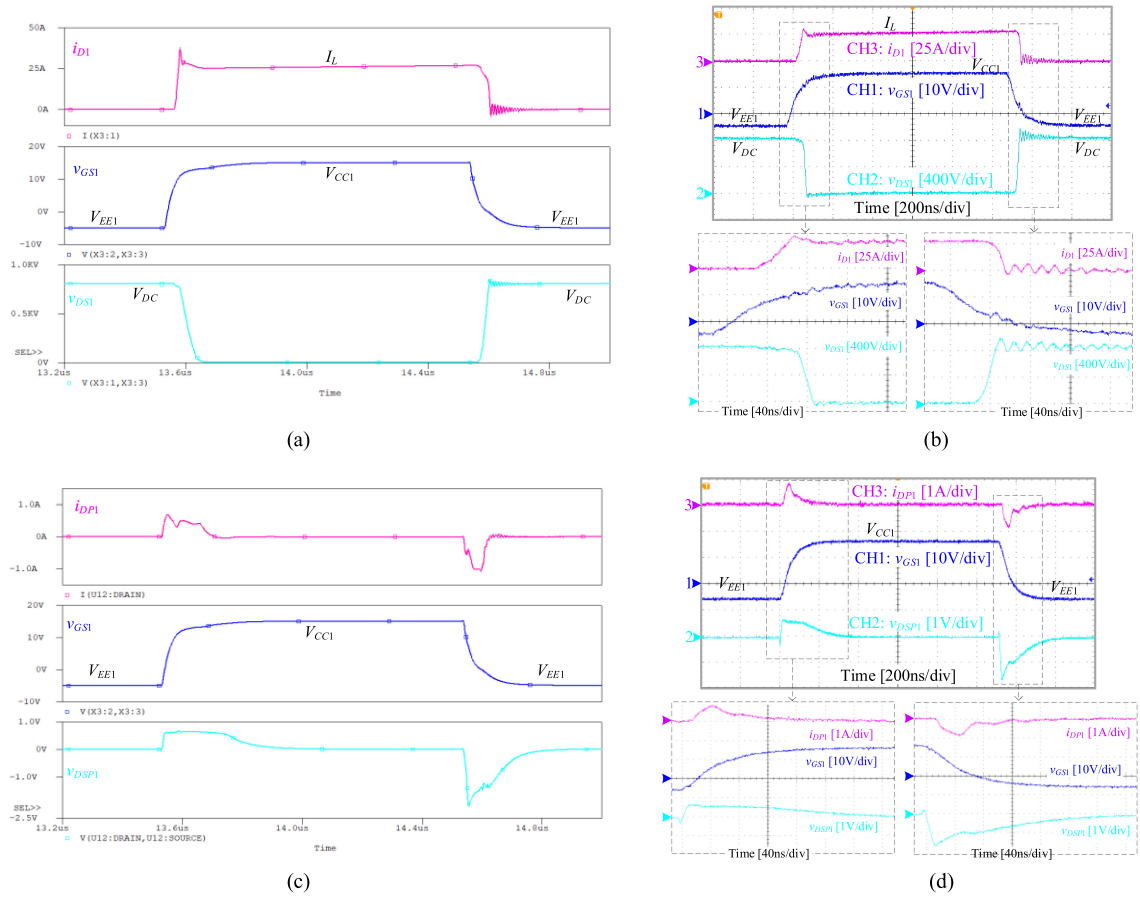

Fig. 9. Accurate waveforms of the controlled SiC MOSFET. (a) Simulation results of i_{D1} v_{GS1} v_{DS1}. (b) Experimental results of i_{D1} v_{GS1} v_{DS1}. (c) Simulation results of i_{DP1} v_{GS1} v_{DSP1}. (d) Experimental results of i_{DP1} v_{GS1} v_{DSP1}.

ON. The current of the auxiliary MOSFET i_{DP1} flows through its ON-state resistance, along with the internal gate resistance to discharge the input capacitance of the controlled SiC MOSFET. Gate voltage v_{GS1} gradually falls from V_{CC1} to V_{EE1}, following the operation rule of NFAGD given in Section III. The experimental waveforms of i_{DP1}, v_{GS1} and v_{DSP1} in Fig. 9(d) coincide with their simulation counterparts in Fig. 9(c).

The simulation and experimental waveforms in Fig. 9 show that the experiment results coincide with the simulation results. In Fig. 9, it should be noticed that v_{GS1} has a smooth transient waveform without great oscillation during the switching processes. The parasitic capacitance introduced by auxiliary MOSFET in the drive circuit will not cause great oscillations, which can be observed from both the simulation and the experiment results, especially the zoomed-in waveforms. Although the auxiliary MOSFET has parasitic capacitance, the parasitic capacitance does not cause great oscillations. Both the simulation and the experimental results are shown that justify the feasibility of the proposed gate drive.

C. Comparison With Conventional Drive Strategies

Gate drives with different strategies of crosstalk suppression are taken into comparison for further investigation. The same SiC MOSFET with different gate drives operated under the same operating point, $V_{\rm DC} = 800$ V and $I_L = 25$ A. The turn-ON and turn-OFF bias voltage remain unchanged, see Table I.

Case 1: Without Suppression (WOS). Fig. 10(a) shows the circuit schematic diagram of this drive. The gate drive with larger and smaller drive resistances are considered, where the drive resistance is $R_1 = R_2 = 10\ \Omega$ and $R_1 = R_2 = 6.7\ \Omega$, respectively. The gate drivers for Q_H and Q_L are conventional circuits with drive resistors R_1 and R_2. The drive circuit embedded no specific auxiliary circuit for crosstalk suppression. The experimental results of case 1 are given in Fig. 10.

Fig. 10(b) shows the waveforms when the drive resistance is $R_1 = R_2 = 10\ \Omega$. CH1 is the gate voltage of Q_L, CH3 is the drain current of Q_H, CH4 is the drain voltage of Q_L. The gate voltage of Q_L shows obvious oscillation during the turning-ON and turning-OFF of Q_H. The induced gate voltage reached about 10 V higher than the turn-OFF bias voltage and about 10 V lower than the turn-OFF bias voltage. Hence, the peak-to-peak induced gate voltage is as large as 20 V. The zoomed-in waveforms of Fig. 10(b) show that during the rising edge of the Q_L drain voltage, its drain voltage rose from 10% to 90% of the operation dc voltage in 15.2n s, which corresponds to a 42.1V /ns slew

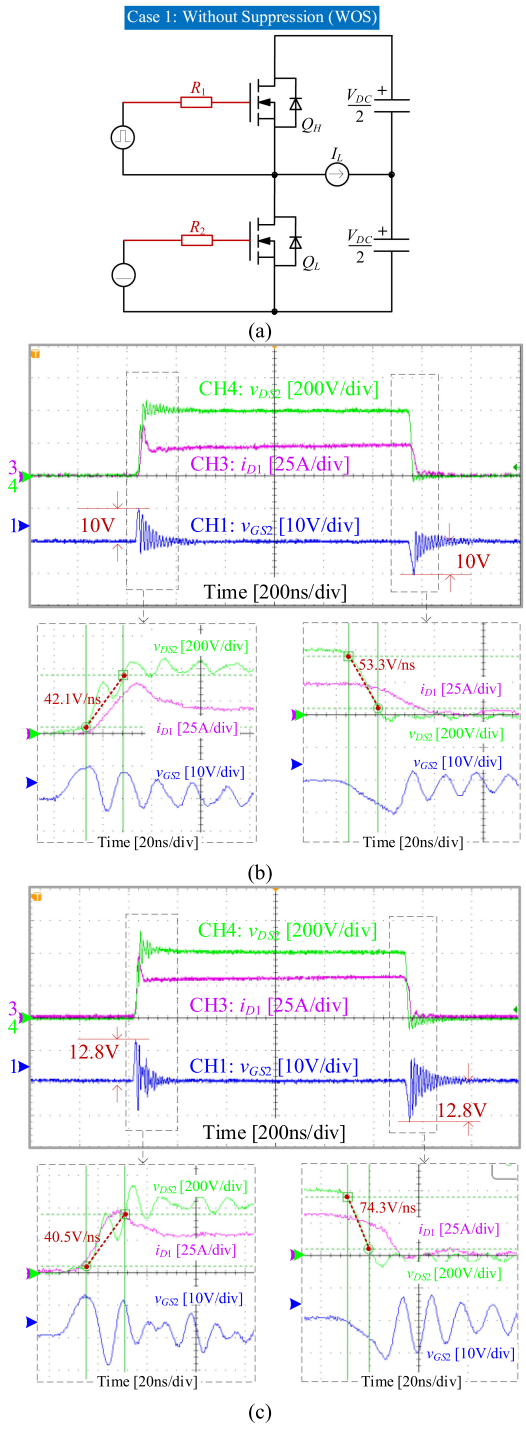

Fig. 10. Experimental results of case 1. (a) Circuit schematic diagram. (b) Waveforms with larger drive resistance. (c) Waveforms with smaller drive resistance.

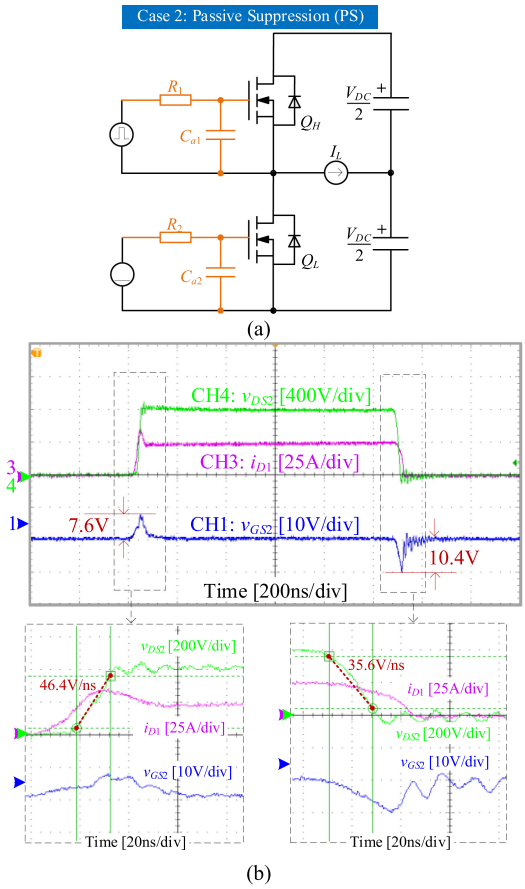

Fig. 11. Experimental results of case 2. (a) Circuit schematic diagram. (b) Waveforms during a switching period.

rate. A high-frequency oscillation mixes with the rising edge, during the falling edge of the Q_L drain voltage. Its drain voltage fell from 90% to 10% of the operation dc voltage in 12 ns, corresponding to a 53.3 V/ns slew rate.

Fig. 10(c) shows the waveforms when the drive resistance is $R_1 = R_2 = 6.7\ \Omega$. The gate voltage of Q_L also shows obvious oscillation during the turning-ON and turning-OFF of Q_H. The induced gate voltage reached about 12.8 V higher than the turn-OFF bias voltage and about 12.8 V lower than the turn-OFF bias voltage. Hence, the peak-to-peak induced gate voltage is as large as 25.6 V. The zoomed-in waveforms of Fig. 10(c) show that during the rising edge of the Q_L drain voltage, its drain voltage has a 40.5 V/ns slew rate. During the falling edge, its drain voltage has a 74.3 V/ns slew rate. If a small value of drive resistors is used, although its switching loss is decreased, the induced gate voltage would be increased.

The waveforms in Fig. 10 indicate that, following the high switching speed, obviously induced gate voltage occurred on the nonactive device Q_L. Crosstalk suppression should be embedded into the gate drive circuit to avoid potential performance degradation and even device failure under this circumstance.

Case 2: Passive Suppression (PS). Fig. 11(a) shows the circuit schematic diagram of this drive. It is one of the common methods to suppress induced gate voltage, featured using passive components in the auxiliary circuit. The auxiliary capacitor is parallel connected between the gate and source of the SiC MOSFET. For obtaining a relatively small value of the induced voltage on the gate voltage of Q_L, the drive resistance remains $R_1 = R_2 = 10\ \Omega$ and the auxiliary capacitance is set to be $C_{a1} = C_{a2} = 2$ nF by the try and error tests, which has a balanced character between crosstalk suppression and

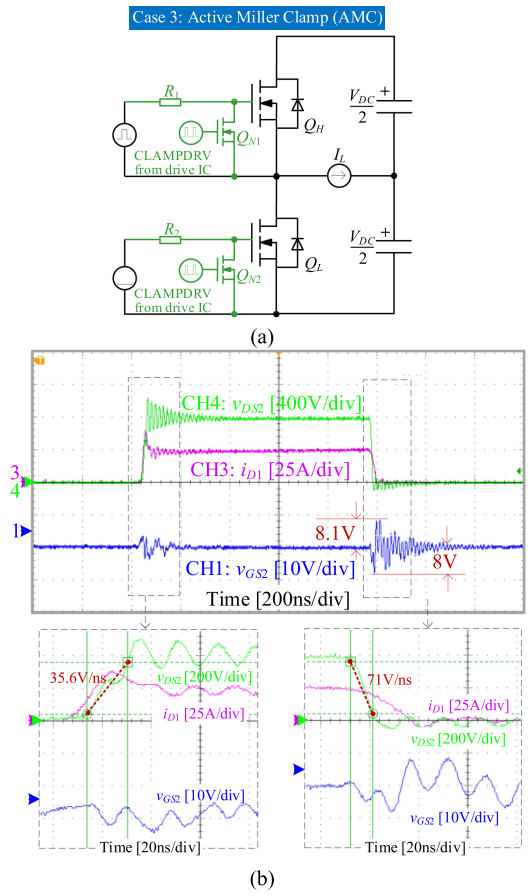

Fig. 12. Experimental results of case 3. (a) Circuit schematic diagram. (b) Waveforms during a switching period.

switching speed. The experimental waveforms of case 2 are given in Fig. 11(b).

In Fig. 11(b), the gate voltage of Q_L shows decreased oscillation during the turning-ON and turning-OFF of Q_H. However, the induced gate voltage is still apparent and reached about 7.6 V higher than the turn-OFF bias voltage and about 10.4 V lower than the turn-OFF bias voltage. Hence, the peak-to-peak induced gate voltage is 18 V, 10% lower than case 1 with the same value of drive resistance. The zoomed-in waveforms of Fig. 11(b) show that during the rising edge of the Q_L drain voltage, its drain voltage rose from 10% to 90% of the operation dc voltage in 13.8 ns, corresponding to a 46.4 V/ns slew rate. During the falling edge of the Q_L drain voltage, its drain voltage fell from 90% to 10% of the dc voltage in 18 ns, corresponding to a 35.6 V/ns slew rate. The rising and falling transients of drain voltage consume about 31.8 ns, 13.6% longer than case 1 with the same value of drive resistance.

The waveforms in Fig. 11 indicate that in case 2, compared with case 1 with the same value of drive resistance, the passive suppression method decreased the induced gate voltage that occurred on the nonactive device Q_L. However, the transient time is increased accordingly.

Case 3: Active Miller Clamp (AMC). Fig. 12(a) shows the circuit schematic diagram of this drive. AMC is one of the typical active crosstalk suppression techniques. In the experiment, the driver IC 1ED3491M provides both the drive voltage and the additional CLAMPDRV signal. When the SiC MOSFET is turned OFF, the drive IC also turns ON the auxiliary transistor Q_{N1} and Q_{N2}. Those auxiliary transistors locate between the gate and source, which form a low impedance path shorting the gate to the negative bias, thus shunting the *dv/dt* induced Miller current and suppressing the consequent voltage spikes on the gate. For simplification, Fig. 12(a) shows the circuit schematic diagram of AMC with two separate voltages sources, one for the drive voltage and the other for CLAMPDRV. In this experiment, we tuned drive resistors R_1 and R_2 valued with 2.35 Ω (two 4.7 Ω resistors connected in parallel) to provide a suitable switching transient for comparison. The experimental results of case 3 are given in Fig. 12(b).

In Fig. 12(b), the gate voltage of Q_L shows a decreased induced gate voltage during the turning-ON and turning-OFF of Q_H. The induced gate voltage reached about 8.1 V higher than the turn-OFF bias voltage and about 8 V lower than the turn-OFF bias voltage. Hence, the peak-to-peak induced gate voltage is 16.1 V, about 20% lower than that of case 1. However, the gate voltage has obvious high-frequency oscillation. During the rising edge of the Q_L drain voltage, its drain voltage rose from 10% to 90% of the operation dc voltage in 16.6 ns, which corresponds to a 35.6 V/ns slew rate. During the falling edge of the Q_L drain voltage, its drain voltage fell from 90% to 10% of the operation dc voltage in 9 ns, which corresponds to a 71 V/ns slew rate. The rising and falling transients of drain voltage consume about 25.6 ns.

The waveforms in Fig. 12 indicate that, in case 3, the AMC method further decreased the induced gate voltage. In the meantime, the transient time is also decreased accordingly. However, due to the high switching speed, some high-frequency oscillations are visible in practical situations, which coincide with [11] and [25].

Case 4: is the proposed NFAGD. Two sets of time constant are considered. Fig. 13(a) is the waveform with a smaller time constant, valued $\tau = 16.5$ ns. The drive resistance $R_1 = R_2 = 1.65\ \Omega$ and auxiliary capacitance $C_1 = C_2 = 10$ nF. Fig. 13(b) is the waveforms with a larger time constant, valued $\tau = 33$ ns. The drive resistance $R_1 = R_2 = 1.65\ \Omega$ and auxiliary capacitance $C_1 = C_2 = 20$ nF.

In Fig. 13(a), the gate voltage of Q_L shows a dramatically decreased induced gate voltage during the turning-ON and turning-OFF of Q_H. The induced gate voltage reached about 3.2 V higher than the turn-OFF bias voltage and about 4.4 V lower than the turn-OFF bias voltage. Hence, the peak-to-peak induced gate voltage is 7.6 V. The percentage of suppression is larger than case 2 (10%) and case 3 (20%). The gate voltage high-frequency oscillation is also suppressed. During the rising edge of the Q_L drain voltage. Its drain voltage rose from 10% to 90% of the operation dc voltage in 14.8 ns, corresponding to a 43.2 V/ns slew rate. During the falling edge of the Q_L drain voltage. Its drain voltage fell from 90% to 10% of the operation dc voltage

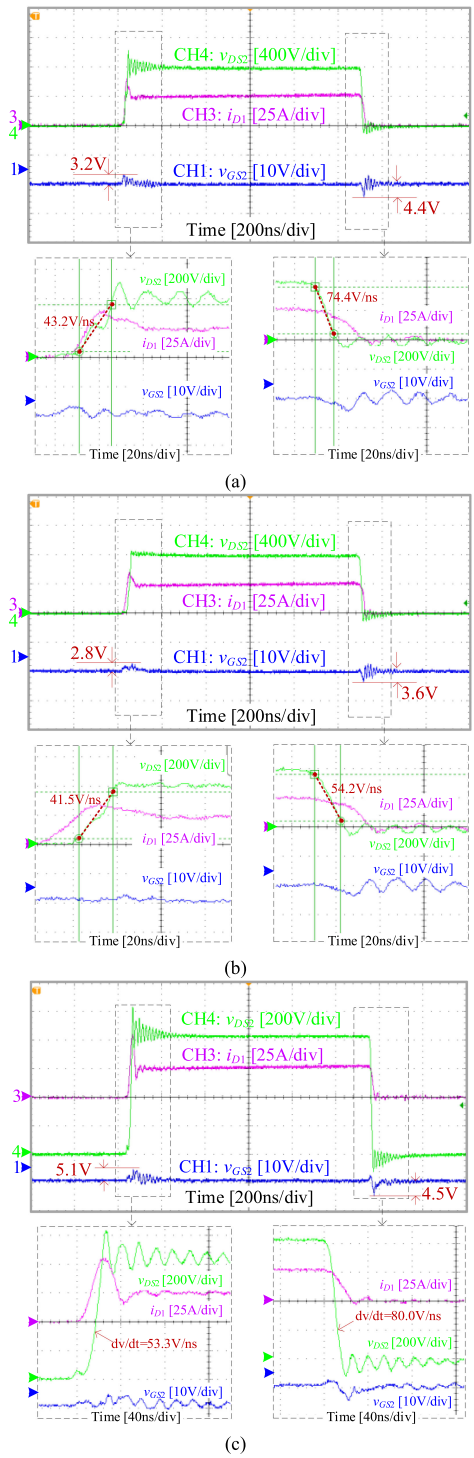

Fig. 13. Experimental results of case 4 the proposed NFAGD. (a) Waveforms with a smaller time constant. (b) Waveforms with a larger time constant. (c) Under high temperature @125 °C.

in 8.6 ns, corresponding to a 74.4 V/ns slew rate. The rising and falling transients of drain voltage consume about 23.4 ns.

The waveforms in Fig. 13(a) indicate that the proposed NFAGD method dramatically decreased the induced gate voltage, as well as the high-frequency oscillation. In the meantime, the transient time is also dramatically decreased.

In Fig. 13(b), the gate voltage of Q_L shows a dramatically decreased induced gate voltage during the turning-ON and turning-OFF of Q_H. The induced gate voltage reached about 2.8 V higher than the turn-OFF bias voltage and about 3.6 V lower than the turn-OFF bias voltage. Hence, the peak-to-peak induced gate voltage is 6.4 V. The percentage of suppression is similar to NFAGD with a smaller time constant (62%). During the rising edge of the Q_L drain voltage, its drain voltage rose from 10% to 90% of the operation dc voltage in 15.4 ns, corresponding to a 41.5 V/ns slew rate. During the falling edge of the Q_L drain voltage, its drain voltage fell from 90% to 10% of the operation dc voltage in 11.8 ns, corresponding to a 54.2 V/ns slew rate. The rising and falling transients of drain voltage consume about 27.2 ns, similar to case 1 with a larger value of drive resistance. The drain voltage shows smooth transient waveforms without additional oscillation.

The above waveforms in Fig. 13(a) and (b) are obtained at room temperature. In Fig. 13(c), the proposed NFAGD experimental platform is heating up to operate under high temperatures. The time constant is the same as Fig. 13(a), with a smaller time constant valued $\tau = 16.5$ ns. During the rising edge, the drain voltage slew rate is 53.3 V/ns, while during the falling edge, the drain voltage slew rate is 80.0 V/ns. At high temperatures, the slew rate is larger than in Fig. 13(a), mainly because increasing the junction temperature will lead to a long carrier lifetime, resulting in a fast switching speed [38]. The faster switching speed enlarged the induced gate voltage. It reached about 5.1 V higher than the turn-OFF bias voltage and about 4.5 V lower than the turn-OFF bias voltage. Hence, the peak-to-peak induced gate voltage is 9.6 V. At high temperatures, the induced gate voltage is still smaller than 10 V and smaller than case 3. The proposed NFAGD can operate at a reasonably high temperature.

The waveforms in Fig. 13 indicate that the proposed NFAGD with a larger time constant dramatically decreased the induced gate voltage, as well as the high-frequency oscillation. The suppression percentage is similar to NFAGD with a smaller time constant. The changing of the time constant has a minor impact on the crosstalk suppression performance. In the meantime, the transient drain voltage waveform has a much smoother performance without obvious high-frequency oscillation. With a smaller time constant, the NFAGD in case 4 shows good crosstalk suppression and high switching speed. However, in some circumstances, it should avoid strong electromagnetic interference by high-speed drain voltage, with a larger time constant to show the excellent crosstalk suppression performance and the flexible switching transients.

D. Summary and Discussion

The above comparison shows the waveforms under a fixed load current $I_L = 25$ A, which is about 44.6% of the maximum rating drain current of SiC MOSFET IMZ120R030M1H (56 A) and is a typical operating current when using this type. Fig. 14 shows further investigation results considering the varying load current I_L, from 17.9% to 44.6% rating.

Fig. 14(a) is the induced peak–peak gate voltage under different load current I_L. The induced peak–peak gate voltage

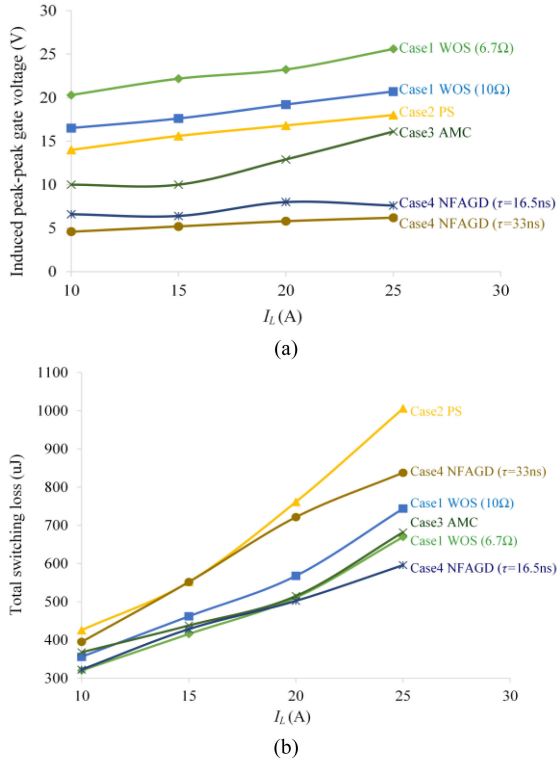

Fig. 14. Characteristics under different load current I_L. (a) Induced peak–peak gate voltage. (b) Total switching loss.

V_{pp} is the differential between the maximum value and the minimum value of v_{GS2}. The data in Fig. 14(a) is collected by reading the waveform from the oscilloscope. From light load to heavy load, case 1 with 6.7 Ω drive resistance has the largest induced gate voltage. Case 1 with 10 Ω drive resistance has a smaller value of induced gate voltage, but it is still relatively large. Case 2 using the passive suppression method can slightly decrease the induced gate voltage, but the induced peak–peak gate voltage is still far larger than 10 V. Case 3 using the AMC technique has a decreased induced peak–peak gate voltage to around 10 V. However, following the load current increase, the induced gate voltage occurs an obvious increase showing a weakened crosstalk suppression performance. Using the proposed NFAGD, both using a smaller time constant τ and larger time constant τ, obtain an obvious decreased induced gate voltage, far smaller than 10 V over the light load and the heavy load. It provides a robust crosstalk suppression against the varying operating current.

Fig. 14(b) is the total switching loss under different load current I_L. The total switching loss is obtained by calculating the area of overlapping waveforms of Q_H drain voltage and drain current during the turn-ON and turn-OFF processes. Compared with case 1 with 10 Ω drive resistance, which has no specific crosstalk suppression, but has a relatively smaller value of induced gate voltage, NFAGD (τ = 33 ns) and the driver with passive suppression (case 2) have an increased switching loss over the light and heavy load current. Meanwhile, NFAGD ($\tau = 16.5$ ns) and the driver with AMC (case 3) have a decreased switching loss over the light and heavy load current. Although

TABLE II
PER-UNITED EXPERIMENTAL SWITCHING PERFORMANCE RESULTS WITH DIFFERENT GATE DRIVES

Gate drives	V_{pp}	Switching loss	t_v	t_i
Case1 WOS (10Ω)	2.7	1.25	1.2	1.22
Case1 WOS (6.7Ω)	3.4	1.12	1.07	1.10
Case2 PS	2.3	1.69	1.36	2.04
Case3 AMC	2.1	1.14	1.09	1.63
Case 4 NFAGD (τ=16.5ns)	1.0	1.00	1.00	1.00
Case 4 NFAGD (τ=33ns)	0.8	1.41	1.16	1.67

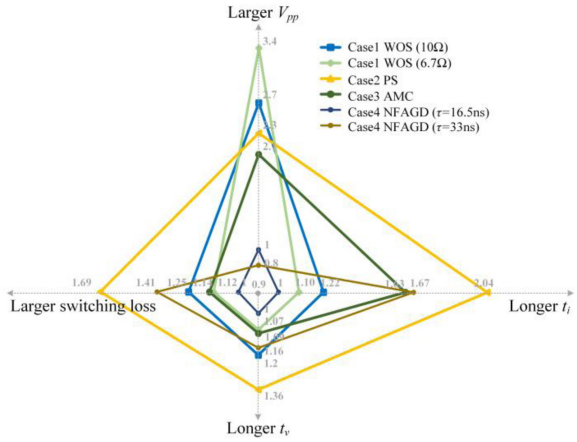

Fig. 15. Switching performance of different gate drives.

case 1 with 6.7 Ω drive resistance also has a similar switching loss performance with NFAGD ($\tau = 16.5$ ns) under different load current I_L, the proposed NFAGD has a superior performance in balancing induced gate voltage and switching loss. Compared to conventional gate drives, the proposed drive can suppress the crosstalk without influencing the switching speed, thus enables coordinated optimization of gate voltage stability and switching behavior.

Table II summarized the experimental results about the switching performance of different gate drives. Under the typical test point $V_{\rm DC}$ = 800 V and I_L = 25 A, four aspects are considered, i.e., induced peak–peak gate voltage, current transient, voltage transient, and switching loss. The induced peak–peak gate voltage V_{pp} is the differential between the maximum value and the minimum value of v_{GS2}. The current transient time t_i is the sum of drain current rising time and falling time. The voltage transient time t_v is the sum of drain voltage rising time and falling time. The total switching loss is obtained by calculating the area of overlapping waveforms of drain voltage and drain current during the turn-ON and turn-OFF processes. In the table, the denoted data is the per-unit value based on case 4 NFAGD ($\tau = 16.5$ ns).

Fig. 15 illustrates the radar map of switching performance data in Table II. For the induced peak–peak gate voltage V_{pp}, NFAGD with different time constant has a similar value of V_{pp}.

The proposed NFAGD only has about 30% of case 1 with 10 Ω drive resistance, which is also far smaller than case 2 and case 3. The changing of the time constant in parameter design does not affect the final crosstalk suppression performance. Hence, the proposed NFAGD provides a robust drive solution with crosstalk suppression for end-users.

NFAGD ($\tau = 16.5$ ns) has the shortest t_v and the shortest t_i, about 50% of the longest t_v and about 70% of the longest t_i. Although when $\tau = 33$ ns NFAGD shows a longer transient time, it is still shorter than the conventional crosstalk passive suppression method in case 2, about 20% shorter. Owing to a relatively short switching transient, NFAGD ($\tau = 16.5$ ns) obtains the smallest switching loss, only about 60% of the largest loss. It gets a 20% decrease from the switching loss of case 1 with 10 Ω drive resistance, which is the common gate drive without any embedded crosstalk suppression auxiliary circuit.

Compared to the conventional gate drives (WOS, PS, AMC), the overall switching performance has been improved using the proposed NFAGD. It has the minimized induced gate voltage and provides a robust crosstalk suppression with flexibility, obtains the shortest voltage transient and the shortest current transient, and minimized switching loss. The proposed NFAGD can suppress the induced gate voltage in fast switching SiC MOSFET. The time constant τ of NFAGD can be flexibly adjusted according to the comprehensive requirements of efficiency, loss, electromagnetic compatibility. The smaller value of τ is suggested when using in a condition with a high power density and cares conversion efficiency. The larger value of τ is suggested when using a condition with high switching frequency and high requirements for electromagnetic capability. The proposed NFAGD enables coordinated optimization of gate voltage stability and switching behavior.

VI. Conclusion

Base on the negative feedback control mechanism, an NFAGD employing one auxiliary P-channel MOSFET and one auxiliary capacitor together with the drive resistor is proposed for fast switching and crosstalk suppression. The object of the NFAGD is to control the gate voltage track the variation of drive reference with a feedback control loop. Thus, the feedback mechanism would attenuate the disturbance, decrease the induced gate voltage. The test results with commercial 1200 V SiC MOSFETS verify that the negative feedback control loop controls the gate voltage to track the drive reference. The deviation between them is small enough, does not affect the turn-ON and turn-OFF of the controlled SiC MOSFET. The switching speed can flexibly change with the designed time constant, which increases the degree of freedom in application. Compared to the conventional gate drives (WOS, PS, AMC), the overall switching performance has been improved using the proposed NFAGD. Under the tested operating point, the proposed NFAGD minimizes induced gate voltage and provides a robust crosstalk suppression with flexibility. It obtains the shortest voltage transient and the shortest current transient, and the minimized switching loss. Thus, the proposed NFAGD enables coordinated optimization of gate voltage stability and switching behavior.

References

[1] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.,* vol. 29, no. 5, pp. 2155–2163, May 2014.

[2] D. Tan, "Emerging system applications and technological trends in power electronics: Power electronics is increasingly cutting across traditional boundaries," *IEEE Power Electron. Mag.,* vol. 2, no. 2, pp. 38–47, Jun. 2015.

[3] A. Bindra, "Wide-bandgap-based power devices: Reshaping the power electronics landscape," *IEEE Power Electron. Mag.,* vol. 2, no. 1, pp. 42–47, Mar. 2015.

[4] F. Wang and Z. Zhang, "Overview of silicon carbide technology: Device, converter, system, and application," *CPSS Trans. Power Electron. Appl.,* vol. 1, pp. 13–32, 2016.

[5] F. Wang, Z. Zhang, and E. A. Jones, *Characterization of Wide Bandgap Power Semiconductor Devices*, Croydon, U.K.: CPI Group (U.K.) Ltd, 2018.

[6] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET," *IEEE Trans. Power Electron.,* vol. 21, no. 2, pp. 310–319, Mar. 2006.

[7] M. Liang, T. Q. Zheng, C. Ke, Y. Li, and X. You, "Performance comparison of SiC MOSFET, Si CoolMOS and IGBT for DAB converter," *Trans. China Electrotech. Soc.,* vol. 30, pp. 41–50, 2015.

[8] R. Bosshard and J. W. Kolar, "All-SiC 9.5 kW/dm^3 On-board power electronics for 50 kW/85 kHz automotive IPT system," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 5, no. 1, pp. 419–431, Mar. 2017.

[9] Z. Zhang, B. Guo, and F. Wang, "Evaluation of switching loss contributed by parasitic ringing for fast switching wide band-gap devices," *IEEE Trans. Power Electron.,* vol. 34, no. 9, pp. 9082–9094, Sep. 2019.

[10] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert, and B. J. Blalock, "Methodology for wide band-gap device dynamic characterization," *IEEE Trans. Power Electron.,* vol. 32, no. 12, pp. 9307–9318, Dec. 2017.

[11] "Mitigation technique of the SiC MOSFET gate voltage glitches with Miller clamp," STMicroelectronics, Geneva, Switzerland, Application Note AN-5355, 2019, Accessed: Mar. 18, 2020. [Online]. Available: https://www.st.com

[12] "Active Miller clamp," Avago Technol., Singapore, Application Note AN-5314, 2010, Accessed: Mar. 18, 2020. [Online]. Available: http://www.avagotech.com

[13] T. Aichinger, G. Rescher, and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectron. Rel.,* vol. 80, pp. 68–78, 2018.

[14] D. Peters, T. Aichinger, T. Basler, G. Rescher, K. Puschkarsky, and H. Reisinger, "Investigation of threshold voltage stability of SiC MOSFETs," in *Proc. IEEE 30th Int. Symp. Power Semicond. Devices ICs*, 2018, pp. 40–43.

[15] "Guidelines for coolsic$^{\mathrm{TM}}$ MOSFET gate drive voltage window," Infineon Technol., Neubiberg, Germany, Application Note AN-2018-09, 2018, Accessed: Mar. 18, 2020. [Online]. Available: http://www.avagotech.com

[16] Z. Zhang, W. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Analysis of the switching speed limitation of wide band-gap devices in a phase-leg configuration," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2012, pp. 3950–3955.

[17] T. Shao *et al.*, "Impact of common source inductance on the gate-source voltage negative spike of SiC MOSFET in phase-leg configuration," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf.*, 2020, pp. 3361–3365.

[18] T. Shao *et al.*, "Induced gate-source voltage mechanism and gate driver design in All-SiC PWM rectifier with ultra-high voltage slew rate (dv/dt)," in *Proc. IEEE 9th Int. Power Electron. Motion Control Conf.*, 2020, pp. 1863–1867.

[19] Z. Zeng and X. Li, "Comparative study on multiple degrees of freedom of gate drivers for transient behavior regulation of SiC MOSFET," *IEEE Trans. Power Electron.,* vol. 33, no. 10, pp. 8754–8763, Oct. 2018.

[20] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An experimental investigation of the tradeoff between switching losses and EMI generation with hard-switched all-Si, Si-SiC, and all-SiC device combinations," *IEEE Trans. Power Electron.,* vol. 29, no. 5, pp. 2393–2407, May 2014.

[21] S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, and M. Melito, "A new adaptive driving technique for high current gate controlled devices," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 1994, pp. 480–486.

[22] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Trans. Power Electron.,* vol. 29, no. 7, pp. 3720–3732, Jul. 2014.

[23] D. Peftitsis and J. Rabkowski, "Gate and base drivers for silicon carbide power transistors: An overview," *IEEE Trans. Power Electron.,* vol. 31, no. 10, pp. 7194–7213, Oct. 2016.

[24] S. Zhao, X. Zhao, A. Dearien, Y. Wu, Y. Zhao, and H. A. Mantooth, "An intelligent versatile model-based trajectory-optimized active gate driver for silicon carbide devices," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 8, no. 1, pp. 429–441, Mar. 2020.

[25] Z. Zhang, F. Wang, L. M. Tolbert, and B. J. Blalock, "Active gate driver for crosstalk suppression of SiC devices in a phase-leg configuration," *IEEE Trans. Power Electron.,* vol. 29, no. 4, pp. 1986–1997, Apr. 2014.

[26] Z. Zhang, J. Dix, F. Wang, B. J. Blalock, D. Costinett, and L. M. Tolbert, "Intelligent gate drive for fast switching and crosstalk suppression of SiC devices," *IEEE Trans. Power Electron.,* vol. 32, no. 12, pp. 9319–9332, Dec. 2017.

[27] Z. Chen, M. Danilovic, D. Boroyevich, and Z. Shen, "Modularized design consideration of a general-purpose, high-speed phase-leg PEBB based on SiC MOSFETs," in *Proc. 2011 14th Eur. Conf. Power Electron. Appl.*, 2011, pp. 1–10.

[28] G. C. Goodwin, S. F. Graebe, and M. E. Salgado, *Control System Design*. London, U.K.: Pearson, 2000.

[29] S. Zhao, X. Zhao, Y. Wei, Y. Zhao, and H. A. Mantooth, "A review on switching slew rate control for silicon carbide devices using active gate drivers," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 9, no. 4, pp. 4096–4114, Aug. 2021.

[30] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, and B. J. Blalock, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Trans. Power Electron.,* vol. 29, no. 7, pp. 3720–3732, Jul. 2014.

[31] Y. Lobsiger and J. W. Kolar, "Closed-loop di/dt and dv/dt IGBT gate driver," *IEEE Trans. Power Electron.,* vol. 30, no. 6, pp. 3402–3417, Jun. 2015.

[32] L. Michel, X. Boucher, A. Cheriti, P. Sicard, and F. Sirois, "FPGA implementation of an optimal IGBT gate driver based on posicast control," *IEEE Trans. Power Electron.,* vol. 28, no. 5, pp. 2569–2575, May 2013.

[33] L. Dang, H. Kuhn, and A. Mertens, "Digital adaptive driving strategies for high-voltage IGBTs," *IEEE Trans. Ind. Appl.,* vol. 49, no. 4, pp. 1628–1636, Jul./Aug. 2013.

[34] H. Riazmontazer, A. Rahnamaee, A. Mojab, S. Mehrnami, S. K. Mazumder, and M. Zefran, "Closed-loop control of switching transition of SiC MOSFETs," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2015, pp. 782–788.

[35] H. Riazmontazer and S. K. Mazumder, "Dynamic optical turn-off control of a high-voltage SiC MOSFET," in *Proc. 28th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2013, pp. 1274–1278.

[36] A. Meyer, S. K. Mazumder, and H. Riazmontazer, "Optical control of 1200-V and 20-A SiC MOSFET," in *Proc. 27th Annu. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 2530–2533.

[37] K. Ogata, *System Dynamics,* 4th ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2004.

[38] Z. Wang, J. Ouyang, J. Zhang, X. Wu, and K. Sheng, "Analysis on reverse recovery characteristic of SiC MOSFET intrinsic diode," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2014, pp. 2832–2837.