State-of-Charge Balancing With Parallel and Series Output Connected Battery Power Modules

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***Abstract*—This article presents a new state-of-charge (SOC) balancing method with parallel and series output connected battery power modules (BPMs) in an active battery management system (BMS.) To increase both the battery pack and system-level modularity, the BMS controls the average SOC of the entire battery pack by regulating the input currents of all BPMs to a common reference. A balancing loop introduces input current offsets to regulate all cells SOCs. The BMS functions are distributed between a central controller for battery pack SOC regulation, and a module controller that regulates the input current of the individual BPMs. Experimental results are presented on a 1.5 kWh 1C-rate prototype with five series output connected battery bricks. Each battery brick consists of three parallel output connected BPMs, which employ three battery cells and three 100 W dc/dc converters.**

***Index Terms*—Active balancing, battery management systems (BMSs), battery power modules (BPMs), state-of-charge (SOC) control.**

I. Introduction

LITHIUM-ION battery cells have a relatively low terminal voltage than typical high-voltage (HV) applications [1], [2]. A battery pack utilizes groups of parallel and series connected cells to increase the overall capacity and voltage. However, cell mismatches contribute to unequal state-of-health (SOH) degradation among the cells, where the role of a battery management system (BMS) and state-of-charge (SOC) balancing algorithms are critical [3]. Thus, the battery pack employs balancing circuits to control the cells' SOCs, which is feasible by modulating the individual cell currents.

Fig. 1(a) shows a battery pack with N series-connected cells that is interfaced to an HVdc bus through a dc/dc converter. The kth cell current is the superposition of two components, i.e., $i_k = i_{\text{bat}} + i_{bk}$. The common battery current i_{bat} flows into the dc/dc converter. However, i_{bk} is a unique current for each cell that flows into the balancing circuits to regulate the SOC of the cell SOC_k. The balancing circuits can be dissipative or nondissipative [4]–[7]. Dissipative balancing is relatively simple, inexpensive, and inefficient, where the highest SOC cell dissipates energy in a resistor [5]. Nondissipative balancing conserves the excess energy, which is more efficient and expensive [8]–[19].

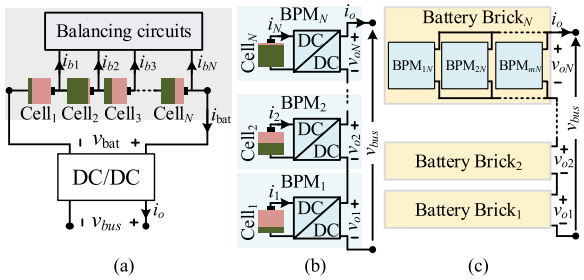

Fig. 1. Different architectures for a HV battery pack. (a) Typical approach with a central dc/dc converter. (b) Battery pack utilizing N series output connected BPMs. (c) Battery pack employing N series output connected battery bricks with m paralleled BPMs in each.

A battery power module (BPM) is a dc/dc converter that interfaces an individual battery cell to the dc bus, where the entire cell current flows through the converter, enabling individual cell-level control and nondissipative balancing [20]. Series output connected BPMs shown in Fig. 1(b) are an emerging solution to replace the HV dc/dc converters in large battery packs [21]–[34]. SOC balancing between the N series output connected BPMs has been presented in [28]–[32], where the BMS regulates the output voltages of the modules. A decentralized solution is presented in [33], where all BPMs regulate their output currents. However, the BPMs requires input and output current sensing circuits. Increasing the battery pack capacity is feasible by employing m parallel output connected BPMs that form a brick, where N series output connected bricks achieve the desired HV bus, as shown in Fig. 1(c) [34]. In [34], balancing between the m parallel and N series output connected BPMs is demonstrated. The BMS balances the N series output connected bricks by regulating their output voltages. Within a brick, the m paralleled BPMs utilize a common output voltage loop that generates a reference duty cycle d_{vN}; however, m distinct SOC balancing compensators scale the reference duty cycle d_{vN} to achieve balancing between the BPMs.

SOC balancing strategies based on output voltage regulation are simple for implementation. However, the battery system

Manuscript received October 25, 2021; accepted December 23, 2021. Date of publication January 19, 2022; date of current version February 18, 2022. This work was supported by the Office of Naval Research Award under Grant N00014-16-1-2986. Recommended for publication by Associate Editor S. Williamson. *(Corresponding author: Mohamed Kamel.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2022.3143835.

Digital Object Identifier 10.1109/TPEL.2022.3143835

appears as a voltage source, degrading the overall modularity and paralleling capabilities. On the other hand, wide variations in the HVdc bus simplify modularity, hot-swapping, and paralleling capabilities of the entire battery system [35]–[37]. Therefore, there is a need for new SOC balancing methods that suit the wide variations in the HVdc bus and differ from module output voltage regulation.

This article presents a simple solution for individual cell SOC control with m parallel and N series output connected BPMs. The balancing strategy relies on input current regulation in all BPMs. The average input current in all BPMs regulates the average SOC of the battery pack SOC_{avg}. However, differential input current references are introduced for SOC balancing, resulting in hierarchical SOC balancing between the series and parallel BPMs. The key contributions of this article can be summarized as follows.

1) The battery pack behaves as a variable current source. Therefore, modularity, paralleling capabilities, and PnP features of the entire battery system are improved, overcoming the limitations in [28]–[31], [34].
2) The SOC balancing method relies on the input current sensing circuit, which is utilized by the BMS balancing algorithms. Therefore, it eliminates the need for additional output current sensors, as presented in [33].

The rest of this article is organized as follows. Section II describes the system and proposes an SOC balancing technique based on individual cell current regulation. Section III explains the hierarchical SOC balancing mechanism. Section IV discusses system-level restrictions in the individual balancing loops. Section V presents the SOC balancing algorithm. Section VI validates the approach on a 1.5 kWh 1C-rate battery pack, with five series output connected bricks in each subsystem and three parallel output connected BPMs in each brick. Finally, Section VII concludes this article.

II. System Description and Control Architecture

Fig. 2 illustrates a battery pack consisting of N series output connected bricks with a BMS controller. Each battery brick consists of m parallel output connected BPMs, as shown in Fig. 2(b), where the total number of the BPMs in the battery pack is mN. Overall system control functions are distributed between the N bricks and the central controller, as shown in Fig. 2(b), and Fig. 2(a), respectively. SOC balancing between all BPMs is achieved by continuously tracking the average SOC of the battery pack SOC_{avg}, which is enabled by regulating the input current of all BPMs. However, the desired current references for the individual BPMs are unique for balancing. The central controller generates the balancing currents, as shown in Fig. 2(a).

A. Battery Pack Controller Roles

The pack controller (BMS) is responsible for system-level control, cell SOC estimation and balancing algorithms, as shown in Fig. 2(a). The BMS acquires all battery cell voltages, currents, and temperatures from the brick controllers through an isolated controller area network (CAN) communication bus at a 1 Hz rate. By definition, the N series output connected battery bricks share

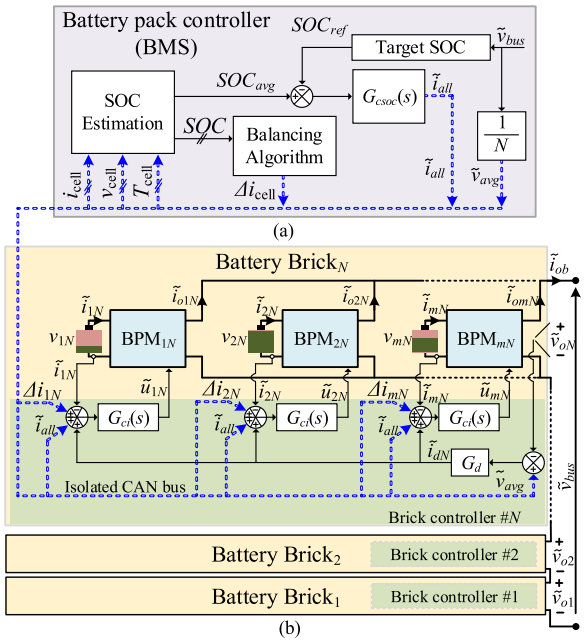

Fig. 2. System-level control diagram. (a) Battery pack controller, and (b) battery pack consisting of N series output connected bricks with m parallel output connected BPMs.

the same output current. Therefore, balancing between the N battery bricks is feasible as the battery charges or discharges into the HVdc bus. Thus, loads or sources in the dc bus dictate charging or discharging modes that govern SOC_{avg}. In this article, the battery pack features PnP capabilities, where the dc bus voltage dictates the state of the microgrid [37]. Consequently, the BMS monitors the bus voltage v_{bus} and utilizes a SOC compensator G_{soc} to track the desired (target) average SOC $\tilde{\text{SOC}}_{\text{ref}}$. The SOC compensator output is the common (average) input current reference $\tilde{i}_{\text{all}}$ in all BPMs to regulate the pack average SOC_{avg}, which is discussed in Section III

$$\tilde{i}_{\text{all}} = G_{\text{soc}}\left(\tilde{\text{SOC}}_{\text{avg}} - \tilde{\text{SOC}}_{\text{ref}}\right). \tag{1}$$

B. Brick Controller Roles

Each of the N bricks utilizes a single controller board that enables control and modulation of the m paralleled BPMs, as shown in Fig. 2(b). Each brick controller hosts m independent input current loop compensators G_{ci} to regulate the individual input port currents of the m BPMs. The N brick controllers receive two identical quantities from the BMS, (1) the common input current reference $\tilde{i}_{\text{all}}$, and (2) the averaged bus voltage $v_{\text{avg}} = v_{\text{bus}}/N$.

Practically, even at balanced SOCs, there are mismatches between the battery cell voltages. Therefore, with a common input current reference in all BPMs (1), the bricks' powers are different, where output voltage mismatches between the N battery bricks introduce a system-level instability [37]. Droop control is utilized to stabilize the overall system by sharing the output voltage between the bricks around v_{avg}. Consequently, the jth battery brick controller establishes a local input current reference $i_{\text{ref},j}$, which is obtained by adding a local droop current

i_{dj} to i_{all} for output voltage sharing

$$\tilde{i}_{\text{ref},j} = \tilde{i}_{all} + \tilde{i}_{dj} \tag{2}$$

$$\tilde{i}_{dj} = G_d\left(\tilde{v}_{\text{avg}} - \tilde{v}_{oj}\right) \tag{3}$$

where G_d is a droop conductance and $\tilde{v}_{oj}$ is the jth brick output voltage. At equilibrium, the output current is identical for the N battery bricks. At steady-state, all bricks' output voltages are equal to v_{avg}, where the droop currents are nullified

$$\sum_{j\in N} i_{dj}(t) = 0. \tag{4}$$

However, each BPM requires a unique differential input current reference ΔI_{ij} to control the individual SOC, which is the backbone for SOC balancing that is discussed in Section IV. Therefore, the input current reference of the ith BPM within the jth brick $\tilde{i}_{ij,\text{ref}}$ is

$$\tilde{i}_{\text{ref},ij} = \tilde{i}_{\text{ref},j} + \Delta I_{ij} \tag{5}$$

where $\tilde{i}_{\text{ref},j}$ is the common input current reference in the jth brick, and ΔI_{ij} is a differential input current for SOC control. The input current compensator G_{ci} of the ith BPM within the jth brick adjusts the control command $\tilde{u}_{ij}$ to track the desired battery cell current reference $\tilde{i}_{\text{ref},ij}$ (5). The settling time for SOC balancing is significantly longer than the settling times of the current regulation loops [37], [38]. Therefore, the remaining sections of this article focus on the steady-state conditions for SOC balancing, assuming stable and fast response with input current regulation loops.

III. Hierarchical SOC Balancing Mechanism

This section develops the mathematical foundation of the hierarchical SOC balancing strategy between the mN BPMs. Balancing between the mN BPMs is achieved in two following steps.

1) Within each brick, the m paralleled BPMs are balanced when the SOCs of the individual BPMs are equal to the average SOC of the brick, i.e., $\text{SOC}_{1j} = \text{SOC}_{2j}, \ldots, \text{SOC}_{mj}$.
2) SOC balancing among the N battery bricks is achieved when the average SOC in each brick is equal to the average SOC in the entire battery pack SOC_{avg}, i.e., $\text{SOC}_1 = \text{SOC}_2 \cdots \text{SOC}_N = \text{SOC}_{\text{avg}}$.

The SOC of the kth BPM can be expressed in terms of the input current, and cell capacity Q that is assumed equal in all BPMs

$$\text{SOC}_k(t) = \text{SOC}_{k,0} - \underbrace{\frac{1}{Q}\int_0^t i_k(t)dt}_{\delta\text{SOC}_k(t)} \tag{6}$$

where $\text{SOC}_{k,0}, i_k$, are the initial SOC and input current of the kth BPM. The change in SOC of the kth cell $\delta\text{SOC}_k(t)$ is controlled by regulating $i_k(t)$. Assuming (1) all BPMs are ideal, (2) the BPMs regulate their input currents with zero steady-state error, and (3) the follow the current reference (2), the change in the average SOC of the battery pack $\delta\text{SOC}_{\text{avg}}(t)$ is evaluated

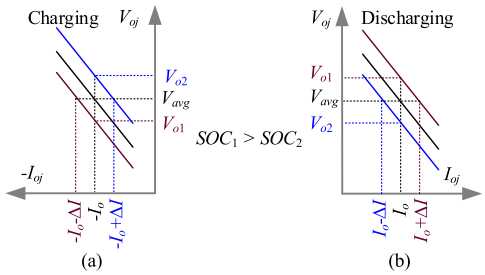

Fig. 3. Desired droop characteristics. (a) Charging behavior, and (b) discharging behavior.

$$\delta\text{SOC}_{\text{avg}}(t) = \frac{-1}{Nm}\sum_{j\in N}\sum_{i\in m}\delta\text{SOC}_{ij}(t) = \frac{-1}{Q}\int_0^t i_{\text{all}}(t)dt \tag{7}$$

where the droop currents are nullified according to (4). Similarly, the change in the average SOC of each brick $\delta\text{SOC}_j(t)$ can be deduced from (5) that depends on i_{all}, and the droop current that is critical for voltage sharing (3). However, equal voltage sharing between the N series connected bricks counters SOC balancing because all bricks inject or absorb equal powers. The average input current references in the N bricks must be different such that $\delta\text{SOC}_j(t)$ is unique. Therefore, δi_j is introduced as an average input current offset in the jth brick to achieve SOC balancing between the N series output connected bricks.

$$\delta\text{SOC}_j(t) = -\frac{1}{Q}\int_0^t \left(i_{\text{all}}(t) + i_{dj}(t) + \delta i_j(t)\right)dt. \tag{8}$$

Similarly, the change in the SOC of the ith BPM within the jth brick δSOC_{ij}, is controlled by introducing a current offset δi_{ij}. As a result, the change in the average SOC of a BPM is unique

$$\delta\text{SOC}_{ij}(t) = -\frac{1}{Q}\int_0^t \left(i_{\text{all}}(t) + i_{dj}(t) + \delta i_j(t) + \delta i_{ij}(t)\right)dt. \tag{9}$$

where δi_j is the average input current offset in the jth brick to achieve SOC balancing between the N series output connected bricks.

IV. Input Current Offset Restrictions

The previous section explains the roles of the common input current reference and the balancing currents. However, the choice of the balancing current offsets is not arbitrary. This section discusses restrictions in the input current offsets to achieve SOC balancing. Section II-B has discussed the droop loops, which ensure that the N bricks share the dc bus voltage equally at V_{avg}. Consider the steady-state droop characteristics $V_o - I_o$ of a two-brick system during charging and discharging modes, as shown in Fig. 3(a) and (b), respectively. At a given output current I_o, the characteristics of the two bricks overlap in the middle lines, where the voltage across each brick is equal to V_{avg}.

With the goal of balancing the average SOCs of the bricks, the balancing current offsets $\pm\Delta I$ must ensure that the highest SOC

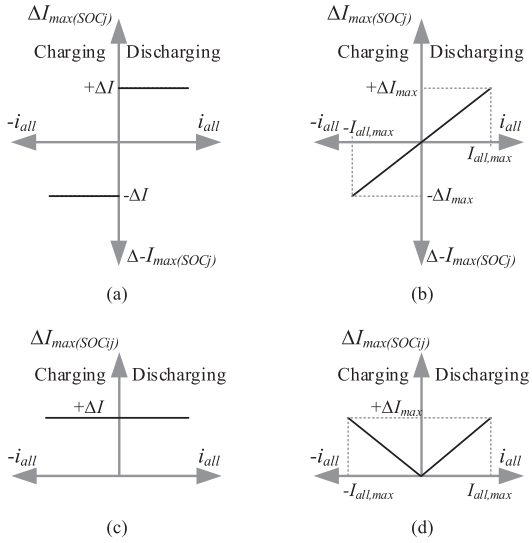

Fig. 4. Desired balancing current relationship versus i_{all}. (a) Polarity dependent characteristics for the series output connected bricks. (b) Linear relationship with the common input current reference i_{all} for the series output connected bricks. (c) Fixed positive current offset characteristics for the parallel output connected BPMs. (d) Linear relationship with the modulus of i_{all} for the parallel output connected BPMs.

brick $\max(\text{SOC}_j)$ carries the lowest voltage during charging and the highest voltage during discharging, as shown in Fig. 3(a) and (b), respectively. Therefore, during charging, the current offset in the highest SOC brick $\Delta I_{\max(\text{SOC}_j)}$ is negative, while the current offset in the lowest SOC brick is positive, as shown in Fig. 3(a). However, during discharging, the current offset in the highest SOC brick is positive, while the current offset in the lowest SOC brick is negative, as shown in Fig. 3(b). This behavior is achieved by incorporating the polarity of the common input current reference i_{all} in the desired input current offset for the highest SOC brick, as shown in Fig. 4(a). Furthermore, the rate of change of a brick SOC is proportional to the average input current in the brick, as expressed in (8). Thus, to decrease the balancing time, the input current offsets scale linearly with i_{all} instead of utilizing fixed balancing currents, as shown in Fig. 4(b).

On the other hand, the individual current offsets in the m paralleled BPMs within a brick change the individual output currents of the BPMs. In an ideal BPM, the input and output powers are equal

$$V_{\text{in}} I_{\text{in}} = I_o V_o \tag{10}$$

where V_o is the output voltage at a given output current I_o, I_{in} is the input current, and V_{in} is the battery cell voltage across the BPM. If the output voltage is held constant and neglecting the change in the battery cell voltage, the input current offset changes the BPM's output current ΔI_o

$$\Delta I_{\text{in}} = \frac{V_o}{V_{\text{in}}} \Delta I_o \tag{11}$$

where the change in the output port current and the input current offset has the same polarity, i.e., $\text{sgn}(\Delta I_o) = \text{sgn}(\Delta I_{\text{in}})$. The balancing current offsets in the m paralleled BPMs within a brick ensure that the output current from the highest SOC BPM is the largest in the entire brick during discharging. However, during charging, the absolute value of the output current from the highest SOC BPM is the smallest in the entire brick. Thus, for balancing the m paralleled BPMs within a brick, the input current offset of the highest SOC BPM $\Delta I_{\max(\text{SOC}_{ij})}$ is always positive, as shown in Fig. 4(c). Finally, to decrease the balancing time, the input current offsets scale linearly with $|i_{\text{all}}|$ instead of utilizing fixed balancing currents, as shown in Fig. 4(d).

V. Balancing Algorithm

The balancing algorithm calculates the individual current offsets to achieve SOC balancing between the mN BPMs. The balancing algorithm relies on the SOC estimations to achieve SOC balancing in three main steps.

Step #1: The algorithm determines the differences in SOCs between the average SOC of the N bricks relative to SOC_{avg} (12)

$$\delta\text{SOC}_j = \text{SOC}_j - \text{SOC}_{\text{avg}} \quad \forall j \in N. \tag{12}$$

Similarly, the algorithm calculates the difference between the SOCs of the m paralleled BPMs relative to their parent brick SOC (13)

$$\delta\text{SOC}_{ij} = \text{SOC}_{ij} - \text{SOC}_j \quad \forall j \in N, i \in m. \tag{13}$$

Step #2: The balancing algorithm minimizes the balancing time by penalizing the brick with the absolute maximum difference in SOC from SOC_{avg}, which is achieved by converting (12) to a per-unit quantity

$$\Delta pu_j = \frac{\text{SOC}_j - \text{SOC}_{\text{avg}}}{\max_{j \in N} \{|\delta\text{SOC}_j|\}} \quad \forall j \in N. \tag{14}$$

Similarly, in each of the N bricks, the balancing algorithm utilizes the BPM with the absolute maximum difference in SOC from the brick's average SOC, i.e., SOC_j to convert (13) to a per-unit quantity

$$\Delta pu_{ij} = \frac{\text{SOC}_{ij} - \text{SOC}_j}{\max_{i \in m} \{|\delta\text{SOC}_{ij}|\}} \quad \forall j \in N, i \in m. \tag{15}$$

Step #3: Considering the desired input current offsets' polarities that are discussed in Section IV, the balancing algorithm converts Δpu_j and Δpu_{ij} into balancing currents for the individual cells ΔI_{ij}

$$\begin{aligned} \Delta I_{ij} &= \alpha \cdot i_{all} \cdot \Delta pu_j + \alpha \cdot |i_{all}| \cdot \Delta pu_{ij} \\ &= \alpha \Big(\frac{i_{all} \cdot \delta\text{SOC}_j}{\max_{j \in N} \{|\delta\text{SOC}_j|\}} \\ &\quad + \frac{|i_{all}| \cdot \delta\text{SOC}_{ij}}{\max_{i \in m} \{|\delta\text{SOC}_{ij}|\}} \Big) \quad \forall j \in N, i \in m, \end{aligned} \tag{16}$$

where $\alpha < 1$ is a scalar that is limited by the ratings of the converters; Thus, the balancing currents are limited to $\Delta I_{\max}$ as the common current reference approaches $\pm I_{\max}$.

VI. Experimental Results

A 1.5-kWh 1C-rate battery pack prototype consisting of 15 parallel and series output connected BPMs has been developed. A single BPM employs a 100 W four-switch buck–boost dc/dc

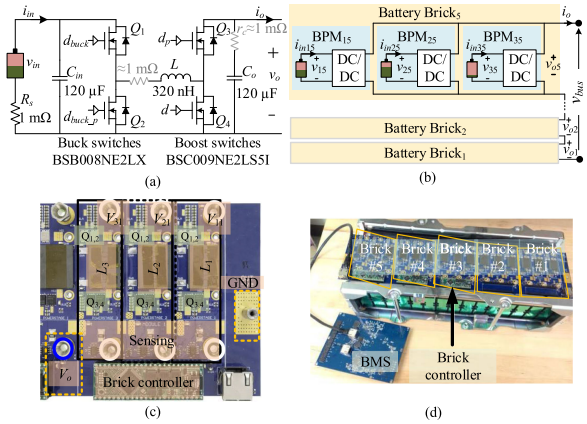

Fig. 5. Experimental prototype. (a) Four-switch buck–boost converter forming a BPM. (b) Three parallel output BPMs forming a brick. (c) Printed circuit board (PCB) of a brick. (d) Battery pack consisting of five series output connected bricks.

TABLE I
EXPERIMENTAL PROTOTYPE PARAMETERS

Parameter	Value
Battery pack prototype capacity	1.5 kWh
Power Rating of the prototype	1.5 kW
Number of BPMs mN	15
Number of battery bricks N	5
Number of BPMs in a brick m	3
Battery cell capacity	25±5% Ah
Maximum common current $I_{all,max}$	±25 A
Maximum balancing current ΔI_{max}	6 A
Minimum droop gain $G_{d,min}$ [37]	2 A/V
Maximum droop gain $G_{d,max}$ [37]	14 A/V

converter, as shown in Fig. 5(a). The individual BPMs are connected across 25 Ah battery cells. Moreover, each group of three BPMs forms a battery brick by paralleling the converter outputs. Therefore, the overall battery pack consists of five series output connected battery bricks, as illustrated in Fig. 5(b). Table I summarizes the prototype parameters.

Each battery brick utilizes a Piccolo TMS320F280049 microcontroller for modulation and control of the individual dc/dc converters, as shown in Fig. 5(c). The switching frequency of the individual BPMs is 200 kHz. During the battery pack startup, all BPMs regulate the cell currents and operate in buck mode to allow a soft-starting mechanism. However, the BPMs operate in boost mode during normal operation. Therefore, the brick controller implements three identical current PI compensators G_{ci} for differential input current regulation. Each of the three compensators takes the form

$$G_{ci} = K_p + \frac{K_i}{s}. \tag{17}$$

Details on small-signal analysis and controller design procedure are addressed in [38]. The input current loop compensator G_{ci} is designed to achieve a phase margin of 84° and a crossover frequency of 1 kHz, when the three BPMs supply a 300 W resistive load and operate with differential balancing currents at $M(D) = 2.5$. The PI current compensator gains are

$$K_i = 2, K_p = \frac{0.001}{\pi}. \tag{18}$$

Fig. 5(d) shows the battery pack prototype and a BMS board that utilizes a Piccolo TMS320F280049 microcontroller for system-level control. Moreover, the BMS implements a sigma-point Kalman filter (SPKF) for SOC estimation, which considers the measurement noise [39]. The microcontrollers in the BMS and brick controllers establish an isolated CAN communication bus. The BMS communicates with the bricks and acquires the sampled currents, voltages, and temperatures from all BPMs to run the SOC estimation algorithm at 1 Hz rate. Charging and discharging the battery pack is determined by sources and loads at the output terminal. The battery pack features PnP capabilities and allow for hot-swapping, where the BMS determines the target SOC, i.e., SOC_{ref} according to the bus voltage [37]

$$\text{SOC}_{\text{ref}}[\%] = \begin{cases} 0, & v_{\text{bus}} \le 24 \\ 50\,(v_{\text{bus}} - 24), & 24 < v_{\text{bus}} \le 26 \\ 50\,(v_{\text{bus}} - 26), & 26 < v_{\text{bus}} \le 28 \\ 100, & 28 < v_{\text{bus}} \le 32. \end{cases} \tag{19}$$

Moreover, the BMS computes the average SOC of the battery pack SOC_{avg}, and hosts the average SOC compensator G_{csoc} to track SOC_{ref} (19). The average SOC compensator G_{csoc} takes the form

$$G_{\text{csoc}} = \frac{\left(K_{\text{Psoc}} + \frac{K_{\text{Isoc}}}{s}\right)}{\left(1 + \frac{s}{2\pi f_{p1}}\right)\left(1 + \frac{s}{2\pi f_{p2}}\right)} \tag{20}$$

resulting in a phase margin of 100° and a crossover frequency of 45 Hz, when the three BPMs supply a 300 W resistive load and operate at $M(D) = 2.5$. The gains of the compensator are

$$K_{\text{Isoc}} = 200, K_{\text{Psoc}} = \frac{10}{\pi}, f_{p1} = 1000, f_{p2} = 2000. \tag{21}$$

The SOC compensator output is the common input current reference i_{all}, which is transmitted to the 15 BPMs over the isolated CAN bus at 2 kHz along with the averaged bus voltage v_{avg}. Finally, the BMS runs the balancing algorithm and transmits the computed current offsets at 1 Hz rate.

Fig. 6(a) shows the experimental setup, where a bidirectional supply is connected across the battery pack. The bidirectional supply operates in positive and negative constant current mode with a voltage limit to emulate sources and loads to allow charging and discharging of the battery pack. In this section, a positive battery pack output current is associated with discharging, and a negative battery pack output current is associated with charging.

A. Balancing Between the Series Output Connected Bricks

Fig. 6(b) depicts the probed voltages and currents in the experiment. The scope captures are depicted in a single figure by using TekScope software. Fig. 7 shows the scope traces for the output voltages across the five series output connected bricks, the dc bus voltage v_{bus}, and the output current i_o. Moreover, Fig. 8 summarizes the individual brick results as acquired through the CAN bus at 1 sec rate. Initially, the individual brick SOCs are 55.1%, 54.2%, 54.6%, 51.6%, and 59.6%, as shown in Fig. 8(a). At the beginning of the test, brick #5 has the highest SOC, and brick #4 has the lowest SOC, where the difference in SOC between the two bricks is 8%.

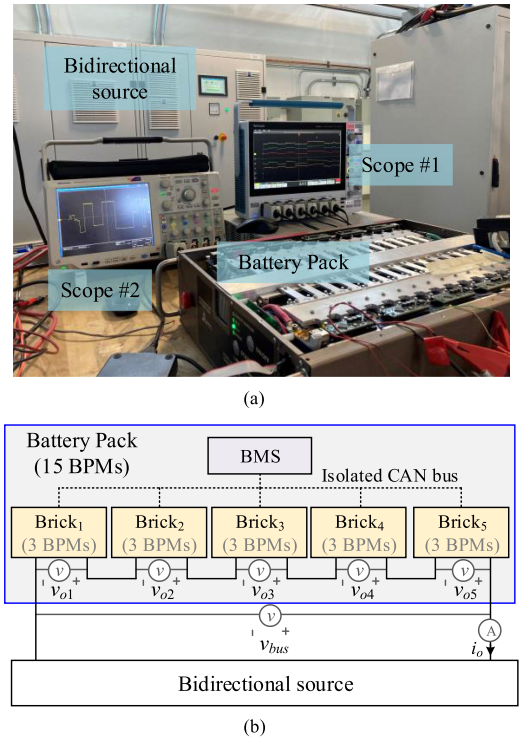

Fig. 6. Validation setup. (a) Experimental setup with the battery pack and bidirectional load, and (b) schematic diagram of the setup and the probed signals.

At 30 s, the battery pack output is enabled by discharging into a 10 A constant current load, where the dc bus voltage is 25 V that is distributed equally across the five series output connected bricks, as shown in Fig. 7. At 60 s, the SOC balancing algorithm introduces individual brick average input current offsets to achieve SOC balancing between all BPMs. Therefore, the average input current in each brick is different, as shown in Fig. 8(b). Thus, the output voltages across the five bricks are different and inject different powers while maintaining the same dc bus voltage, as shown in Fig. 7. Therefore, the rates of change in the SOCs between the bricks are different, as shown in Fig. 8(a). The SOC in the 5th brick SOC_5 is the highest in the entire battery pack, as shown in Fig. 8(a); thus, the output voltage v_{o5} is the highest among the five bricks to inject the greatest power into the dc bus, on the other hand, the output voltage v_{o4} is the lowest among the five bricks to inject the lowest power into the dc bus, as shown in Fig. 7. At 90 s, the bidirectional supply is set to 15 A load, where the average input current reference in all bricks and the input current offsets increase, as shown in Fig. 8(b).

However, at 231 s, the bidirectional supply is set to 5 A with 30 V as a voltage limit in source mode. At 423 s, the bidirectional current is increased to 50 A in source mode. As a result, all BPMs charge from the dc bus, which is held at approximately 27.25 V between 231 s$\rightarrow$423 s interval. Moreover, the input current references and the current offsets are negative to charge the battery cells, as shown in Fig. 8(b). In contrast to the discharging case, the output voltage v_{o5} is the lowest among the five bricks to absorb the lowest power from the dc bus, whereas the output voltage v_{o4} is the highest among the five bricks to absorb the highest power from the dc bus, as shown in Fig. 7. At 638 s, the absolute maximum difference in SOC between the lowest and highest SOC bricks is 5.4%.

Between 638 s$\rightarrow$1025 s and 1445 s$\rightarrow$2005 s, the bidirectional source is set to 55 A load, where the battery pack discharges into the dc bus; however, between 1025 s$\rightarrow$1445 s the bidirectional source is set to 30 A in source mode with a 30 V as a maximum voltage limit, as shown in Fig. 7. The balancing current offsets between 638 s$\rightarrow$1025 s and 1445 s$\rightarrow$2005 s are larger than the current offsets between 1025 s$\rightarrow$1445 s because the average input current in the bricks is higher in the discharging intervals, as shown in Fig. 8(b). Moreover, the output voltage v_{o5} is the highest among the five bricks to during the discharging intervals, whereas the output voltage v_{o4} is the highest among the five bricks to during the charging intervals, as shown in Fig. 7. Consequently, at 2005 s, the absolute maximum difference in SOC between the lowest and highest SOC bricks is approximately 0.4%.

Between 2005 s$\rightarrow$2693 s, the bidirectional source is set to 50 A in source mode with a 30 V as a maximum voltage limit, which charges the battery pack. Despite the mismatches between the cells capacities, the SPKF algorithm continuously updates the individual cell SOCs; at approximately 2100 s, the estimated SOCs in the bricks are updated, where the input current offsets slightly change the average input currents in the bricks, as shown in Fig. 8(b). However, the absolute maximum difference in SOC between the lowest and highest SOC bricks remains within 0.4%. However, the bidirectional source settings are continuously changed to allow charging and discharging the battery pack; thus, SOC balancing among the individual BPMs is achieved. For example, between 2693 s$\rightarrow$2970 s and 3045 s$\rightarrow$3156 s, the bidirectional source is set to 55 A load with 24 V as a minimum dc bus voltage. At 3141 s, regulation is disabled, where the battery pack output current is zero, and the dc bus is held constant at 24 V by the bidirectional source, where the average SOCs in the bricks are balanced within 0.2%. In conclusion, the analysis presented in the previous sections is validated by balancing the series-output connected bricks experimentally.

B. Cell-Level SOC Balancing

Fig. 9 shows experimental results for the three BPMs within brick #1 as acquired through the CAN bus at 1 s rate. The initial SOCs for cells #11, #21, and #31 are 52.8%, 51.8%, and 60.8%, respectively. Thus, the absolute difference in SOCs within the brick is 9.1%, and the average SOC in brick #1, i.e., SOC_1 is approximately 55.1%, as shown in Fig. 9(a). The average SOC in the brick SOC_1 is lower than the average SOC in cell #31, SOC_{31}; however, the average SOC in the brick SOC_1 is higher than the estimated SOC in cell #11, SOC_{11}, and cell #21 SOC_{21}, respectively. Therefore, the balancing algorithm introduces the current offsets to the individual cells such that the input current in cell #31, i_{31} is higher than the average current in the brick i_1 during discharging, as shown in Fig. 9(b). However, the balancing algorithm ensures that the absolute value of the current i_{31} is higher than the absolute value of the average current in the brick i_1 during charging, as shown in Fig. 9(b).

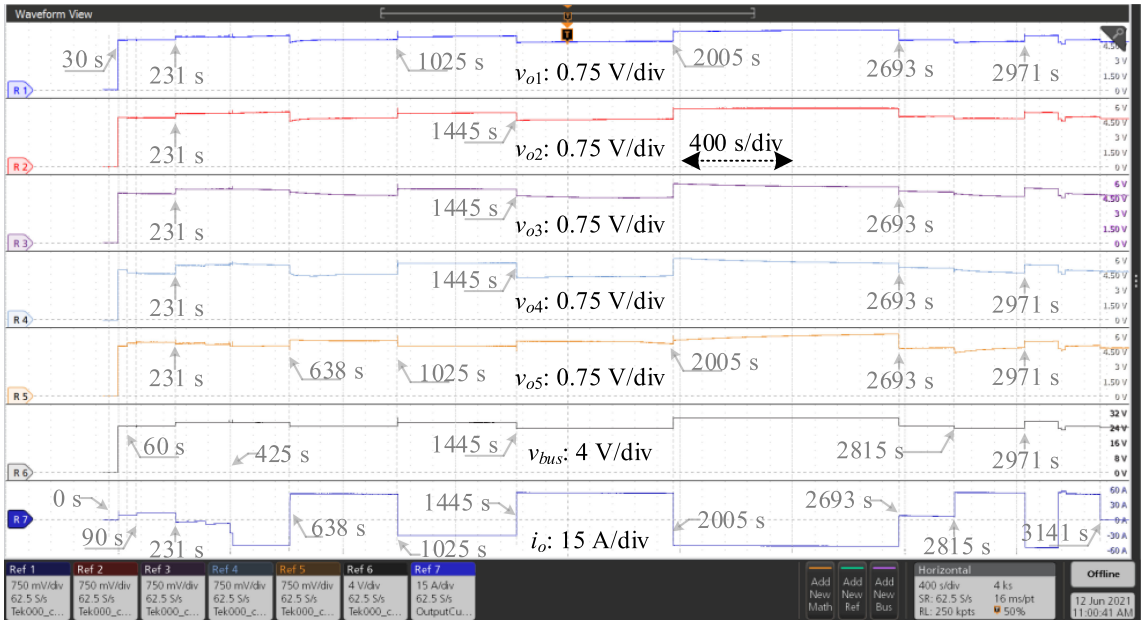

Fig. 7. Experimental results for the probed signals. R(1)→R(5) the output voltage across the five series output connected bricks $v_{o1} \rightarrow v_{o5}$, R(6) the dc bus voltage v_{bus}, and R(7) the battery pack output current i_o.

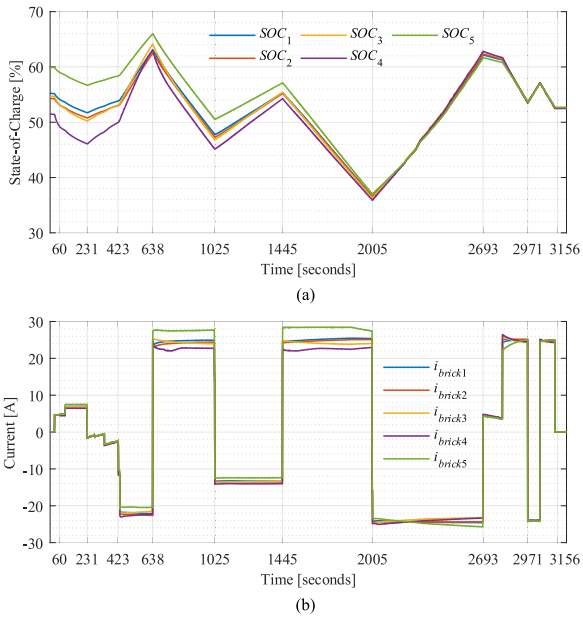

Fig. 8. Experimental results in the bricks. (a) Estimated SOCs and (b) average input currents.

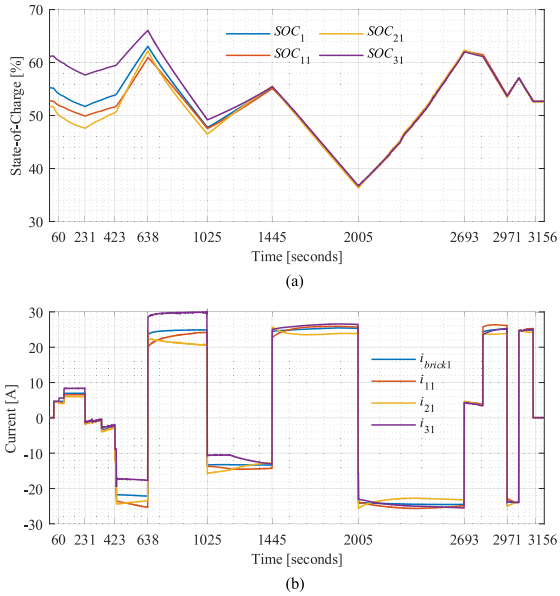

Fig. 9. Experimental results in brick #1. (a) Estimated SOCs and (b) individual BPM currents.

Similarly, the input current in cell #11 i_{11}, and the input current in cell #21 i_{21} are lower than i_1 during discharging to inject lower power into the output terminal of the brick. However, i_{11} and i_{21} are higher than i_1 during charging to absorb more power from the output terminals of the brick. The balancing algorithm introduces the current offsets to the cells until balancing is achieved; thus, at 2005 s the absolute difference in SOCs within the brick is 0.3%. Moreover, the SPKF algorithm continues to update the SOC estimates for all BPMs in the system. Therefore, at 3015 s the absolute difference in SOCs within the brick is 0%, where the input currents in all BPMs within Brick #1 are equal, as shown in Fig. 9(b). Fig. 10 summarizes the experimental results for the 15 BPMs and all battery cells, which are acquired through the CAN bus at 1 s rate. At the beginning of the test, the absolute maximum difference in SOC between all battery cells is approximately 10%, as shown in Fig. 10(a). Regulation is enabled at $t = 2$ min, where all battery cells tracked the common current reference i_{all}, as shown in Fig. 10(b). However, balancing is enabled at $t = 3$ min, where individual current offsets are transmitted to all BPMs, as shown in Fig. 10(b). Therefore, the absolute maximum

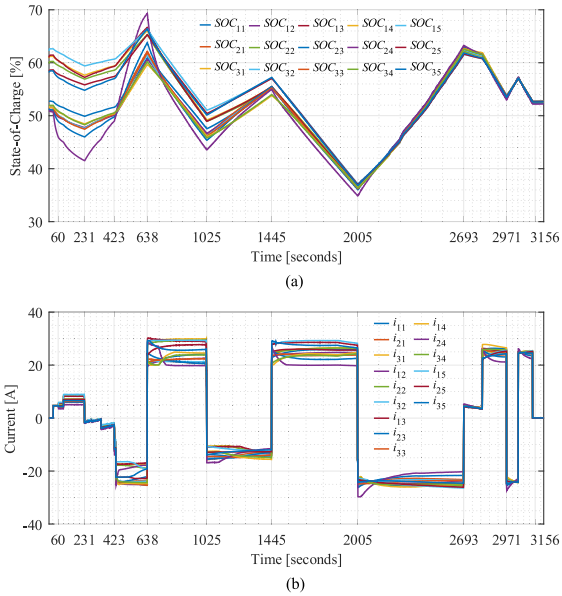

Fig. 10. Experimental results in the battery pack with 15 BPMs/cells. (a) Estimated SOCs and (b) input currents.

difference in SOCs between all battery cells is controlled. After $t = 12$ min in the test, the absolute maximum difference in SOCs between all battery cells is approximately 8.3%, as shown in Fig. 10(a). The common current reference is significantly low between $t = 14 \rightarrow 24$ min, as shown in Fig. 10(b). As a result, the absolute maximum difference in SOCs between all battery cells remains approximately 7.3% after $t = 24$ min. However, between $t = 24 \rightarrow 38$ min, the current in all cells is relatively higher. As a result, at $t = 38$ min the absolute maximum difference in SOCs between all battery cells is approximately 2%, as shown in Fig. 10(a). The SPKF algorithm continuously updates the individual cell SOCs for the balancing algorithm. Thus, the balancing algorithm updates the individual cell current offsets to achieve SOC balancing between all cells. At the end of the test, the absolute maximum difference in SOCs between all battery cells is approximately 0.9%, as shown in Fig. 10(a).

VII. Conclusion

This article focuses on SOC balancing with parallel and series output connected BPMs in active BMSs. In contrast to the existing SOC balancing schemes that rely on output voltage regulation, this article employs current regulation instead to enhance modularity and paralleling capabilities in large battery packs. Moreover, the proposed method relies on the cell current sensors for balancing, eliminating the need for additional output current sensing circuitry. The BMS regulates all cell currents to a common current reference for average SOC regulation. The BMS balances the individual battery cells by introducing unique current offsets to all BPMs for SOC balancing. The balancing current offsets depend on the common current reference, and the BPMs ratings. The approach is validated experimentally using a 1.5 kWh 1C-rate active BMS consisting of 15 parallel and series output connected BPMs for a 24 V system. Experimental results prove successful SOC balancing between the 15 battery cells.

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