Single-Phase Rectifier With Reduced Common-Mode Current, Auto-PFC, and Power Decoupling Ability

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***Abstract*—Transformer and electrolytic capacitors (Ecaps) in light-emitting diode (LED) drivers lead to increased cost and shortened lifespan. Therefore, eliminating the transformer and Ecaps of the LED driver can not only achieve a lightweight design but also extend the service life. In this article, a novel single-phase transformerless capacitorless power factor correction rectifier is proposed. The proposed topology shares a common ground with the grid and the load. Thus, the reduced common-mode current is obtained, and the demand for an isolation transformer is eliminated. In addition, this article presents a unidirectional active buffer circuit to isolate the pulsating power, and the capacitor of the buffer circuit is multiplexed as an output filter. Compared with similar works, a lower voltage on the decoupling capacitor, fewer power components, and a simple control unit are obtained. Then, the operation principle and switching modes as well as the parameter design and implementation of the control strategy are elaborated systematically. Finally, an 80-W experimental prototype is built, and the experimental results confirm the feasibility of the proposed rectifier by reaching the efficiency up to 97.1% and the power factor to 0.984 at a wide range of operating voltage.**

***Index Terms*—Common-mode current (CMC), electrolytic capacitorless, power decoupling, single-phase ac–dc converter.**

I. Introduction

SINGLE-PHASE power factor correction (PFC) rectifiers have attracted wide attention in recent years due to their advantages of high power density, high conversion efficiency, high reliability, and so on [1], [2]. The functions of H^3 are expected to provide significant economic benefits because it is suitable for many emerging applications, especially light-emitting diode (LED) lighting. According to statistics, lighting losses account for about 25% of the total global losses [3]. Unfortunately, most of the single-phase LED rectifiers still require bulky electromagnetic interference (EMI) circuits and electrolytic capacitors (Ecaps) for ensuring normal operation. Generally speaking, the size of bulky Ecaps makes it hard to achieve high power density [4]. What is worse, the lifetime of the rectifiers is far less than that of LEDs. Moreover, one-third of circuit faults are caused by Ecaps [5].

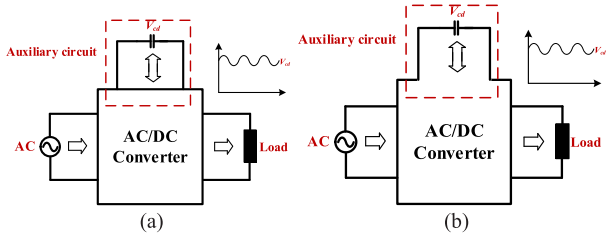

Fig. 1. Power conversion architecture with active pulsating power buffering. (a) Parallel decoupling. (b) Series decoupling.

Recently, many scholars have focused on improving the rectifier topology to achieve non-Ecaps by adding one active circuit in parallel or series with a dc link to buffer the pulsating power, as shown in Fig. 1. The method of the dc side in parallel is shown in [6]–[10]. Some topologies of power buffering converters, such as buck–boost type, boost-type, buck-type, and single-ended-primary-inductor-type converters, have been introduced separately to store the pulsating power to remove the Ecaps in the dc link. However, in [7] and [8], the active buffer circuit capacitor voltage is higher than the peak value of the input voltage, which is not reliable for the overall system. In addition, MOSFETs are often replaced by insulated-gate bipolar transistors. Considering this, the power decoupling method using a series-connected active buffer is proposed.

Flyback circuits based on a three-port network are shown in [11] and [12], where the third port is utilized to deal with ripple power and recovery leakage energy. The efficiency has been significantly improved, and the voltage stress of circuit elements is small in the active buffer unit. Nevertheless, the cost must be taken into consideration when it comes to industrial manufacture. However, the buffer circuit and the main circuit of the topologies above are relatively independent, leading to high redundancy of components and increase in manufacturing costs.

The dual flyback circuits are presented in [13] and [14]. The difference is to share the main switch with single-stage rectifiers. The cost and the power density will be further improved. However, all the switches in the rectifiers are in a high-frequency (HF) state. The low cost is at the expense of transmission efficiency.

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Instead of such combinations, the traditional H-bridge converter and the active buffer circuit are cascaded in [15]–[17] and can realize only four-switch operation by sharing one bridge arm. There are only two switches in the HF state. However, the bidirectional transfer in the active decoupling circuit makes it difficult to optimize the efficiency of such a converter. Therefore, unidirectional active buffer circuits are studied in [18]–[20]. Most of the energy is transferred directly to the load through energy-flow-path optimization in those rectifiers, while the single-stage active buffer circuit only handles the pulsating power. Then, the energy processing link is further reduced in the active buffer circuits. However, it is well known that the miniaturization of the LED drivers is an inevitable trend, but the transformer in the above solutions should be regarded as a redundant device and needs to be eliminated.

Another challenge is that most of the commercial rectifiers employ either line-frequency (LF) or HF isolation transformers. LF transformers are large and heavy, making the whole system bulky and reducing the power density. Most topologies with HF transformers usually contain several power stages, which increases the system complexity and reduces the efficiency [21], [22]. Unfortunately, common-mode (CM) leakage current between the grid and LED arrays causes high EMI and total harmonic distortion (THD) without a transformer. In this regard, H5-type inverters, HERIC inverters, H6-type inverters, and Karschny inverters are presented in [23]–[26] and are excellent candidates to achieve transformerless operation by the topology structure of neutral point clamped type or common-ground type. The above solutions connect the neutral point of the grid directly to the midpoint of the voltage-divided capacitors on the dc side. As a result, the overall CM voltage is kept constant at each instant, and the common-mode current (CMC) is suppressed. However, the above schemes are not suitable for dc–ac applications and not suitable for LED loads. Moreover, the CMC is effectively attenuated but still present. To meet the needs of ac–dc applications, a single-phase converter consisting of two legs with four switches, called the θ-converter, is proposed in [16]. In addition, it has a common ac and dc ground, which eliminates CMCs and removes the need for an isolation transformer. Unfortunately, the problem of overcurrent in the circuit leads to limited application, and the power decoupling is also not considered. Therefore, it is urgent to propose a miniaturized, high-efficiency, long-life, and nonisolated LED driver.

A novel single-phase PFC rectifier with reduced CMC and power decoupling ability has been proposed in this article. Compared with the existing topologies, the main merits are that there is no leakage current, and the problem of pulsating power is absence after eliminating the Ecaps. The output voltage of the proposed rectifier is common ground with the input voltage, and the leakage current could be eliminated. In addition, a unidirectional energy buffer unit is created by inserting an extra switched network into a buck–boost converter, and the pulsating power is absorbed. It is worth noting that the main switch and the decoupling capacitor are time-sharing multiplex though the common-ground structure and the buffer unit are integrated into the buck–boost converter, so fewer additional components are required. What is more, the prototype analysis will confirm that such a topology could eliminate overcurrent.

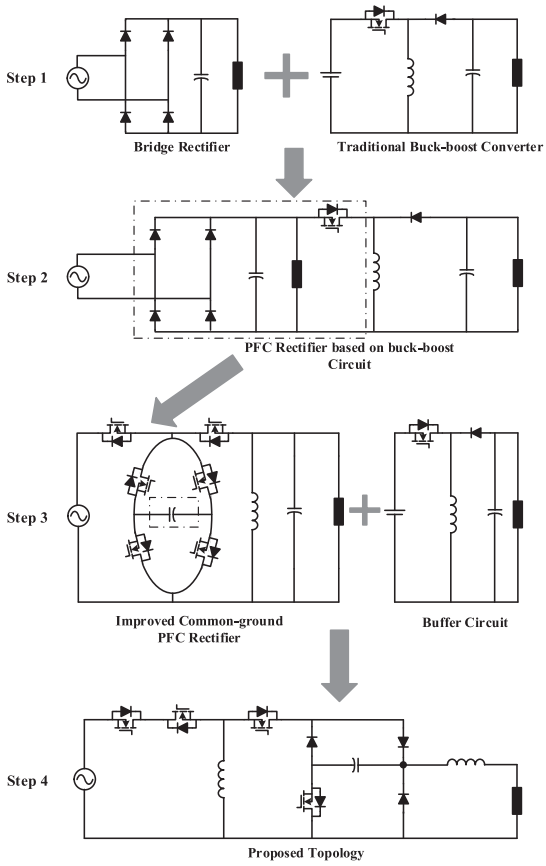


Fig. 2. Topological deduction.

The rest of this article is organized as follows. In Section II, the structure of the new transformerless buck–boost rectifier is presented in detail. The basic operating principles in a discontinuous conduction mode (DCM) and the corresponding characteristic analyses are provided in Section III. The design of the parameters is presented in Section IV. The experimental prototype, the simulation and experimental results, and the test results are shown in Section V. Finally, Section VI concludes this article.

II. Proposed Topology

The proposed converter is obtained from the derivation of four steps, as shown in Fig. 2. First, the converter needs to perform the basic PFC and rectification functions. Second, the PFC rectifier is obtained by integrating the two parts. Third, the improved common-ground structure and the buffer circuit are introduced. Fourth, the two parts are integrated by devices sharing and multiplexing. Finally, the proposed rectifier is obtained. It is worth noting that the circuit components within the boxes in Fig. 2 are the parts that will be modified.

As shown in Fig. 3, the proposed energy buffering LED driver consists of two parts: PFC rectifier and unidirectional energy buffer circuit. Compared with the H5 inverter, the Karschny

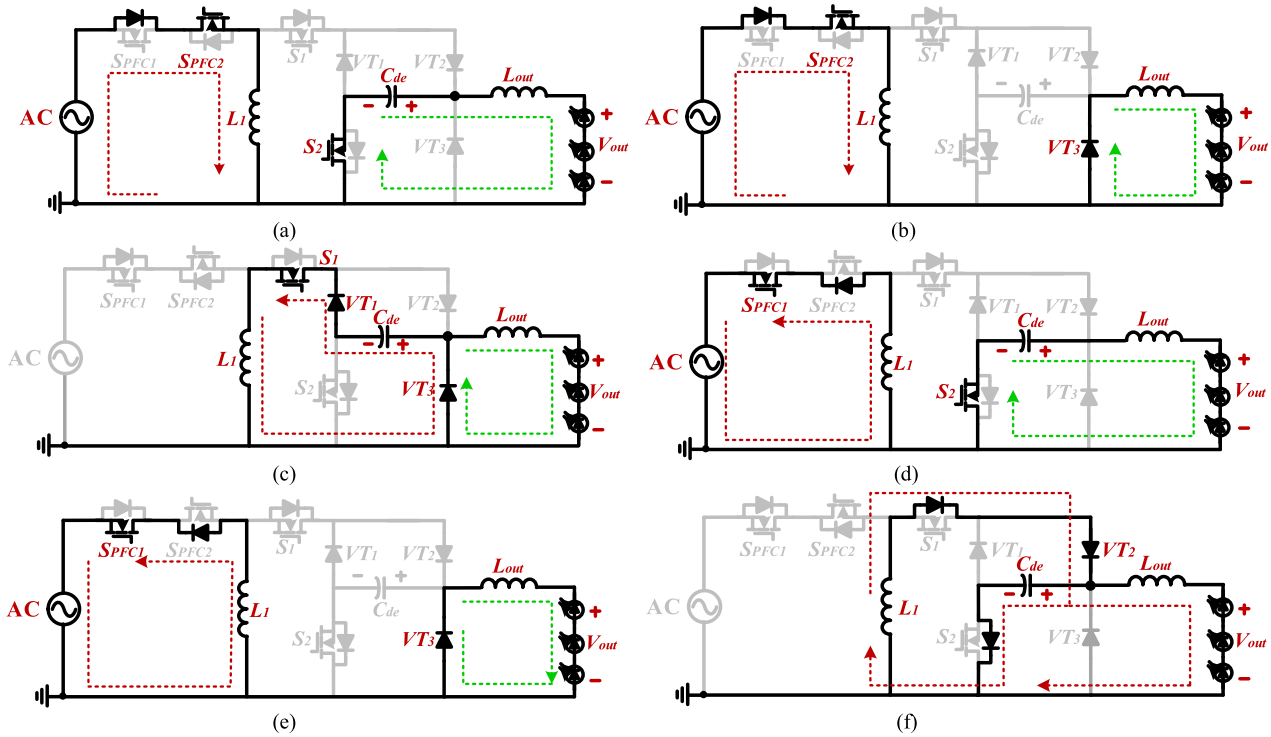


Fig. 3. Proposed energy buffering driver.

inverter, and the full-bridge inverter with dc bypass and one inverter with two paralleled buck converters to achieve the purpose of the electrolytic capacitorless system, only four switches are utilized to construct a converter. The dimming and PFC function is achieved by the PFC rectifier, which consists of the switches $S_{\mathrm{PFC1/2}}$, the inductor L_1, and the mode switch S_1. The electrolytic capacitorless system is obtained by the energy buffering tank, which includes three diodes $VT_{1\text{-}3}$, the decoupling capacitor C_{de}, and the switches $S_{1/2}$, where L_1 and S_1 are multiplexed by two units and S_1 is used to switch whether the circuit works in the decoupling mode or the rectifier mode. Moreover, the voltage ratings of VT_3 and S_2 are always clamped by the voltage of decoupling capacitor V_C, which can be designed at a low voltage level.

It is worth highlighting that two units are controlled independently, which means that the topology could flexibly select the different objectives. In the rectification mode, the switches $S_{\mathrm{PFC1/2}}$ are employed to regulate the input current i_s and the out current I_{out}, and the switch S_2 is responsible for controlling the output peak current $I_{\mathrm{out\text{-}p}}$ and diverting the ripple energy away from the load.

III. Operational Principle and Characteristic Analysis

A. Operating States

As shown in Fig. 4, one switching period is divided into two three-mode according to the polarity of the input voltage v_s. Fig. 4 shows theoretical voltage and current waveforms. The switching sequences and the devices' conditions for $v_s > 0$ and $v_s < 0$ are presented in Table I.

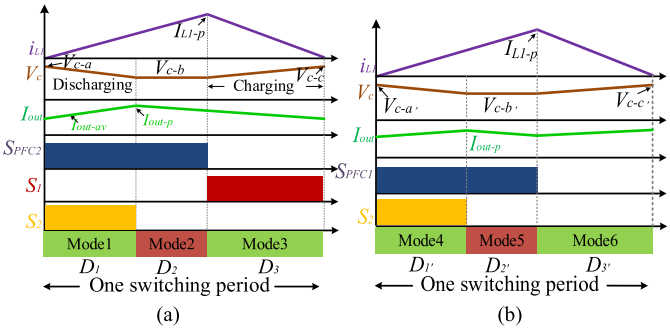


Fig. 4. Equivalent circuit of one switching period. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

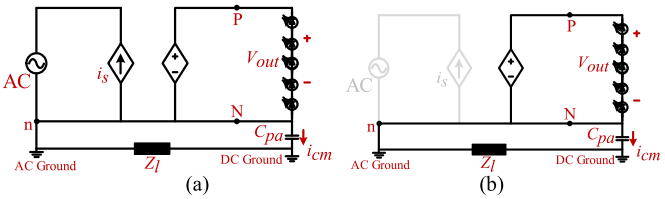


Fig. 5. Key switching waveforms of the proposed LED driver. (a) For $v_s > 0$. (b) For $v_s < 0$.

The switch S_{PFC2} remains intermittent conduction state during a positive period. In Mode 1, the switch S_{PFC2} is ON, as shown in Fig. 4(a). The current through L_1, i_{L1}, increases linearly. Moreover, the energy is transferred from the input source v_s to L_1. The decoupling capacitor C_{de} is connected to the series combination of the output inductor L_{out} and the load. The linear growth of the output current I_{out} is slow due to the existence

TABLE I
SUMMARY OF SWITCHING PATTERNS

Operating Mode	S_{PFC1}	S_{PFC2}	S_1	S_2	C_{de}	L_1
Mode 1	0	1	0	1	Discharge	Charge
Mode 2	0	1	0	0	Idle	Charge
Mode 3	0	0	1	0	Charge	Discharge
Mode 4	1	0	0	1	Discharge	Charge
Mode 5	1	0	0	0	Idle	Charge
Mode 6	0	0	0	0	Charge	Discharge

of large filter inductance. The phase ends when the upper peak value required for the output current $I_{\text{out-p}}$ is reached. During Mode 2, the current of the inductor L_{out} is freewheeling through VT_3, and the current keeps on increasing, as shown in Fig. 4(b). This phase ends while the switch S_{PFC2} is turned OFF. During Mode 3, the energy stored in the inductor L_1 is transferred to the decoupling capacitor C_{de}. When the energy of L_1 is completely released to C_{de}, this stage ends, as shown in Fig. 4(c).

The switches S_{PFC2} and S_1 remain OFF during the negative period. Modes 4–6 have similar functions to Modes 1–3, respectively. However, the polarity of the PFC inductor is different. What is more, in Mode 6, the energy stored in the inductor L_1 is transferred to the capacitor C_{de} and the output inductor L_{out}.

B. Steady-State Analysis

The duration of Modes 1–3 are D_1T_s, D_2T_s, and D_3T_s, respectively, shown in Fig. 5(a). And the durations of Modes 4–6 are $D_{1'}T_s$, $D_{2'}T_s$, and $D_{3'}T_s$, respectively, shown in Fig. 5(b). Thus, D_1-D_3 and $D_{1'}-D_{3'}$ must meet

$$D_1 + D_2 + D_3 = 1 \tag{1}$$

$$D_{1'} + D_{2'} + D_{3'} = 1. \tag{2}$$

According to Table I, the duty ratios of the switches S_{PFC1} and S_{PFC2} are shown as

$$D_{\text{PFC1}} = D_{\text{PFC2}} = D_1 + D_2 = D_{1'} + D_{2'}. \tag{3}$$

Since, the inductor current reaches the peak value $I_{L1\text{-}p}$ as given in

$$I_{L1-p}(t) = \frac{V_s \sin(\omega t)}{L_1} D_{\text{PFC}} T_s \tag{4}$$

where ω is the grid angular frequency.

The energy released by the decoupling capacitor E_{de} has two parts: L_{out} and the LED. Then, the total energy from C_{de} under $v_s > 0$ and $v_s < 0$ can be expressed as

$$\begin{cases} E_{\text{de}} = \frac{1}{2} C_{\text{de}} V_{C-a}^2 - \frac{1}{2} C_{\text{de}} V_{C-b}^2 \\ E_{\text{de}'} = \frac{1}{2} C_{\text{de}} V_{C-a'}^2 - \frac{1}{2} C_{\text{de}} V_{C-b'}^2 \end{cases} \tag{5}$$

$$\begin{cases} E_{\text{out}} = \frac{L_{\text{out}}\left(I_{\text{out-p}}^2 - I_{\text{out-av}}^2\right)}{2} + I_{\text{out-av}} V_{\text{out}} D_1 T_s \\ E_{\text{out}'} = \frac{L_{\text{out}}\left(I_{\text{out-p}}^2 - I_{\text{out-av}}^2\right)}{2} + I_{\text{out-av}} V_{\text{out}} D_{1'} T_s \end{cases} \tag{6}$$

where $I_{\text{out-av}}$ and $I_{\text{out-p}}$ are the average and peak values of the output current, respectively.

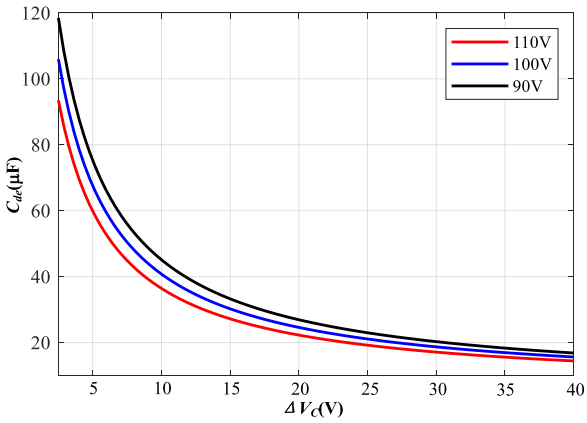


Fig. 6. Equivalent circuit for analyzing the leakage current. (a) Under Modes 1, 2, 4, and 5. (b) Under Modes 3 and 6.

Substituting (5) into (6), the duty cycles D_1 and $D_{1'}$ can be obtained

$$\begin{cases} D_1 T_s = \frac{\left[C_{\text{de}}\left(V_{C-a}^2 - V_{C-b}^2\right) - L_{\text{out}}\left(I_{\text{out-p}}^2 - I_{\text{out-av}}^2\right)\right]}{2 I_{\text{out-av}} V_{\text{out}}} \\ D_{1'} T_s = \frac{\left[C_{\text{de}}\left(V_{C-a'}^2 - V_{C-b'}^2\right) - L_{\text{out}}\left(I_{\text{out-p}}^2 - I_{\text{out-av}}^2\right)\right]}{2 I_{\text{out-av}} V_{\text{out}}}. \end{cases} \tag{7}$$

Based on Faraday's law, the peak current is also expressed as

$$\begin{cases} I_{L1-p} = \left| \frac{\frac{V_{C-b} + V_{C-c}}{2}}{L_1} \right| D_3 T_s \\ I_{L1-p} = \left| \frac{\frac{V_{C-b'} + V_{C-c'}}{2}}{L_1} \right| D_{3'} T_s \end{cases} \tag{8}$$

where $V_{C\text{-}a}/V_{C\text{-}a'}$ and $V_{C\text{-}c}/V_{C\text{-}c'}$ are the peak and valley values in the charging and discharging stages of the capacitor, respectively.

Then, the duty cycles D_3 and $D_{3'}$ can be obtained according to (8).

It should be noticed that the pulsating power P_{de} is buffered in Mode 3/6 before it flows through the load from the steady-state analysis. The relationship between P_{in} and P_{de} can be determined by the following formula:

$$P_{\text{in}} = v_s \; i_s = V_{\text{out}} \; I_{\text{out}} \sin^2(\omega t) \tag{9}$$

$$P_{\text{in}} = \frac{V_{\text{out}} I_{\text{out}}}{2} + \frac{V_{\text{out}} I_{\text{out}} \cos(2\omega t)}{2} = P_{\text{out}} + P_{\text{de}}. \tag{10}$$

C. CM Voltage

According to the circuit analysis in Fig. 4, the equivalent circuit of the proposed topology for CMC analysis is presented in Fig. 6(a) and (b). The parasitic capacitor C_{pa} from the dc side to the earth is short-circuited by the common ac and dc ground. According to the standard grid code [4], the impedance Z_l between the grid and the ground is low. The expression of CMV across C_{pa} is given by [10]

$$V_{\text{cmv}} = (V_{Pn} + V_{Nn})/2 \tag{11}$$

where P and N are the positive and negative terminals of the LED array and n is the terminal of the ac ground.

TABLE II
MAXIMUM VOLTAGE STRESS OF EACH DEVICE

Device	Maximum voltage stress	Set value
S_{PFC1}	$(V_s+V_{C\text{-}a})/2$	
S_{PFC2}	$(V_s+V_{C\text{-}a})/2$	
S_1	Max (V_s+V_C, $V_{C\text{-}a}-V_{out}$)	90V-RMS Input
S_2	Max ($V_{C\text{-}a}-V_{out}$)	
VT_1	Max ($V_{C\text{-}a}$)	
VT_2	Max ($V_{C\text{-}a}$, V_{out})	V_{out} of 80V
VT_3	Max ($V_{C\text{-}a}$, V_{out})	

From Fig. 6(a) and (b), we have

$$\begin{cases} V_{PN} = V_{\text{out}} \\ V_{Nn} = 0 \end{cases} \tag{12}$$

$$V_{Pn} = V_{PN} + V_{Nn}. \tag{13}$$

Therefore, the CMV expression of the common-ground-type transformerless converter is as follows:

$$V_{\text{cmv}} = V_{\text{out}}/2. \tag{14}$$

There are two methods of reducing CM to make the CM voltage frequency lower and to stabilize the CM voltage to a constant. The value of v_{cmv} is constant and does not emerge HF components, which practically eliminates the CMC i_{cm}.

IV. DESIGN CONSIDERATIONS

To have high power density and reliability, it is desirable to minimize the number of required passive components. Some necessary instructions are given, such as the section of power devices, the section of decoupling capacitor and input inductor, and the analysis of the control unit.

A. Component Voltage and Current Stresses

To ensure the safe operation of the proposed rectifier, the withstand voltage of the devices must be considered. According to the operating modes of a switching cycle shown in Fig. 4, the maximum voltage stress at switches and diodes can be calculated, as shown in Table II. $V_{C\text{-}a}$ is the peak voltage across the decoupling capacitor, and its value should be (1+15%) V_C after considering the ripple voltage of 30%.

For the current stress of S_{PFC1} and S_{PFC2}, the maximum current stress must occur at I_{L1-p} according to (4). In Mode 2, the energy delivered to the LED load, E_{LED}, can be expressed as

$$E_{\text{LED}} = \frac{\left(I_{\text{out-p}}^2 - I_{\text{out-av}}^2\right) L_{\text{out}}}{2}. \tag{15}$$

At the same time, E_{LED} can also be expressed as

$$E_{\text{LED}} = [(I_{\text{out-p}} + I_{\text{out-av}})/2] V_{\text{out}} T_s. \tag{16}$$

Combining (15) and (16) yields

$$I_{\text{out-p}} = \frac{V_{\text{out}} T_s}{L_{\text{out}}} + I_{\text{out-av}}. \tag{17}$$

Thus, the maximum current of $VT1$ is calculated. Combining (5), (6), and (17), the maximum current of VT_1, VT_3, and S_1 can also be obtained.

B. Selection of a Decoupling Capacitor

Due to the fact that different operation modes are in $v_s > 0$ and $v_s < 0$, there are two calculation results for C_{de}. The relationship between the capacitance and the voltage ripple is

$$\Delta U = \frac{Q}{C_{\text{de}}} \tag{18}$$

where ΔU is the voltage ripple across the capacitor C_{de}, and Q is the amount of charge of the capacitor C_{de}.

Through the analysis of Mode 3, Mode 6, and (3), we have

$$Q_1 > Q_{1'}. \tag{19}$$

It is known that no matter what conditions are in $v_s > 0$ and $v_s < 0$, the final selection of C_{de} is the same. Hence, combining (18) and (19), we have

$$\Delta U_1 > \Delta U_{1'} \tag{20}$$

where ΔU_1 and $\Delta U_{1'}$ are the voltage ripples under the conditions $v_s > 0$ and $v_s < 0$, respectively.

According to (20), it can be seen that a larger capacitance is required under $v_s > 0$ to maintain the voltage ripple within the preset range. Thus, if C_{de} meets the condition of $v_s > 0$, it can ensure the stable operation under $v_s < 0$. Therefore, the following capacitor selection is based on the condition of $v_s > 0$. In the converter based on the power factor (PF) of 1, the instantaneous voltage of the decoupling capacitor V_c [20] is

$$V_c\ (t) = \sqrt{V_{C-c}^2 - \frac{P_{\text{out}}\left[\sin(2\omega t) - 1\right]}{\omega C_{\text{de}}}} \tag{21}$$

where the minimum voltage of V_c is V_{C-c} and ω is the grid angular frequency.

The above equation is deduced based on zero power loss in the proposed converter. According to Fig. 4, the condition that V_{C-c} satisfies is

$$V_{C-c} > V_s + V_{\text{out}}. \tag{22}$$

Combining (17) and (21), the maximum value of V_c is expressed as

$$V_{C-\max} = V_{C-a} = \sqrt{V_{C-c}^2 + \frac{2P_{\text{out}}}{\omega C_{\text{de}}}}. \tag{23}$$

Hence, the selection of the decoupling capacitor should be higher than that described in (23).

Additionally, the current of the decoupling capacitor i_{de} is

$$i_{\text{de}}\ (t) = -\frac{P_{\text{out}} \cos(2\omega t)}{\sqrt{V_{C-c}^2 - \frac{P_{\text{out}}[\sin(2\omega t)-1]}{\omega C_{\text{de}}}}}. \tag{24}$$

When $2\omega t = \pi$, i_{de} becomes its maximum, i.e.,

$$i_{\text{de}}\ (t) = \frac{P_{\text{out}}}{\sqrt{V_{C-c}^2 + \frac{P_{\text{out}}}{\omega C_{\text{de}}}}}. \tag{25}$$

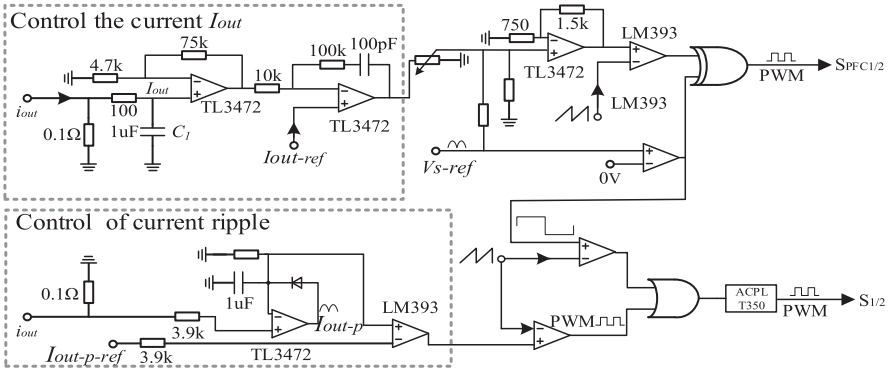


Fig. 7. Decoupling capacitance versus ripple voltage.

Additionally, $2\omega t = 0$; $i_{\rm de}$ becomes its minimum, i.e.,

$$i_{\rm de}\ (t) = -\frac{P_{\rm out}}{\sqrt{V_{C-c}^2 + \frac{P_{\rm out}}{\omega C_{\rm de}}}}. \tag{26}$$

V_{c-a} is often preset. Combining (22) and (23), the minimum capacitance is calculated by

$$C_{\rm de-min} = \frac{2P_{\rm out}}{\omega\left[V_{C-a}^2 - (V_s + V_{\rm out})^2\right]}. \tag{27}$$

According to (23), a larger value of V_C leads to a smaller capacitance for $C_{\rm de}$. Based on (27), the decoupling capacitance at different output voltage levels is plotted in Fig. 7. Obviously, with the increase of the voltage ripple of the decoupling capacitor, the required capacitance is decreasing. In this design, to avoid the degradation of the output power quality, the ripple value is designed at about 30%.

C. Inductor Requirement

The design of L_1 is similar to the inductor of the boost-type converter. The detailed loss and volume optimization are given in [27]. The design criterion for the main inductor L_1 is that the rectifier should operate in the DCM.

According to the volt–second balance principle, during the charging period with reference to Fig. 4, the inductor current ripple can be expressed as

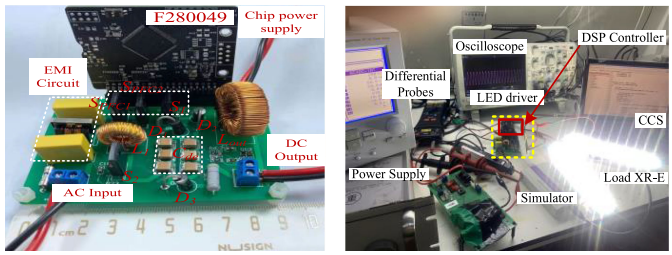
$$\Delta i_{L1}\ (t) = \frac{v_{s(D_1+D_2)T_s}}{L_1} = \frac{v_s}{L_1}\frac{|i_s| + i_{\rm de}}{|i_s| + I_{\rm out}}T_s. \tag{28}$$

During the discharging period, we have

$$\Delta i_{L1}\ (t) = \frac{v_s D_2 T_s}{L_1} = \frac{v_s}{L_1}\frac{|i_s| - i_{\rm de}}{|i_s| + I_{\rm out}}T_s. \tag{29}$$

To meet the design standard of the current i_L, the maximum inductance is given as [30]

$$L_{1-\max} = \text{Max}\begin{cases} \frac{|v_s|T_s}{\Delta i_{L1}}\frac{|i_s|-i_{\rm de}}{|i_s|+I_{\rm out}} & (when\ i_c \geq 0) \\ \frac{V_{\rm out}}{\Delta i_{L1}}\frac{I_{\rm out}+i_{\rm de}}{|i_s|+I_{\rm out}} & (when\ i_c < 0). \end{cases} \tag{30}$$



(a) (b)

Fig. 8. Structure of the control circuit.

According to (30), the required inductance can be designed, and thus, the reverse recovery losses associated with diodes are eliminated.

D. Control Strategy

The output current control method and ripple current of the proposed driver is presented in Fig. 8. To simplify the control strategy, $S_{\rm PFC1}$ and $S_{\rm PFC2}$ are adopted to realize PFC and adjust the output current. After the output instantaneous current $i_{\rm out}$ passes through the 0.1-Ω detection resistance, the average output current $I_{\rm out}$ is obtained by the LC low-pass filter. The detection signal is compared with the reference signal $I_{\rm out-ref}$. The error signal is amplified and adjusted and then transmitted to the proportional–integral regulator. Subsequently, the output of the regulator is multiplied by $V_{s-\rm ref}$ to obtain the PFC tracking signal, which is compared with the sawtooth wave signal after the amplifier, and finally, the pulsewidth modulation (PWM) signal is obtained. Then, the required driving signals are obtained through logic operation and transmitted to the switches $S_{\rm PFC1}$ and $S_{\rm PFC2}$. $V_{s-\rm ref}$ is the electric signal after the input voltage takes the absolute value.

The output current ripple control is as follows. The peak output current $I_{\rm out-p}$ is obtained by peak current detection, and then, $I_{\rm out-p}$ is compared with the peak reference current $I_{\rm out\text{-}p\text{-}ref}$ to obtain the control signal of the output current ripple. $V_{s-\rm ref}$ gets a square-wave signal with the same frequency after zero detection to determine the working status of S_1 and S_2. After comparing the low-frequency square-wave signal, ripple current control signal, and sawtooth wave, the driving signals are

TABLE III
SUMMARY TABLE OF COMPARATIVE RESULTS

Converter	Total no. components				No. of state switches	Output Filter		PD Feature	CMC	PFC
	S	D	L	C		L_f	C_f			
[17]	2	8	4	3	2	600 μH	220 μF	√	×	×
[19]	2	6	2	2	2	No report	30 μF	√	×	√
[23]	6	2	2	1	4	0.8 mH	500 μF	×	√	×
[26]	7	2	2	1	4	2.3 mH	0.5 mF	×	√	×
[27]	4	1	2	1	4	2.2 mH	5 μF	√	√	×
Proposed	4	3	2	1	2 or 3	1 mH	0	√	√	√

Where, S=switch, D=Diode, C=Capacitor, L=Inductor, PD=Power decoupling

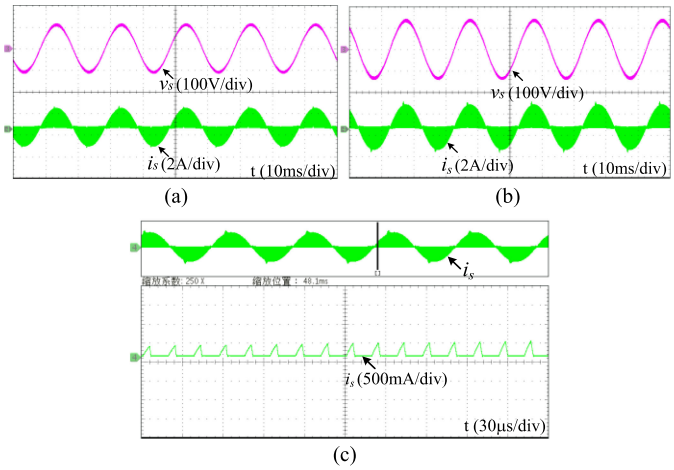


Fig. 9. Experimental photos. (a) Experimental prototype. (b) Experimental platform.

TABLE IV
COMPONENT PARAMETERS OF THE PROPOSED DRIVER

Description	Values
Input Voltage V_s	90V AC
Switching Frequency f_s	50kHz
Line Frequency f	50Hz
Ceramic capacitors C_{de}	6×1μF/400V
Resistance of LEDs	100Ω
Filtering capacitor C_f	220nF/330V
PFC inductor L_1	400μH
Filtering inductor L_{out}	1mH

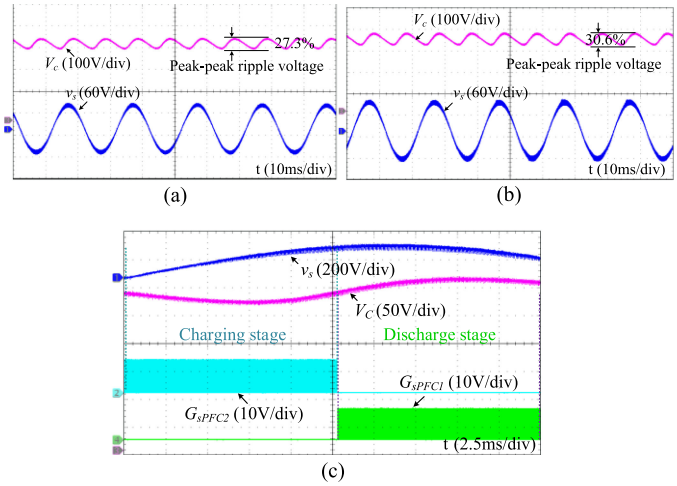


Fig. 10. Key experimental results of the proposed circuit. (a) Under 90 V_{rms}. (b) Under 110 V_{rms}. (c) Under DCM under 220 V_{rms}.

obtained through the logic gates and transmitted to the switches S_1 and S_2.

E. Comparative Analysis

The proposed converter topology and the existing works in this section will be analyzed and compared in terms of the circuit elements, the function, and the performance at the full-power condition, as shown in Table III.

According to Table III, it can be seen that proposed topology applies to only four power switches and reducing number of passive components due to the integration of multiple units and the time-sharing multiplexing of circuit components. In other words, the total number of control objects is reduced, and the control unit is simplified. In addition, the proposed LED driver structure includes promising features such as complete leakage current suppression, PFC ability, and power decoupling ability.

V. PERFORMANCE EVALUATIONS

To verify the correctness of the theoretical analysis, an 80-W experimental prototype presented in Fig. 9(a) has been completed. Fig. 9(b) shows the whole experimental platform, where Cree Cool white XR-E series LEDs are employed to street lighting applications. Based on the analysis of Section IV, the parameters are shown in Table IV. Besides, the experimental waveforms of key electrical signals, such as V_C, i_s, v_s, and I_{out}, are shown in Figs. 10–13, respectively.

Fig. 10(a) and (b) shows the measured input current waveforms current i_s at a wide range of input voltages. The input current fully tracks the input voltage and can be approximately regarded as a perfect sine wave. A higher PF is achieved, and the values are 0.984 and 0.976, respectively. Besides, this article takes $v_s = 220$ V_{rms} as an example to illustrate the situation because of the same working mode under different input voltages. The result is presented in Fig. 10(c), which shows the verification of the working mode of the DCM. Thus, the operation under the DCM can effectively eliminate the reverse recovery time of the later-stage diodes and reduce the loss.

Fig. 11(a) and (b) shows the measured waveforms of the voltage V_c under the different input voltage. A higher ripple is set to help obtain a smaller output filter capacitor, and the maximal ripple is about 96.4 V, which is 30.6% of the average bus voltage. In addition, from the following experimental results, it can be seen that the output current is disturbed by the large ripple voltage. From Fig. 11(c), it can be noticed that S_{PFC1} is turned ON and V_C increases since C_{de} is charged when $v_s > 0$ and *vice versa*. Therefore, the correctness of the control unit design can be proved.

In order to meet the requirements of energy saving, a wide range of brightness adjustments should be required. Fig. 12(a)

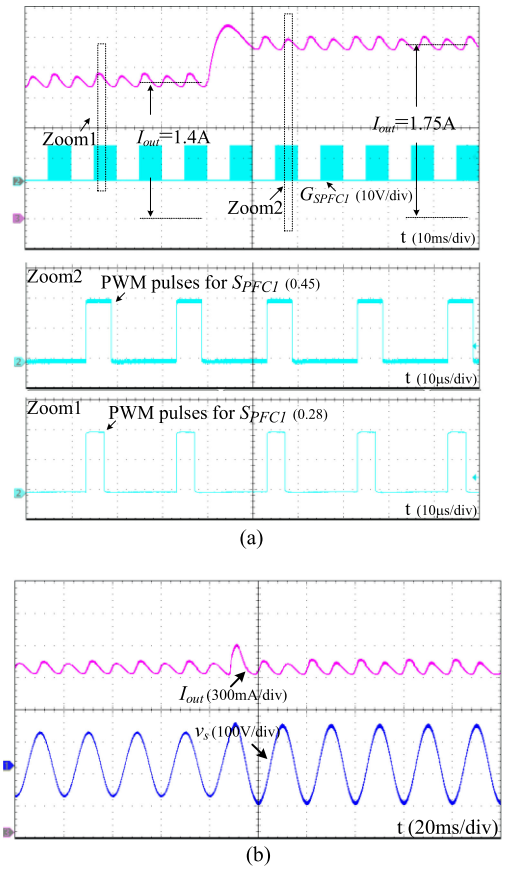


Fig. 11. Measured decoupling capacitor voltage. (a) Under $v_s = 90$ V. (b) Under $v_s = 110$ V. (c) With the charging–discharging process.

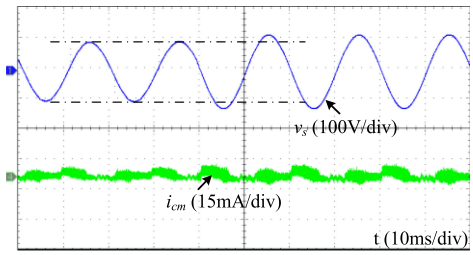


Fig. 12. Measured waveforms of the output current. (a) Under different duty cycles. (b) Under different input voltages.

shows measured waveforms of the output current and the corresponding driving signals. The duty cycle of the switch S_{PFC1} is 0.28–0.45, and the amplitude of the output current is 1.4–1.75 A, which are consistent with the theoretical analysis. Another case is shown in Fig. 12(b), in which the amplitude of the output current ripple is almost constant under a wide range of input voltage, and the maximum output current ripple is 7.3%. The proposed circuit is significantly improved and is more stable when compared with the output current ripple of 14.1% in [23].

To verify the effectiveness of the proposed converter in suppressing the CMC, a parasitic capacitor ($C_{\mathrm{pa}} = 110$ nF) is installed in the experimental prototype. Fig. 13 shows the leakage current with different voltage levels. The leakage current gradually increases with the increasing value of the

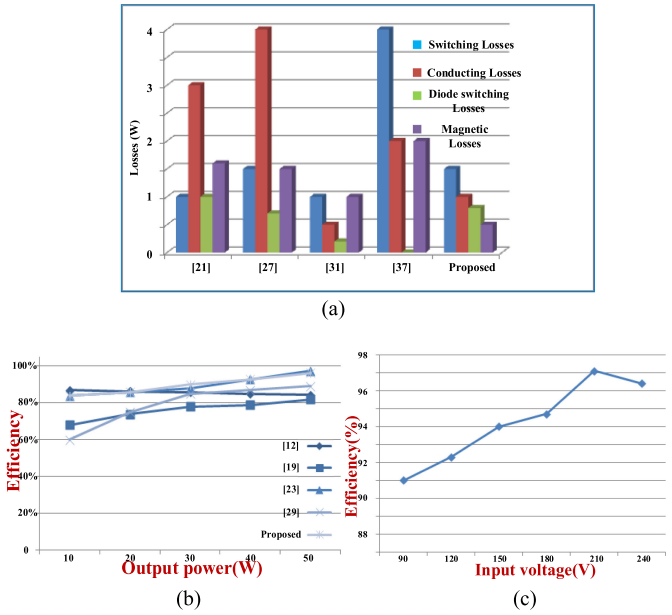


Fig. 13. Leakage current measurement waveform.

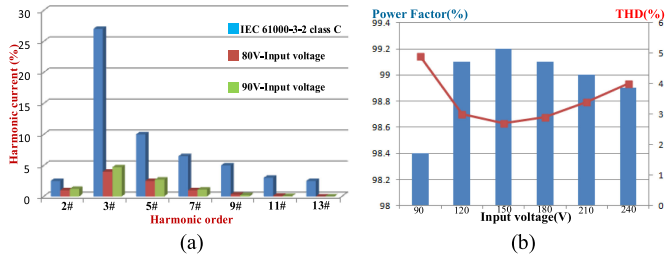
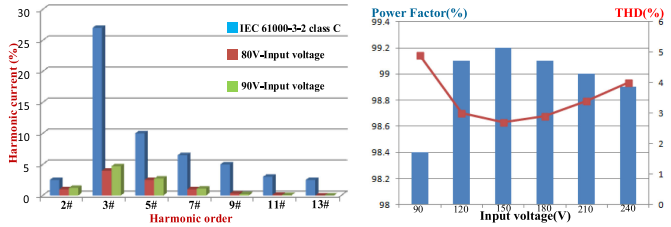


Fig. 14. Loss distribution and efficiency variation of the proposed driver under the variation of output power and input voltage. (a) Loss distribution, (b) efficiency under different output power, and (c) efficiency under different input voltage.

input voltage. For example, when $v_s = 90$ V, i_{cm} reaches 8.3 mA (rms value), and when $v_s = 110$ V, i_{cm} reaches 11.7 mA (rms value). Therefore, the transformerless converter fully complies with strict safety standards DIN VDE 0126-1-1 [28].

Fig. 14(a) shows the semiconductor loss distribution according to the switching frequency under the rated power of similar works with the same circuit parameters, and the switching loss is calculated according to the device datasheet. The precision power analyzer called PROVA 6800 has been employed to measure the efficiency. Moreover, the conduction loss of diodes and switches is the main loss, which is consistent with the analysis in Section V. A new valley switching is presented in [29] and [30], and it uses a resonance between the converter's inductor and parasitic output capacitance. It is one of the most effective ways to reduce the switching loss and provides a new direction for the improvement of the proposed rectifier. Fig. 14(b) displays the efficiency curves, including the comparison of previous topologies. The system proposed in [12] has the highest efficiency for low-power applications, but the leakage current characteristic is worse in comparison to the proposed topology. Fig. 14(c) shows



(a) (b)

Fig. 15. Performance analysis. (a) Input harmonic current versus IEC-61000-3-2. (b) Measured PF and THD.

the efficiency of the input voltage ranging from 90 to 240 V_{ac} at rated power. Finally, the maximum efficiency of the proposed converter can reach 97.1%.

Fig. 15(a) and (b) shows the result of performance evaluation, which includes the measurement of input harmonic current THD and PF under different input voltages. The result shows that all harmonic currents are below the limit of IEC-610003-2. The proposed circuit achieves a PF of 0.992, which meets the requirement from Energy Star. What is more, the THD of the input current is less than 4.9% within the input voltage ranging from 85 to 110 V_{rms}. Therefore, LED interconnection with the proposed LED driver can be achieved.

VI. Conclusion

In this article, a novel transformerless single-phase rectifier for LED application was introduced. The proposed LED rectifier benefits from several merits. The capacitors of the proposed rectifier allowed large voltage ripple and did not cause LED flicker. Hence, Ecaps were eliminated and replaced by 6 × 1-μF/400-V ceramic capacitors. The proposed rectifier had a common ground between the input and output terminals, which resulted in the elimination of leakage current in systems. The decoupling capacitor can not only realize the energy buffering but also eliminate the influence of the high-order harmonics generated by the switches. Therefore, filter capacitors were not required in this topology. Operational principles were described and theoretical analysis was done. An 80-W prototype was built, and the experimental results proved the performance of the proposed inverter.

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