Sampled-Data Model of a Two-Phase, Dual Interleaved Buck–Boost Converter With PCM

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***Abstract*—A sample-data modeling strategy for a 30-kW, two-phase dual interleaved buck–boost converter with peak current control is analyzed in this article. A small-signal converter model is derived to characterize the system utilizing the current peaks of the two interleaved phases and a half-symmetry, state-space representation of the circuit. The model is experimentally verified using a 32-kW, 350-V prototype that owns 7.6 kW/kg and 97.1% of power density and efficiency, respectively. A description of the controller, developed in a high-performance microcontroller, is also presented together with the experimental verification, detailing the design of the compensating ramp for a wide load range. Measured results are contrasted with the sample-data model predictions, using both transient and frequency responses, and evaluating the controlled converter dynamics at 14, 21, 26, and 30 kW. The comparison reveals the effective validity of the presented sample-data model and the effects of the supply to the dynamic performance of the high-density converter.**

***Index Terms*—Coupled inductors, dc–dc converters, interleaved converters, peak-current control, sampled-data.**

I. Introduction

THE increasing research and development of high-performance electric vehicles has led to focus special attention to high power density dc–dc converters [1]–[8]. Multiphase topologies with interleaved switching and integrated magnetics [4]–[9] are commonplace strategies used in these converters due to their nature to optimize power density [8], [9]. The dynamic behavior for current phase sharing and balance is a principal challenge of these converters to guarantee stability, performance, and get high-power density, a critical factor nowadays for electromobility solutions [1]–[8].

Modeling and control analysis of medium-power, interleaved converters have been described in [10]–[15], in search of reliable energy management. The latter relies on straightforward, easy-to-drive one-switch averaged models for general dynamic analyses while forgetting the potentiality of other modeling techniques. For example, the behavior and limits of a boost interleaved converter in continuous current mode (CCM) or discontinuous current mode (DCM) are described and tested in a 72-kW prototype in [9], whereas two interleaved variants of high-density, medium-power boost converters are discussed in [10] and [11], whose power densities, respectively, rely on a multidevice interleaved configuration and a multistage, interleaved coupled arrangement of inductors; furthermore, a description of a current-balancing method for a bidirectional dc–dc converter is given in [12], which uses a variable frequency control technique that may be applied to multiphase circuits.

Phase-current balance studies of interleaved converters with coupled inductors are hardly reported due to the presence of extra operating modes. An example is presented in the boost converter in [15], whose model is analyzed on a sampled data basis reviewed in [16] and [17], whereas the works in [13] and [14] show averaged-switch modeling techniques for boost and buck configurations also using an averaged coupled inductors model. These techniques reveal better dynamic insight of interleaved switching with coupled magnetics as summarized in [6].

Current control strategies for medium-power, interleaved converters are critical systems for tracking the reference generated by the energy management unit [6], [13]–[15]. Peak current mode (PCM) control [6], [15] and averaged current control [6], [10]–[14] are commonplace techniques that use digital, analog, or mixed signal technologies for medium power rating. Control systems with integrated or improvised mixed-signal architecture have been reported in [18]–[25]; for example, Taeed and Nymand [25] integrate an FPGA and a microcontroller to implement PCM control; however, this task may result complex, expensive, and time-consuming as described in [26]. In recent years, microcontroller manufacturers have focused their efforts on the construction of single-chip devices with mixed-signal processing capabilities; by instance, Calderon-Lopez *et al.* [6] describe a single microcontroller combination of digital and analog technologies [27] to implement control loops of PCM together with averaging signal for a 60-kW, dc–dc converter.

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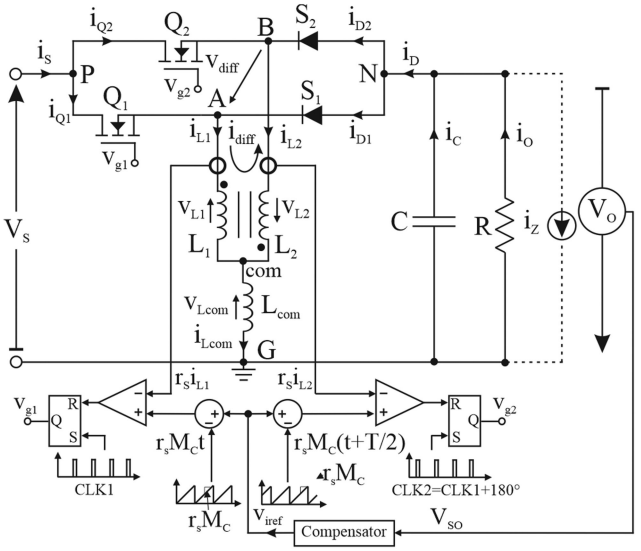


Fig. 1. Schematic of the dual-interleaved buck–boost converter with IPT and peak current-mode control.

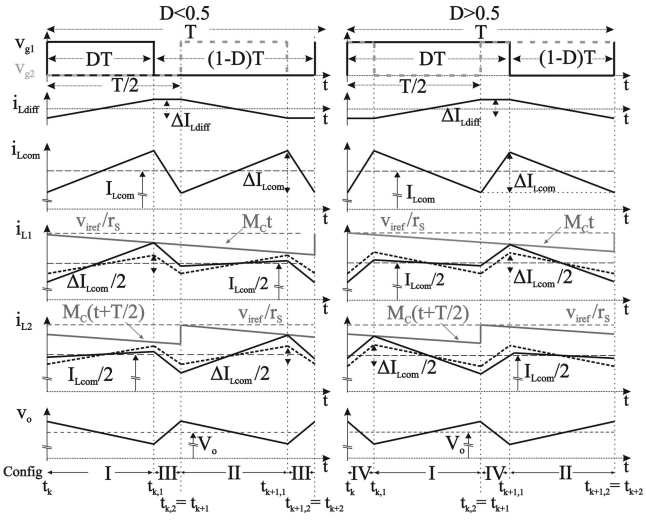


Fig. 2. Ideal waveforms for the dual interleaved converter under steady-state conditions for (a) $D < 0.5$ and (b) $D > 0.5$.

This article presents a sample-data model of a two-phase, dual interleaved buck–boost converter in CCM that uses an interphase transformer (IPT) and a mixed-signal PCM control scheme, exploiting the half-cycle symmetry inherent to the topology. The converter is intended to regulate power drawn from a unidirectional source of energy, such as fuel cells for automotive applications. The main contributions of this article are the following: the mathematical model of this converter topology, the stability region analysis, the determination procedure to select a compensating slope value for the PCM control scheme, the controller implementation in a mixed-signal, single-chip microcontroller, and the demonstration of current balance in each phase. Additionally, this article fulfills the study of the conventional interleaved dc–dc topologies that use IPT [6], [14], and [15]. Experimental measurements, obtained with a 350-V, 32-kW prototype and 7.6-kW/kg power density, are presented evaluating the accuracy of the sample-data model in time and frequency domains under steady state and transient conditions from 14 to 30 kW.

II. Converter Summary

A. Converter Scheme Summary

Fig. 1 shows the dual interleaved buck–boost converter, the peak current-mode inner controller, and an outer voltage compensator. The circuit is comprised of two paralleled buck–boost switching legs connected through their transistor drain nodes to the supply V_S and through their diode anode nodes to an output filter capacitor *C*. Nodes *A* and *B* are connected to an IPT whose central tap node, *com*, links a common inductor $L_{\rm com}$.

The current controller drives the transistors turning ON and OFF, respectively, using two complementary high-frequency (HF) clock pulses and two compensated latched comparators, feedbacking and equalizing the phase currents i_{L1} and i_{L2} to the compensated reference while i_{L1} and i_{L2} peaks are determined at instants $t_{k,1}$, for $D < 0.5$, and t_{k+11}, for $D > 0.5$, when the comparison events take place, entitling the control strategy as PCM [28]. An outer voltage controller, which is out of the scope of this work, will set the reference current depending on the desired operating point of the electric power train of the vehicle.

B. Steady-State Operation

Steady-state operation of the converter shown in Fig. 1 is described assuming CCM of i_{L1} and i_{L2}, lossless components, unity coupling of the IPT windings, and identical self-inductances, $L_1 = L_2$, such that the differential inductance $L_{\rm diff}$ between the *A* and *B* nodes is equal to $4L_1$. Further steady-state analysis for the performance and high power density assessment of this converter is found in [7].

Two circuit configuration sequences, extensively analyzed in [7] for $D > 0.5$ or $D < 0.5$, determine the CCM dynamic behavior of the circuit of Fig. 1. The CCM circuit configurations are given in Table I as indicated at the bottom of Fig. 2, where i_{L1} and i_{L2} are presented with the common inductor current $i_{\rm Lcom}$ and the differential current $i_{\rm diff}$ respective to the transistor switching states v_{g1} and v_{g2}. The slope sequence of i_{L1} and i_{L2} depends on the active configuration and, thereby, this determines the dynamic characteristics of the current controller as explained ahead.

III. Circuit Dynamics Analysis

A. State-Space Model

Each converter configuration can be described by

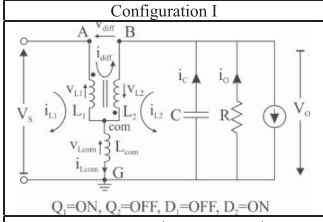
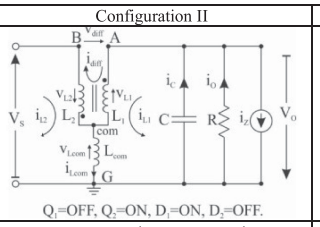
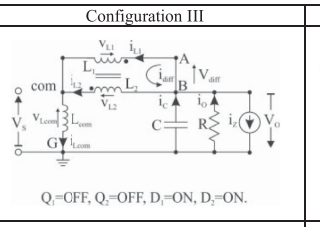
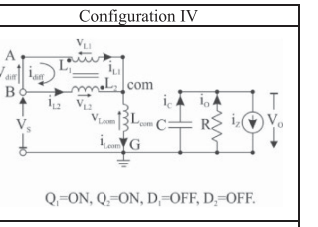
$$\dot{\mathbf{x}} = \mathbf{A}_n \mathbf{x} + \mathbf{B}_n \mathbf{u} \tag{1}$$

and solved using (2) [28]

$$\mathbf{x}\,(t_1 + T) = e^{\mathbf{A}T}\mathbf{x}(0) + \int_{t_1}^{t_1+T} e^{\mathbf{A}T} dt \mathbf{B}\mathbf{u} \tag{2}$$

where the input vector comprises v_s and i_z, a current source in parallel with the load, such that $\mathbf{u} = [v_s\ i_z]^t$ whose values change slower than the switching frequency. The state vector variables

TABLE I
CIRCUIT CONFIGURATIONS AND THEIR CORRESPONDING STATE-SPACE MATRICES

Configuration I	Configuration II	Configuration III	Configuration IV
			
Q_1=ON, Q_2=OFF, D_1=OFF, D_2=ON	Q_1=OFF, Q_2=ON, D_1=ON, D_2=OFF.	Q_1=OFF, Q_2=OFF, D_1=ON, D_2=ON.	Q_1=ON, Q_2=ON, D_1=OFF, D_2=OFF.
$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 & -\frac{1}{2L_{com}} \\ 0 & 0 & \frac{1}{L_{diff}} \\ \frac{1}{2C} & -\frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$ $\mathbf{B}_1 = \begin{bmatrix} \frac{1}{2L_{com}} & 0 \\ \frac{1}{L_{diff}} & 0 \\ 0 & \frac{1}{C} \end{bmatrix}$	$\mathbf{A}_2 = \begin{bmatrix} 0 & 0 & -\frac{1}{2L_{com}} \\ 0 & 0 & -\frac{1}{L_{diff}} \\ \frac{1}{2C} & \frac{1}{C} & -\frac{1}{RC} \end{bmatrix}$ $\mathbf{B}_2 = \begin{bmatrix} \frac{1}{2L_{com}} & 0 \\ -\frac{1}{L_{diff}} & 0 \\ 0 & \frac{1}{C} \end{bmatrix}$	$\mathbf{A}_3 = \begin{bmatrix} 0 & 0 & -\frac{1}{L_{com}} \\ 0 & 0 & 0 \\ \frac{1}{C} & 0 & -\frac{1}{RC} \end{bmatrix}$ $\mathbf{B}_3 = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & \frac{1}{C} \end{bmatrix}$	$\mathbf{A}_4 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{RC} \end{bmatrix}$ $\mathbf{B}_4 = \begin{bmatrix} \frac{1}{L_{com}} & 0 \\ 0 & 0 \\ 0 & \frac{1}{C} \end{bmatrix}$

are i_{Lcom}, i_{diff}, and v_{out}, such that $\mathbf{x} = [i_{\mathrm{Lcom}}\ i_{\mathrm{Ldiff}}\ v_{\mathrm{out}}]^t$ is the state vector. $\mathbf{A}_n$ and $\mathbf{B}_n$ depend on the active configuration as given in Table I, being time-invariant matrices.

B. Converter Symmetry

A symmetrical behavior of $\mathbf{x}$ is present every half-cycle in a steady state, as shown in Fig. 2, which may reduce the dynamic analysis since

$$\mathbf{x}\left(t + {}^{T}/_{2}\right) = \mathbf{W}\mathbf{x}(t) \tag{3}$$

where $\mathbf{W}$ is

$$\mathbf{W} = \begin{pmatrix} 1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & 1 \end{pmatrix} \tag{4}$$

a matrix with properties $\mathbf{W}^{-1} = \mathbf{W}$ and $\mathbf{W}^2 = \mathbf{I}$, being $\mathbf{I}$ the identity matrix [16]. The presented model uses only the equations of the first two sequences configurations to describe the state vector of a whole switching cycle *T*.

According to [17], the state vector at the end of the first half-cycle of the converter may be expressed as

$$\mathbf{x}_{k+1} = \mathbf{\Phi}_{k,1}\mathbf{\Phi}_{k,2}\mathbf{x}_k + \left[\mathbf{\Phi}_{k,2}\Psi_{k,1}\mathbf{B}_1 + \Psi_{k,2}\mathbf{B}_2\right]\mathbf{u}_k \tag{5}$$

where

$$\begin{aligned} \Psi_{k,_1} &= \mathbf{A}_1^{-1}\left(\mathbf{\Phi}_{k,1} - \mathbf{I}\right), \Psi_{k,2} = \mathbf{A}_2^{-1}\left(\mathbf{\Phi}_{k,2} - \mathbf{I}\right) \\ \mathbf{\Phi}_{k,1} &= e^{\mathbf{A}_1(t_{k,1} - t_k)}, \mathbf{\Phi}_{k,2} = e^{\mathbf{A}_2(t_{k,2} - t_{k,1})} \end{aligned} \tag{6}$$

and $\mathbf{A}_1$, $\mathbf{A}_2$, $\mathbf{B}_1$, and $\mathbf{B}_2$ are the configurations matrices of the first half-cycle depending on the duty cycle condition. $\Psi_{\mathrm{k},1}$ and $\Psi_{\mathrm{k},2}$ may be numerically approximated using a truncated Taylor series method.

The first half cycle of the converter can be thereby modeled using (4) together with a constrain equation as follows:

$$\begin{aligned} \mathbf{x}_{k+1} &= \mathbf{f}\left(\mathbf{x}_k, \mathbf{p}_k, \mathbf{t}_k\right) \\ \mathbf{c}\left(\mathbf{x}_k, \mathbf{p}_k, \mathbf{t}_k\right) &= \mathbf{0} \end{aligned} \tag{7}$$

where $\mathbf{x}_k$ is $\mathbf{x}$ at the beginning of the period, $\mathbf{c}(\mathbf{x}_k, \boldsymbol{p}_k,\ \boldsymbol{t}_k)$ is the constrain equation and $\mathbf{p}_k$ is the vector of the controlling parameters, which includes $\mathbf{u}_k$ input vector and the current controller reference v_{iref}. The time vector $\mathbf{t}_k$ is comprised by the first half-cycle transition instants t_k, $t_{k,1}$, t_{k+1}, as shown in Fig. 2, whereas $t_{k,1}$ and t_{k+11} are determined by the current controller and $\mathbf{p}_k$; thereby, the i_{L1} waveform of Fig. 2 is used to determine $\mathbf{c}(\mathbf{x}_k, \boldsymbol{p}_k,\ \boldsymbol{t}_k)$ for $D < 0.5$ as

$$\mathbf{c} = \begin{bmatrix} \left[\frac{1}{2} + 1 + \left(\frac{1}{L\mathrm{diff}} - \frac{1}{4L_{\mathrm{com}}}\right)t_{k,1}\right]\mathbf{x}_k \\ + \left[\left(\frac{1}{4L_{\mathrm{com}}} + \frac{1}{L_{\mathrm{diff}}}\right)t_{k,1} + 0 + \frac{1}{r_S}\right]\mathbf{p}_k + \frac{M_C t_{k,1}}{r_S} \\ t_{k,2} - \frac{T}{2} \end{bmatrix} = \mathbf{0} \tag{8}$$

and for $D > 0.5$ as

$$\mathbf{c} = \begin{bmatrix} \left[\frac{1}{2} + 1 + 0\right]\mathbf{x}_k + \left[\frac{t_{k,1}}{2L_{com}} + 0 + 1\right]\mathbf{u}_k \\ + \frac{M_C T}{2R_S} + \frac{M_C t_{k,1}}{r_S} \\ t_{k,2} - \frac{T}{2} \end{bmatrix} = \mathbf{0}. \tag{9}$$

According to [16], the second half-cycle of half-cycle symmetry converters are governed by **W,** acting on the first cycle function and the constrain (6), which may thereby be expressed as

$$\begin{aligned} \mathbf{x}_{k+2} &= \mathbf{W}^{-1}\mathbf{f}\left(\mathbf{W}\mathbf{x}_{k+1}, \mathbf{p}_{k+1}, \mathbf{t}_{k+1}\right) \\ \mathbf{c}\left(\mathbf{W}\mathbf{x}_{k+1}, \mathbf{p}_{k+1}, \mathbf{t}_{k+1}\right) &= \mathbf{0}. \end{aligned} \tag{10}$$

C. Small-Signal Model

The large-signal model of (6) can be used to determine a small-signal model $\tilde{\mathbf{x}}_{k+1}$ assuming cyclic steady-state and retaining only the linear terms of a multivariable Taylor series, such that

$$\begin{aligned} \tilde{\mathbf{x}}_{k+1} &= \left[\partial\mathbf{f}/\partial\mathbf{x}\right]\tilde{\mathbf{x}}_k + \left[\partial\mathbf{f}/\partial\mathbf{p}\right]\tilde{\mathbf{p}}_k + \left[\partial\mathbf{f}/\partial\mathbf{t}\right]\tilde{\mathbf{t}}_k \\ \left[\partial\mathbf{c}/\partial\mathbf{x}\right]\tilde{\mathbf{x}}_k &+ \left[\partial\mathbf{c}/\partial\mathbf{p}\right]\tilde{\mathbf{p}}_k + \left[\partial\mathbf{c}/\partial\mathbf{t}\right]\tilde{\mathbf{t}}_k = \mathbf{0} \end{aligned} \tag{11}$$

which is used to solve $\tilde{\mathbf{t}}_k$ and, thereby, rewrite (11) as

$$\tilde{\mathbf{x}}_{k+1} = \mathbf{F}_0\tilde{\mathbf{x}}_k + \mathbf{G}_0\tilde{\mathbf{p}}_k \tag{12}$$

where

$$\begin{aligned} \mathbf{F}_0 &= \left[\partial\mathbf{f}/\partial\mathbf{x}\right] - \left[\partial\mathbf{f}/\partial\mathbf{t}\right]\left[\partial\mathbf{c}/\partial\mathbf{t}\right]^{-1}\left[\partial\mathbf{c}/\partial\mathbf{x}\right] \\ \mathbf{G}_0 &= \left[\partial\mathbf{f}/\partial\mathbf{p}\right] - \left[\partial\mathbf{f}/\partial\mathbf{t}\right]\left[\partial\mathbf{c}/\partial\mathbf{t}\right]^{-1}\left[\partial\mathbf{c}/\partial\mathbf{p}\right]. \end{aligned} \tag{13}$$

The small-signal model at the end of the switching period *T* is determined using (12) and $\mathbf{W}$ as described in [15], becoming the small-signal model for the whole switching period

$$\tilde{\mathbf{x}}_{k+2} = \mathbf{F}_W{}^2\tilde{\mathbf{x}}_k + \mathbf{G}_W\tilde{\mathbf{p}}_k \tag{14}$$

where

$$\begin{aligned} \mathbf{F}_W &= \mathbf{W}\mathbf{F}_0 \\ \mathbf{G}_W &= \mathbf{W}\mathbf{F}_0\mathbf{W}\mathbf{G}_0 + \mathbf{W}\mathbf{G}_0. \end{aligned} \tag{15}$$

TABLE II
DERIVATION OF STABILITY LIMITS OF THE DUAL INTERLEAVED CONVERTER

	$D < 0.5$	$D > 0.5$
$\boldsymbol{M_R}$	$\frac{V_S - V_O}{4L_{com}} - \frac{V_S + V_O}{L_{diff}}$	$\frac{V_S}{2L_{com}}$
$\boldsymbol{M_F}$	$\frac{V_O}{2L_{com}}$	$\frac{V_S - V_O}{4L_{com}} - \frac{V_S + V_O}{L_{diff}}$
$\boldsymbol{M_F/M_R}$	$\frac{2D}{(1-2D)+\frac{4}{L_r}}$	$\frac{(2D-1)+\frac{4}{L_r}}{2(1-D)}$
Stability Limits (Eq. 17)	$D < 0.25 + 1/L_r$	$D < 0.75 - 1/L_r$

A mathematical model expression may be determined by applying the Z transformation to the sample-data, small-signal model of (14) to verify the frequency response of the converter. In this fashion, a global transfer function matrix is determined using the expression shown ahead

$$\frac{\tilde{\mathbf{x}}(z)}{\tilde{\mathbf{p}}(z)} = [z\mathrm{I} - \mathbf{F}_W]^{-1}\mathbf{G}_W. \tag{16}$$

The analytical derivation of each individual transfer function of the model of (16) requires an extensive matrix manipulation process, which was not feasible to derive due to the matrix order and the considerable number of matrices operations; the transfer functions were thereby numerically calculated utilizing MATLAB.

D. Stability Analysis of the PCM Control

A stability analysis of the converter of Fig. 1 with PCM control can be performed utilizing the description given in [29], which uses the rising and falling slopes of L_1, M_R, and M_F, respectively, throughout a Volt–seconds balance equilibrium to derive the following a constrain equation:

$$\left|\frac{M_F - M_C}{M_R + M_C}\right| < 1 \tag{17}$$

where M_C is the compensating ramp slope. The stability limits of the controlled converter can be preliminarily determined without the compensating slope assuming $M_C = 0$ in (17), as shown in Table II. The resultant M_F/M_R ratio reveals that the converter stability depends only on the duty cycle and inductance ratio, $L_r = L_{\mathrm{diff}}/L_{\mathrm{com}}$. Equation (17) is plotted in Fig. 3 ranging L_r from 1 to 100 and D from 0 to 1. This figure is split into two sections, Fig. 3(a) and (b), to clearly depict system stability and instability as gray and dark gray surfaces respectively, showing stability for $0 < D < 0.25$ or for $0.5 < D < 0.75$; however, when the inductance ratio becomes $L_r > 4.0$, the stability limits increase for $0.5 < D < 1$ or decrease for $0. < D < 0.5$ causing unstable operation of the converter. Other dual interleaved topologies, such as [15], report that a critical factor of $L_r = 4.0$ may increase or decrease the unstable region. Fig. 3(a) and (b) suggests that the PCM control requires slope compensation with a high M_F/M_R ratio, enough to obtain stable CCM operation in a wide power range. The determination of the M_C compensating slope depends on the device parameters of the converter as described ahead.

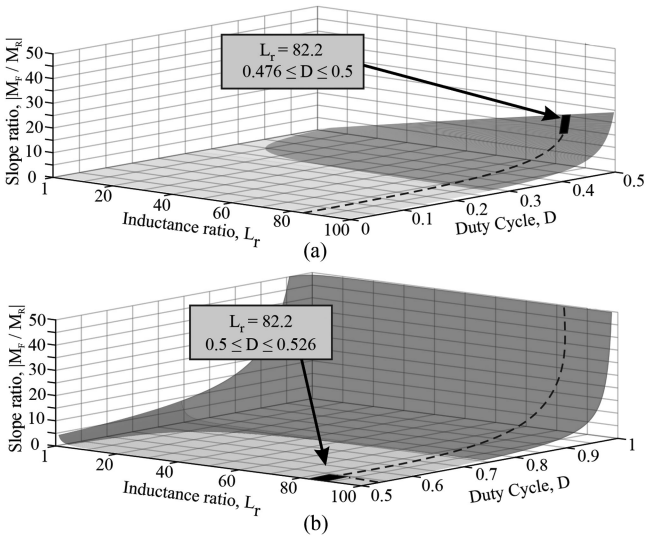


Fig. 3. Stability region of the two-phase, dual interleaved buck–boost converter for (a) $0 < D < 0.5$ and (b) $0.5 < D < 1$.

TABLE III
CONVERTER PARAMETERS AND CONDITIONS

Critical operating conditions	
Parameter	**Value**
Power, P	32 kW
Switching Frequency, f_{SW}	75 kHz
Supply Voltage Range, V_S	350 ± 10 %
Averaged Output Voltage, V_O	350 V
Duty Ratio Range, D	0.476 to 0.526
Components	
Parameter	**Value**
IPT differential Inductance, L_{diff}.	576 µH
IPT self-inductances, L_1 and L_2	144 µH
Common Inductance, L_{com}.	7 µH
Input and Output Capacitance, C_{in} and C_{out}.	20 µF
MOSFET Snubber Capacitor	680 nF
Inductance ratio, $L_r = L_{diff}/L_{com}$	82.5
Current sensing gain, r_s	3.33×10^{-3} V/A
Power Semiconductors	SiC bridges CAS120M12BM2

IV. EXPERIMENTAL VERIFICATION

A. Converter and Control System Characteristics

Table III present the operating critical conditions and parameters of the converter designed to feed a 350-V, 30-kW load equivalent to a PM traction motor drive [30], which will be part of an electric vehicle powertrain.

The control strategy was implemented utilizing a 32-b, 200-MHz dual-core microcontroller [27], which has mixed-signal architecture, comprised with a set of digital ramp generators whose outputs are connected to analog comparators throughout 12-b, digital-to-analog converters (DAC). i_{L1} and i_{L2} were sensed using Hall-effect sensors, corresponding these to $r_S i_{L1}$ and $r_S i_{L2}$ as shown in Figs. 1 and 2. $r_S i_{L1}$ and $r_S i_{L2}$ were thereby analogically compared with the DAC ramp outputs to turn OFF the transistors as described in Section II-A of this article.

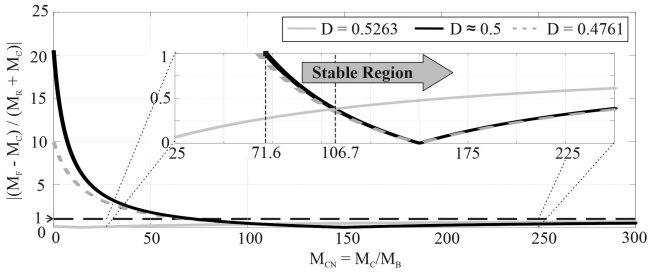


Fig. 4. Constrain equation trajectories for $L_r = 82.2$, $L_{\rm com} = 7$ μH, $V_O = 350$ V and the duty cycle operating range of the converter, $0.476 < D < 0.526$.

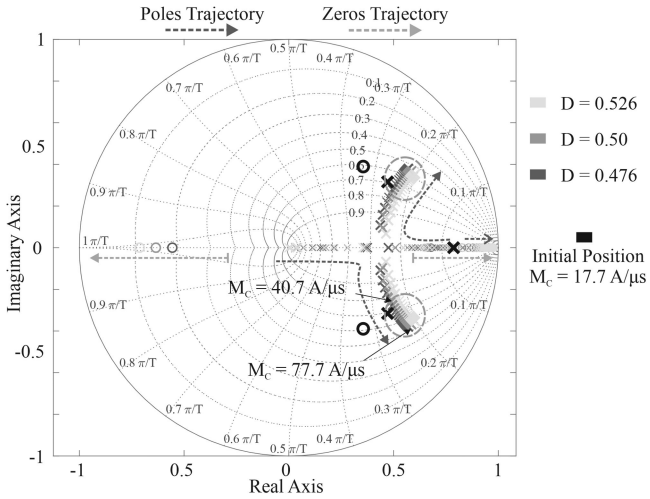


Fig. 5. Root-locus of the poles and zeros trajectory of the closed-loop control to the output transfer function, $V_O(j\omega)/V_{\rm iref}(j\omega)$, for increasing M_C values for the three critical duty cycle conditions.

B. Determination of the $\rm M_C$ Compensating Slope

The M_C compensation slope can be determined using (17), the converter parameters of Table III, and the M_F and M_R slope expressions listed in Table II. Fig. 4 shows a plot of this equation for $L_r = 82.2$ and the duty cycle values of $D = 0.476$, 0.5, and 0.526, versus a normalized compensating slope ratio $M_{CN} = M_C/M_B$, where $M_B = V_o r_s/L_{\rm com}$, which was ranged from 0 to 300. A magnification of (17) from 0 to 1 is shown inset Fig. 4, being M_{CN} enclosed from 25 to 250, which initially suggested a minimum M_{CN} value of 71.6% required as a design constrain, such that this was considered critical for the analysis of the compensated closed-loop converter behavior; however, a suitable value of the compensated slope was determined as $M_{CN} = 106.7\%$, or $M_C = 17.7$ A/μs, such that (17) at this point has the lowest values for the duty cycle range condition.

Another stability criterion used to choose a suitable M_C value is through the root-locus map depicted in Fig. 5, which shows the pole-zero trajectories of the closed-loop control-to-output transfer function, $V_O(j\omega)/\nu_{\rm iref}(j\omega)$, obtained from (16). The pole-zero trajectories plot ranges from 17.7 A/μs, in black symbols, to 77.7 A/μs for the D conditions of Fig. 4, having a 2 A/μs, M_C increasing step. The characteristic zeros stay on the real axis as M_C increases, being the right zero canceled with one real pole while the two remaining poles settle at complex conjugates neighborhoods when M_C becomes greater than 40 A/μs and fixing these poles when $M_C \geq 77.7$ A/ μs. The latter means that the converter settling time decreases as M_C increases ensuring converter stability for any duty cycle condition. In this work, it was judged that $M_C = 50$ A/μs was a suitable value for the digital ramp implementation in the microcontroller to ensure a fast transient response.

C. Verification of Steady-State Operation

Preliminary experimental results were obtained using the prototype rig to verify the operation of the circuit in steady-state conditions at full load within the duty cycle range. Fig. 6(a) and (b) shows a straightforward comparison of the experimental measurement and numerical estimation results of the $i_{\rm Ldiff}$, $i_{\rm Lcom}$, i_{L1}, and i_{L2} waveforms in steady-state having a supply voltage and peak current control reference set at 385 V, 202.6 A and 315 V, 222.7 A, respectively, in both figures, and having a 350-V, 30-kW constant load. The numerical estimation was performed using a fourth-order Runge–Kutta algorithm solution, implemented in MATLAB, with a 266-ps step, such that the large-signal model of (1) and the constraint equations of (7) and (8) were solved in 800 μs per switching period of simulation utilizing a 2.5-GHz Intel Core i5 processor. $i_{\rm Lcom}$ and $i_{\rm Ldiff}$ were, thereby, calculated and processed in MATLAB using $i_{\rm Lcom} = i_{L1} + i_{L2}$ and $i_{\rm Ldiff} = (i_{L1}\text{-}i_{L2})/2$ with the measured i_{L1} and i_{L2} data [7]. The measured waveforms closely agree with the numerical estimation, which approximately converged to the same steady-state operating point $(\mathbf{x}_{DC}, \boldsymbol{p}_{DC}, \boldsymbol{t}_{DC})$ of the experiment, as detailed in Section V. The latter was numerically confirmed using the same Runge–Kutta algorithm to analyze the instantaneous duty cycle behavior of transistors Q_1 and Q_2, D_1 and D_2, as presented in Fig. 7(a) and (b) for $V_S = 385$ V and 315 V, respectively. In these figures, both duty cycles closely converge to 0.476 and 0.526, which correspond to the expected duty cycle range predicted in Section IV-A. Slight high-frequency overshoots are noticeable in the measured i_{L1} and i_{L2} waveforms of Fig. 6, which were thought to be caused by the semiconductors hard switching and the effect of small stray inductances.

D. Verification of Dynamic Operation

Fig. 8(a) and (b) shows Microcap simulation result responses of i_{L1}, $i_{\rm Lcom}$, $i_{\rm Ldiff}$, and v_O, straightforwardly contrasted to sampled-data results of the model of (14), for two $v_{\rm iref}/r_S$ current reference steps respective to the 385-V and 315-V supply voltage cases. This comparison demonstrates that the model closely predicts the transient response of the currently controlled converter and the selected compensating ramp slope, ensuring stability at the respective operating point, since the cycle-by-cycle, sample-datapoints, marked with "$*$" symbols, match the simulation results traced in dark gray. The estimated steady-state duty cycle, output voltage and power, and phase peak current of the predictions of Fig. 8(a) moved from 0.476 to 0.492, 350 V, 30 kW to 374 V, 34 kW and 90 A to 97 A, respectively, whereas the latter parameters for Fig. 8(b) changed from 0.526 to 0.538, 350 V, 30 kW to 367 V, 33 kW and 99 A to 108 A. The i_{L1} sampled-data points of the first row of Fig. 8 were determined using $i_{L1} = i_{\rm Lcom}/2 + i_{\rm Ldiff}$, which are shown together with the

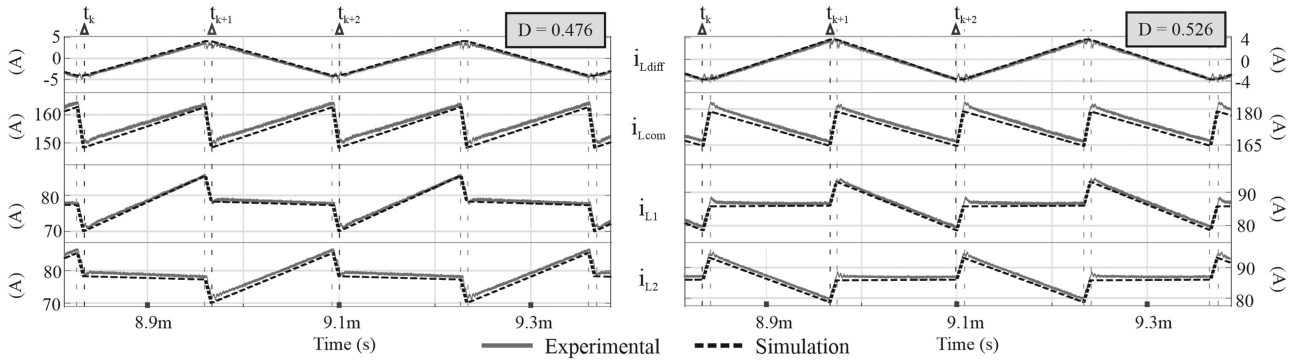


Fig. 6. Experimental and large signal model current waveforms, i_{Ldiff}, i_{Lcom}, i_{L1}, and i_{L2}, $M_{CN} = 106.3\%$, 30 kW. (a) $V_S = 385$ V, $D = 0.476$, and $v_{\mathrm{iref}} = 202.6$ V. (b) $V_S = 385$ V, $D = 0.476$, and $v_{\mathrm{iref}} = 222.7$ V.

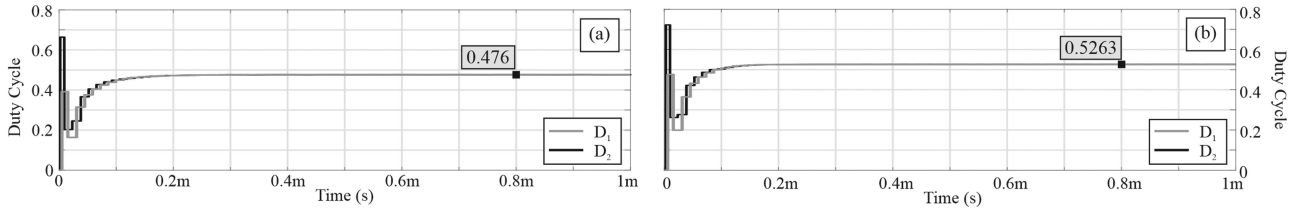


Fig. 7. Instantaneous duty cycle behavior, D_1 and D_2 for Q_1 and Q_2, for experiments presented in Fig. 8.

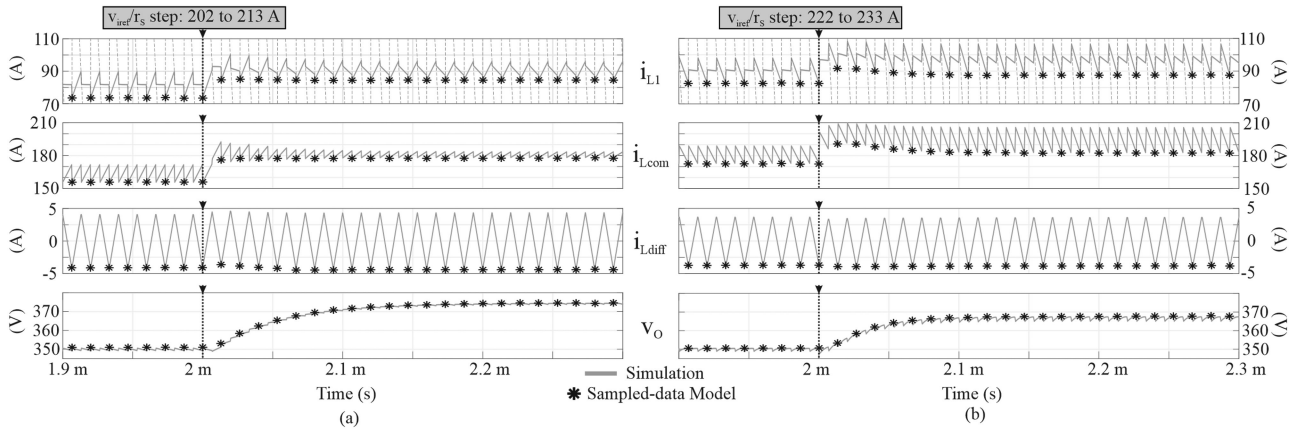


Fig. 8. Straight forward comparison between simulation and sampled-data model for a $v_{\mathrm{iref}}/\mathrm{r_s}$ current reference step at 2 ms, with $M_{CN} = 106.3\%$. (a) $V_S = 385$ V, $D = 0.476$, 34 kW. (b) $V_S = 315$ V, $D = 0.526$, 33 kW.

M_C compensating ramp depicted in dashed gray lines. i_{Lcom} and i_{Ldiff}, in the second and third rows of Fig. 8, reflects the predicted triangular ripples that become reduced when the duty cycle is near to 0.5, producing a virtual null ripple in i_{Lcom}. Finally, Fig. 8 shows the fast response of v_O to the current reference steps, becoming the output voltage virtually free of ripple when the duty cycle approaches 0.5.

Fig. 9(a) shows a large-time scale response of the experimental and ideal simulated i_{Lcom} and v_o waveforms, plotted in black and dark gray and gray, to a 355-to-386 A, v_{iref}/r_S current reference step at 0 ms with a 315 V supply. The measured duty cycle, output voltage and power, respectively, moved from 0.5 to 0.526 and from 315V, 23 kW to 350 V, 29 kW.

The measured i_{Lcom} revealed a subharmonic oscillation, particularly near to 800 Hz, which, ideally, the controlled converter of Fig. 1 should produce an i_{Lcom} flat step response, as shown in Fig. 9(a). The disappointing dynamic response of i_{Lcom} was attributed to the output impedance of the electronic power supply since, according to the manufacturer, the power source has a *LC* output filter with a corner frequency near the measured subharmonic oscillation. A Microcap simulation was performed with an equivalent 800 Hz *LC* filter placed between the voltage supply and the converter of Fig. 1, such that the subharmonic oscillation was confirmed by straightforward comparison of the i_{Lcom} waveform of this simulation, plotted in dashed lines in Fig. 9(a), with the measured data.

Further insight analysis between the measured and simulated i_{Lcom} waves of Fig. 9(a) also revealed an HF cycle-by-cycle discrepancy, as shown in the square inset Fig. 9(a) that corresponds to a small period before the v_{iref}/r_S step. On one hand,

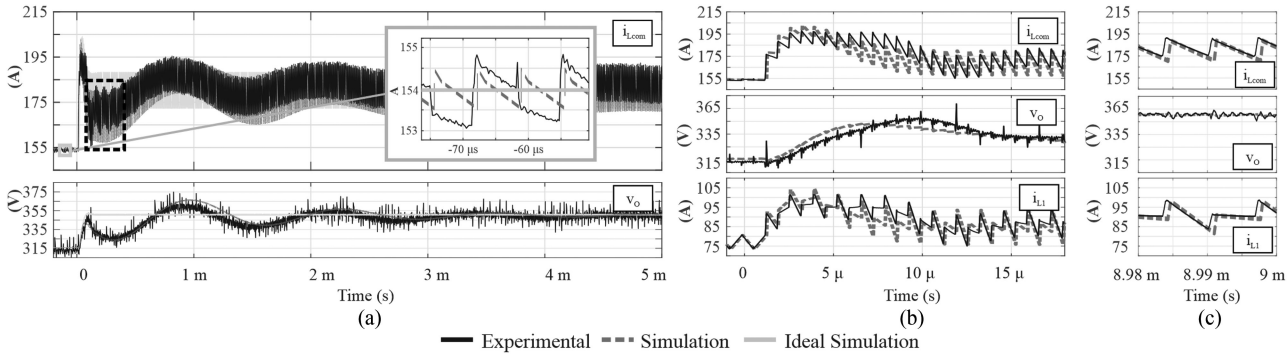


Fig. 9. Transient response to a v_{iref}/r_S current reference step from 385 to 386 A at a supply voltage of 315 V and $M_c = 50$ A/μs. (a) Large-time step response i_{Lcom} and v_o waveforms. (b) i_{Lcom}, v_o, and i_{L1}waveforms at the transient instant. (c) i_{Lcom}, v_o, and i_{L1} waveforms at steady-state operation after transient response.

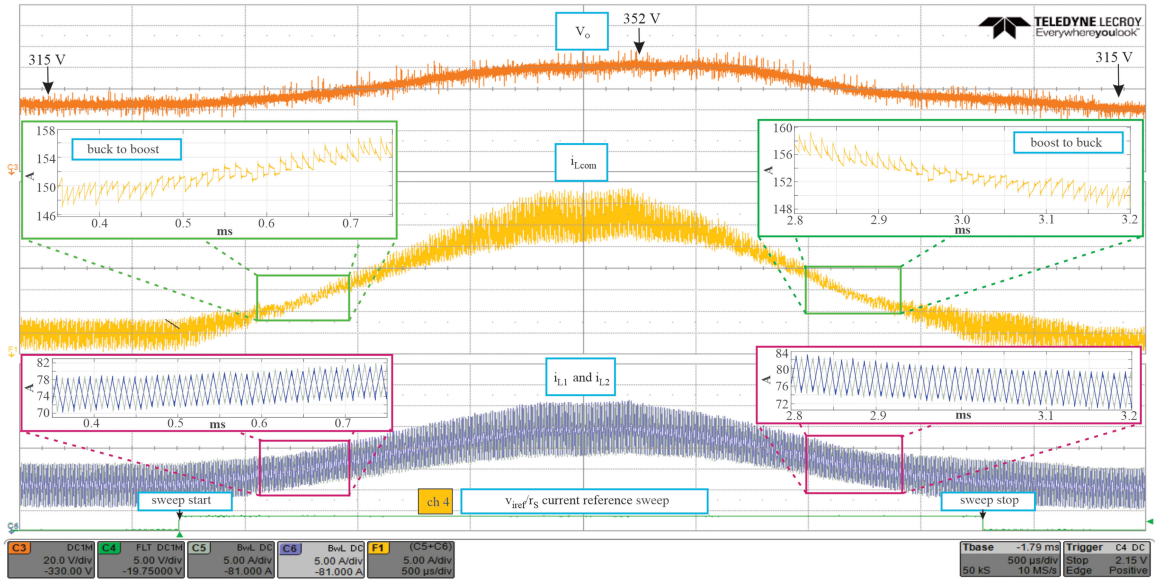


Fig. 10. V_{iref}/r_S sweep experimental waveforms with a constant voltage $V_S = 330$ V, and a constant load $R = 4.21\ \Omega$. v_O (20 V/div, offset of -330 V), i_{Lcom} (5 A/div, offset of -162 A), i_{L1} and i_{L2} (5 A/div, offset of -81 A) at 500 μ/div.

the ideal i_{Lcom} has a null ripple since $D = 0.5$; however, the i_{Lcom} measurement shows a 2-A ripple, which was thought to be produced by the IPT core loss. This was confirmed including an estimated 43 W core loss, described in [7], in the performed Microcap simulation with the *LC* supply filter, as two 600-Ω resistors connected in parallel with L_1 and L_2, whereas, after the control step, this ripple is imperceptible in i_{Lcom} due to the expected L_{com} ripple when $D \neq 0.5$. On the other hand, the i_{Lcom} experimental waveform shows 0.5 A, HF overshoots attributed to the transistor hard switching. The discrepancies noticed in the dashed square shown in i_{Lcom} of Fig. 9(a) were attributed to the presence of stray elements in the experimental resistive arrangement load.

A straightforward comparison between the experimental and simulated waveforms results of i_{Lcom}, v_o, and i_{L1} is depicted in Fig. 9(b) and (c) for transient and steady-state operation points, respectively, which closely agree in these figures confirming the accuracy of the simulation model.

v_{iref}/r_S was experimentally ranged from 333 to 373 A and backward, with a 1.1 A step per switching cycle, to verify a smooth buck-to-boost and boost–buck mode transitions of the converter operation. The resultant v_o, i_{Lcom}, i_{L1}, and i_{L2} waveforms are shown in the oscilloscope screen capture of Fig. 10 together with a digital signal to point the start and end of the v_{iref}/r_S sweep. The prototype was supplied with a 330-V source and a 4.21-Ω constant load. v_o is shown at the first plot of Fig. 10, which reflects a clear sweep visualization of v_o between 315 V and 352 V corresponding to a duty cycle range of $0.488 \leq D \leq 0.516$. The second and third plots depict the sweeping of i_{Lcom} and i_{L1} and i_{L2}, respectively, showing the transition between the converter modes in the magnification squares inset of Fig. 10. The top magnification squares depict a smooth shape transition of the i_{Lcom} waveform, along with the rising and falling sweep slopes, having the predicted periodic shapes in Fig. 2, although it is seen again that the small ripple is present when D is close to 0.5, as described for Fig. 9(a). The bottom magnification squares

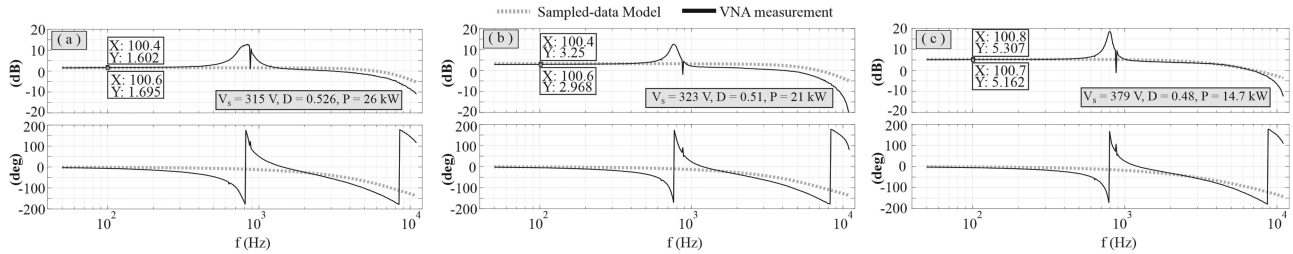


Fig. 11. Model and experimental measurements of the $V_O(j\omega)/V_{\mathrm{iref}}(j\omega)$ control-to-output response. (a) $P = 26$ kW. (b) $P = 21$ kW. (c) $P = 14.7$ kW.

demonstrate an appropriate IPT current balance, proving good performance of the mixed-signal based controller.

V. Frequency-Response Verification

Fig. 11 shows the experimental frequency-response measurements, using a Keysight E5061B Vector Network Analyzer (VNA), of the control-to-output transfer function $V_O(j\omega)/V_{\mathrm{iref}}(j\omega)$. The prototype rig was operated with different loads and supply voltages while v_{iref} was adjusted to produce a constant output voltage of $V_O = 350$ V. Fig. 11(a) shows the VNA extracted data of the measured V_O/V_{iref} frequency response of the converter operating with a 315-V supply and a 26-kW output power, which caused convergency of the duty cycle to $D = 0.526$. The same process was used to obtain the measured results plotted in Fig. 11(b) and (c) for 21 kW with $V_S = 323$ V and 14 kW with $V_S = 379$ V, which caused D to converge to 0.52 and 0.48, respectively.

The steady-state operating vector $\mathbf{x}_{\mathrm{DC}}$ is required in the calculation of (17), which can be determined using a numerical iterative approach or the phase-plane method, as reported in [15], [16], and [31]. It was judged in this article that an iterative process, like the one described in Section IV-C for Fig. 7, was a straightforward method to determine $\mathbf{x}_{\mathrm{DC}}$ as detailed below.

First, the converter simulation was initialized with null conditions for a specific $\tilde{\boldsymbol{p}}$ input vector. This is shown in the 3-D graph of Fig. 12(a), where $\mathbf{x}_k$ is plotted from null conditions until this vector reaches a steady-state value close to the reported in the experimental conditions of Fig. 11(a). In Fig. 12(a), every switching period end is marked with "$*$" symbols showing the main trajectory of $\mathbf{x}_k$ while the inset magnification depicts the trajectory convergency to the steady-state point. The found steady-state vector $\mathbf{x}_{\mathrm{DC}}$ was used to satisfy one of the constrain equations, (8) or (9), depending on the duty cycle condition. For example, alike the vector trajectory shown in Fig. 12(a), a dual duty-cycle discrete-time trajectory is plotted in Fig. 12(b), which corresponds to the same state-vector behavior shown in Fig. 12(a), but tracing D_1 and D_2 respective to the axis time. In this figure, both D_1 and D_2 settle close to 0.526, as shown in the cubic approach inset of Fig. 12(b), which indicates that the system reached equilibrium. At this steady-state point, where the frequency-response measurement of Fig. 11(a) was performed, constraint (9) was used to thereby determine the small-signal matrices of (15). Second, after the later process was done, the presented frequency responses in Fig. 11 were determined using expression (16) for the specific operating points of the experiments, such that the $V_O(j\omega)/V_{\mathrm{iref}}(j\omega)$ frequency responses

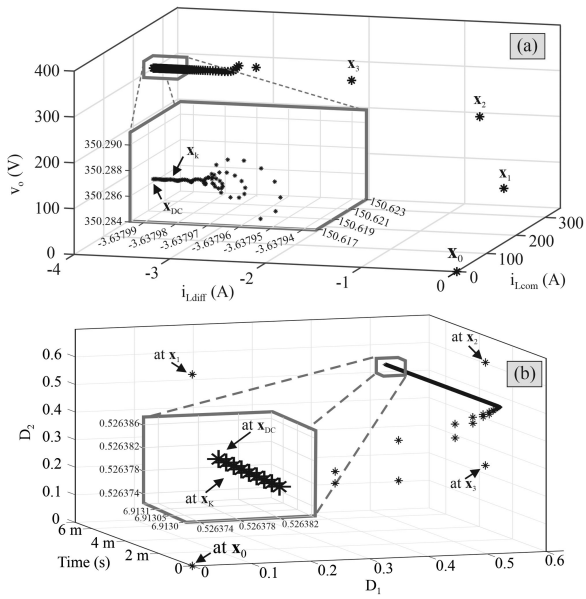


Fig. 12. $\boldsymbol{x}_{\mathrm{DC}}$ determination. (a) Plane trajectory of $\boldsymbol{x}_{\boldsymbol{k}}$ for experimental conditions of Fig. 11(a). (b) Plane trajectory of the duty cycles at $\boldsymbol{x}_{\boldsymbol{k}}$ for the experimental conditions of Fig. 11(a).

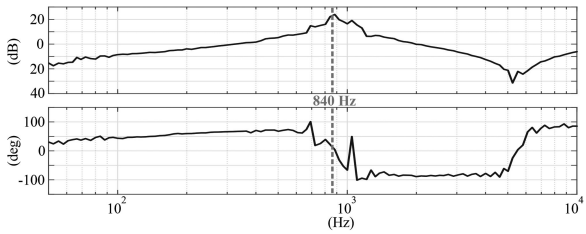


Fig. 13. Output-impedance frequency response of the power supply.

of Fig. 11 show the numerical responses obtained with the above description in contrast of the measured responses.

The comparison of the experimental data and model predictions shown in Fig. 11(a)–(c) closely agree between each pair of traces for the output powers of 26, 21, and 14 kW, respectively. The presence of a resonant peak in the magnitude plots was attributed to impedance interaction [29], [32], [33], mainly between the characteristic input impedances of the converter and the supply output impedance, which was measured as shown in Fig. 13 revealing an 840-Hz corner frequency. Fig. 11 shows that the control-to-output, low-frequency response magnitudes nearly match between the numerical prediction and the measured results, being the discrepancies below 0.3 dB, but with an increment of the resonant peak magnitude as the load is reduced

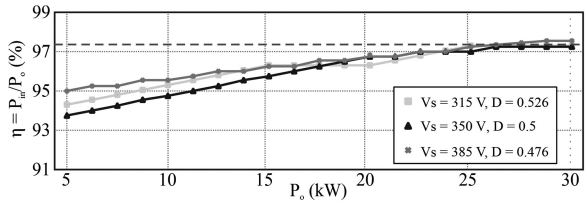


Fig. 14. Prototype measured efficiency ranging the load from 5 to 30 kW.

while after the resonant peak frequency, the comparison slightly matches due to the model accuracy.

VI. Efficiency of the DC–DC Converter

The converter efficiency curve is presented in Fig. 14, depicting the three main duty cycle conditions in the CCM throughout a load range of 5–30 kW, with a 350 V $\pm$ 10% supply and a 350-V output, as listed in Table III. The measured efficiency was realized with a 16-b high-performance power analyzer. A deeper insight into the converter estimated losses in CCM operation is detailed in [7].

VII. Conclusion

A sampled-data technique is a suitable strategy to obtain the small-signal model of a dual interleaved buck–boost converter with a PCM control scheme. The dynamic behavior of the differential and phase currents of the converter IPT are analyzed and predicted using this modeling technique taking advantage of the symmetry nature of its resultant configurations. The stability limits of the converter with the PCM strategy were analyzed in this article, confirming that the L_r inductance ratio and the duty cycle establish the boundaries of stable operation. The analysis done in this article aids to confer that $L_r > 4$ compromises the stability region of the dual interleaved topologies of dc–dc converters with PCM.

A method to determine the minimum compensating slope for the PCM control scheme of the dual interleaved buck–boost converter was described and resumed in a plot for different trajectories relative to the duty cycle boundaries, being 50 A/μs, the appropriate slope for this converter with a 32-kW power rating. Experimental results verified the steady-state operation of the converter and the effectiveness of the calculated ramp slope contrasted with numerical predictions. Experiments also revealed that the IPT power losses increase the amplitude of the common inductor current ripple that was not predicted by the model.

The presented iterative approaches to obtain the steady-state operating point for this circuit are practical and suitable for the sample-data modeling exposed in this article since these supported verification of the reference step and frequency-response experiments by numerical predictions. Frequency response measurements of the control-to-output transfer function confirmed the validity of the transfer functions but exhibiting the impedance interaction between the supply and converter.

Despite the resulting limitation of the inverted output voltage for this type of dc–dc, buck–boost converter, the sample-data model and the presented analysis support a high degree of dynamic reliability, mainly due to the reduced number of active devices and its simple control system, which confer attractive indexes of performance, efficiency, and power density, desirable characteristics for electromobility.

Future work with this high-density converter with PCM will expand the power flow to a bidirectional capability, a desirable feature for electric vehicles that utilize supercapacitors and/or high-density batteries. Also, the dynamic current tracking performance within an electric vehicle is an expected aim to be examined in the time ahead.

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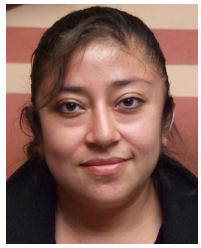

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