RPEM: Design and Realization of Reconfigurable Power Electronic Modules

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***Abstract*—A series of novel externally reconfigurable power electronic modules (RPEMs) are invented to increase the flexibility of power modules and their application purposes. In this article, the concept of RPEMs, their switching arrangements, and power-module-based architectural design are demonstrated. An RPEM is then designed, analyzed through simulations, and compared with the conventional fixed-configuration power electronic modules. The sizes of the power modules and used power terminals are kept similar to avoid any differences in power loop inductance values solely due to various trace pad sizes. In addition, similar gate/source pads and signal pins are used for all of the designed power modules to have constant switching dynamics in all modules. The comparison results show that the internal parasitic inductance and performance are still comparable with the conventional modules despite having high configurability. The designed RPEM and a conventional full-bridge (FB) power module are fabricated and characterized. The experimental tests show that the difference between the overshoot voltages on both RPEM and FB power modules is less than 2%. Such flexibility without compromising the power module performance decreases the engineering time for designing different power modules for various power electronic converters; hence, the production speed can be improved while decreasing the overall module cost.**

***Index Terms*—Active neutral point clamped, full-bridge (FB), half-bridge (HB), hybrid neutral point clamped (HNPC), reconfigurable power electronic module (RPEM), T-inverter.**

I. Introduction

HIGH power density [1], [2], high voltage capability [3], and high efficiency [4] are today's trends in power electronics. The advent of wide-bandgap (WBG) devices has pushed researchers to improve power module packaging technology. Efforts on reducing the module internal stray inductance values [5], utilizing novel cooling methodologies [6], and increasing the voltage capability in the confine of power module packages [7] prove that research has mostly focused on improving the thermal and electrical performances of power modules to further help the system-level design requirements. As the research in power electronics moves forward, novel power electronic topologies emerge to meet the power density, voltage capability, and efficiency requirements [8], [9]. Multilevel inverters have gained increasing interest because they can handle higher voltage levels, have lower losses, achieve higher reliability, and, most importantly, have smaller output filters in comparison with the conventional two-level inverters because of harmonic suppression in their stepped output voltages [10], [11].

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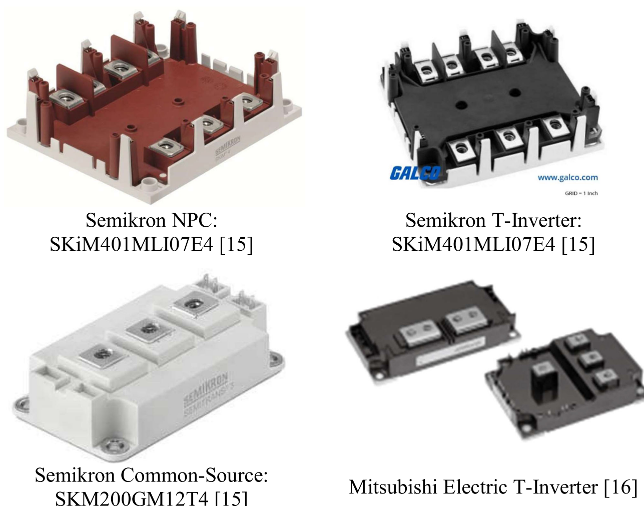


Fig. 1. Commercially available IGBT-based power modules with different switching arrangements.

Improvement of power module packaging for WBG devices is becoming critical. Yet, the focus is on half-bridge (HB) switching arrangements; in fact, not many types of research have been performed on module switch arrangements for other inverter topologies. Commercially available power modules suitable for multilevel inverter topologies are very limited. For instance, the bidirectional, T-inverter, and neutral-point-clamped power modules either rarely exist or can be designed and made upon a customer's order, which may end up being costlier than the HB power modules available on the market. According to a 2015 report, the most expensive parts of power control units in electric vehicles are the power modules with 39% of the overall traction inverter cost using Si insulated-gate bipolar transistor (IGBT)-based designs [12]. This cost percentage can be even higher according to the engineering design and fabrication process.

Fig. 1 shows some of the IGBT-based commercially available power modules other than the HB and full-bridge (FB) topologies. Infineon's EconoDUAL 3, EconoPACK 4, and Easy lines are power modules for the three-level inverters. Microsemi,

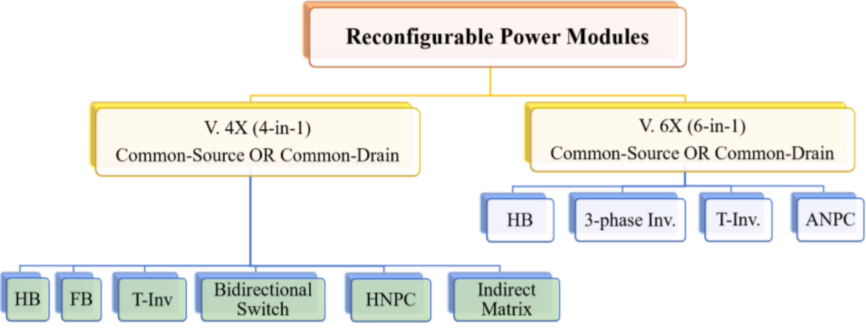


Fig. 2. Hierarchy of the RPEM series.

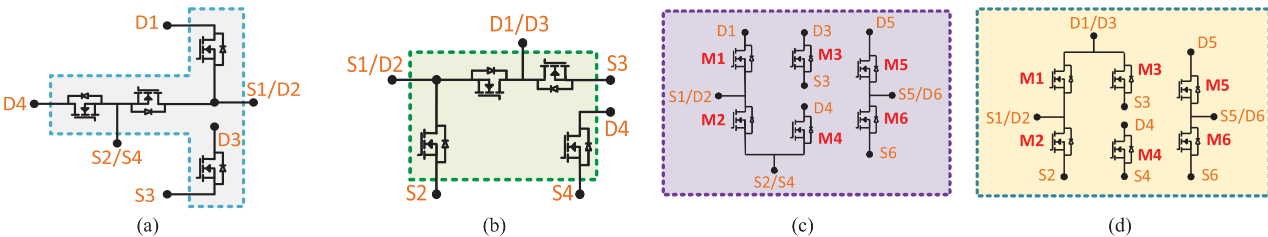


Fig. 3. RPEM switching arrangements. (a) Common-source 4X. (b) Common-drain 4X. (c) Common-source 6X. (d) Common-drain 6X.

Semikron, and Mitsubishi Electric also offer power module structures for dc choppers and multilevel inverters [13]–[17].

In this article, a series of unique switch arrangements are proposed to enable the capability of using a power module in different converter topologies, providing both compactness and freedom in converter design. As such, these reconfigurable power electronic modules (RPEMs) reduce production and engineering costs and accelerate high-volume production procedures.

II. Switching Arrangements in RPEMs

The hierarchy of the RPEM series is described in Fig. 2. Two series of switching arrangements are designed to enhance the flexibility of the power module applications. These two series are defined by the number of switching positions, 4X or 6X. The versions 4X and 6X are 4-in-1 and 6-in-1 modules, respectively. The numbers 4 and 6 are derived from the division of the number of switches required for a power electronic converter to the number of the switching positions in a power module, which obviously should be an integer and either equal to or larger than 1. For instance, to build a converter topology with six switches, three power modules with two or a single module with six switches are required. It is not possible to use a power module with four or eight switching positions to build such a power electronic converter. Hence, two different series of RPEMs are proposed to be able to cover more power electronic converter topologies.

The possible switching arrangements for the 4X series are shown in Fig. 3(a) and (b), and the switching arrangements related to the 6X series are provided in Fig. 3(c) and (d). Both 4X and 6X versions can be configured as a common-source or a common-drain architecture, which means they can either have a common-source or common-drain node in their switching arrangements. As such, the configurations shown in Fig. 3(a) and (c) have a common-source node, S2/S4, and the configurations shown in Fig. 3(b) and (d) have a common-drain node, D1/D3. Moreover, all the switching configurations have a floating switch, i.e., M3 in the common-source or M4 in the common-drain configurations.

The 4X version has six power terminals, while the 6X version has nine power terminals. All the power electronic converter topologies provided in Fig. 2 can be built using these 4X and 6X RPEMs with suitable interconnections/busbars for their power terminals.

Figs. 4 and 5 list the power electronic topologies that can be built using the 4X and 6X common-source RPEMs, respectively.

Although the bidirectional devices on the T-inverter topology could have a lower voltage rating in comparison with its HB leg, the recent improvements in SiC have resulted in increased availability of high-voltage SiC devices. For instance, there are many 1200-V SiC bare die commercially available in comparison with 600-V SiC bare die. Hence, considering the availability, the voltage rating is not a limiting factor as much as the current rating is. Moreover, new generations of SiC semiconductor devices come with intrinsic diodes that eliminate the need for extra Schottky diodes. The bidirectional switches of T-type inverters can be either common drain or common source. This bidirectional switch can be determined by the configuration of the utilized power module. For example, the bidirectional switches will be common source if their power modules are selected from the common-source series.

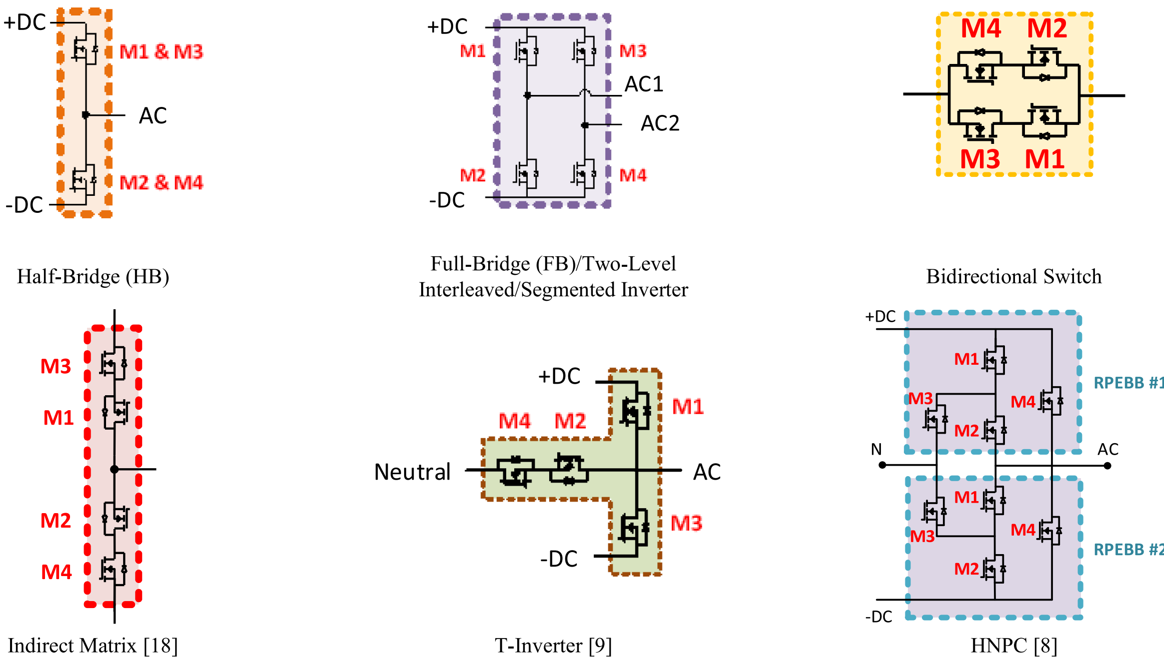


Fig. 4. Topologies that can be built by the 4X common-source RPEM.

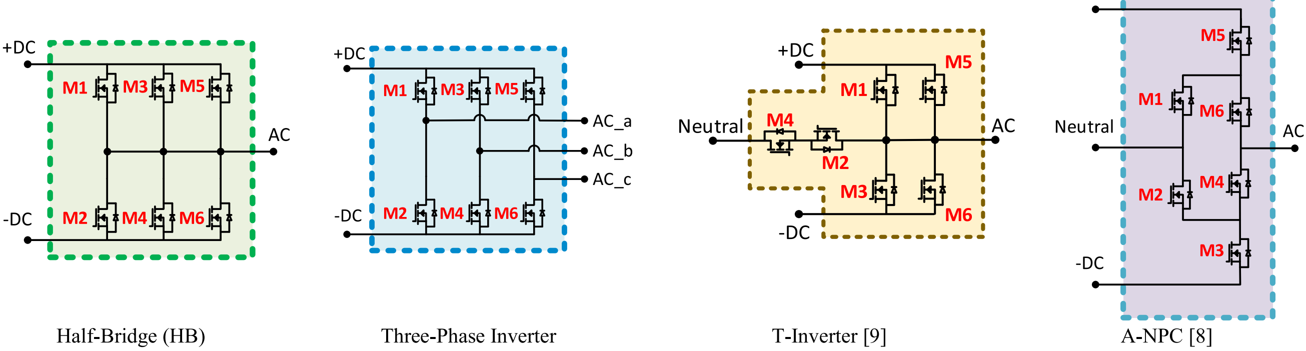


Fig. 5. Topologies that can be built by the 6X common-source RPEM.

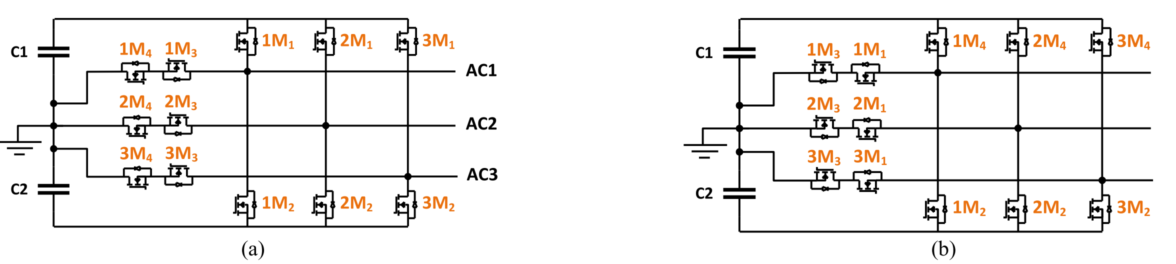


Fig. 6. Three-phase T-type inverters with (a) common-source and (b) common-drain RPEMs.

Fig. 6 shows the common-source and common-drain three-phase T-type inverters that are designed using externally RPEMs shown in Fig. 3(a) and (b). In a three-phase T-type inverter, a common-drain configuration might be preferred because of fewer isolated gate driver supplies required in a common-drain mode in comparison with a common-source mode. In a common-source mode, nine isolated gate driver supplies are needed: six for the conventional six-switch inverter part and an additional three for the common-source bidirectional switches. In a common-drain mode, only seven isolated gate driver supplies are required because three switches will have a common source at the dc-link capacitor neutral node, $1M_3/2M_3/3M_3$, and the top switches will have common sources with the other three bidirectional switches, $1M_4/1M_1$, $2M_4/2M_1$, and $3M_4/3M_1$ [9].

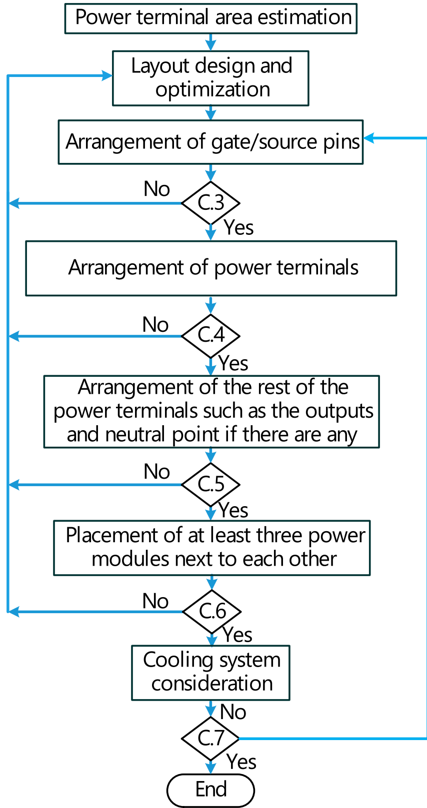


Fig. 7. Design flowchart of RPEM [19].

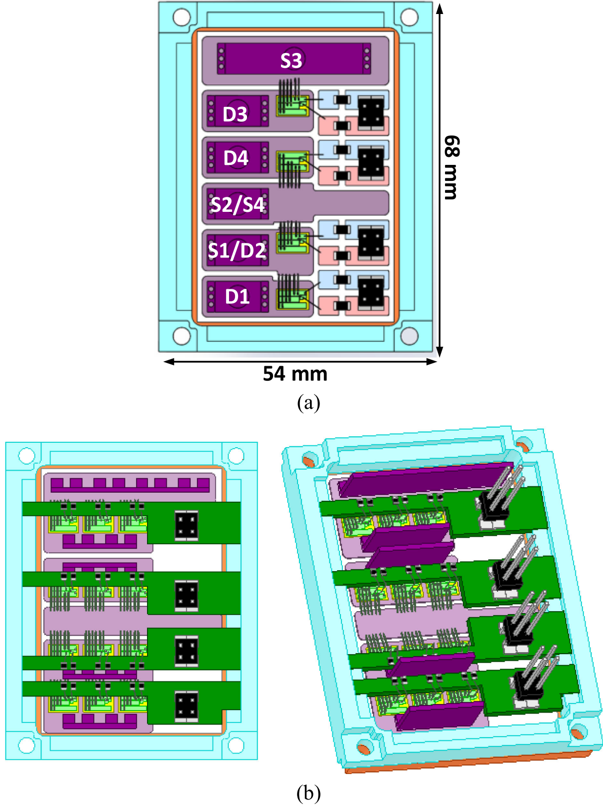


Fig. 8. Designed 4X common-source RPEM. (a) Single die per switching position. (b) Three parallel die per switching position.

TABLE I
POWER TERMINAL FUNCTIONS IN A 4X RPEM IN DIFFERENT POWER ELECTRONIC SYSTEM TOPOLOGIES

		D1	S1/D2	S2/S4	D3	S3	D4
Half-Bridge		+DC	AC	-DC	+DC	AC	AC
Full-Bridge		+DC	AC1	-DC	+DC	AC2	AC2
T-Inverter		+DC	AC	-	AC	-DC	Neutral
HNPC	(1)	+DC	-	AC	-	Neutral	+DC
	(2)	-	-	-DC	Neutral	AC	-
Indirect Matrix		-	AC	-	-	-DC	+DC
Bidirectional		-	-	-	-	-	-

III. RPEM DESIGN PROCEDURE

Fig. 7 provides a design flowchart for terminal arrangement of the RPEM and is explained in detail in the following. To experimentally verify the concept of the RPEM, a 4X common-source version is designed, as shown in Fig. 8(a). The designed RPEM measures 54 mm $\times$ 68 mm, even though any module size can be adapted to suit different applications.

A. *RPEM Terminal Arrangement and Busbar Design*

The version 4X RPEM has two additional power terminals compared to a conventional FB power module. More importantly because of the versatility of the RPEM, the function of each terminal can change according to the converter topology that it is being used for. Table I presents the functions of each terminal in different power electronic system topologies. As shown in Fig. 4, two 4X RPEMs are required for each leg of a hybrid neutral-point-clamped (HNPC) topology. Table I presents these two power modules with numbers (1) and (2) in the HNPC row.

The terminal arrangement of the RPEM takes into account the external busbar of the power electronic topology as well. In addition, in a system-level design, the placement of the power modules affects the placements of the dc-link capacitors, gate driver board, power supply, and load. As such, these terminals should be designed to accommodate all the aforementioned power electronic topologies. The power module internal stray inductance, external busbar inductance, and system power density are carefully considered in designing this RPEM to make it compatible with all the power electronic topologies mentioned in Fig. 4 [19]. Fig. 7 shows the design flowchart.

Conditions C.3–C.7 in Fig. 7 are defined as follows.

1) *C.3:* A distance between gate driver pins and connection busbars is needed. The gate signal pins should not surround the power terminals to achieve optimized system busbar design.
2) *C.4:* After considering creepage and clearance, +DC and −DC terminals should be arranged as close as possible to each other to have the maximum minimizing mutual inductance.
3) *C.5:* Terminals that should be attached together in an RPEM to create the required switching arrangement are better to be in close proximity to each other to reduce the path inductance.

4) *C.6:* Power terminal connection of several power modules in multiphase systems should be considered.
5) *C.7:* Coolant system and its inlet/outlet arrangement regarding the power module design.

As mentioned before, the terminal arrangements in the RPEM shown in Fig. 8(a) are designed simultaneously with the external busbar and power electronic system design to ensure its applicability for all power electronic system topologies shown in Fig. 4. The power module terminals shown in Fig. 8(a) are arranged in a gamma (Γ) shape. The ac or output terminal is along the longer edge of the module as the length of these output busbars does not affect the power electronic system performance [19]. The gate driver pins are placed at the opposite side of the output terminal to mitigate high electromagnetic interference at the center of the power path [20]. The best optimized external busbar design will be when the positive and negative terminals are arranged next to each other to create the largest minimizing mutual inductance between the system busbars [19]. In the power module design shown in Fig. 8, these terminals are positioned as close as possible to each other considering all six power electronic converters mentioned in Table I. The arrangement of these two power terminals is a compromise between the power module internal inductance and its output busbar inductance.

As shown in Table I, D1 is mostly the positive terminal (DC+), while S2/S4 is its negative pair (DC–). These power terminals are all placed alongside each other to create laminated busbars and achieve the maximum minimizing mutual inductance possible. Hence, terminal D1 is placed as close as possible to the shorter edge of the power module to connect to the dc-link capacitor bank with the shortest busbar possible.

It is important to note that in some topologies, D3 is also a positive terminal and must be connected to D1. In an ideal case, these two power terminals would be as close as possible to each other to create the shortest positive busbar, but a compromise is needed to design a power module with the lowest internal inductance and an optimized overall size as well. To compensate for this matter, the negative power terminal, S2/S4, is placed in the middle of these two positive terminals to minimize the busbar inductance with a large mutual inductance. S3 terminal is bigger than the rest of the terminals to reduce the stray inductance especially when it is used as a negative (–DC) power terminal. Hence, using the information given in Table I and an iterative design process with both the power module and power electronic system design for all six topologies, the 4X version of the RPEM is designed and optimized, as shown in Fig. 8. Such power module codesign methodology is explained in detail in [19], and the validity of the RPEM layout design is further analyzed in Section IV.

A similar power module design with three die in parallel and printed circuit board (PCB) assembly for gate/source signal pins is shown in Fig. 8(b). Symmetricity of the power terminals and signal pins with respect to all paralleled die is critical in such a power module to guarantee simultaneous turn ON/OFF of all the devices in a switching position. Wide power terminals make symmetric current distribution across the devices possible and symmetric signal loop inductances help equal turn ON/OFF dynamics. The gate signal pins use external PCBs that are

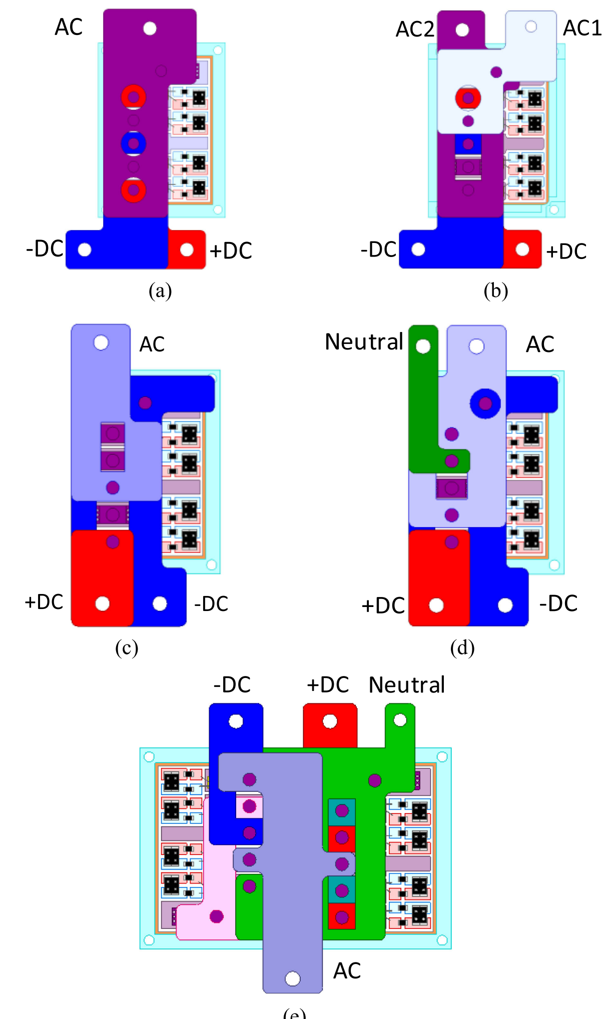


Fig. 9. Busbar designs for each topology using the designed 4X RPEM. (a) HB. (b) FB. (c) Indirect matrix. (d) T-inverter. (e) HNPC.

positioned along all the paralleled devices. Internal source/gate resistors are positioned on the PCBs, and the pins are arranged at one edge of the power module. The power terminals are widened across all the paralleled die to create a symmetrical current distribution.

Fig. 9(a)–(e) provides the detailed busbar designs for the HB, FB, indirect matrix, T-inverter, and HNPC legs built using the designed RPEM, respectively. As mentioned above, two RPEMs are needed for each switch leg of an HNPC.

Obviously, busbar design is flexible and may be subject to change according to the dc-link capacitor bank to achieve wider laminated low-inductance paths. An example of a power electronic system design with such a planar busbar and using six 4X RPEMs is provided for a three-phase HNPC system with commercially available SBE's 700A26797-245 Power Ring dc-link capacitors in Fig. 10.

B. Internal Inductance Calculation

The designed RPEM is simulated using ANSYS Q3D to evaluate its internal parasitic inductances. The node-to-node

TABLE II
INDUCTANCE VALUES FOR HB AND FB CONFIGURATIONS

Inductance Values	$L_{D1}+L_{S1}$ (nH)		$L_{D2}+L_{S2}$ (nH)		$L_{D3}+L_{S3}$ (nH)		$L_{D4}+L_{S4}$ (nH)	
	HB	FB	HB	FB	HB	FB	HB	FB
$L_{D1}+L_{S1}$ (nH)	2.9		-0.38	-0.38	-0.0024	+0.0024	-0.43	+0.43
$L_{D2}+L_{S2}$ (nH)	-0.38	-0.38	2.8		-0.006	+0.006	+0.41	-0.41
$L_{D3}+L_{S3}$ (nH)	-0.0024	+0.0024	-0.0067	+0.0067	2.9		-0.055	-0.055
$L_{D4}+L_{S4}$ (nH)	-0.43	+0.43	+0.41	-0.41	-0.055	-0.055	3.1	

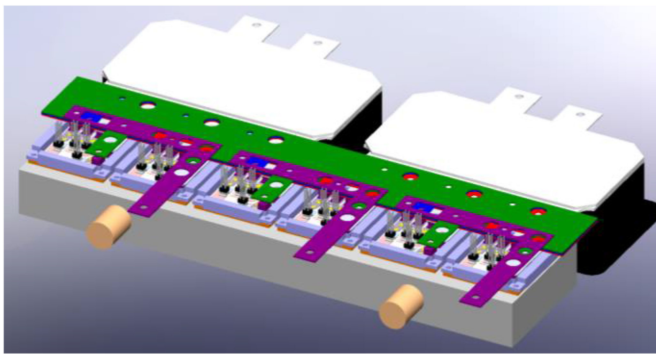


Fig. 10. Three-phase HNPC system designed using the RPEM and commercially available SBE's 700A26797-245 Power Ring dc-link capacitors.

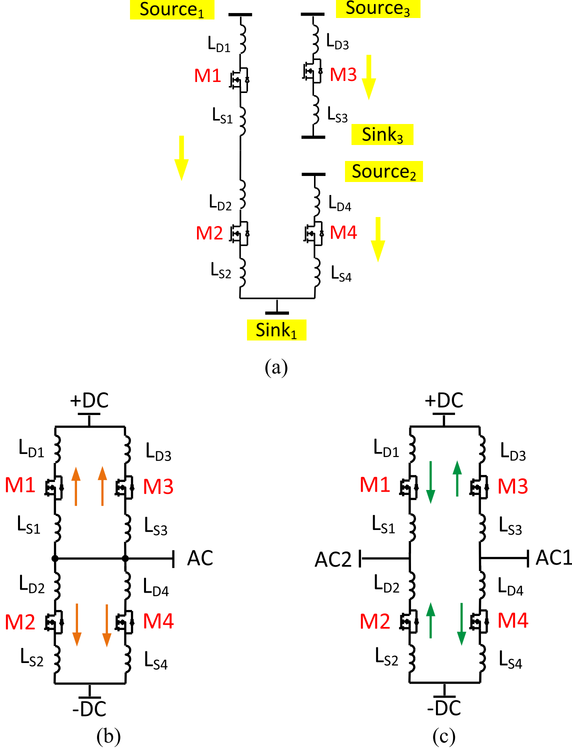


Fig. 11. (a) ANSYS Q3D parasitic inductance evaluation. (b) Current direction for HB. (c) FB topologies.

internal inductances are evaluated, and the results are provided in Table II. The source/sink and current direction considerations for the HB and FB topologies are shown in Fig. 11(a). The current directions during the *di/dt* time intervals are shown for both the HB and FB topologies in Fig. 11(b) and (c), respectively.

As shown in Table II, the current directions affect the mutual inductances. The leg inductance of an FB RPEM is 6 nH per leg, which means that the leg inductance will be 3 nH for an HB topology because in the HB mode, the two legs are paralleled to each other. The mutual inductance sign is evaluated according to the current direction during the *di/dt* time intervals [21]. It is important to note that the signs of the mutual inductances in the RPEM depend on the power module application because the switch position and the current direction are related to its system topology; hence, the node-to-node inductance values provided in Table II will help such analysis. The inductance values are simulated considering the power terminals. In addition, since decoupling capacitors cannot be embedded in this power module because of its varying positive/negative rails for different applications, the power loop inductance cannot be mitigated inside the power module.

C. Thermal Simulation of the Designed RPEM

The thermal performance of the designed RPEM of Fig. 8(a) is simulated using SolidWorks with the results shown in Fig. 12. Using CREE's CPW3-1200-0016A SiC devices, at a maximum junction temperature of 160 °C for 5000-W/m^2·K convection coefficient, the maximum current handling capability of the power module is 90 A. It is important to note that if a custom-made cooling system is being designed for RPEMs, the application of the module can affect the thermal management

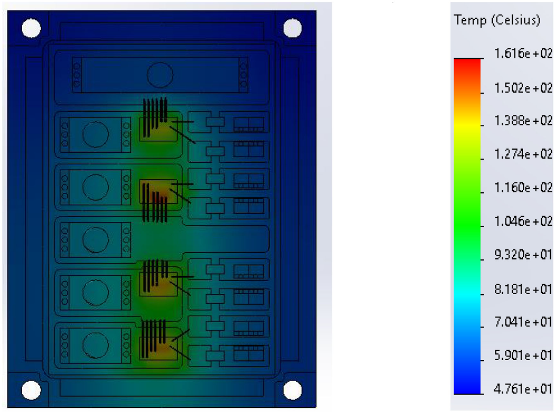


Fig. 12. Thermal simulation in SolidWorks for the RPEM with four CPW3-1200-0016A SiC MOSFETs.

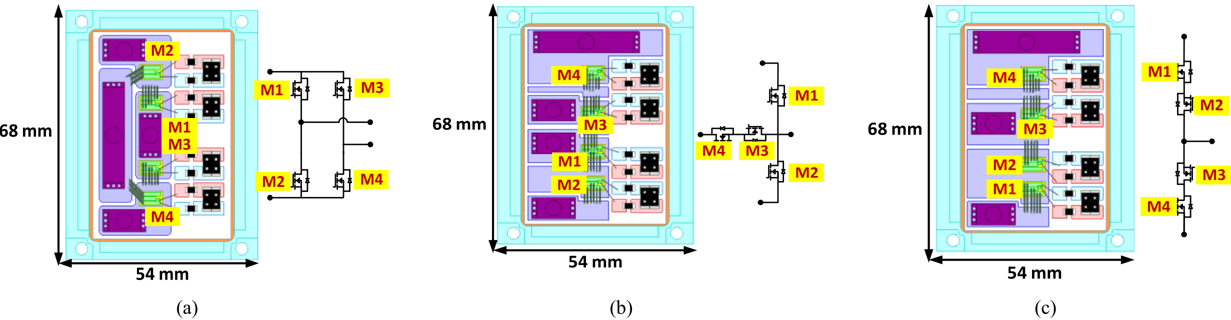


Fig. 13. Power module design for (a) FB, (b) T-inverter leg, and (c) indirect matrix leg with the same size as the designed 4X RPEM.

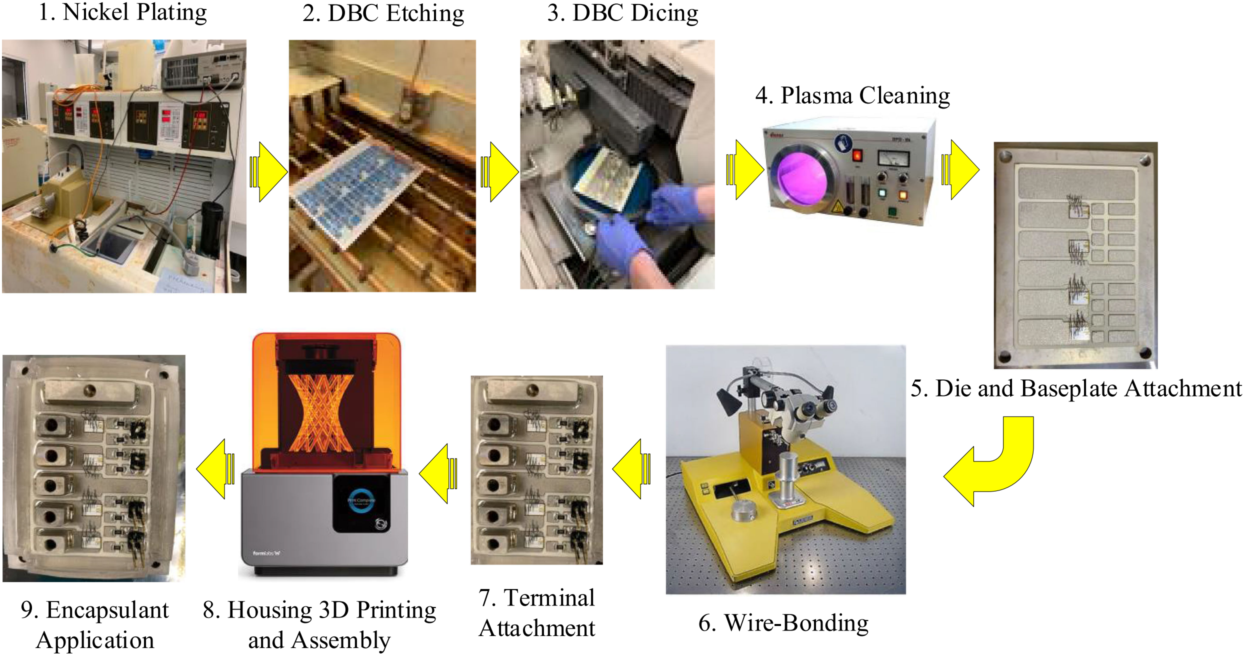


Fig. 14. Power module fabrication process sequence for the RPEM and FB power modules.

requirements. This is because, in some applications, the losses of some switches can be lower than the rest, which results in different cooling requirements for each switching position dependent on the system.

IV. Experimental Results and Comparison

To compare the RPEM with conventional fixed-configuration power modules, three modules are designed with FB, T-inverter leg, and indirect matrix switching arrangements, as shown in Fig. 13. The FB power module [see Fig. 13(a)] and the RPEM [see Fig. 8(a)] are fabricated. The switching performances of these two modules are then experimentally compared using double pulse test (DPT) analysis.

The module fabrication process sequence for RPEM and FB power modules is provided in Fig. 14. As shown in this figure, after nickel plating a direct-bond copper (DBC) power substrate, copper etching was performed on it. This is then followed by dicing the DBC substrate, plasma cleaning, and die-to-DBC attachment. After wire bonding and attachment of the power terminals and signal pins, a high-temperature housing is 3-D-printed using Form Labs 3-D printer to hold the encapsulation inside the module until it is fully cured. The encapsulant ensures that the power module is protected from its working environments and voltage clearance and creepage.

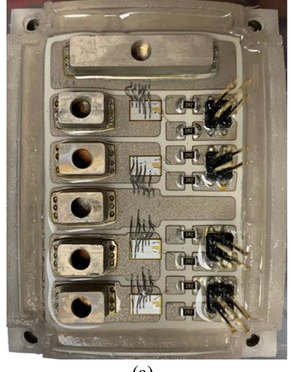
The fabricated modules are shown in Fig. 15. These modules are fabricated using CREE's third-generation CPW3-1200-0016A SiC MOSFETs (1200 V, 112 A@$T_C = 25\,^{\circ}$C) with intrinsic freewheeling diodes; hence, no additional Schottky diodes are used in these module designs.

All the power modules use the same SiC MOSFET bare die devices, use similar gate/source pads, and have the same module size. The characteristics of these power modules are listed in Table III. Similar to RPEM inductance evaluation, node-to-node inductance analysis is done to determine the parasitic inductances.

ANSYS Q3D simulation analysis shows an internal inductance of 5 nH per leg for the conventional FB power module, while the parasitic inductance of the RPEM is 6 nH per leg in an FB mode. The power terminals are designed to enhance their

TABLE III
COMPARISON OF THE CHARACTERISTICS OF THE DESIGNED FB, T-INVERTER LEG, AND INDIRECT MATRIX LEG SHOWN IN FIG. 13

	Full-Bridge (FB)	**T-Inverter**	**Indirect Matrix**	**RPEM**
Size	54mm × 68mm	54mm × 68mm	54mm × 68mm	54mm × 68mm
Internal Inductance (terminal – to – terminal)	5 nH (per leg)	Loop 1: 1 nH Loop 2: 6 nH	17 nH	**FB:** 6 nH (per leg) **T-Inv:** Loop 1: 5 nH Loop 2: 7 nH **Indirect Matrix:** 14 nH
# of Topologies	3 topologies	1 topology	2 topologies	6 topologies
Maximum Junction Temperature for 200 W power dissipation per die	163.6°C	155°C	163.8°C	157°C


(a)

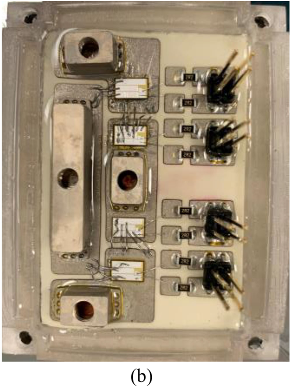

(b)

Fig. 15. Fabricated (a) RPEM and (b) FB power module.

low-price machinability. Because of the design, the terminals are robust but take a large space in the power module. The RPEM has six power terminals compared to the four power terminals for the conventional FB power module. Both the power modules have a similar gate/source pad design, as such, considering two extra power terminals in the module, the 1-nH higher inductance in the RPEM is reasonable. However, as will be shown in the test results and is also explained in [19], it is not only the module internal inductance but also the busbar attachment around the power module that eventually defines the electrical performance of the power electronic system. Hence, although a higher number of power terminals introduce slightly higher internal inductance to the module, their correct arrangement considering the module system compatibility and accurate busbar design around it can prevent high-inductance current paths.

For inductance evaluation simulations of Table III, the required terminal connection busbars for each configuration mode are considered in the RPEM, and inductance values are evaluated through the critical current paths from one power terminal to the other. This provides a fair module-level comparison taking into account the connection busbars necessary for the RPEM.

The conventional T-inverter power module shown in Fig. 13(b) has parasitic inductances of 1 and 6 nH in each of its current loops. The evaluated parasitic inductances for the RPEM in a T-inverter mode are 5 and 7 nH for each current path. Although the T-inverter module has lower path inductance values, the RPEM has symmetrical current loop inductance values. For the conventional indirect matrix power module shown in Fig. 13(c) and the RPEM in the indirect matrix mode, the parasitic inductances from the positive terminal to the negative terminal are 17 and 14 nH, respectively. From the above analysis, the parasitic inductances of the RPEM are comparable to their conventional fixed-configuration power module equivalents. In Table III, the number of topologies shows the different switching arrangements that the power modules can be used for. The conventional FB power module can be either used as an HB, an FB, or a bidirectional switch. The conventional indirect matrix converter can also be used as a bidirectional switching arrangement using suitable external busbars. However, as mentioned previously, the RPEM can be used either in six or four different power electronic topologies depending on its version, 4X or 6X.

Using the same SiC bare die, the current handling capabilities are slightly different for the same maximum junction temperature variation. To compare the thermal performance of the four types of power modules using SolidWorks simulation, a current flow of 89 A is assumed for each switching position that results in power dissipation of 200 W per bare die, considering only the conduction losses. The convection coefficient is kept at 5000 $W/m^2 \cdot K$ for these power modules. The maximum junction temperatures of the bare die devices are listed in Table III. The semiconductor devices arranged in the proximity of each other, especially those attached to the same pads such as M1 and M2 in indirect matrix module, are the ones with the highest junction temperature that slightly limit the module current capability in comparison with the rest of the modules. According to Table III, the designed RPEM has similar features as its equivalent conventional FB, T-Inverter, and indirect matrix power modules. Although fixed-configuration power modules can be optimized further for a specific application, the RPEM can be designed considering its flexibility with different power electronic systems.

DPTs are performed on the switching legs of the fabricated power modules. Fig. 16(a) and (b) shows the two switching legs defined for the 4X RPEM and FB, respectively. DPT is performed on each switching leg to evaluate the performance of each leg independently.

For comparison purposes, a standard DPT setup for conventional 62-mm power modules is used for testing both modules.

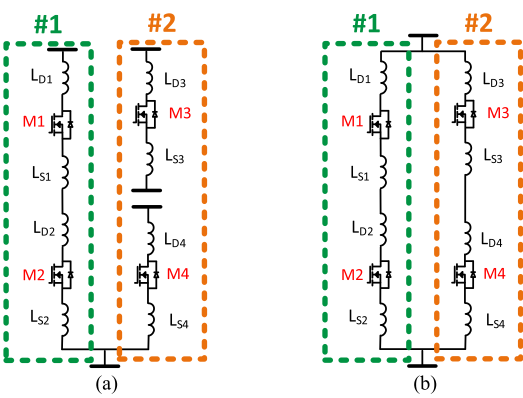
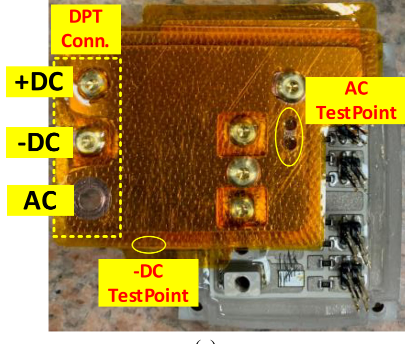
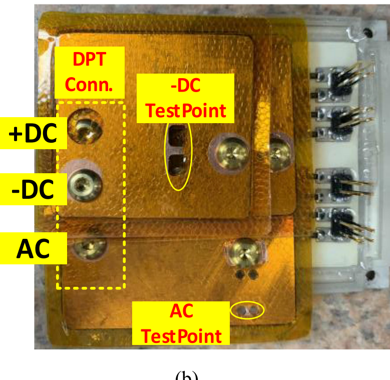


Fig. 16. DPT legs in (a) RPEM and (b) FB power modules.



(a)



(b)

Fig. 17. Fabricated adapter busbars attached to (a) RPEM and (b) FB power module.

Four sets of adaptor busbars are designed and fabricated to test each leg of the RPEM and FB power module with the same test setup. The busbars are computer numerical control (CNC) machined using copper. A Kapton tape with a thickness of 0.0035 in and a voltage rating of 10 kV is used to create isolation between the layers. The isolation capability of this Kapton is 4000 V/mil. The thickness versus current capability of the busbars is calculated as follows [1]:

$$A = 400(I)(0.785)[1 + 0.05(N - 1)](10^{-6}) \text{ in}^2 \quad (1)$$

where A is the cross-sectional area of the conductor in square inches, I is the maximum dc current in Amperes, and N is the number of conductors in the busbar. Like the conventional busbar attachment to commercial power modules, in this RPEM design, the busbars are bolted down on the power terminals using screws and appropriate spacers. These busbars on one hand are used as adaptors to connect the power modules to the test setup and, on the other hand, create the necessary connections in the second leg of the RPEM, from node S3 to node D4. To have comparable conditions for testing both modules, the busbars are designed with symmetrical path inductance values. The busbar inductance for both legs in RPEM and FB modules is 6 nH. In addition, test points are designated on the busbars to attach the oscilloscope probes to the closest proximity of the power terminals. Fig. 17(a) and (b) shows two sets of the fabricated busbars that are attached to the RPEM and FB power modules, respectively.

As mentioned previously, the gate–source pins and pads are kept similar in both power modules. Hence, a similar gate driver board along with a differential board is designed, assembled, and used for both power modules. The designed gate driver board is shown in Fig. 18. This board contains four gate driver ICs and four isolated gate driver supplies to control each switch separately in the process of DPT. For instance, to keep one of the switching legs turned OFF during the DPT, a gate–source voltage of –5 V is applied. It is important to note that the gate driver board design can be adjusted according to the application of the RPEM in a power electronic converter. While the T-inverter and the indirect matrix need separate gate drivers for each switching position, in an HB arrangement, the gates and sources of the parallel switches can be connected on the board level to prevent an unnecessary increase of the gate driver IC numbers and the difficulties of synchronizing them.

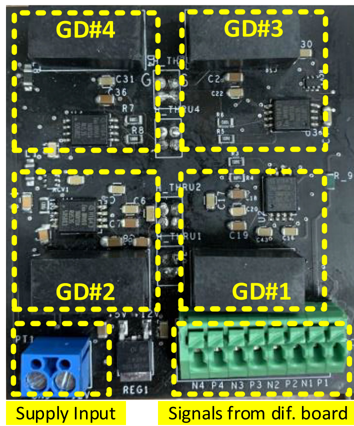


Fig. 18. Designed gate driver board for DPT on both RPEM and FB power modules.

A 90-μH inductor is used in the DPT setup, and a dc input voltage of 300 V is applied to the power module legs. The DPT waveforms across the switching legs of the RPEM and FB power modules are shown in Fig. 19(a)–(c), respectively. Both FB legs have identical designs; therefore, the DPT result of only one leg is provided in Fig. 19. As shown, the *dv/dt* and *di/dt* of the tested legs are almost similar for both power modules.

The voltage overshoot is between 20% and 22% for both legs in RPEM and FB modules. From these results, the difference of 1 nH in the parasitic inductance for these two power modules does not yield a significant difference in switching performance.

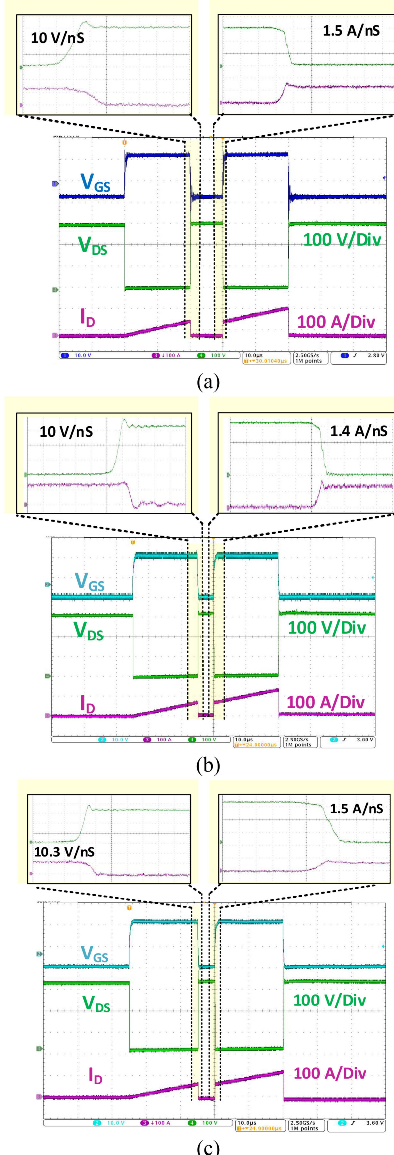


Fig. 19. DPT results of the fabricated RPEM and FB power modules. (a) Switching leg #1 in the RPEM. (b) Switching leg #2 of the RPEM. (c) Switching leg #1 of the FB power module (identical with its leg #2).

V. Conclusion

A series of RPEMs were introduced. Two versions of these power modules, the 4X (4-in-1) and 6X (6-in-1) versions, were proposed. The 4X version could be implemented in the HB, FB, T-inverter, indirect matrix, bidirectional, and HNPC topologies, while the 6X version could be used in the HB, three-phase inverter, T-inverter, and active-neutral-point-clamped topologies. As such, their reconfigurability enables these power modules to be adapted into different power electronic topologies. The 4X RPEM along with three other conventional power modules, FB, T-inverter leg, and indirect matrix leg were designed and simulated in ANSYS Q3D and SolidWorks to compare the introduced RPEM with more conventional fixed-configuration power modules. The designed RPEM and FB modules were also fabricated and tested to verify the efficacy of the proposed concept. DPT results showed that with the same testing conditions, both legs of the fabricated module had similar voltage overshoots and, as a result, comparable stray inductances.

In the future, the proposed RPEM can be used in different power electronic converters to evaluate its system-level performance.

References

[1] R. Alizadeh, T. Adamson, J. C. Balda, Y. Zhao, M. Asheghi, and K. E. Goodson, "A compact 50-kW traction inverter design using off-the-shelf components," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Anaheim, CA, USA, 2019, pp. 2414–2619.
[2] H. A. Mantooth, T. Evans, C. Farnell, Q. Le, and R. Murphree, "Emerging trends in silicon carbide power electronics design," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 3, pp. 161–169, Sep. 2017.
[3] B. Passmore *et al.*, "The next generation of high voltage (10 kV) silicon carbide power modules," in *Proc. IEEE 4th Workshop Wide Bandgap Power Devices Appl.*, Fayetteville, AR, USA, 2016, pp. 1–4.
[4] J. Guo *et al.*, "A comprehensive analysis for high-power density, high-efficiency 60 kW interleaved boost converter design for electrified powertrains," *IEEE Trans. Veh. Technol.*, vol. 69, no. 7, pp. 7131–7145, Jul. 2020.
[5] F. Yang, Z. Liang, Z. J. Wang, and F. Wang, "Design of a low parasitic inductance SiC power module with double-sided cooling," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, 2017, pp. 3057–3062.
[6] C. Chen, Z. Huang, L. Chen, Y. Tan, Y. Kang, and F. Luo, "Flexible PCB-based 3-D integrated SiC half-bridge power module with three-sided cooling using ultralow inductive hybrid packaging structure," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5579–5593, Jun. 2019.
[7] J. Zhou, S. Ang, A. Mantooth, and J. C. Balda, "A nano-composite polyamide imide passivation for 10 kV power electronics modules," in *Proc. IEEE Energy Convers. Congr. Expo. Conf.*, Raleigh, NC, USA, 2012, pp. 4262–4266.
[8] T. B. Soeiro and J. W. Kolar, "The new high-efficiency hybrid neutral-point-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1919–1935, May 2013.
[9] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level T-type converter for low-voltage applications," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 899–907, Feb. 2013.
[10] J. A. Anderson, E. J. Hanak, L. Schrittwieser, M. Guacci, J. W. Kolar, and G. Deboy, "All-silicon 99.35% efficient three-phase seven-level hybrid neutral point clamped/flying capacitor inverter," *CPSS Trans. Power Electron. Appl.*, vol. 4, no. 1, pp. 50–61, 2019.
[11] R. Pilawa-Podgurski, "The future of power electronics circuits: New technologies and managed complexity will drive the future," *IEEE Power Electron. Mag.*, vol. 7, no. 2, pp. 41–43, Jun. 2020.
[12] "Electrical and electronics technical team roadmap," Driving Research and Innovation for Vehicle Efficiency and Energy Sustainability, Oct. 2017. [Online]. Available: https://www.energy.gov/sites/prod/files/2017/11/f39/EETT%20Roadmap%2010-27-17.pdf
[13] Product Brief EconoDUAL™, EconoPACK™ 4, EconoPACK™ + Econo Medium-Power product family.
[14] *Microsemi Power Portfolio*, Microsemi, Aliso Viejo, CA, USA, 2018.
[15] Semikron Catalogue 2016/2017.
[16] Mitsubishi Power Modules.
[17] N. Lakshmanan, T. Radke, and S. Kawabata, "Power modules for combining innovation, flexibility, and power capability in the various 3-level topologies," *Bodo's Power Syst.*, pp. 26–29, Apr. 2016.
[18] L. Wei, T. A. Lipo, and H. Chan, "Matrix converter topologies with reduced number of switches," in *Proc. IEEE 33rd Annu. Power Electron. Spec. Conf.*, Cairns, QLD, Australia, 2002, vol. 1, pp. 57–63.
[19] R. Alizadeh and H. A. Mantooth, "A review of architectural design and system compatibility of power modules and their impacts on power electronics systems," *IEEE Trans. Power Electron.*, vol. 36, no. 10, pp. 11631–11646, Oct. 2021.
[20] A. Dutta and S. S. Ang, "Electromagnetic interference simulations for wide-bandgap power electronic modules," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 757–766, Sep. 2016.
[21] F. Yang, Z. Liang, Z. Wang, and F. Wang, "Parasitic inductance extraction and verification for 3D planar bond all module," in *Proc. Int. Symp. 3D Power Electron. Integr. Manuf.*, Raleigh, NC, USA, 2016, pp. 1–15.