PWM Control of *N*-Phase Interleaved Active Front-End Boost Stage-Based Impedance Source Inverter

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***Abstract*—Non-isolated high gain inverters, such as impedance source inverters (ZSI), are suitable for applications with limited input dc source voltage, e.g., microinverters. High gain in these inverters is attributed to the front-end boost stage (FBS). High step-up ratio results in very high input current as the power rating of the inverter goes up. This leads to significant conduction loss in the non ideal elements of the inverter, specifically in the FBS, thereby degrading the efficiency. Paralleling and interleaving the FBS is a feasible solution to achieve higher efficiency. This demands for a generalized pulsewidth modulation (PWM) scheme, which can enable paralleling of multiple interleaved FBSs. In this article, a novel PWM scheme is proposed to implement *n*-phase interleaving of active FBS-based ZSIs. The PWM scheme ensures synchronized operation between the "*n*" interleaved FBS and the single inverter stage. As case studies, the PWM scheme is implemented in *n*-phase interleaved current fed switched inverter, switched boost inverter, and quasi switched boost inverter. Steady-state operation of these topologies with three interleaved phases is verified using PLECS simulation. Operation of an interleaved current fed switched inverter with three interleaved phases is verified experimentally using a 200-W proof of concept prototype.**

***Index Terms*—High gain, interleaving, pulsewidth modulation (PWM).**

I. Introduction

TO MEET the increasing demand in renewable integration, there has been a significant surge in installation of roof-top Photovoltaic (PV systems. Typically, for roof-top integration, several PV panels are connected in series while supplying an inverter. This inverter is known as a string inverter. However, series connection of PV panels reduces the power output during partial shading condition [1]. A microinverter processes the solar power from a single or few PV panels connected in parallel; thereby, improving the partial shading performance. Paralleled PV panels have lower terminal voltage. Hence, the microinverter is desired to have high gain property for meeting the voltage requirement of the household loads.

The conventional inverter for obtaining high gain, i.e., a transformer-based voltage source inverter (VSI), as shown in Fig. 1(a), is bulky and hence degrades the power density. As an alternative, boost-VSI, as shown in Fig. 1(b), eliminates the bulky transformer. However, the presence of the stiff dc link makes the inverter prone to failure due to shoot-through [2].

A high gain inverter categorized as impedance source inverter (ZSI), as shown in Fig. 1(c), with an inherent boost-stage and shoot-through protection is an effective alternative for obtaining high gain. Various non-isolated ZSIs are explored in the literature as potential choices for micro-inverters [3], [4]. Some of the special characteristics as mentioned in the following make these converter topologies suitable for microinverter.

1) Ability to provide high gain, which enables the inverter to convert the output of low voltage PV source (typically in the range of 48–60 V) to high ac voltage, required by the household loads.
2) Improved reliability due to inherent shoot-through protection.

As depicted in Fig. 1(c), ZSIs consist of two stages. 1) High gain front-end boost stage (FBS) which converts the solar PV output to a high voltage dc, and 2) inverter stage which converts the high voltage dc to ac. Depending on the configuration of the FBS, ZSIs can be classified into three categories as follows. ZSIs with passive FBS are proposed in [5]–[7]. Higher passive component count makes these topologies bulky and complex. Moreover, mismatch in the passive components in the converter leads to dynamic instability. In order to address this issue, various active front-end boost stage (AFBS) based ZSIs, such as current-fed switched inverter (CFSI), switched boost inverter (SBI), and quasi switched boost inverter (Q-SBI) are proposed in [8]–[12]. ZSIs with coupled inductors in the FBS were introduced in [13]–[17]. These topologies have very high gain at the cost of increased complexity due to coupled inductors and the associated leakage inductance.

Table I presents the comparison of boost VSI (conventionally used for obtaining high gain) and various ZSIs in terms of their component count and dc gain. Among these, AFBS-based ZSIs have optimum component count with required high gain characteristics, hence best suited for micro-inverter applications. Pulsewidth modulation (PWM) scheme of these inverters is such that, in the inverter stage, shoot-through is inherently inserted

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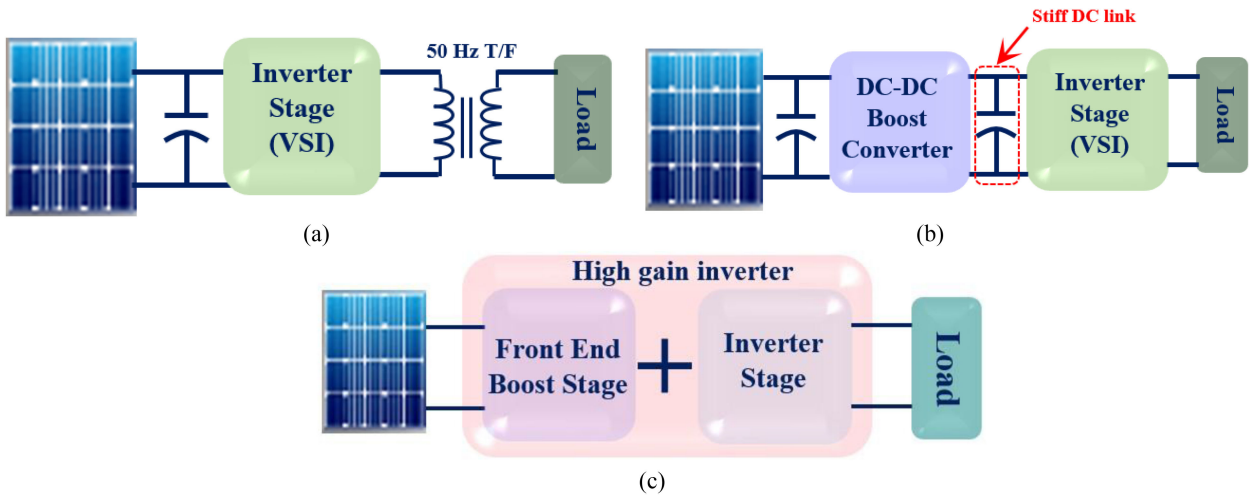
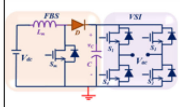
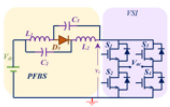
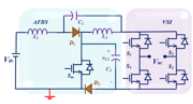
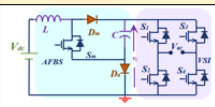
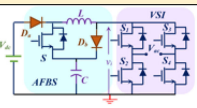
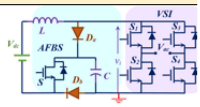


Fig. 1. (a) Conventional inverter with 50 Hz transformer. (b) Voltage source inverter (VSI) with dc–dc boost converter at the front end. (c) High gain inverter.

TABLE I
COMPARISON OF BOOST VSI AND IMPEDANCE SOURCE INVERTERS

Topology	Boost VSI [2]	Quasi ZSI [4] Passive Front-end Boost Stage based ZSI (PFBS based ZSI)	Continuous input current QZSI [11]	CFSI [8]	SBI [9]	QSBI [10]
Schematic						
Components	8 (5 switches, 1 diode, 1 inductor, 1 capacitor)	9 (4 switches, 1 diode, 2 inductors, 2 capacitors)	11 (5 switches, 2 diodes, 2 inductors, 2 capacitors)	9 (5 switches, 2 diodes, 1 inductor, 1 capacitor)	9 (5 switches, 2 diodes, 1 inductor, 1 capacitor)	9 (5 switches, 2 diodes, 1 inductor, 1 capacitor)
DC gain	$\frac{1}{1-D}$	$\frac{1}{1-3D}$	$\frac{1}{D^2-3D+1}$	$\frac{1}{1-2D}$	$\frac{1-D}{1-2D}$	$\frac{1}{1-2D}$
Advantages	Less component count	High gain	➢ High gain ➢ Shoot-through protected	➢ High gain ➢ Less component count ➢ High power density ➢ Shoot-through protected	➢ High gain ➢ Less component count ➢ High power density ➢ Shoot-through protected	➢ High gain ➢ Less component count ➢ High power density ➢ Shoot-through protected
Disadvantages	➢ Limited gain ➢ Presence of stiff DC link makes the converter prone to failure due to shoot-through	➢ High passive component count ➢ Bulky	➢ High passive component count ➢ Bulky	➢ Due to high voltage conversion ratio, input current increases with increase in power rating. ➢ High input current leads to high conduction loss.	➢ Due to high voltage conversion ratio, input current increases with increase in power rating. ➢ High input current leads to high conduction loss.	➢ Due to high voltage conversion ratio, input current increases with increase in power rating. ➢ High input current leads to high conduction loss.

and it is synchronized with the AFBS to boost up the low input voltage and thereby obtaining high ac output voltage. PWM schemes of these inverters which include the shoot-through interval are discussed in more details in [8]–[12]. A modified PWM scheme for Q-SBI, capable of providing high gain is proposed in [18]. In [19], a scheme based on both pulse amplitude and width modulation is proposed for quasi ZSIs. Different space vector modulation techniques for three-phase quasi ZSIs are also proposed in [20].

Very high conversion ratio of AFBS-based ZSI leads to a considerable high input current and consequently to significant conduction loss in the converter. This reduces the efficiency of the system drastically. Reduction in efficiency worsens with the increase in power rating. Hence, to increase the power rating of the microinverter, without sacrificing the efficiency, paralleling them, as shown in Fig. 2(a), is a prospective solution. This philosophy has been implemented in a variety of power electronics applications in order to achieve better performance in terms of efficiency. Paralleling and interleaving have been implemented in voltage regulator modules and various dc–dc converters to reduce the current stress in each phase [21]–[23]. In [24]–[26], multiple inverter modules are paralleled to deal with higher power rating. However, with high input current, conduction loss in FBS is significantly higher as compared to that of the inverter stage [27].

Therefore, paralleling the entire converter is not an optimal solution in terms of component count. Paralleling the FBS, while keeping the inverter stage intact, as shown in Fig. 2(b), is a better solution for the aforementioned problem. This impels for a generalized PWM scheme, which can ensure paralleling and interleaving of multiple AFBS and synchronize the operation of the paralleled phases with the single inverter stage. In prior works [27], an interleaved topology for an AFBS-based ZSI with optimum component count and high efficiency was

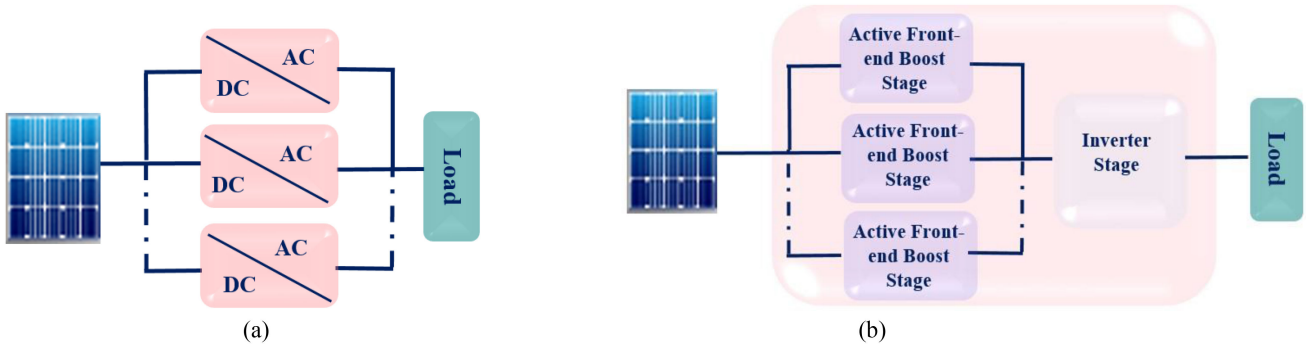


Fig. 2. (a) Paralleling of microinverters. (b) Paralleling of front-end boost stage (FBS) with single inverter stage.

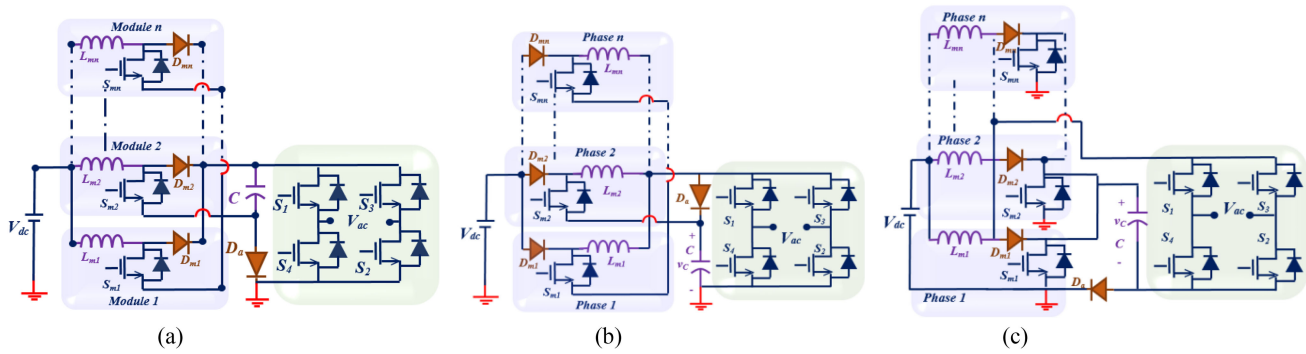


Fig. 3. Schematic of (a) n-phase interleaved current fed switched inverter, (b) n-phase interleaved switched boost inverter, and (c) n-phase interleaved quasi switched boost inverter.

proposed based on the above philosophy. However, the PWM scheme discussed in [27] is applicable only for two phases of one particular topology. Moreover, PWM schemes proposed in [8]–[10] and [18]–[20] are not directly applicable for interleaved topologies. Hence, there is a need to develop a generalized PWM scheme which can be used for interleaving of multiple phases in AFBS-based ZSIs.

The overall objective of this article is to generalize the philosophy established in [27] and to propose a generalized PWM scheme, which can drive n-phase interleaved AFBS-based ZSIs. Topologies, such as CFSI [8], SBI [9], and Q-SBI [10], are explored as potential inverters under the category of AFBS-based ZSI. This article analyzes n-phase interleaved topologies for each of these inverters along with their steady-state and dynamic characteristics based on the proposed PWM scheme. The PWM scheme incorporates shoot-through in the inverter stage in order to achieve high gain. The scheme also ensures the synchronization of shoot-through with the power and zero intervals of the inverter stage. This ascertains synchronized operation of the interleaved phases and the single inverter stage.

The rest of this article is organized as follows. In Section II, n-phase interleaved topologies for CFSI, SBI, and Q-SBI are discussed. Proposed PWM scheme to implement the n-phase interleaving is also discussed and analyzed in this section. Section III presents the steady-state operation of the interleaved topologies with various operating modes. Mathematical formulation of the dc and ac gain of the inverters and the gain characteristics are also analyzed in this section, followed by PLECS simulation results of the steady-state operation of interleaved topologies with three interleaved phases. Section IV reports the small signal and loss analysis of n-phase interleaved current fed switched inverter (n-ICFS-I). In Section V, n-ICFSI with interleaved phases is verified experimentally using a 200-W proof of concept experimental prototype. Finally, Section VI concludes this article.

II. Proposed PWM Scheme

Interleaved topologies for CFSI, SBI, and Q-SBI with "n" phases are depicted in Fig. 3. As shown in the figures, the inductor (L_m), the switch (S_m), and the diode (D_m) are connected to form a phase and "n" such phases are connected in parallel. This facilitates the sharing of input current among various phases and thereby leading to improvement in efficiency.

In inverters, such as CFSI, SBI, and Q-SBI, shoot-through is a valid operating state, where switches of the same leg of the inverter stage and the switch of the AFBS are deliberately turned ON simultaneously. Insertion of shoot-through in the inverter stage and its synchronization with the AFBS ensures reliable and high gain operation of these inverters [8]–[11]. Similar to that, in the interleaved inverters also, shoot-through in the inverter stage is a valid state. Hence, in order to synchronize the shoot-through state with the "n" phases of FBS, a novel and generalized PWM scheme is proposed in this article. As shown in Fig. 4, pulsewidth modulated intervals in a switching period of T_S are divided into 1) *power and zero intervals* and 2) *shoot-through interval*.

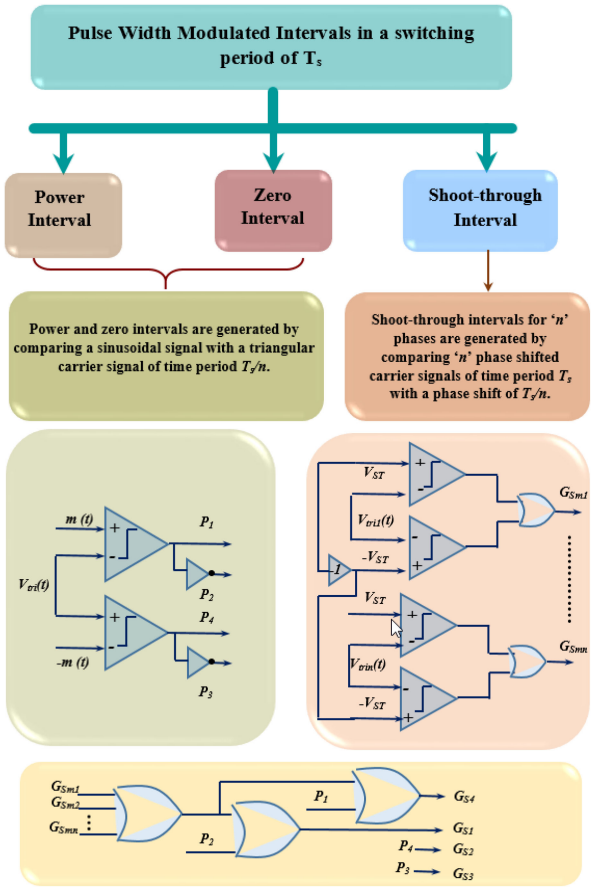


Fig. 4. Proposed PWM scheme for *n*-phase interleaved active front end boost stage-based impedance source inverter.

For deciding the power and the zero interval, unipolar sine PWM scheme is implemented and the pulses P_1–P_4 are generated by comparing a low-frequency (desired frequency of the ac output voltage) sinusoidal modulating signal ($m(t)$) with the high-frequency carrier signal $V_{\text{tri}}(t)$. Implementation of the unipolar sine PWM is depicted in Fig. 5(a). $V_{\text{tri}}(t)$ has a time period of T_s/n. Depending on the modulation index (peak of the modulating signal, m_a), sine PWM results in two intervals *1) power interval and 2) zero interval*.

Gate pulses for the switches (S_{m1} through S_{mn}) of "*n*" FBS phases are generated by comparing the dc signals (V_{ST} and $-V_{ST}$) with "*n*" phase shifted high-frequency carrier signals ($V_{\text{tri}1}(t)$–$V_{\text{tri}n}(t)$) with a phase shift of ($T_s/2n$) as shown in Fig. 5(b). This results in phase shifted signals (G_{sm1} through G_{Smn}) with pulsewidth of $D_1T_s/2$, $D_2T_s/2$, …, $D_nT_s/2$ and a phase shift of $T_s/4n$. As a result of this, the shoot-through interval in a switching cycle of T_s (DT_s) is equally divided into "*n*" intervals (D_1T_s–D_nT_s). Synchronization of the shoot-through interval and the power and zero interval is ensured by implementing the logic as shown in Fig. 4 and generating the gate pulses for the switches of the inverter legs (G_{S1}–G_{S4}). Implementing the PWM scheme results in the decrease in switching frequency of the boost-stage switches as compared with that of inverter switches, where switching frequency of the inverter leg switches (f_s) is "*n/2*" times that of the switching frequency interleaved switches of the boost-stage (f_{sb}). However, the proposed PWM scheme introduces a constraint as follows:

$$D = 1 - m_a. \tag{1}$$

This constraint stems from the condition that ZSIs operate in zero state during shoot-through interval. Hence, the power delivered to the load during this interval is zero, thereby leading to the constraint that the power interval and shoot-through interval cannot overlap.

Fig. 6 shows the comparison between the conventional PWM schemes for AFBS-based ZSIs and the proposed PWM scheme in order to implement the *n*-phase interleaving. In the conventional PWM schemes, shoot-through interval (where the boost-stage switch is turned ON along with one of the inverter leg switches) is introduced in single FBS [8]–[11], whereas the proposed PWM scheme has the following key features.

1) Proposed generalized PWM scheme ensures sharing of the shoot-through interval (DT_s) into "*n*" equal phase shifted intervals (D_1T_s, D_2T_s, …, D_nT_s), where each of the "*n*" FBS switches (S_{m1}, S_{m2}, …, S_{mn}) are turned ON in an interleaved fashion along with the inverter leg switches.
2) In addition to that, synchronization of the "*n*" shoot-through interval with the power and zero intervals is done, such that the constraint $D+m_a<1$ is satisfied.

III. Steady-State Analysis

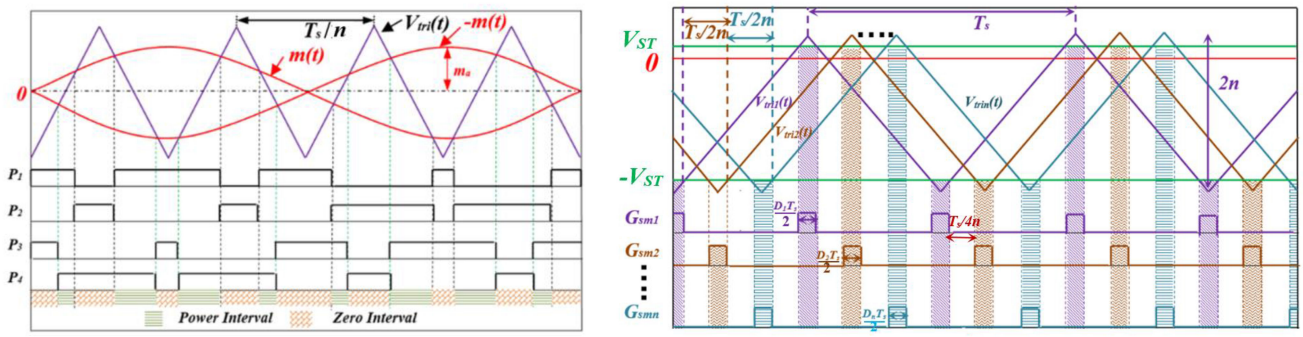
Different operating modes of *n*-ICFSI, *n*-SBI, and *n*-IQSBI over a switching period of T_s based on the proposed PWM scheme are analyzed in this section. The entire steady-state analysis is carried out with the assumption $D_1 = D_2 = \cdots = D_n = D/n$. DC resistance (DCR) of the interleaved inductors are taken into consideration in the analysis.

A. CASE 1 (Steady-State Analysis of n-ICFSI)

1) Operating Modes:

a) Shoot-through interval (ST_1), Ref: *Table II:* The equivalent schematic of ICFSI during (D_1T_s) interval is shown in Table II. In this interval, switches S_{m1}, S_1, and S_4 are turned ON simultaneously. Turning ON of switch S_{m1} reverse biases the diode D_{m1} by dc-link voltage V_c and turns it OFF. Similarly, turning ON of S_1 and S_4 reverse biases the diode D_a and turns it OFF. However, diodes D_{m2}, D_{m3}, …, D_{mn} are turned ON and forced to carry the inductor currents i_{Lm2}, i_{Lm3}, …, i_{Lmn}. The proposed PWM scheme is such that the inverter is operated in zero state during the shoot-through interval. Instantaneous voltage across the interleaved inductors and the current through the capacitor during this interval are listed in Table II.

b) Non shoot-through interval, Ref: *Table II:* During this interval ($(1–D)T_s$), interleaved switches of the FBS are turned OFF. Interleaved diodes (D_{m1}, D_{m2}, …, D_{mn}) and D_a are forward biased to maintain the currents through the inductors. Inductors L_{m1} and L_{m2}, …, L_{mn} are connected in parallel and discharge themselves through D_a as shown in Table II. In this interval, modulating signals $m(t)$ and $-m(t)$, as given in Fig. 5(a), decide the switching for the four switches of the inverter legs.



(a) (b)

Fig. 5. (a) Sine PWM for generating the gate pulses of the switches in the inverter. (b) PWM scheme for generating the gate pulses for the interleaved switches of the active front end boost stage.

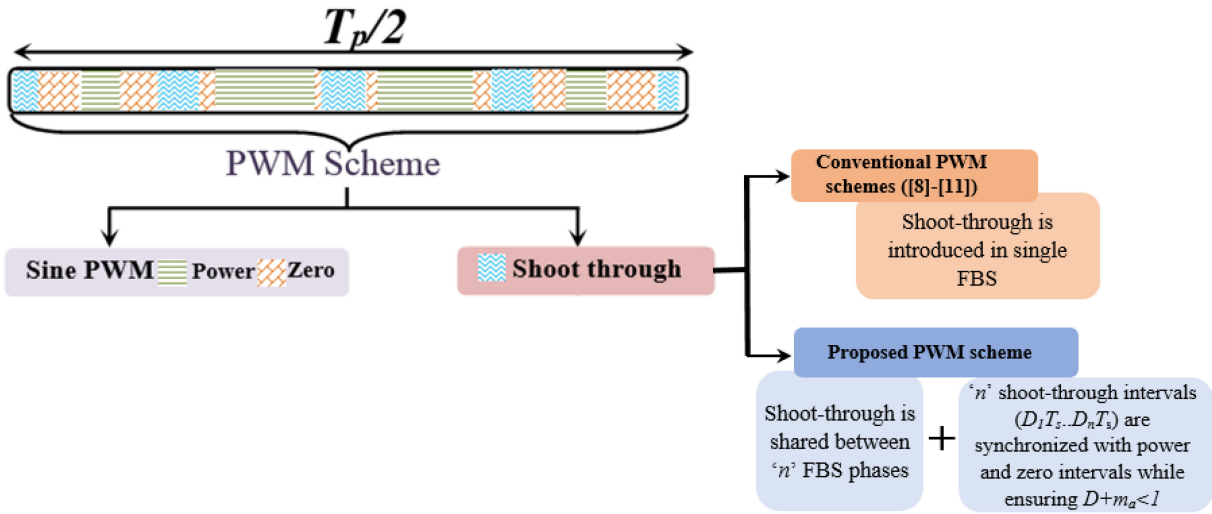


Fig. 6. Comparison of the conventional PWM scheme for active front-end boost stage based ZSI and proposed PWM scheme for interleaved AFBS-based ZSIs.

Depending on the modulation index m_a, power and the zero intervals are distributed in the non shoot-through interval. Instantaneous voltage across the interleaved inductors and the current through the capacitor during this interval are listed in Table II.

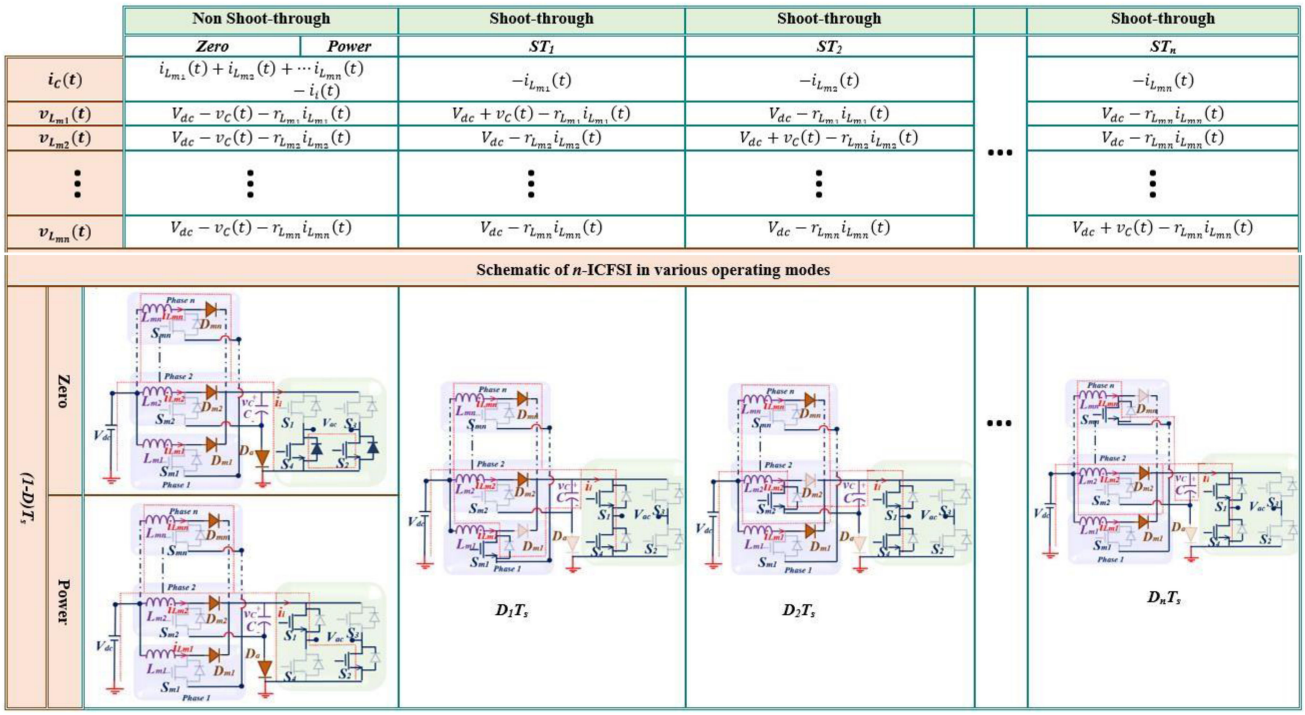
c) Shoot-through interval (ST_n), Ref: *Table II:* The equivalent schematic of *n*-ICFSI during this interval ((D_nT_s) interval) is shown in Table II. It is similar to the ST_1 interval. Instead of turning ON S_{m1} in this mode, switche S_{mn} of phase "*n*" is turned ON along with inverter switches S_1 and S_4. Similar to ST_1, the inverter is in zero state in this interval too. Inductor voltages (v_{Lm1} and v_{Lm2}) and the capacitor current (i_C) in this interval are given in Table II.

2) PLECS Simulation: Steady-state operation of an ICFSI with three interleaved phases is verified using PLECS simulation. Fig. 7(a) shows the waveforms of currents through the interleaved inductors (i_{Lm1}, i_{Lm2}, and i_{Lm3}), dc-link voltage (V_C), and the ac output voltage (V_{out}) (after passing V_{ac} through an *LC* filter). An ac output voltage of 110 V ($V_m = 155$ V) is obtained from a dc input voltage (V_{dc}) of 48 V. Hence, an ac gain of 3.24 is obtained with the operating points ($D = 0.675$ and $m_a = 0.325$). Waveforms of inductor currents with the gate

$$\left.\begin{aligned}
\langle v_{Lm1}\rangle_{T_s} &= V_{\text{dc}} - (1 - nD_1 - D_2 - \cdots D_n)\langle v_C\rangle_{T_s} - r_{L1}\langle i_{Lm1}\rangle_{T_s}\\
\langle v_{Lm2}\rangle_{T_s} &= V_{\text{dc}} - (1 - nD_2 - D_1 - \cdots D_n)\langle v_C\rangle_{T_s} - r_{L2}\langle i_{Lm2}\rangle_{T_s}\\
&\vdots\\
\langle v_{Lmn}\rangle_{T_s} &= V_{\text{dc}} - \left(1 - nD_n - D_1 - \cdots D_{(n-1)}\right)\langle v_C\rangle_{T_s} - r_{Ln}\langle i_{Lmn}\rangle_{T_s}\\
\langle i_C\rangle_{T_s} &= (1 - nD_1 - D_2 - \cdots D_n)\langle i_{Lm1}\rangle_{T_s} + (1 - nD_2 - D_1 - \cdots D_n)\langle i_{Lm2}\rangle_{T_s}\\
&\quad + \left(1 - nD_n - D_1 - \cdots D_{(n-1)}\right)\langle i_{Lmn}\rangle_{T_s} - (1 - D)\langle i_i\rangle_{T_s}
\end{aligned}\right\} \quad (2)$$

TABLE II
VARIOUS OPERATING MODES OF ICFSI WITH THE PROPOSED PWM SCHEME

	Non Shoot-through		Shoot-through	Shoot-through		Shoot-through
	Zero	*Power*	ST_1	ST_2	...	ST_n
$i_C(t)$	$i_{L_{m_1}}(t)+i_{L_{m_2}}(t)+\cdots i_{L_{mn}}(t)-i_i(t)$		$-i_{L_{m_1}}(t)$	$-i_{L_{m_2}}(t)$		$-i_{L_{mn}}(t)$
$v_{L_{m1}}(t)$	$V_{dc}-v_C(t)-r_{L_{m_1}}i_{L_{m_1}}(t)$		$V_{dc}+v_C(t)-r_{L_{m_1}}i_{L_{m_1}}(t)$	$V_{dc}-r_{L_{m_1}}i_{L_{m_1}}(t)$		$V_{dc}-r_{L_{mn}}i_{L_{mn}}(t)$
$v_{L_{m2}}(t)$	$V_{dc}-v_C(t)-r_{L_{m_2}}i_{L_{m_2}}(t)$		$V_{dc}-r_{L_{m_2}}i_{L_{m_2}}(t)$	$V_{dc}+v_C(t)-r_{L_{m_2}}i_{L_{m_2}}(t)$		$V_{dc}-r_{L_{mn}}i_{L_{mn}}(t)$
⋮	⋮		⋮	⋮		⋮
$v_{L_{mn}}(t)$	$V_{dc}-v_C(t)-r_{L_{mn}}i_{L_{mn}}(t)$		$V_{dc}-r_{L_{mn}}i_{L_{mn}}(t)$	$V_{dc}-r_{L_{mn}}i_{L_{mn}}(t)$		$V_{dc}+v_C(t)-r_{L_{mn}}i_{L_{mn}}(t)$



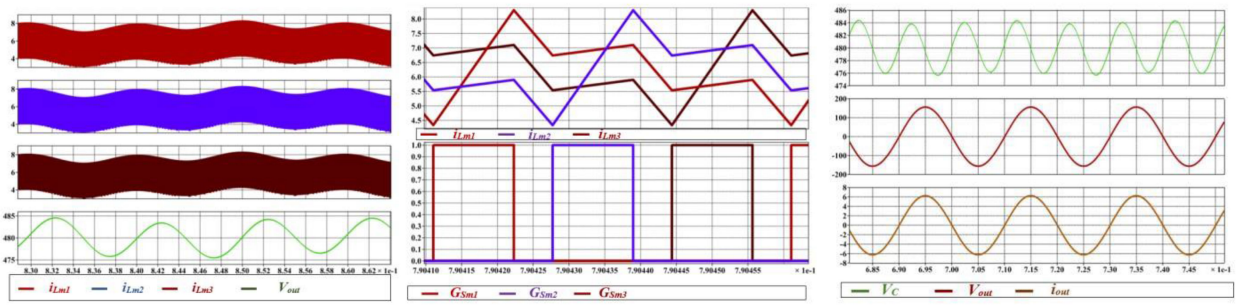


Fig. 7. Simulation results of an ICFSI with three interleaved phases. (a) Steady-state waveforms of the inductor currents (i_{Lm1}, i_{Lm2}, and i_{Lm3}), and the ac output voltage ($V_{\rm ac}$). (b) Inductor current ripple in the switching cycle ($T_s/2$) with the gate pulses of the interleaved switches (G_{Sm1}, G_{Sm2}, and G_{Sm3}). (c) Steady-state waveforms of the dc-link voltage (V_C), ac output voltage ($V_{\rm out}$), and ac output current ($i_{\rm out}$).

pulses of the interleaved switches (G_{Sm1}, G_{Sm2}, and G_{Sm3}) are shown in Fig. 7(b). Waveforms of $V_{\rm out}$, ac output current ($i_{\rm out}$), and the dc-link voltage (V_C) an ICFSI with three interleaved phases (three-phase ICFSI) are shown in Fig. 7(c).

3) Gain Characteristic: In order to obtain a relationship between the dc-link voltage (V_C) and $V_{\rm dc}$, voltages across the interleaved inductors ($v_{Lm1}, v_{Lm2}, \ldots, v_{Lmn}$) and current through the capacitor (i_C) are averaged over one switching period (T_s) as given in (2). Solving the averaged equations yields (3). Here the DCR of the inductors L_{m1} through L_{mn} are assumed to be same (r_L) and $D_1 = D_2 = \cdots = D_2 = D/n$

$$V_C = \frac{\begin{array}{c} V_{dc}\left[{r_L}^{n-1}\left(1-\frac{D}{n}-D\right)+{r_L}^{n-1}\left(1-\frac{D}{n}-D\right)\right] \\ +\cdots+{r_L}^{n-1}\left(1-\frac{D}{n}-D\right)-I_i{r_L}^{n}(1-D) \end{array}}{\left[r_L\left(1-\frac{D}{n}-D\right)^2+r_L\left(1-\frac{D}{n}-D\right)^2+\cdots+r_L\left(1-\frac{D}{n}-D\right)^2\right]}. \tag{3}$$

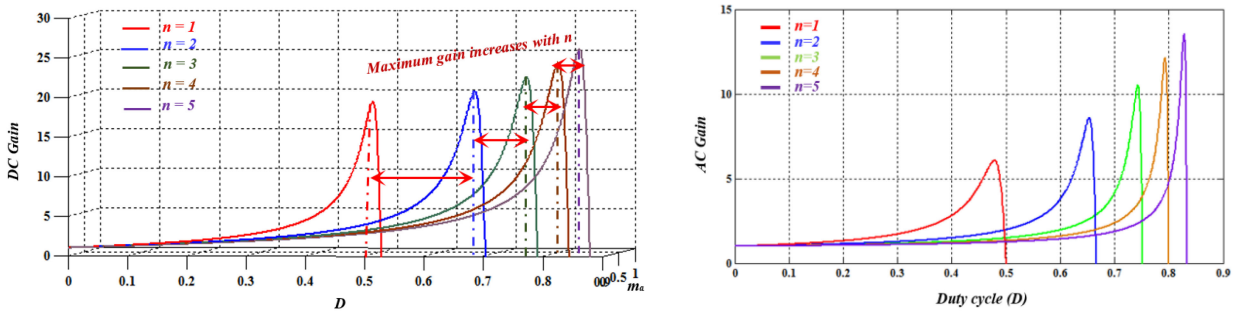
The average current (I_i) drawn by the inverter can be obtained by applying power balance for a unity power factor load ($R_{\rm ac}$)

$$V_i\, I_i = \frac{{V_m}^2}{2R_{\rm ac}} = \frac{{m_a}^2{V_C}^2}{2R_{\rm ac}} \Rightarrow I_i = \frac{{m_a}^2 V_C}{2R_{\rm ac}\,(1-D)} \tag{4}$$

where $V_m\,(=m_a\,V_C\,)$ is the peak of ac output voltage. After eliminating I_i from (3), then *dc gain* $(\frac{V_C}{V_{\rm dc}})$ and *ac gain* $(\frac{V_m}{V_{\rm dc}})$ can be given as follows:

$$\frac{V_C}{V_{\rm dc}} = \frac{1}{\left(1-D-\frac{D}{n}\right)+\frac{{m_a}^2}{2nR_{\rm ac}\left(1-D-\frac{D}{n}\right)}r_L} \tag{5}$$

$$\frac{V_m}{V_{\rm dc}} = \frac{m_a}{\left(1-D-\frac{D}{n}\right)+\frac{{m_a}^2}{2nR_{\rm ac}\left(1-D-\frac{D}{n}\right)}r_L}. \tag{6}$$



(a) (b)

Fig. 8. (a) DC gain characteristic of *n*-ICFSI w.r.t. *D* and m_a as the number of phases (*n*) is varied from 1 to 5. (b) AC gain characteristic of *n*-ICFSI at the boundary $D=1–m_a$.

The dc gain of *n*-ICFSI (5) is plotted in Fig. 8(a) with respect to varying duty cycle (*D*) and the modulation index (m_a) with the number of phase (*n*) varying from 1 to 5. As depicted in the figure, as "*n*" increases, the maximum achievable dc gain increases due to the extended operating region in terms of *D*. AC gain of *n*-ICFSI (6) is plotted in Fig. 8(b). The plot is obtained at the boundary of the constraint $D = 1–m_a$.

B. CASE 2 (Steady-State Analysis of n-ISBI)

1) Operating Modes:

a) Shoot-through interval (ST_1), Ref: *Table III:* The equivalent schematic of *n*-ISBI during (D_1T_s) interval is shown in Table III. In this interval, switches S_{m1}, S_1, and S_4 are turned ON simultaneously. By turning ON the switch S_{m1}, diode D_{m1} gets reverse biased with a voltage of $V_{\rm dc}–V_C$ across it. Similarly, turning ON of S_1 and S_4 reverse biases the diode D_a and turns it OFF. However, diodes D_{m2}, D_{m3}, …, D_{mn} are turned ON and forced to carry the inductor currents i_{Lm2}, i_{Lm3}, …, i_{Lmn}. The proposed PWM scheme is such that the inverter is operated in zero state during the shoot-through interval. Instantaneous voltage across the interleaved inductors and the current through the capacitor during this interval are listed in Table III.

b) Non shoot-through interval, Ref: *Table III:* Similar to the non shoot-through interval of *n*-ICFSI, in *n*-ISBI, also during this interval *($(1-D)T_s$),* interleaved switches of the FBS are turned OFF. Interleaved diodes ($D_{m1}, D_{m2}, \ldots, D_{mn}$) and D_a are forward biased. Inductors L_{m1} and $L_{m2}, \ldots, L_{mn}$ are connected in parallel and discharge themselves through D_a as shown in Table III. In this interval, modulating signals *m(t)* and *–m(t),* as given in Fig. 5(a), decide the switching for the four switches of the inverter legs. Depending on the modulation index m_a, power and the zero intervals are distributed in the non shoot-through interval. Instantaneous voltage across the interleaved inductors and the current through the capacitor during this interval are listed in Table III.

c) Shoot-through interval (ST_n), Ref: *Table III:* The equivalent schematic of *n*-ISBI during this interval ((D_nT_s) interval) is shown in Table III. It is similar to the ST_1 interval. Instead of turning ON S_{m1} in this mode, switch S_{mn} of phase "*n*" is turned ON along with inverter switches S_1 and S_4. Similar to ST_1, the inverter is in zero state in this interval too.

Inductor voltages (v_{Lm1} and v_{Lm2}) and the capacitor current (i_C) in this interval are given in Table III.

2) PLECS Simulation: Steady-state operation of an ISBI with three interleaved phases is verified using PLECS simulation. Fig. 9(a) shows the waveforms of currents through the interleaved inductors (i_{Lm1}, i_{Lm2}, and i_{Lm3}), dc-link voltage (V_C), and the ac output voltage ($V_{\rm out}$). An ac output voltage of 110 V ($V_m = 155$ V) is obtained from a dc input voltage ($V_{\rm dc}$) of 48 V. Hence, an ac gain of 3.24 is achieved at a duty cycle of 0.695 and a modulation index (m_a) of 0.305. Waveforms of inductor currents with the gate pulses of the interleaved switches (G_{Sm1}, G_{Sm2}, and G_{Sm3}) are shown in Fig. 9(b). Steady-state waveforms of ac output voltage ($V_{\rm out}$), ac output current ($i_{\rm out}$), and the dc-link voltage (V_C) is shown in Fig. 9(c).

3) Gain Characteristic: In order to establish a relation between the dc-link voltage (V_C) and $V_{\rm dc}$, the inductor voltages and the capacitor current are averaged over one switching period (T_s) as given in (7). Solving the averaged equations, considering equal DCR and shoot-through intervals, and using the I_i as obtained from (4), the dc-link voltage (V_C) can be expressed as follows:

$$V_C = \frac{(1-D)}{\left(1-D-\frac{D}{n}\right)+\frac{{m_a}^2}{2nR_{ac}\left(1-D-\frac{D}{n}\right)}r_L}. \tag{8}$$

$$\left.\begin{aligned}
\langle v_{Lm1}\rangle_{T_s} &= V_{\rm dc}\left[1-D+D_2+\cdots D_n\right]-\langle v_C\rangle_{T_s}\left[1+D_1-D\right]-r_{L1}\langle i_{Lm1}\rangle_{T_s}\\
\langle v_{Lm2}\rangle_{T_s} &= V_{\rm dc}\left[1-D+D_1+\cdots D_n\right]-\langle v_C\rangle_{T_s}\left[1+D_2-D\right]-r_{L2}\langle i_{Lm1}\rangle_{T_s}\\
&\vdots\\
\langle v_{Lmn}\rangle_{T_s} &= V_{\rm dc}\left[1-D+D_1+\cdots D_{(n-1)}\right]-\langle v_C\rangle_{T_s}\left[1+D_n-D\right]-r_{Ln}\langle i_{Lmn}\rangle_{T_s}\\
\langle i_C\rangle_{T_s} &= \left(1-nD_1-D_2-\cdots D_n\right)\langle i_{Lm1}\rangle_{T_s}+\left(1-nD_2-D_1-\cdots D_n\right)\langle i_{Lm2}\rangle_{T_s}\\
&\quad+\left(1-nD_n-D_1-\cdots D_{(n-1)}\right)\langle i_{Lmn}\rangle_{T_s}-\left(1-D\right)\langle i_i\rangle_{T_s}
\end{aligned}\right\} \tag{7}$$

TABLE III
VARIOUS OPERATING MODES OF ISBI WITH THE PROPOSED PWM SCHEME

	Non Shoot-through		Shoot-through	Shoot-through		Shoot-through
	Zero	*Power*	ST_1	ST_2		ST_n
$i_C(t)$	$i_{Lm_1}(t)+i_{Lm_2}(t)+\cdots i_{Lmn}(t)-i_i(t)$		$-i_{Lm_1}(t)$	$-i_{Lm_2}(t)$		$-i_{Lmn}(t)$
$v_{Lm1}(t)$	$V_{dc}-v_C(t)-r_{Lm_1}i_{Lm_1}(t)$		$v_C(t)-r_{Lm_1}i_{Lm_1}(t)$	$V_{dc}-r_{Lm_1}i_{Lm_1}(t)$		$V_{dc}-r_{Lmn}i_{Lmn}(t)$
$v_{Lm2}(t)$	$V_{dc}-v_C(t)-r_{Lm_2}i_{Lm_2}(t)$		$V_{dc}-r_{Lm_2}i_{Lm_2}(t)$	$v_C(t)-r_{Lm_2}i_{Lm_2}(t)$	...	$V_{dc}-r_{Lmn}i_{Lmn}(t)$
⋮	⋮		⋮	⋮		⋮
$v_{Lmn}(t)$	$V_{dc}-v_C(t)-r_{Lmn}i_{Lmn}(t)$		$V_{dc}-r_{Lmn}i_{Lmn}(t)$	$V_{dc}-r_{Lmn}i_{Lmn}(t)$		$v_C(t)-r_{Lmn}i_{Lmn}(t)$
Schematic of *n*-ISBI in various operating modes						
$(1-D)T_s$	Zero		D_1T_s	D_2T_s	...	D_nT_s
	Power					

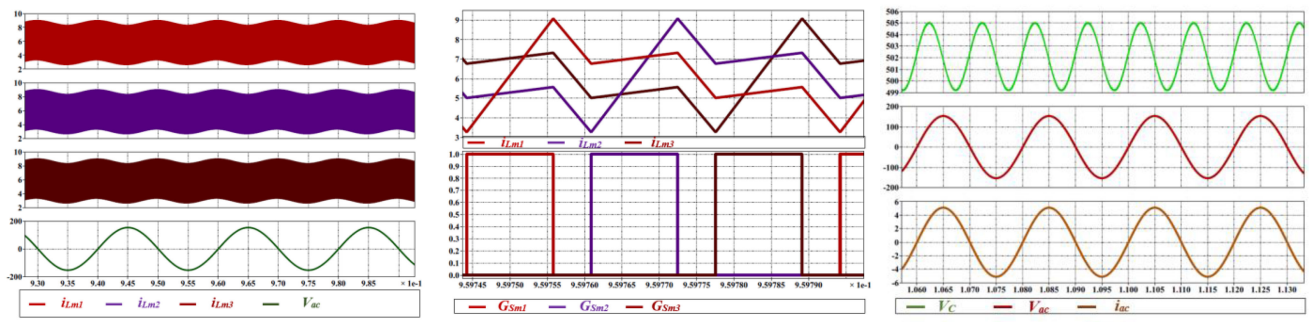


Fig. 9. Simulation results of a ISBI with three interleaved phases. (a) Steady-state waveforms of the inductor currents (i_{Lm1}, i_{Lm2}, and i_{Lm3}), and the ac output voltage ($V_{\rm ac}$). (b) Inductor current ripple in the switching cycle ($T_s/2$) with the gate pulses of the interleaved switches (G_{Sm1}, G_{Sm2}, and G_{Sm3}). (c) Steady-state waveforms of the dc-link voltage (V_C), ac output voltage ($V_{\rm out}$), and ac output current ($i_{\rm out}$).

Hence, the dc gain and the ac gain can be expressed as follows:

$$\frac{V_C}{V_{\rm dc}}=\frac{1-D}{\left(1-D-\frac{D}{n}\right)+\frac{{m_a}^2}{2nR_{\rm ac}\left(1-D-\frac{D}{n}\right)}r_L} \tag{9}$$

$$\frac{V_m}{V_{\rm dc}}=\frac{m_a\,(1-D)}{\left(1-D-\frac{D}{n}\right)+\frac{{m_a}^2}{2nR_{\rm ac}\left(1-D-\frac{D}{n}\right)}r_L} \tag{10}$$

$$\left.\begin{aligned}
\langle v_{Lm1}\rangle_{T_s}&=V_{\rm dc}-(1-D-D_1-\cdots D_n)\langle v_C\rangle_{T_s}-r_{L1}\langle i_{Lm1}\rangle_{T_s}\\
\langle v_{Lm2}\rangle_{T_s}&=V_{\rm dc}-(1-D-D_1-\cdots D_n)\langle v_C\rangle_{T_s}-r_{L2}\langle i_{Lm2}\rangle_{T_s}\\
&\vdots\\
\langle v_{Lmn}\rangle_{T_s}&=V_{\rm dc}-(1-D-D_1-\cdots D_n)\langle v_C\rangle_{T_s}-r_{Ln}\langle i_{Lmn}\rangle_{T_s}\\
\langle i_C\rangle_{T_s}&=(1-D-D_1-\cdots D_n)\langle i_{Lm1}\rangle_{T_s}+(1-D-D_1-\cdots D_n)\langle i_{Lm2}\rangle_{T_s}\\
&\quad+(1-D-D_1-\cdots D_n)\langle i_{Lmn}\rangle_{T_s}-(1-D)\langle i_i\rangle_{T_s}
\end{aligned}\right\} \tag{11}$$

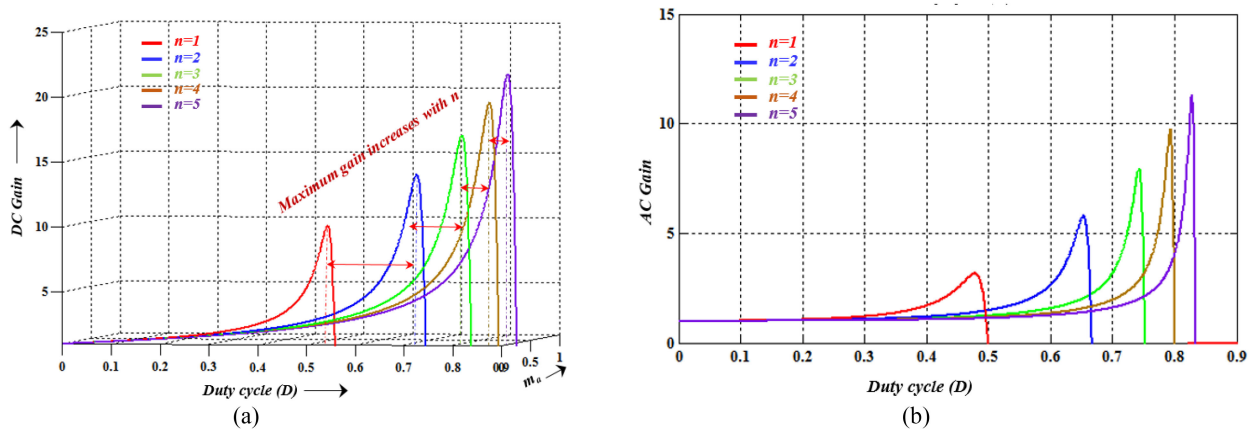


Fig. 10. (a) DC gain characteristic of n-ISBI w.r.t D and m_a as the number of phases (n) is varied from 1 to 5. (b) AC gain characteristic of n-ICFSI at the boundary $D=1-m_a$.

TABLE IV
VARIOUS OPERATING MODES OF IQSBI WITH THE PROPOSED PWM SCHEME

	Non Shoot-through		Shoot-through	Shoot-through		Shoot-through
	Zero	*Power*	ST_1	ST_2		ST_n
$i_C(t)$	$i_{Lm_1}(t)+i_{Lm_2}(t)+\cdots i_{Lmn}(t)-i_i(t)$		$-(i_{Lm_1}(t)+i_{Lm_2}(t)+..i_{Lmn}(t))$	$-(i_{Lm_1}(t)+i_{Lm_2}(t)+..i_{Lmn}(t))$		$-(i_{Lm_1}(t)+i_{Lm_2}(t)+..i_{Lmn}(t))$
$v_{Lm_1}(t)$	$V_{dc}-v_C(t)-r_{Lm_1}i_{Lm_1}(t)$		$V_{dc}+v_C(t)-r_{Lm_1}i_{Lm_1}(t)$	$V_{dc}+v_C(t)-r_{Lm_1}i_{Lm_1}(t)$		$V_{dc}+v_C(t)-r_{Lmn}i_{Lmn}(t)$
$v_{Lm_2}(t)$	$V_{dc}-v_C(t)-r_{Lm_2}i_{Lm_2}(t)$		$V_{dc}+v_C(t)-r_{Lm_2}i_{Lm_2}(t)$	$V_{dc}+v_C(t)-r_{Lm_2}i_{Lm_2}(t)$		$V_{dc}+v_C(t)-r_{Lmn}i_{Lmn}(t)$
⋮	⋮		⋮	⋮		⋮
$v_{Lmn}(t)$	$V_{dc}-v_C(t)-r_{Lmn}i_{Lmn}(t)$		$V_{dc}+v_C(t)-r_{Lmn}i_{Lmn}(t)$	$V_{dc}+v_C(t)-r_{Lmn}i_{Lmn}(t)$		$V_{dc}+v_C(t)-r_{Lmn}i_{Lmn}(t)$
Schematic of n-IQSBI in various operating modes						
$(1-D)T_s$	Zero		D_1T_s	D_2T_s		D_nT_s
	Power					

The dc gain and ac gain of n-ISBI [(9), (10)] are plotted in Fig. 10(a) and (b), respectively, with respect to varying duty cycle (D) and the modulation index (m_a) with the number of phase (n) varying from 1 to 5. Similar to that of n-ICFSI, the maximum achievable dc and ac gain increases in n-ISBI with the increase in the number of phase. However, the maximum gain of n-ISBI is lower as compared to that of n-ICFSI.

C. CASE 3 (Steady-State Analysis of n-IQSBI)

1) Operating Modes:

a) Shoot-through interval (ST_1), Ref: *Table IV:* The equivalent schematic of n-IQSBI during (D_1T_s) interval is shown in Table IV. In this interval switches S_{m1}, S_1, and S_4 are turned ON simultaneously. Turning ON of switch S_{m1}, S_1, and S_4 reverse biases the diodes D_{m1}, D_{m2},..., D_{mn} by dc-link voltage V_C and turns them OFF. Similarly, turning ON of S_1 and S_4 reverse biases the diode D_a. The proposed PWM scheme is such that the inverter is operated in zero state during the shoot-through interval. Instantaneous voltage across the interleaved inductors and the current through the capacitor during this interval are listed in Table IV.

b) Non shoot-through interval, Ref: *Table IV:* Similar to that of both n-ICFSI and n-ISBI, during this interval ($(1-D)T_s$) interleaved switches of the FBS are turned OFF. Interleaved diodes (D_{m1}, D_{m2},..., D_{mn}) and D_a are forward biased to

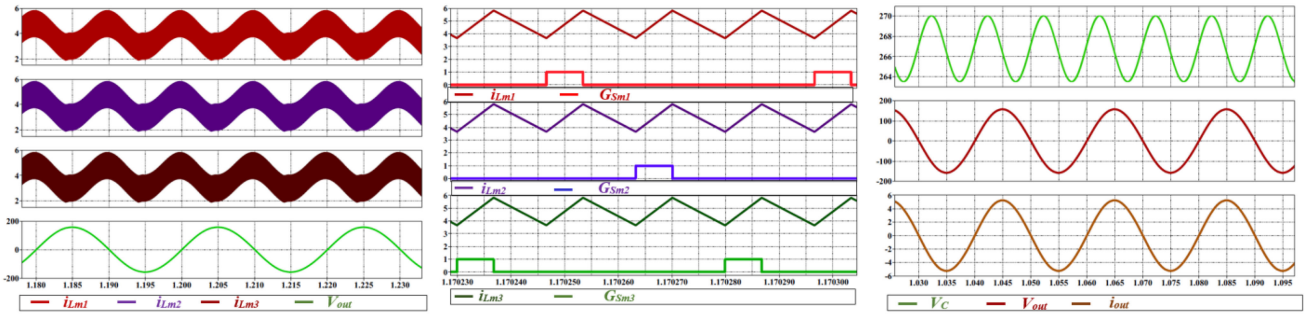


Fig. 11. Simulation results of a IQSBI with three interleaved phases. (a) Steady-state waveforms of the inductor currents (i_{Lm1}, i_{Lm2}, and i_{Lm3}), and the ac output voltage ($V_{\rm ac}$). (b) Inductor current ripple in the switching cycle ($T_s/2$) with the gate pulses of the interleaved switches (G_{Sm1}, G_{Sm2}, and G_{Sm3}). (c) Steady-state waveforms of the dc-link voltage (V_C), ac output voltage ($V_{\rm out}$), and ac output current ($i_{\rm out}$).

maintain the currents through the inductors. Inductors L_{m1} and L_{m2}, …, L_{mn} are connected in parallel and discharge themselves through D_a as shown in Table IV. In this interval, modulating signals *m(t)* and *–m(t),* as given in Fig. 5(a), decide the switching for the four switches of the inverter legs. Depending on the modulation index m_a, power and the zero intervals are distributed in the non shoot-through interval. Instantaneous voltage across the interleaved inductors and the current through the capacitor during this interval are listed in Table IV.

c) Shoot-through interval (ST_n), Ref: *Table IV:* The equivalent schematic of *n*-IQSBI during this interval ((D_nT_s) interval) is shown in Table IV. It is similar to ST_1 interval. Instead of turning ON S_{m1} in this mode, switches S_{mn} of phase "*n*" is turned ON along with inverter switches S_1 and S_4. Similar to ST_1, the inverter is in zero state in this interval too.

Inductor voltages (v_{Lm1}, v_{Lm2}, …, v_{Lmn}) and the capacitor current (i_C) in this interval are given in Table IV.

2) PLECS Simulation: Steady-state operation of an IQSBI with three interleaved phases is verified using PLECS simulation. Fig. 11(a) shows the waveforms of currents through the interleaved inductors (i_{Lm1}, i_{Lm2}, and i_{Lm3}), dc-link voltage (V_C), and the ac output voltage ($V_{\rm out}$). An ac output voltage of 110 V (V_m = 155 V) is obtained from a dc input voltage ($V_{\rm dc}$) of 48 V. Hence, an ac gain of 3.24 is achieved at a duty cycle of 0.41 and modulation index (m_a) of 0.59. Waveforms of inductor currents with the gate pulses of the interleaved switches (G_{Sm1}, G_{Sm2}, and G_{Sm3}) are shown in Fig. 11(b). Steady-state waveforms of ac output voltage ($V_{\rm out}$), ac output current ($i_{\rm out}$), and the dc-link voltage (V_C) are shown in Fig. 11(c).

3) Gain Characteristic: To derive a relation between the dc-link voltage (V_C) and $V_{\rm dc}$, voltage across the interleaved inductors and the capacitor current as given in Table III are averaged over one switching period (T_s), as given in (11). Solving the averaged equations, considering equal DCR and shoot-through intervals, and using I_i as obtained from (4), the dc-link voltage (V_C) can be expressed as follows:

$$V_C = \frac{V_{\rm dc}}{(1-2D) + \frac{{m_a}^2}{2nR_{\rm ac}(1-2D)} r_L}. \tag{12}$$

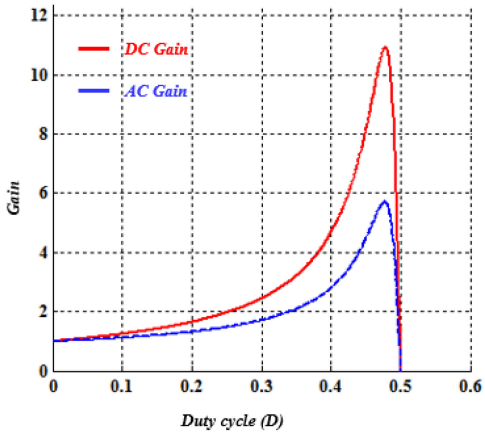


Fig. 12. Gain characteristic of IQSBI.

Hence, the dc gain and the ac gain can be expressed as follows:

$$\frac{V_C}{V_{\rm dc}} = \frac{1}{(1-2D) + \frac{{m_a}^2}{2nR_{\rm ac}(1-2D)} r_L} \tag{13}$$

$$\frac{V_m}{V_{\rm dc}} = \frac{m_a}{(1-2D) + \frac{{m_a}^2}{2nR_{\rm ac}(1-2D)} r_L}. \tag{14}$$

The dc gain and ac gain of *n*-IQSBI [(13), (14)] are plotted in Fig. 12, with respect to varying duty cycle (*D*). The plot in Fig. 12 is obtained at the boundary condition as given in (1). From (13) and (14), it is evident that the dc and ac gain of *n*-IQSBI is independent of the number of phases (*n*). Hence, the maximum achievable dc and ac gain in case of *n*-IQSBI is significantly lower as compared with that of *n*-ICFSI and *n*-ISBI.

IV. Small Signal and Loss Analysis of *N* –ICFSI

A. Small-Signal Analysis

For analyzing the dynamic or small-signal characteristics of *n*-ICFSI, the averaged equation given in (2) are perturbed around the dc operating point. $\hat{v}_{\rm dc}$, $\hat{v}_C$, $\hat{i}_{L_{m1}}$, $\hat{i}_{Lm_2}$, $\hat{i}_i$, $\hat{d}_1$, $\hat{d}_2$, …, $\hat{d}_n$ are the small perturbations near the dc operating bias points $V_{\rm dc}$, V_C, I_{Lm1}, I_{Lm2}, I_i, D_1 and D_2, …, D_n, respectively. After the addition of small-signal perturbations in (2), the higher order

TABLE V
SMALL-SIGNAL ANALYSIS OF ICFSI

After adding the small perturbations $\hat{v}_{dc}$, $\hat{v}_C$, $\hat{\imath}_{Lm_1}$, $\hat{\imath}_{Lm_2}$, $\hat{\imath}_i$, $\hat{d}_1$, and $\hat{d}_2$ near the DC operating bias points V_{dc}, V_C, I_{Lm1}, I_{Lm2}, I_i, D_1 and D_2, respectively, averaged equations as given in Table. I can be written as follows.

$C\frac{d\hat{v}_C}{dt}$	$\hat{\imath}_{Lm_1}(1-nD_1-D_2-..D_n)+\hat{\imath}_{Lm_2}(1-nD_2-D_1-..D_n)+\cdots\hat{\imath}_{Lm_n}(1-nD_n-D_1-..D_{(n-1)})$ $-I_{Lm_1}(n\hat{d}_1+\hat{d}_2+..\hat{d}_n)\quad -I_{Lm_2}(\hat{d}_1+n\hat{d}_2+..\hat{d}_n)-..\ I_{Lm_2}(\hat{d}_1+n\hat{d}_n+..\hat{d}_{(n-1)})\quad -\hat{\imath}_i(1-D_1-D_2-..D_n)$ $+I_i(\hat{d}_1+\hat{d}_2+..\hat{d}_n)$
$L_1\frac{d\hat{\imath}_{Lm_1}}{dt}$	$\hat{v}_{dc}-r_{L_1}\hat{\imath}_{Lm_1}-\hat{v}_C(1-nD_1-D_2-..D_n)+V_C(n\hat{d}_1+\hat{d}_2+..\hat{d}_n)$
$L_2\frac{d\hat{\imath}_{Lm_2}}{dt}$	$\hat{v}_{dc}-r_{L_2}\hat{\imath}_{Lm_2}-\hat{v}_C(1-nD_2-D_1-..D_n)+V_C(n\hat{d}_2+\hat{d}_1+..\hat{d}_n)$
⋮	⋮
$L_n\frac{d\hat{\imath}_{Lm_n}}{dt}$	$\hat{v}_{dc}-r_{L_n}\hat{\imath}_{Lmn}-\hat{v}_C\left(1-nD_n-D_1-..D_{(n-1)}\right)+V_C\left(n\hat{d}_n+\hat{d}_1+..\hat{d}_{(n-1)}\right)$

Control to output transfer functions

$$\begin{bmatrix}\hat{v}_C(s)\\ \hat{\imath}_{Lm_1}(s)\\ \hat{\imath}_{Lm_2}(s)\\ \vdots\\ \hat{\imath}_{Lm_n}(s)\end{bmatrix}=\begin{bmatrix}G_{vd1}(s) & G_{vd2}(s) & \cdots & G_{vdn}(s) & G_i(s) & G_a(s)\\ G_{id11}(s) & G_{id12}(s) & \cdots & G_{id1n}(s) & G_{im1}(s) & G_{a1}(s)\\ G_{id12}(s) & G_{id22}(s) & \cdots & G_{id1n}(s) & G_{im2}(s) & G_{a2}(s)\\ \vdots & \vdots & \cdots & \vdots & \vdots & \vdots\\ G_{id1n}(s) & G_{id2n}(s) & \cdots & G_{idnn}(s) & G_{imn}(s) & G_{an}(s)\end{bmatrix}\begin{bmatrix}\hat{d}_1(s)\\ \hat{d}_2(s)\\ \vdots\\ \hat{d}_n(s)\\ \hat{\imath}_i(s)\\ \hat{v}_{dc}(s)\end{bmatrix}$$

In order to derive the control to output transfer function, perturbations in DC input voltage ($\hat{v}_{dc}$), and the inverter current ($\hat{\imath}_i$) are considered to be zero. Hence the open loop transfer function ($\frac{\hat{v}_C}{\hat{d}}$), for the system can be expressed as follows. (Here L_{m1}, L_{m2}, ...L_{mn}=L and r_{L1}, r_{L2},..r_{Ln}=r_L D_1, D_2, ...D_n = (D/n), $\hat{d}_1, \hat{d}_2..\hat{d}_n = \frac{\hat{d}}{n}$)

$$G_{vd}(s)=\left.\frac{\hat{v}_c(s)}{\hat{d}(s)}\right|_{\hat{d}_2,..\hat{d}_n=0}=G_d\,\frac{(1+a_1s)}{(1+b_1s+b_2s^2)}$$

$$a_1=\frac{L[I_i-(1+\frac{1}{n})\{I_{Lm1}+I_{Lm2}+\cdots I_{Lmn}\}]}{\left(1+\frac{1}{n}\right)n\left(1-D-\frac{D}{n}\right)V_C+r_L[I_i-(1+\frac{1}{n})\{I_{Lm1}+I_{Lm2}+\cdots I_{Lmn}\}]}$$

$$b_1=\frac{r_LLC}{n(1-D-\frac{D}{n})^2}\qquad b_2=\frac{LC}{n(1-D-\frac{D}{n})^2}$$

$$G_d=\frac{r_L\left[I_i-\left(1+\frac{1}{n}\right)\{I_{Lm1}+I_{Lm2}+\cdots I_{Lmn}\}\right]+n(1+\frac{1}{n})(1-D-\frac{D}{n})V_C}{n(1-D-\frac{D}{n})^2}$$

Estimation of steady state operating conditions for specified AC gain (V_m/V_{dc}= G), DCR (r_L), and AC resistance ($R_{ac}=\frac{{V_m}^2}{2P}$) (Where P is the power rating)

Step 1 **Duty Cycle (*D*)**	$a=\left[1+0.5\left(n+\frac{1}{n}\right)\right]+\frac{r_L}{4R_{ac}}-(\frac{1}{G})[0.5(n+1)]$ $b=-[n+1]-\frac{r_L}{2R_{ac}}-(\frac{1}{G})[n+0.5]$ $c=\frac{n}{2}+\frac{r_L}{4R_{ac}}-(\frac{1}{G})[\frac{n}{2}]$ $D=\frac{(-b)-\sqrt{b^2-4*a*c}}{2(a)}$	**Step 2** **DC link voltage (V_C)**	$V_C=\frac{V_{dc}}{\left[1-D-\frac{D}{n}\right]}+\frac{(1-D)^2r_L}{2nR_{ac}\left[1-D-\frac{D}{n}\right]}$	**Step 3** **Inductor currents (I_{Lm1}, I_{Lm2},...I_{Lmn}= I_L)**	$I_L=\frac{0.5{m_a}^2V_{dc}{r_L}^{(n-1)}}{nr_LR_{ac}\left[1-D-\frac{D}{n}\right]^2+0.5{r_L}^n{m_a}^2}$	**Step 4** **Inverter current (I_i)**	$I_L=\frac{{m_a}^2V_C}{2R_{ac}(1-D)}$

terms and the perturbations other than that in the duty cycle are neglected. Derivation of the control to output transfer function and mathematical formulation of the plant transfer function in terms of the number of phases (n) and dc operating bias points are given in Table V. In order to obtain the plant transfer function, dc operating bias points of ICFSI for a specific ac gain ($V_m/V_{\mathrm{dc}} = G$), with given DCR (r_L), and load resistance (R_{ac}) have to be estimated. Using the steps as listed in Table V, bias points of the converter are evaluated and are further used to obtain the control to output transfer function of ICFSI ($G_{vd}(s)$). Magnitude and phase response of $G_{vd}(s)$ with respect to the frequency and number of phases (n) is plotted in Fig. 13. The dc operating bias points for obtaining the plot are estimated for an ac gain of 3.24 and a power rating of 300 W. DCR of 0.21 Ω is considered for the estimation. As shown in the figure, with the increase in "n," the dc gain and the resonant frequency of the plant transfer function increase slightly. Above small-signal analysis can be extended to analyze the dynamic characteristics of n-SBI and n-QSBI.

B. PLECS Simulation of Closed-Loop Operation

Open-loop transfer function (G_d (s)) for ICFSI with three interleaved phases is derived using the small-signal analysis as given in Table V. For closed-loop operation of ICFSI, the

TABLE VI
ANALYSIS OF CONDUCTION LOSS IN *N*-ICFSI

Estimation of steady state operating conditions for specified AC gain (V_m/V_{dc}= G), DCR (r_L), ON state resistance of the switches (r_{dson}), ON state resistance of diode (r_d), forward voltage drop of the diodes (V_f), and AC resistance ($R_{ac}=\frac{V_m^2}{2P}$) (Where P is the power rating)					
Step 1 **Duty Cycle (D)**	$a=\left[1+0.5\left(n+\frac{1}{n}\right)\right]+\frac{r_L}{4R_{ac}}-(\frac{1}{G})[0.5(n+1)]$ $b=-[n+1]-\frac{r_L}{2R_{ac}}-(\frac{1}{G})[n+0.5]$ $c=\frac{n}{2}+\frac{r_L}{4R_{ac}}-(\frac{1}{G})[\frac{n}{2}]$ $D=\frac{(-b)-\sqrt{b^2-4*a*c}}{2(a)}$	**Step 2** **DC link voltage (V_C)**	$V_C=\frac{V_{dc}}{\left[1-D-\frac{D}{n}\right]}+\frac{(1-D)^2 r_L}{2nR_{ac}\left[1-D-\frac{D}{n}\right]}$	**Step 3** **Inductor currents (I_{Lm1}, I_{Lm2},…I_{Lmn}=I_L)**	$I_L=\frac{0.5{m_a}^2{V_{dc}}r_L}{nr_L R_{ac}\left[1-D-\frac{D}{n}\right]^2+0.5{r_L}^n{m_a}^2}$
Loss Calculation for $D_1=D_2=\ldots D_n=D/n$					
Conduction loss in switches	$r_{dson}[({I_{Lm1}}^2 D_1)+({I_{Lm2}}^2 D_2)+\cdots\ldots.({I_{Lmn}}^2 D_n)]$				
Conduction loss in inductor	$({I_{Lm1}}^2 r_{L1})+({I_{Lm2}}^2 r_{L2})+\cdots\ldots\ldots({I_{Lmn}}^2 r_{Ln})$				
Conduction loss in diode (D_a)	$[(I_{Lm1}+I_{Lm2}+\cdots I_{Lmn})^2(1-D)r_d]+[(I_{Lm1}+I_{Lm2}+\cdots I_{Lmn})(1-D)V_f]$				
Conduction loss in diodes	$[\{{I_{Lm1}}^2(1-D+D_1)r_d\}+\{I_{Lm1}(1-D+D_1)V_f\}]+\cdots.[\{{I_{Lmn}}^2(1-D+D_n)r_d\}+\{I_{Lm1}(1-D+D_n)V_f\}]$				

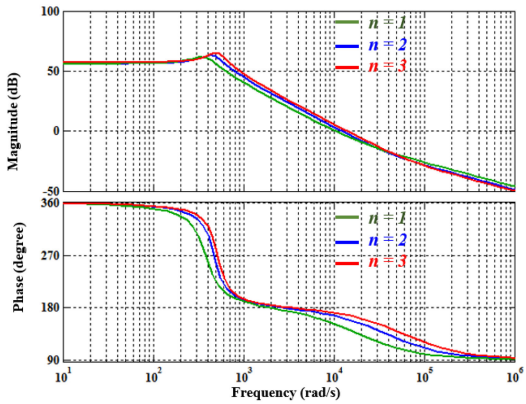


Fig. 13. Frequency response of ICFSI as number of phases varies from 1 to 3.

open-loop transfer function is used to obtain the dc voltage control transfer function ($H_{\mathrm{dc}}(s)$) as shown in Fig. 14(a). As shown in the figure, the output of the dc voltage controller (V_{ST}) is used in the proposed PWM scheme (see Fig. 4 of the updated manuscript) to generate the gate pulses for the switches (S_{m1}, S_{m2}, …, S_{mn}). Similarly, the output of the ac side control loop decides the modulation index (m_a), which is used in the PWM scheme to carry out the sine PWM and generate the gate pulses of the inverter leg switches (G_{S1} through G_{S4}).

Fig. 14(a) shows the control block diagram for closed-loop operation of an ICFSI with three interleaved phases. Closed loop performance of the inverter is verified through PLECS simulation as shown in Fig. 14(b). As shown in the figure, at $t=$ 1.2 s, a step increase in load (150 W) is introduced. Following the step increase, the ac output current (i_{out}) increases from 3 (RMS value) to 4.5 A. However, the dc-link voltage (V_C), and the ac output voltage (V_{out}) are regulated at the reference value of 518 and 110 V (RMS value), respectively. Similarly, following a step decrease in ac load (208 W), i_{out} decreases from 4.5 to 2.5 A, whereas V_C and V_{out} remain controlled at the reference values. AC output voltage (V_{out}) is scaled by 0.1 to show V_{out} and i_{out} in the same window.

C. Loss Analysis

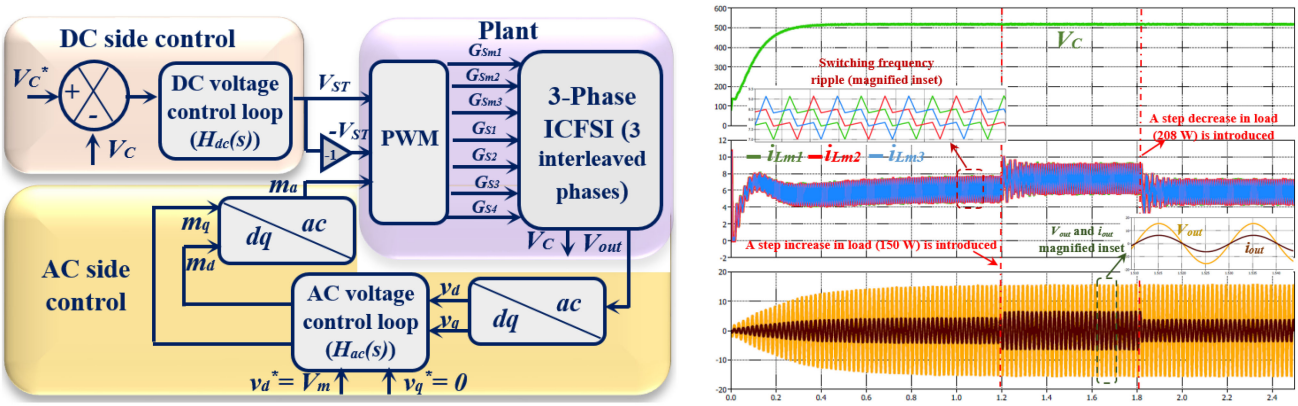
Conduction loss in various elements of the inverter is analyzed in Table VI (losses in the inverter stage are insignificant as compared to AFBS, hence neglected). In order to analyze the conduction loss, operating points of the converter are estimated for a specified ac gain (G), and ac resistance (R_{ac}). Based on these operating points, conduction loss in various elements is calculated by taking the non-ideal elements (r_{dson}, r_d, V_f) into consideration.

Conduction loss in the nonideal elements of an n-ICFSI with the increase in the number of interleaved phases (n) from 1 to 3 is plotted as well as tabulated in Fig. 15(a) for an ac gain of 3.24 and a power rating of 300 W. Breakout of the losses as plotted in the figure is obtained following the analysis as shown in Table VI. As shown in the figure, most dominant conduction loss, i.e., conduction loss in the interleaved inductors and the conduction loss in the diode (D_a) reduces by 67% and 45%, respectively, as n increases from 1 to 3. Fig. 15(b) shows the plot of total conduction loss vs. n. As depicted in the plot, 44% reduction in total conduction loss is achieved as the number of interleaved phases is increased from 1 to 3. It is inferred from the loss analysis (see Fig. 15) that paralleling and interleaving of AFBS result in significant reduction in the overall conduction loss thereby improving the efficiency.

V. VALIDATION OF *N*-ICFSI WITH THE PROPOSED PWM SCHEME

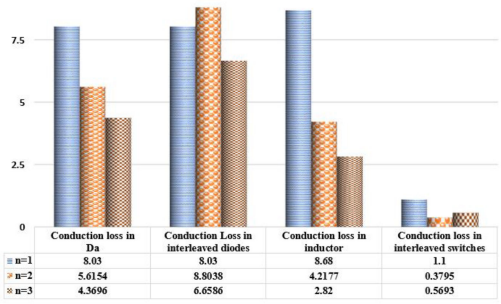
A prototype of 200-W ICFSI with three interleaved phases as shown in Fig. 16 has been developed to validate the theoretical analysis. The designed parameters and operating conditions for ICFSI are listed in Table VII.

PWM scheme as given in Fig. 5(a) and (b) is implemented using the EPWM module of DSP (TMS320F28335) to generate



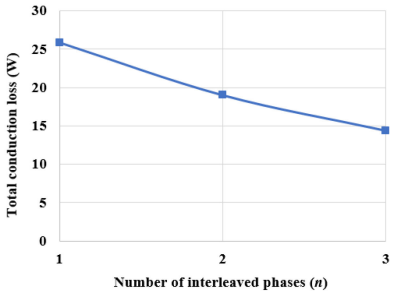
(a) (b)

Fig. 14. (a) Control block diagram of ICFSI with three interleaved phases. (b) PLECS simulation results of dc-link voltage (V_C), inductor currents (i_{Lm1}, i_{Lm2}, i_{Lm3}), ac output voltage (V_{out}), and load current (i_{out}).



	Conduction loss in Da	Conduction Loss in interleaved diodes	Conduction loss in inductor	Conduction loss in interleaved switches
n=1	8.03	8.03	8.68	1.1
n=2	5.6154	8.8038	4.2177	0.3795
n=3	4.3696	6.6586	2.82	0.5693

(a)



(b)

Fig. 15. (a) Conduction loss breakout of n-ICFSI as number of interleaved phases (n) increases from 1 to 3. (b) Plot of total conduction loss vs n of n-ICFSI.

Fig. 16. Experimental prototype of a two-phase ICCFT.

the gate pulses for the switches. Fig. 17(a) shows the generated switching signals for the interleaved switches of the FBS. The proposed PWM scheme has been implemented with a T_s of 100 μs. As shown in Fig. 17(a), three phase shifted switching signals are generated with a phase shift of $T_s/4n = 8.3$ μs. Pulsewidth of the switching signals is $(D/6)T_s = 9.2$ μs. Switching frequency of these switching signal is 20 kHz. Gate pulses for the switches of the inverter legs with a switching frequency of 30 kHz are shown in Fig. 17(b). Hence, the switching frequency of the inverter leg switches is $n/2 = 1.5$ times that of the interleaved switches.

Fig. 17(c)–(e) depicts the steady-state waveforms of the three interleaved phases in switching cycles. Steady-state waveforms of inductor currents (i_{Lm1}, i_{Lm23}), ac output voltage (V_{out}), and dc-link voltage (V_C) are given in Fig. 17(f). A dc-link voltage (V_C) of 185 V and an ac output (V_{out}) of 56 V is obtained from a dc input of 48 V. According to (6), a dc gain of 3.85 and an ac gain of 1.65 is achieved at a duty cycle (D) of 0.55 and a modulation index (m_a) of 0.45. This verifies the theoretical analysis discussed in Section III.

In order to filter out the switching frequency component, an LC filter is used at the output of the inverter. The ac output voltage (V_{out}) of the inverter can be expressed in terms of V_{ac} and the filter parameters (L_f, and C_f) as follows:

$$V_{\text{out}} = V_{\text{ac}} \left[\frac{1}{1 + \frac{sL_f}{R_{\text{ac}}} + s^2 L_f C_f} \right]. \tag{15}$$

Hence

$$\frac{V_{\text{out}}}{V_{\text{ac}}} = \left[\frac{1}{1 + \frac{sL_f}{R_{\text{ac}}} + s^2 L_f C_f} \right]. \tag{16}$$

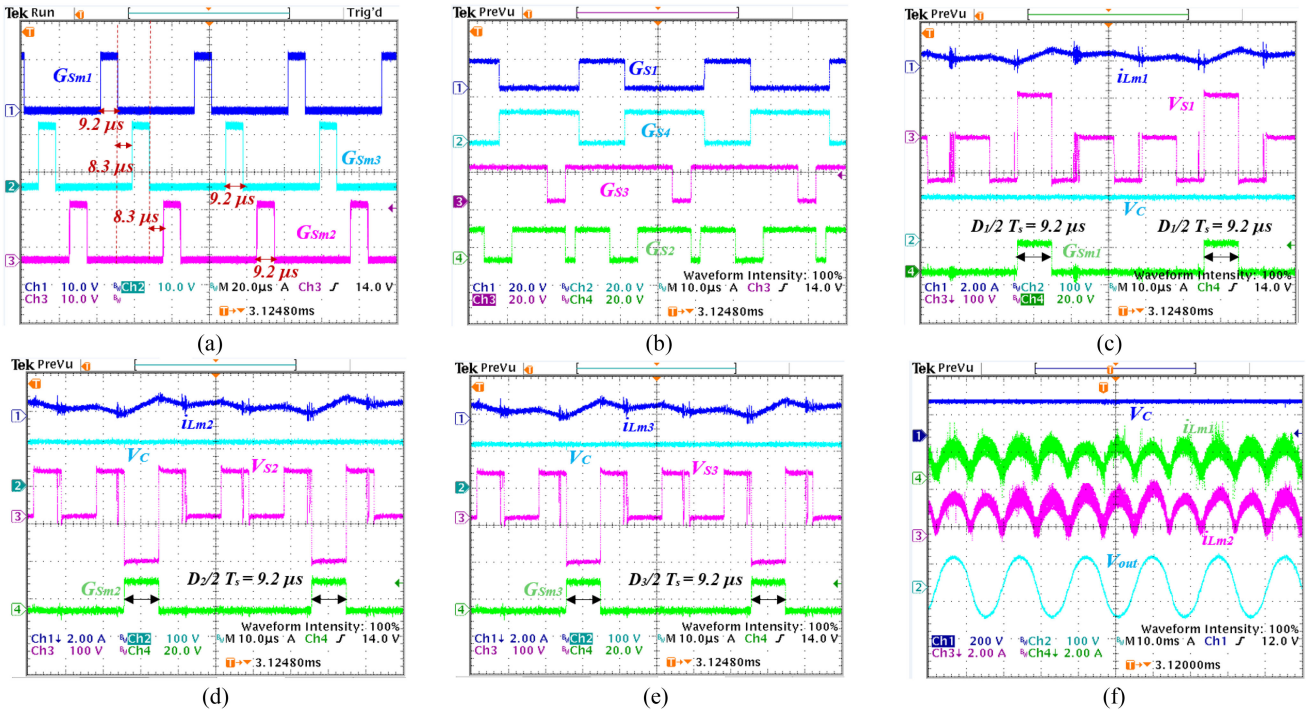


Fig. 17. (a) PWM pulses for the gates of the Boost-stage switches (S_{m1}, S_{m2}, and S_{m3}). (b) PWM pulses for the gates of the inverter-stage switches (S_1, S_2, S_3, and S_4) steady-state waveforms of inductor current, dc-link voltage, switching signal, and switch node voltage in switching cycle of ICFSI with three interleaved phases. (c) Phase 1 (i_{Lm1}, V_C, G_{Sm1}, and V_{S1}). (d) Phase 2 (i_{Lm2}, V_C, G_{Sm2}, and V_{S2}). (e) Phase 3 (i_{Lm3}, V_C, G_{Sm3}, and V_{S3}). (f) Steady-state waveforms of i_{Lm1} and i_{Lm2}, V_C, and V_{out} of ICFSI with three interleaved phases.

TABLE VII
OPERATING CONDITIONS AND PARAMETERS IN EXPERIMENTAL PROTOTYPE

Operating Conditions			Parameters		Devices and controller	
Input Voltage (V_{dc})	48 V (from a CHROMA PV emulator)		L_{m1}	1.49 mH	D_{m1}, D_{m2}, D_{m3} D_a	C3D10065A
DC gain	3.85		L_{m2}	1.45 mH	S_{m1}, S_{m2}, S_{m3}, S_1, S_2, S_3, and S_4	C3M0065090
AC gain	1.65		L_{m3}	1.3 mH		
Switching frequency	For interleaved switches	20 kHz	C	470 µF		
	For inverter leg switches	30 kHz	Filter parameters		Digital Controller	
			L_f	300 µH	TMS320F28335	
			C_f	10 µF		

The cutoff frequency (f_C) of the filter can be given as follows:

$$f_C = \frac{1}{2\pi\sqrt{L_f C_f}}. \tag{17}$$

For a fixed value of C_f, L_f can be expressed in terms of cutoff frequency as follows:

$$L_f = \frac{1}{4\pi^2 {f_C}^2 C_f}. \tag{18}$$

In order to filter out the switching frequency component, the cutoff frequency (f_C) of the filter is chosen to be 1 decade lower than that of the switching frequency (f_s) of the inverter. Hence, (18) can be represented in terms of f_s as follows:

$$L_f = \frac{100}{4\pi^2 {f_s}^2 C_f}. \tag{19}$$

As discussed previously, the switching frequency of the inverter-stage (f_s) is ($\frac{n}{2}$) times that of the switching frequency of the FBS switches (f_{sb}), where n is the number of interleaved phases. Hence, for a fixed f_{sb}, f_C and (5) in terms of n can be given as follows:

$$f_C = \frac{n}{20} f_{sb} \tag{20}$$

$$L_f = \frac{100}{\pi^2 n^2 {f_{sb}}^2 C_f}. \tag{21}$$

It can be inferred from (21) with the increase in the number of interleaved phases (n), the size of the filter inductor reduces, which leads to improvement in the power density of the system. For the prototype validation of an ICFSI with three interleaved phases, an inductor with a ferrite core and ac film capacitor are used as L_f and C_f. Parameters of the filter circuit are given in Table VII.

Fig. 18(a) shows the steady-state waveforms of ac output voltage (V_{out}), ac output current (i_{out}), and the dc-link voltage (V_C). As shown in the figure, the output voltage and the current are in phase, as the inverter is operated with a resistive load. Steady-state waveforms of the currents through three interleaved

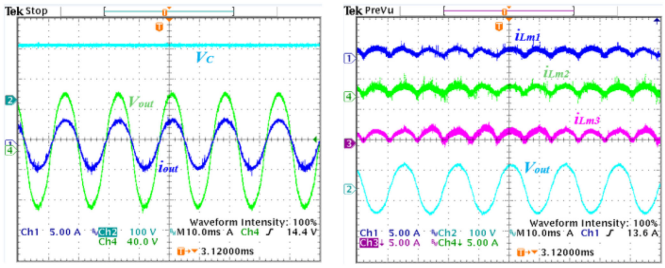


Fig. 18. Steady-state waveforms of (a) V_C, V_{out}, and i_{out}. (b) i_{Lm1} and i_{Lm2}, i_{Lm3}, and V_{out} of ICFSI with three interleaved phases.

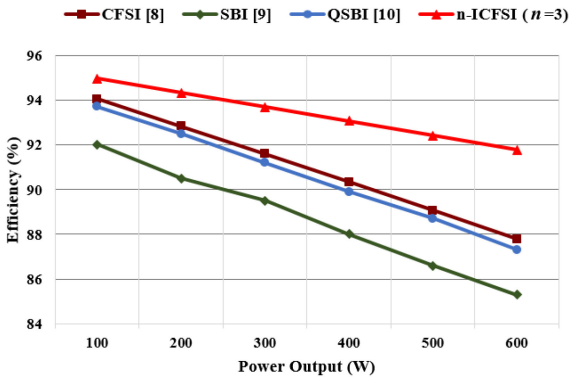


Fig. 19. Comparison of efficiency between the converters proposed in [8]–[10] and n-ICFSI.

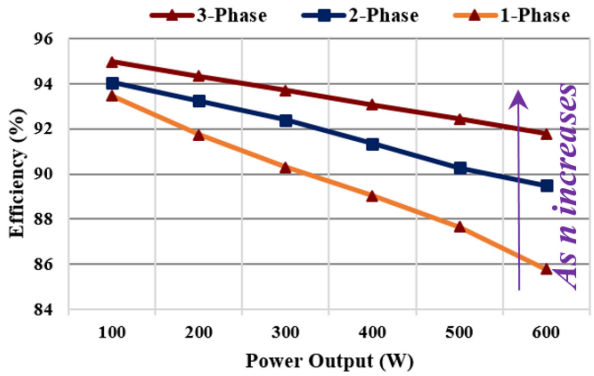


Fig. 20. Efficiency curve of interleaved current fed switched inverter (ICFSI) as the number of phases increases from 1 to 3.

inductors (i_{Lm1}, i_{Lm2}, and i_{Lm3}) V_{out} are shown in Fig. 18(b). As depicted in the figure, inductor currents have a ripple at the frequency twice that of the frequency of V_{out}. This is due to the fact that the inductors act as the low-frequency energy storage elements to cater to the mismatch between the instantaneous ac output power and the dc input power.

Fig. 19 shows the comparison of analytical efficiency between converters proposed in [8]–[10], and n-ICFSI with two interleaved phases. It is evident from the figure that interleaving results in significant improvement in efficiency.

Fig. 20 shows the analytical efficiency curve of an ICFSI, as the number of interleaved phases ("n") increases from 1 to 3. It is evident from the figure with the increase in "n," the efficiency of the inverter improves significantly. At 200 W, the efficiency of the inverter improves by nearly 3%.

VI. Conclusion

This article proposes a generalized PWM scheme for interleaved topologies of active FBS-based ZSIs. Three case studies are carried out to implement the proposed PWM scheme in ICFSI, interleaved SBI, and interleaved Q-SBI with "n" interleaved phases. Steady-state behavior of the inverters based on the PWM scheme is discussed in the presented work. Improvement in the gain characteristic of n-ICFSI and n-ISBI with the increase in the number of interleaved phases is also presented. Steady-state operation of these topologies with three interleaved phases is verified using the PLECS simulation. Steady-state operation of an ICFSI with interleaved phases is verified experimentally using a 200-W proof of concept prototype. Increase in the efficiency as a result of interleaving of the FBSs in CFSI is reported.

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