Modified *LLC* Resonant Converter With *LC* Antiresonant Circuit in Parallel Branch for Wide Voltage Range Application

Xiqi Wu, Rui Li, *Senior Member, IEEE*, and Xu Cai, *Senior Member, IEEE*

***Abstract*—In this article, a modified *LLC* resonant converter with *LC* antiresonant circuit in parallel branch is proposed. The proposed converter is derived by placing *LC* antiresonant circuit on parallel branch. In comparison with *LLC* resonant converter, the equivalent inductance of parallel branch of the proposed converter decreases along with switching frequency within regulating frequency range. This advantageous property contributes for that the turn-OFF current and circulating conduction loss in the primary side can be reduced at unity voltage conversion ratio due to large impedance of *LC* antiresonant circuit. Moreover, by optimizing resonant parameters design of parallel branch based on time-domain analysis, the magnetizing current is in close proximity to a sine wave and the conduction loss in the secondary side will be reduced, especially in the light load. A higher voltage conversion ratio can be achieved at low switching frequency due to decreased impedance in parallel branch. In addition, a design flowchart and a design practical case are given to help to implement an efficiency optimization algorithm to decide five resonant design parameters. Finally, a 2 kW 250 V—400 V-input and 48 V-output prototype is built, and the main experimental results are provided to verify the feasibility of the proposed converter and compare with *LLC* resonant converter. Comparative state-plane trajectories are depicted to compare their characteristics and to verify the model-domain analysis.**

***Index Terms*—*LC* antiresonant circuit, *LLC* converter, resonant converter, wide voltage range.**

I. Introduction

IN MANY dc–dc power conversion applications, such as battery energy storage, server power supply, and new energy electric vehicle, isolated dc–dc converter with capabilities of wide voltage regulation and high efficiency gathers momentum [1]. Among various resonant and nonresonant dc–dc topologies, *LLC* resonant converter shows good soft switching characteristic including zero voltage switching (ZVS) for active switches and zero current switching (ZCS) for rectifier diodes at whole load range and whole wide voltage range when operating below resonant frequency [2], [3]. Despite widely applied in industry and deeply studies in academia, there are still many tradeoffs between wide voltage range, power density, and efficiency to meet needs of different applications.

The magnetizing current of the high-frequency (HF) transformer can be utilized for ZVS under the wide load conditions. This current charges and discharges the junction capacitance of primary switches during dead time and its value is usually not large [4], [5]. When the switching frequency is below the resonant frequency and after rectifier diodes turn OFF under ZCS, the magnetizing inductance of HF transformer participates into resonance and gain above-mentioned unity is obtained [6]. A smaller ratio of the magnetizing inductance and resonant inductance, usually referred to as k value, is required to achieve larger voltage gain [7], [8]. However, a small k value leads to the decreased magnetizing inductance and the increased magnetizing current with the same quality factor. As a result, primary switches turn OFF at a larger current and the primary conduction loss increases [9], [10] since the current flowing the parallel magnetizing branch cannot transfer active power and increases primary rms current.

As a solution for this technical problem, many pulsewide modulation (PWM) methods [11], [12], such as phase shift modulation, and current-fed *LLC* converter [13], [14], have been proposed. For full-bridge *LLC* converter, zero-level voltage can be generated by shifted phase of two full-bridge legs. Therefore, the first harmonic input voltage of resonant tank is regulated by duty cycle of zero-level voltage [15]. Although it can be effective for regulating voltage gain with fixed switching frequency, this technique raises some severe problems compared with pulse-frequency modulation (PFM). A large shifted-phase under light load results in long freewheel time, which leads to that the magnetizing current decreases to a low value and thus the zero-voltage-switching condition of lagging bridge cannot be achieved [16], [17]. In addition, excessively small pulse width of positive-level results to that the active switches of primary side turn OFF at peak of resonant current, which deteriorates efficiency performance like [18] and current-fed *LLC* converter in [14].

Topological variant is a more advantageous solution for wide voltage range. Restructuring the circuit using active switches is

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one way of topological variant and has been proposed in [19] and [20]. In [19], full-bridge *LLC* converter can operate either in full-bridge mode or in half-bridge mode. Since it can switch between the two modes under different voltage gain, it is named topology morphing control. However, the voltage gain range is two times as large in each mode and the tradeoff between wide voltage range and efficiency is still necessary. Similarly, aiming at more modes to achieve wider gain, more active switches are employed in [21] and [22], which brings additional power loss and corresponding cost.

Modifying the structure of resonant network is regarded as another way of topological variant. The method can introduce some good characteristic to improve performance of *LLC* resonant converter [23]–[25]. Among those literature studies, a *LCLC* dc–dc converter for hold-up time has been proposed in [24]. Instead of the magnetizing inductance parallel with load, the parallel branch is composed of an inductor and a capacitor in series. This converter has the following advantages: 1) in normal operation, the *LCLC* converter is equivalent to an *LLC* converter with a large magnetizing inductor, so that the magnetizing current that is circulating on the primary side will be low; and 2) for hold-up operation, when the input voltage reduces, the magnetizing inductor reduces along with the switching frequency, thus, the output-to-input voltage gain increases, and the operational input voltage range is extended. Similar method is adopted in [25]. However, a single inductor and an extra film capacitor are added as a parallel branch and the magnetizing inductance of transformer is wasted and not used to its full potential. Besides, there is a risk of short circuiting, due to the zero impedance at series resonance of the auxiliary inductor and the auxiliary capacitor at their resonance frequency.

LC antiresonant circuit, also called as *LC* parallel-resonant circuit, features the rapid increase of impedance around its resonant frequency. Ideally, the impedance of *LC* antiresonant circuit approaches infinity. Thereby, the antiresonant circuitry-applied dc–dc converter has been proposed in [26] for overcurrent protection (OCP) under the short circuit and overload conditions as well as the start-up process. In addition to the merit of OCP, by injecting the third-harmonic current by the effect of the antiresonance, the harmonic component can be utilized to transfer the active power, which is discussed in [27]. However, evaluation on the performance and parameter design guideline is not deeply analyzed with experimental verifications in [26] and [27]. These critical problems are discussed step-by-step in [28]–[31] and complete experimental verifications about soft-switching performance, output voltage and power regulations, and power conversion efficiency are given in [32] and [33]. One claimed advantage of the converter in [33] is that the PFM scheme contribute for a wider range of buck voltage regulation with a smaller band of switching frequency variations. This characteristic is named by the authors as "sensitivity-improved PFM." Due to the equivalent inductance of *LC* antiresonant circuit increasing along with frequency, *k* value decreases as the frequency increases. Therefore, the buck operation can achieve wider range of voltage regulation. The peak gain of boost mode, however, is reduced since *k* value increases as the frequency decreases on the left of resonant frequency. Besides, boost mode is more adaptable to regulate gain without reverse recovery of diodes and large turn-OFF current compared with buck mode [34], [35]. Furthermore, the parallel branch is the magnetizing inductance and then the problem of deteriorated efficiency for wide voltage gain has not been addressed yet.

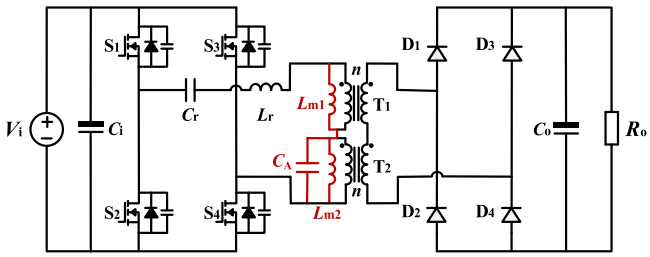

Fig. 1. Schematic of the proposed *LLC* converter with *LC* antiresonant circuit in parallel branch.

If *LC* antiresonant circuit is added in parallel branch, the equivalent *k* value decreases as the frequency decreases below antiresonant frequency. On this basis, a modified *LLC* resonant converter with *LC* antiresonant circuit in parallel branch is proposed in this article. The equivalent inductance of parallel branch of the proposed converter decreases along with switching frequency within regulating frequency range. At unity voltage conversion ratio, low turn-OFF current, and circulating conduction loss are realized in the primary side due to large impedance of *LC* antiresonant circuit. Furthermore, this article presents optimal resonant parameters design of parallel branch based on time-domain analysis; then the magnetizing current is in close proximity to a sine wave and the conduction loss in the secondary side will be reduced, especially in the light load. Additionally, the proposed converter have high voltage conversion ratio at low switching frequency due to decreased impedance in parallel branch. The converter is always operating in boost mode and extra inductor is not needed for *LC* antiresonant circuit by using magnetizing inductance of transformer.

The rest of this article is organized as follows. The steady-state analysis and voltage conversion ratio of proposed topology as well as its operational principle are theoretically described in Section II. The resonant parameters design of parallel branch based on time-domain analysis and optimal parameters design of series resonant tank are explained in Section III, whereby the mechanism behind the reduced conduction loss in the secondary side is revealed. Section IV presents the design case of prototype converter and experimental results, compared with the *LLC* converter. The accuracy of time-domain models is verified by state-plane trajectories in this section. Section V concludes this article.

II. Steady-State Analysis of the Proposed Topology and Operational Principle

Fig. 1 presents the circuit diagram of the proposed converter. L_r and C_r are the series resonant inductor and capacitor and their resonant frequency is named series resonant frequency ($f_r = 1/(2\pi\sqrt{L_rC_r})$). Two transformers ($T_1$ and T_2) with the same turn ratio ($n = N_P/N_S$) have series connection of respective

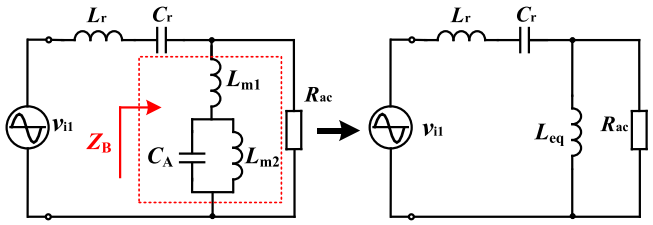

Fig. 2. FHA model of the proposed *LLC* converter.

primary and secondary windings. An auxiliary capacitor ($C_{\rm A}$) is parallel with the primary winding of T_2 and $C_{\rm A}$ and the magnetizing inductance of T_2 ($L_{\rm m2}$) form a *LC* antiresonant circuit. $f_{\rm p}$ is presented as parallel-resonant frequency of $C_{\rm A}$ and $L_{\rm m2}$. Accordingly, a new parallel branch, as shown in Fig. 2, is composed of the magnetizing inductances ($L_{\rm m1}$ and $L_{\rm m2}$) and $C_{\rm A}$.

A. Steady-State Analysis of the Proposed Converter

The first harmonic approximation (FHA) is still suitable for analyzing the proposed converter in steady state and its FHA model is demonstrated in Fig. 2. The fundamental component $v_{\rm i1}$ of the rectangular input voltage is defined by

$$v_{\rm i1}(t) = \frac{4}{\pi} V_{\rm i} \sin \omega_{\rm s} t \tag{1}$$

where $\omega_{\rm s} = 2\pi f_{\rm s}$ is the angular switching frequency and $f_{\rm s}$ is the switching frequency.

The equivalent load resistor after the rectifier network is as follows:

$$R_{\rm ac} = \frac{8n^2}{\pi^2} \cdot \frac{{V_{\rm o}}^2}{P_{\rm o}}. \tag{2}$$

By using the phasor method, the impedance $Z_{\rm B}$ of parallel branch are defined from Fig. 2 as

$$Z_{\rm B} = \left|\dot{Z}_{\rm B}\right| = \left| j\omega_{\rm s} L_{\rm m1} + \frac{j\omega_{\rm s} L_{\rm m2}}{1 - {\omega_{\rm s}}^2 L_{\rm m2} C_{\rm A}} \right|. \tag{3}$$

When the switching frequency is below $f_{\rm p} = 1/(2\pi\sqrt{L_{\rm m2}C_{\rm A}})$, the *LC* antiresonant circuit represents characteristic of inductor. Thereby, the parallel branch can be equivalent as inductor ($L_{\rm eq}$) and $L_{\rm eq}$ can be derived from Fig. 2 as

$$L_{\rm eq} = \frac{Z_{\rm B}}{\omega_{\rm s}} = L_{\rm m1} + \frac{L_{\rm m2}}{1 - \frac{{f_{\rm s}}^2}{{f_{\rm p}}^2}}. \tag{4}$$

After normalizing the equivalent inductor ($L_{\rm eqN}$) by $L_{\rm r}$, the equivalent inductance versus normalized switching frequency by $f_{\rm p}$ curves are drawn in Fig. 3 by referring to

$$L_{\rm eqN} = \frac{L_{\rm eq}}{L_{\rm r}} = k_1 + \frac{k_2}{1 - \frac{{f_{\rm s}}^2}{{f_{\rm p}}^2}} \tag{5}$$

where k_1 is the ratio of $L_{\rm m1}$ to $L_{\rm r}$ and k_2 is the ratio of $L_{\rm m2}$ to $L_{\rm r}$.

From (5), it could be concluded that the equivalent inductance decreases along with the switching frequency. Those curves in Fig. 3 indicate that k_2 has more significant influence on the variation of equivalent inductance within operating frequency range by the effect of *LC* antiresonant circuit.

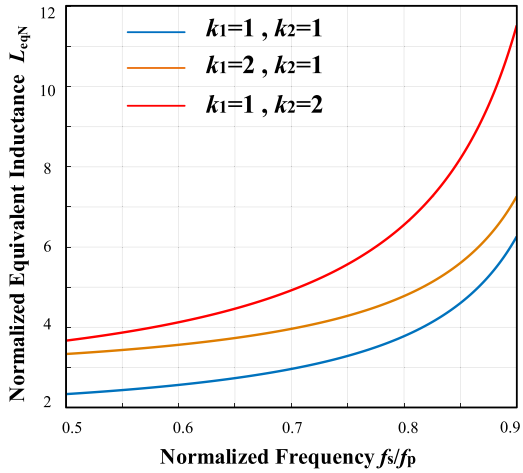

Fig. 3. Equivalent inductance versus switching frequency curves.

The voltage conversion ratio $M = nV_{\rm o}/V_{\rm i}$ of the *LLC* converter can be derived by using FHA as

$$M = \frac{1}{\sqrt{\left(1 + \frac{1}{k} - \frac{1}{k{F_{\rm sN}}^2}\right)^2 + Q^2\left(F_{\rm sN} - \frac{1}{F_{\rm sN}}\right)^2}} \tag{6}$$

where k is the ratio of magnetizing inductance to resonant inductance of *LLC* converter, Q is the quality factor, which are defined as $Q = \sqrt{L_{\rm r}/C_{\rm r}}/R_{\rm ac}$, $F_{\rm sN} = f_{\rm s}/f_{\rm r}$ is the normalized switching frequency by $f_{\rm r}$.

Based on (6), the theoretical voltage conversion ratio $G = nV_{\rm o}/V_{\rm i}$ of the proposed converter can be obtained by replacing the variable k in (6) with the $L_{\rm eqN}$ as (5)

$$G = \frac{1}{\sqrt{\left[1 + \frac{1}{k_1 + \frac{k_2}{1 - {F_{\rm sN}}^2/{F_{\rm pN}}^2}}\left(1 - \frac{1}{{F_{\rm sN}}^2}\right)\right]^2 + Q^2\left(F_{\rm sN} - \frac{1}{F_{\rm sN}}\right)^2}} \tag{7}$$

where $F_{\rm pN} = f_{\rm p}/f_{\rm r}$ is the normalized parallel-resonant frequency by $f_{\rm r}$.

Fig. 4 shows a series of voltage conversion ratio curves versus switching frequency at different load condition. The conventional and simple PFM can still be used. The voltage conversion ratio above unity is achieved below the series resonant frequency. In addition, ZVS for active switches and ZCS for rectifier diodes can be achieved in the ZVS region, in which the input impedance of converter is inductive. It should be noted that when the switching frequency is below the value corresponding to maximum gain, the converter enters into ZCS region, and soft-switching cannot be achieved.

The difference of voltage conversion ratio curves of the proposed converter and conventional *LLC* converter are illustrated in Fig. 5 by referring to (6) and (7). With the same Q value at full-load, they have the same goal that the maximum voltage conversion ratio $G_{\rm max}$ is achieved at the minimum switching

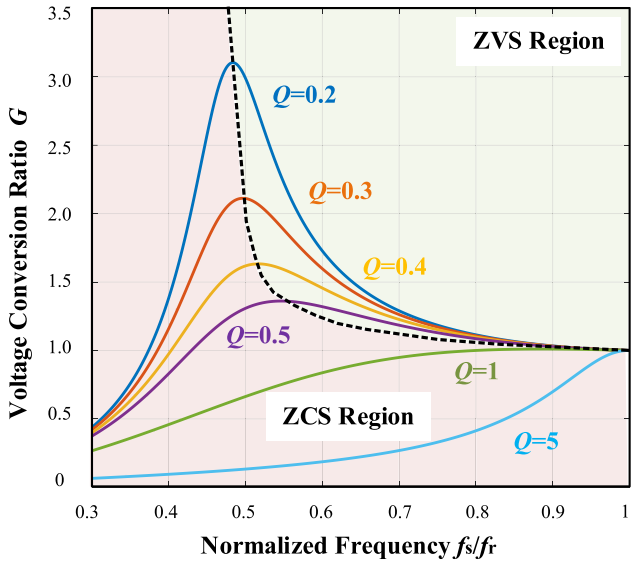

Fig. 4. Voltage conversion ratio curves versus switching frequency at different load conditions.

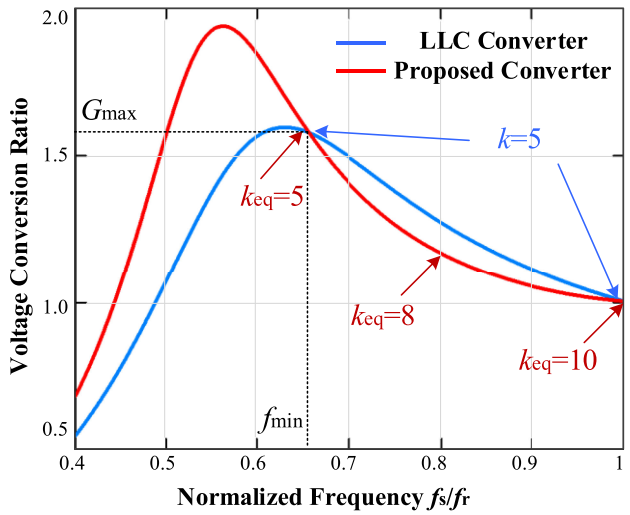

Fig. 5. Voltage conversion ratio curves of the proposed converter and conventional *LLC* converter.

frequency $f_{\min}$. In order to compare their characteristics, the equivalent ratio of magnetizing inductance to resonant inductance of proposed converter is defined as

$$k_{\rm eq} = L_{\rm eqN} = k_1 + \frac{k_2}{1 - {F_{\rm sN}}^2/{F_{\rm pN}}^2}. \tag{8}$$

At the point of unity voltage conversion ratio, the proposed converter has a larger $k_{\rm eq}$ value, which means it has a larger equivalent magnetizing inductor; thus, circulating conduction loss and turn-OFF current of primary switches at whole load range are lower than *LLC* converter.

As shown in Fig. 5, $k_{\rm eq}$ decreases to nearly identical value with k at $f_{\min}$; consequently, the maximum voltage conversion ratio, which needs a relatively smaller k value, can be achieved by the proposed converter.

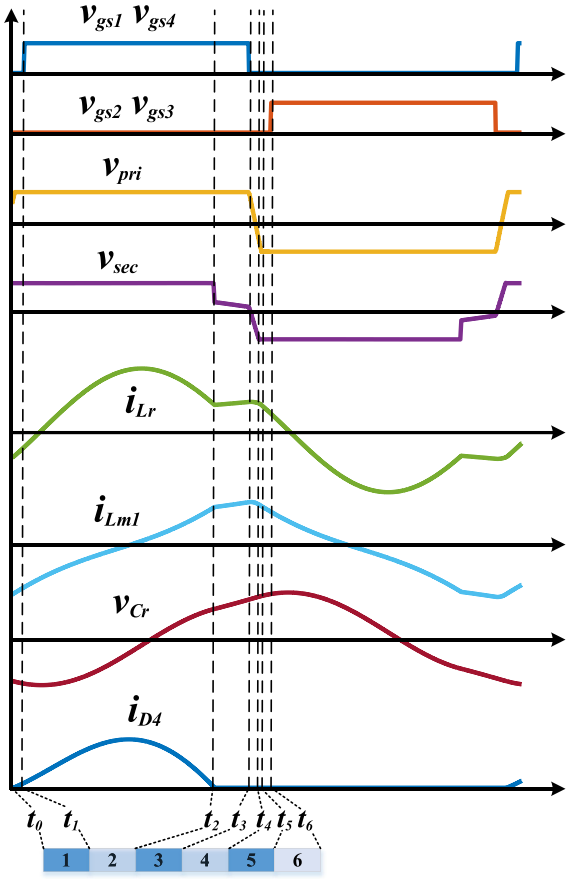

Fig. 6. Key operating waveforms of the proposed converter in ZVS region by PLECS simulation.

On the above basis, although the proposed converter has a large $k_{\rm eq}$ value at $f_{\rm r}$, the equivalent inductance decreases along with the switching frequency to achieve higher voltage conversion ratio. On the contrary, *LLC* converter has a constant k value that must be designed according to $G_{\max}$; thereby its efficiency will deteriorate at the other point of voltage conversion ratio.

B. Operational Principle of the Proposed Converter

The key operating waveforms of the proposed converter in ZVS region obtained by PLECS simulation is shown in Fig. 6 and it operational states are given in Fig. 7. The steady-state operation of the proposed converter can be divided into twelve states in one switching period. However, as a result of its symmetry, only six operational states are discussed in this section.

State 1 [t_0-t_1]: The rectifier diodes D_1 and D_4 are ON at t_0. The voltage across the parallel branch is clamped at $nV_{\rm o}$ and the parallel current is generated by resonance of $L_{\rm m1}$, $L_{\rm m2}$, and $C_{\rm A}$. The magnetizing current i_{Lm1} of T_1 is selected as the state variable to express the steady-state operations of the parallel branch. Its time-domain formula with three-order differential equations can be expressed as

$$\frac{d^3 i_{Lm1}}{dt^3} + \omega_{\rm P}^2 \frac{di_{Lm1}}{dt} = \omega_{\rm P}^2 \frac{nV_{\rm o}}{L_{\rm m1} + L_{\rm m2}} \tag{9}$$

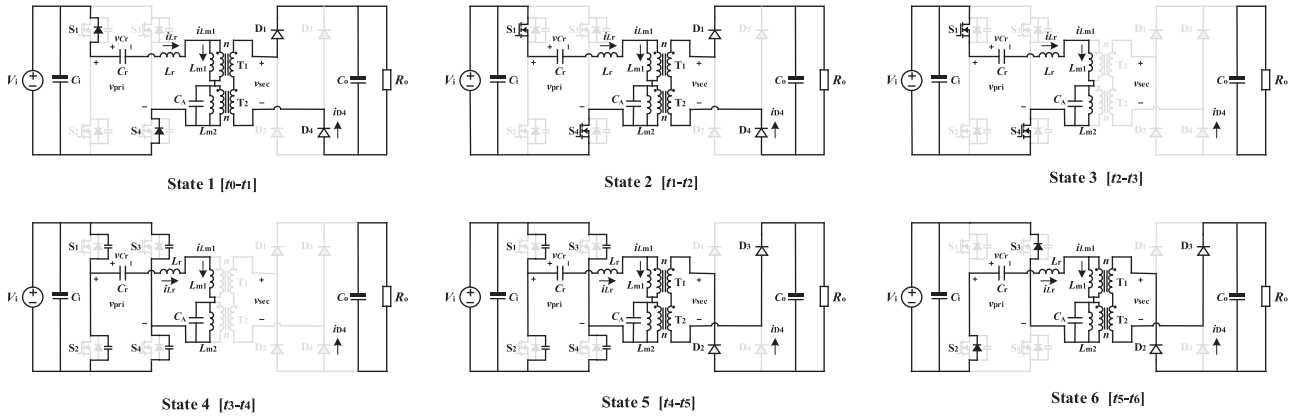

Fig. 7. Six operational states of the proposed converter in ZVS region.

where $\omega_{\rm P} = 1/\sqrt{\frac{L_{\rm m1}L_{\rm m2}}{L_{\rm m1}+L_{\rm m2}}C_{\rm A}}$ is the resonant angular switching frequency of parallel branch.

State 1 ends when S_1 and S_4 are ON under ZVS condition.

State 2 [t_1-t_2]: The main transferred energy from the input to output side occurs in state. $V_{\rm in}$-$nV_{\rm o}$ is applied to the series resonant inductor and capacitor. The resonant current i_{Lr} is selected as the state variable to express the steady-state operations of the series resonant tank. Its time-domain formula with two-order differential equations can be expressed as

$$\frac{d^2 i_{Lr}}{dt^2} + \omega_r^2 i_{Lr} = 0 \tag{10}$$

where $\omega_r = 1/\sqrt{L_r C_r}$ is the resonant angular switching frequency of the series resonant tank.

State 2 ends when the secondary-side current is naturally becomes zero; as a result, D_1 and D_4 is switched OFF under ZCS condition with a minimized reverse recovery current.

State 3 [t_2-t_3]: After D_1 and D_4 enter into discontinuous current mode, the parallel branch is not clamped by the output voltage and participates into resonance with the series resonant tank. The time-domain formula of i_{Lr} with four-order differential equations can be expressed as

$$\frac{d^4 i_{Lr}}{dt^4} + (\omega_{r1}^2 + \omega_{r2}^2)\frac{d^2 i_{Lr}}{dt^2} + \omega_{r1}^2\omega_{r3}^2 i_{Lr} = 0 \tag{11}$$

where $\omega_{r1} = 1/\sqrt{(L_r + L_{\rm m1})C_r}$, $\omega_{r2} = 1/\sqrt{\frac{(L_r+L_{\rm m1})L_{\rm m2}}{L_r+L_{\rm m1}+L_{\rm m2}}C_{\rm A}}$, and $\omega_{r3} = 1/\sqrt{L_{\rm m2}C_{\rm A}}$.

During this interval, the sum voltage $v_{\rm sec}$ of secondary winding of T_1 and T_2 is divided according to ratio of impendence of the parallel branch to that of the series resonant tank.

State 4 [t_3-t_4]: At t_3, S_1 and S_4 are OFF and the circuit enters into interval of dead-time ($t_{\rm dead}$). The parasitic capacitors ($C_{\rm oss}$) of S_1 and S_4 are charged by the inductive current, while the parasitic capacitors of S_2 and S_3 are discharged to maintain the constant bus voltage. As a result, the output voltage of H-bridge $v_{\rm pri}$ decreases from $V_{\rm i}$ to $-V_{\rm i}$

$$v_{\rm sec} = \frac{L_{\rm eq}(v_{\rm pri} - v_{Cr})}{n(L_{\rm r} + L_{\rm eq})}. \tag{12}$$

During this interval, the voltage of resonant capacitor v_{Cr} is almost unchanged, as shown in Fig. 6; then, $v_{\rm sec}$ decreases along with $v_{\rm pri}$ rapidly as (12). This interval ends when the $v_{\rm sec}$ meets as

$$\frac{L_{\rm eq}(v_{\rm pri} - v_{Cr})}{n(L_{\rm r} + L_{\rm eq})} = -V_{\rm o}. \tag{13}$$

State 5 [t_4-t_5]: The $v_{\rm sec}$ reaches to $-V_{\rm o}$ at t_4; as a result, the rectifier diodes D_2 and D_3 are ON under ZVS. During this interval, the parasitic capacitors are charged and discharged continuously until this process is completed.

State 6 [t_5-t_6]: When the parasitic capacitors are charged and discharged completely at t_5, the body diode of S_2 and S_3 are conducted forward. To achieve transition of soft-switching completely during the dead-time, the ZVS condition is expressed by

$$i_{Lr}(t_3)t_{\rm dead} > 4V_{\rm i}C_{\rm oss}. \tag{14}$$

This state ends when S_1 and S_4 are ON under ZVS condition. During the remaining switching period, the proposed converter operates in symmetry with states 1–6.

III. Design Consideration of the Proposed Converter

The design procedures of the proposed converter are similar with that of the *LLC* converter due to their similarity of operational principle as discussed before. However, although the parallel branch is equivalent to an inductor, three parameters should be selected, which is more complicated than *LLC* converter. Thus, this part will be discussed first in this section; then on this basis, the optimal parameters design of series resonant tank is analyzed.

A. Resonant Parameters Design of the Parallel Branch Based on Time-Domain Analysis

In this section, time-domain method is taken due to its high accuracy to design the resonant parameters of parallel branch. Ignoring the effect of dead-time, the equivalent circuit models at unity voltage conversion ratio with respect to the two topological stages over one switching period are plotted in Fig. 8(a) and (b),

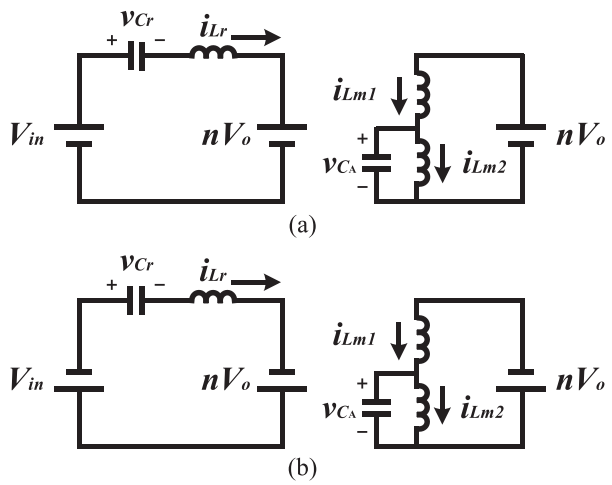

Fig. 8. Equivalent circuit models at unity voltage conversion ratio over one switching period. (a) Positive half-period. (b) Negative half-period.

respectively. According to Fig. 8, L_{r} always resonates with C_{r}, while the parallel branch is always excited by nV_{o}.

The positive half-period process in Fig. 8(a) can be expressed as (9) and (10) and the normalizing factors of current is

$$I_N = \frac{nV_{\mathrm{o}}}{\omega_{\mathrm{r}}(L_{\mathrm{m1}} + L_{\mathrm{m2}})} \tag{15}$$

m is defined as the ratio of ω_{P} to ω_{r} and the general solution for (9) is derived as

$$\frac{di_{\mathrm{Lm1}N}}{dt} = h_1 \sin[m\omega_{\mathrm{r}}(t - t_0) + \theta_1] + \omega_{\mathrm{r}} \tag{16}$$

where h_1 and θ_1 are the coefficients that depend on the initial conditions of the circuit $i_{\mathrm{Lm1}N} = i_{\mathrm{Lm1}}/I_{\mathrm{N}}$.

Since the derivations of $i_{\mathrm{Lm1}N}$ at t_0 and $t_0{+}1/(2f_{\mathrm{s}})$ are identical, one coefficient can be obtained as

$$\theta_1 = \arctan\left[\frac{\sin(m\pi)}{1 - \cos(m\pi)}\right]. \tag{17}$$

Combining (16) and (17), the expression for $i_{\mathrm{Lm1}N}$ can be expressed as

$$i_{\mathrm{Lm1}N} = -\frac{h_1}{m\omega_{\mathrm{r}}}\cos[m\omega_{\mathrm{r}}(t - t_0) + \theta_1] + \omega_{\mathrm{r}}(t - t_0) + h_2 \tag{18}$$

where h_2 is the coefficient that depend on the initial conditions of the circuit. Since the values of $i_{\mathrm{Lm1}N}$ at t_0 and $t_0{+}1/(2f_{\mathrm{s}})$ are symmetric, h_2 can be obtained as

$$h_2 = \frac{h_1}{m\omega_{\mathrm{r}}}\cos\left(\frac{m\pi}{2} + \theta_1\right)\cos\left(\frac{m\pi}{2}\right) - \frac{\pi}{2}. \tag{19}$$

By substituting (19) into (18), the magnetizing current i_{Lm1} is solved out as

$$i_{\mathrm{Lm1}N} = \frac{h_1}{m\omega_{\mathrm{r}}}\left[\cos\left(\frac{m\pi}{2} + \theta_1\right)\cos\left(\frac{m\pi}{2}\right) - \cos[m\omega_{\mathrm{r}}(t - t_0) + \theta_1]\right] + \omega_{\mathrm{r}}(t - t_0) - \frac{\pi}{2}. \tag{20}$$

The general solution for (10) is derived as

$$i_{LrN} = h_3 \cos[\omega_{\mathrm{r}}(t - t_0) + \theta_2] \tag{21}$$

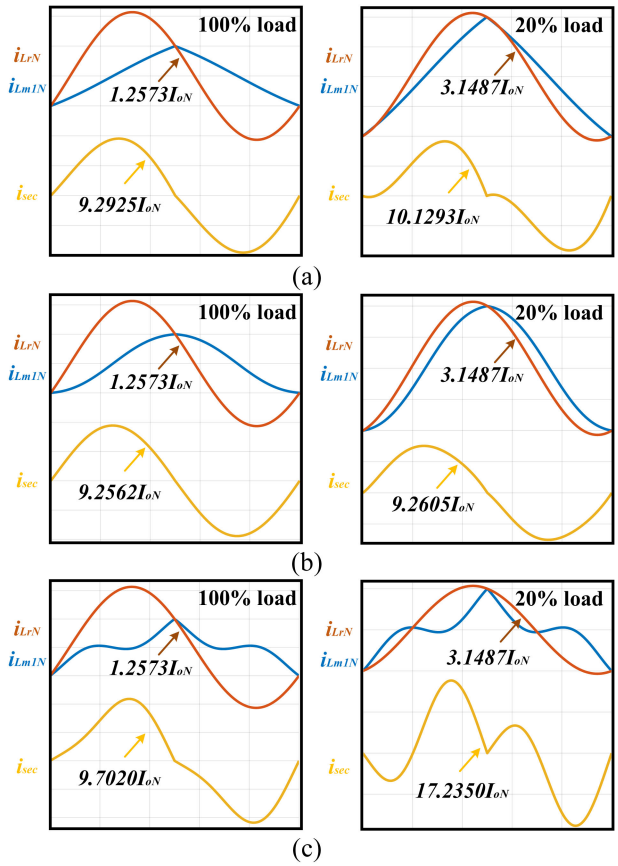

Fig. 9. Current curves with three sets of m and h_1. (a) m=2.00 and h_1= 0. (b) m=1.55 and h_1=1.3 e6. (c) m=2.50 and h_1=1.9 e6.

where h_3 and θ_2 are coefficients that depend on the initial conditions of the circuit $i_{LrN} = i_{Lr}/I_{\mathrm{N}}$.

At unity voltage conversion ratio, the resonant inductor current i_{LrN} equals the magnetic inductor current $i_{\mathrm{Lm1}N}$ at t_0, so

$$h_3\cos(\theta_2) = \frac{h_1}{m\omega_{\mathrm{r}}}\left[\cos\left(\frac{m\pi}{2} + \theta_1\right)\cos\left(\frac{m\pi}{2}\right) - \cos(\theta_1)\right] - \frac{\pi}{2}. \tag{22}$$

Based on the output current of proposed converter, combining (20) and (21), the following equation can be derived:

$$2f_{\mathrm{r}}\int_{t_0}^{t_0+1/2f_{\mathrm{r}}}(i_{LrN} - i_{\mathrm{Lm1}N})dt = I_{\mathrm{o}N} \tag{23}$$

where $I_{\mathrm{o}N} = U_{\mathrm{o}}/(nR_{\mathrm{o}}I_{\mathrm{N}})$.

When the proposed converter is operating at unity voltage conversion ratio, given a set of h_1 and m, the corresponding θ_1 and h_2 can be calculated according to (17) and (19); then, given $I_{\mathrm{o}N}$, the value of h_3 and θ_2 can be derived according to (22) and (23). Accordingly, all current can be calculated with normalized format.

The secondary current of transformer is defined as

$$i_{\mathrm{sec}} = n(i_{LrN} - i_{\mathrm{Lm1}N}). \tag{24}$$

Fig. 9 shows curves of i_{LrN}, $i_{\mathrm{Lm1}N}$, and i_{sec} with different sets of m and h_1. Although the curves of the resonant current i_{LrN} are identical with different parameters, the magnetizing

currents i_{Lm1N} are different under full-load and light-load. Since the secondary current is generated by the difference of i_{LrN} to i_{Lm1N}, three sets of m and h_1 have different shapes of secondary current. As a result, the second set of parameters has the minimum conduction loss in the secondary side with the same output current, especially under the light-load.

Assuming that the magnetizing current is an ideal sine wave, the secondary current is the difference of two sine currents and then is also a sine wave no matter what the load is. As shown in Fig. 9(b) corresponding to the optimal set of $m_{opt} = 1.55$, $h_{1opt} = 1.3e6$, its magnetizing current is in close proximity to a sine wave. Therefore, the conduction loss in the secondary side at whole load range will be reduced with this set of design parameters.

On the above analysis, two equations as (25) and (26) can be obtained to determine three parameters of the parallel branch. One is that

$$m_{opt} = \frac{\omega_{\mathrm{P}}}{\omega_{\mathrm{r}}} = \frac{\sqrt{L_{\mathrm{r}}C_{\mathrm{r}}}}{\sqrt{\frac{L_{\mathrm{m1}}L_{\mathrm{m2}}}{L_{\mathrm{m1}}+L_{\mathrm{m2}}}C_{\mathrm{A}}}}. \tag{25}$$

At unity voltage conversion ratio, in order to minimize the conduction loss in the primary side, the impedance of parallel branch should be selected to be as large as possible. The magnetizing current of the proposed converter can be the smallest value that satisfies the ZVS condition only. Then, the following equations can be derived:

$$\frac{\pi}{2} - \frac{h_{1opt}}{m_{opt}\omega_{\mathrm{r}}}\left[\cos\left(\frac{m_{opt}\pi}{2}+\theta_1\right)\cos\left(\frac{m_{opt}\pi}{2}\right) - \cos(\theta_1)\right] = \frac{4V_{\mathrm{i}}C_{\mathrm{oss}}}{t_{\mathrm{dead}}I_N}. \tag{26}$$

B. Optimal Parameters Design of the Series Resonant Tank

Except for (25), (26) and $f_{\mathrm{r}} = 1/(2\pi\sqrt{L_{\mathrm{r}}C_{\mathrm{r}}})$, two more equations are needed to determine a total of five variables.

At the minimum switching frequency $f_{\min}$, the equivalent ratio of magnetizing inductance to resonant inductance of the proposed converter can be expressed as

$$k_{\mathrm{eq}} = k_1 + \frac{k_2}{1 - {f_{\min}}^2/{f_{\mathrm{p}}}^2}. \tag{27}$$

An important insight is revealed in [7] and [8] that the peak gain, component stresses and waveform shapes are fully determined once the quality factor of the resonant tank (Q) and the inductance ratio (k) are selected. Therefore, k_{eq}-Q analysis for proposed converter with the objective of efficiency optimization is adopted in this article to design the series resonant tank [35]. The power loss minimization process of proposed converter is developed using a traversal algorithm, as shown in Fig. 10. The objective of the entire optimization concept is to determine the optimized variables in the desired design area to achieve optimal efficiency.

As shown in Fig. 11, the k_{eq}-Q feasible region depends on goal that the maximum voltage conversion ratio $G_{\max}$ is achieved at

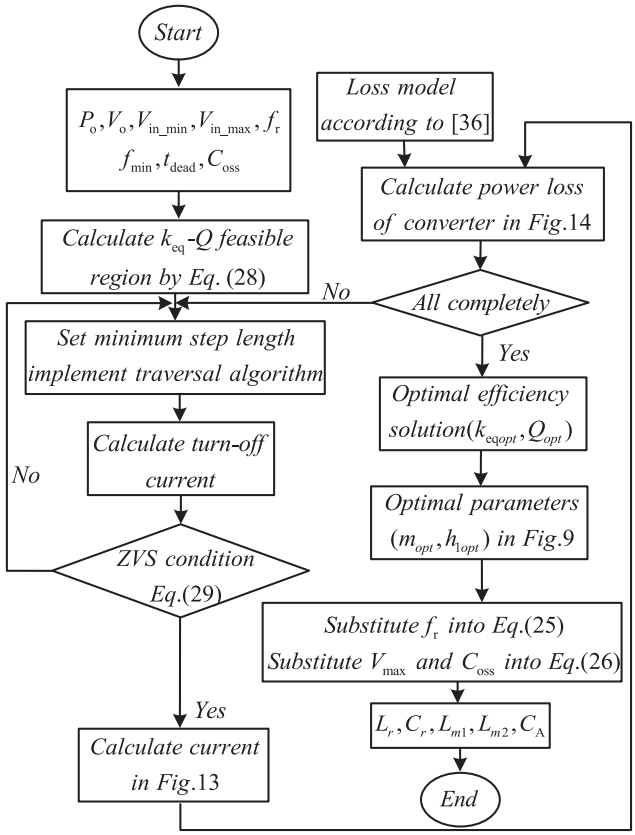

Fig. 10. Design flowchart for output optimal design candidate of five variables.

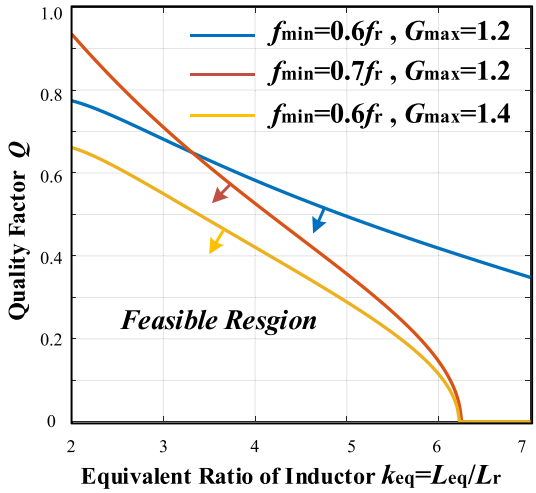

Fig. 11. k_{eq}-Q feasible region considering the maximum voltage conversion ratio.

the minimum switching frequency $f_{\min}$, which is expressed as

$$\frac{1}{\sqrt{\left(1+\frac{1}{k_{\mathrm{eq}}} - \frac{1}{k_{\mathrm{eq}}{f_{\min}}^2/{f_{\mathrm{r}}}^2}\right)^2 + Q^2\left(\frac{f_{\min}}{f_{\mathrm{r}}} - \frac{f_{\mathrm{r}}}{f_{\min}}\right)^2}} > G_{\max}. \tag{28}$$

Besides, ZVS condition as (29) at minimum switching frequency puts further restriction on the k_{eq}-Q feasible region. The

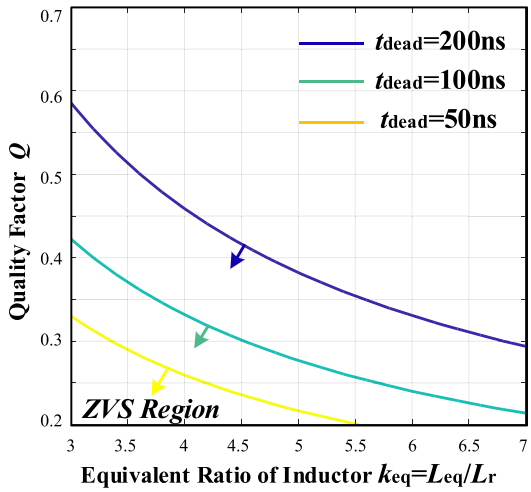

Fig. 12. $k_{\rm eq}$-Q feasible region considering ZVS condition.

soft-switching boundary curves with different dead-time $t_{\rm dead}$ are illustrated in Fig. 12

$$i_{Lr}\left(\frac{1}{2f_{\rm s}}\right) > \frac{4V_{\rm i\_min}C_{\rm oss}}{t_{\rm dead}}. \tag{29}$$

Although the desired design area has been optimized based on the previous considerations, there still exist many possible design candidates; thus, all the possible candidates should be evaluated using a traversal method. The iteration step should also be a tradeoff between the computation time and quality of the final result.

The normalized rms value of primary current of the proposed converter is shown in Fig. 13(a) with respect to the $k_{\rm eq}$ and Q. Note here that this value contributes to the conduction loss of active switches and resonant capacitor as well as copper loss of resonant inductor and primary side of transformer. The normalizing factors of primary current is defined as (30). By projecting the desired design area on the plane surface, the optimal solution of minimum conduction loss of primary side of the proposed converter can be obtained

$$I_N = \frac{V_{\rm in}}{R_{\rm ac}} = \frac{\pi^2 V_{\rm in} P_{\rm o}}{8n^2 {V_{\rm o}}^2}. \tag{30}$$

Similarly, the normalized rms value of secondary current and the normalized turn-OFF current of four active switches of the proposed converter are shown in Fig. 13(b) and (c), respectively. Note that the former one contributes to the conduction loss of rectifier diodes as well as copper loss of secondary side of transformer; the latter one results in the turn-OFF loss of active switches. It can be observed that the primary current and turn-OFF current increase quickly as $k_{\rm eq}$ and Q decrease owing to the increased magnetizing current. In contrast, the secondary current represents an upward trend along with $k_{\rm eq}$ and Q. The main reason for this phenomenon lies in that the switching frequency is far from the resonant frequency with larger value of $k_{\rm eq}$ and Q.

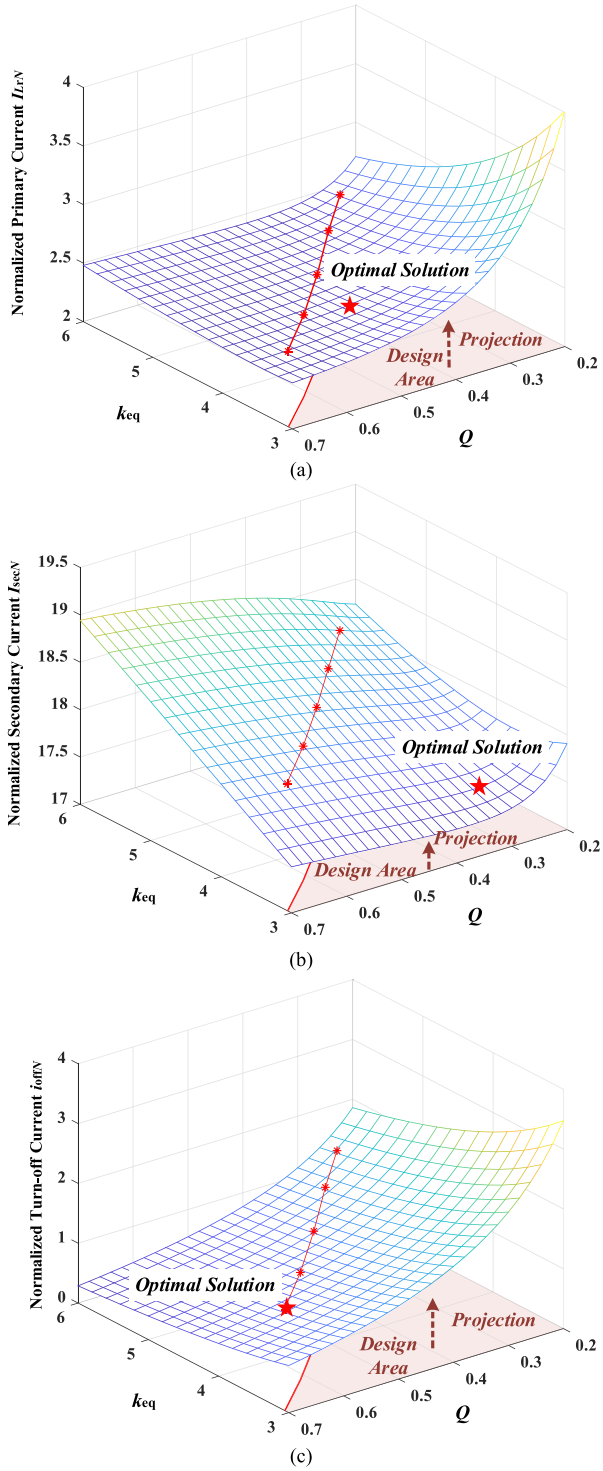

Fig. 13. Normalized current versus $k_{\rm eq}$-Q. (a) Normalized rms value of primary current. (b) Normalized rms value of secondary current. (c) Normalized turn-OFF current of four active switches.

In order to achieve globally optimal efficiency, three parts of loss in Fig. 13 should be taken into consideration at the same time. It is worth noting that the more accurate the loss model, the more, the closer the optimal value is to its actual value, which is not discussed in this article due to length limitation. Thereby, the power loss model discussed in [36] is adopted in this article and

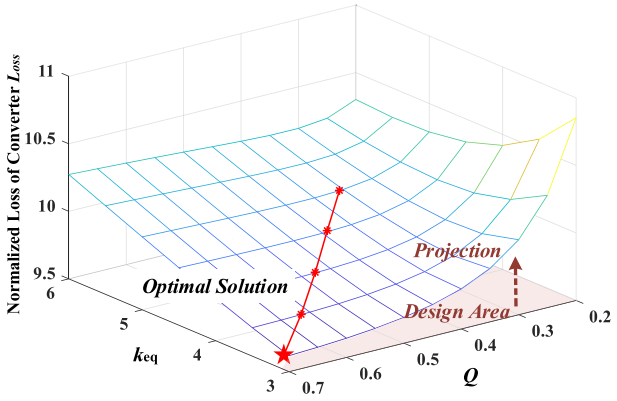

Fig. 14. Calculated loss of the proposed converter based on loss model discussed in [36].

TABLE I
DESIGN SPECIFICATIONS AND PARAMETERS

Symbol	QUANTITY	Parameter
P_o	Output power	2000W
V_o	Output voltage	48V
V_{in}	Input voltage	250V-400V
L_r	Resonant inductance	20μH
C_r	Resonant capacitance	30nF
L_m	Magnetizing inductance of *LLC* converter	80μH
	Magnetizing inductance of proposed converter(L_{m1}, L_{m2})	50μH(T_1) 20μH(T_2)
C_A	Auxiliary capacitor	20nF
N_p:N_s	Transformer turns ratio	25:3
S_1-S_4	Primary MOSFET	IPA60R190C6
Q_1-Q_4	Synchronous rectification MOSFET	IRFB4110pbf

the point of globally optimal efficiency (k_{eq_opt}, Q_{opt}) is shown in Fig. 14

$$L_{m1} + \frac{L_{m2}}{1 - {f_{min}}^2/{f_p}^2} = k_{eq\_opt} L_r \tag{31}$$

$$\sqrt{L_r/C_r}\Big/R_{ac} = Q_{opt}. \tag{32}$$

On the above-mentioned analysis of this section, five design parameters can be decided by these five equations: (25), (26), (31), (32), and $f_r = 1/(2\pi\sqrt{L_r C_r})$.

IV. EXPERIMENTAL RESULTS AND ANALYSIS

To verify the effectiveness of the proposed converter with *LC* antiresonant circuit in parallel branch, two comparative experience prototypes are built with the same design specifications. The detailed design specifications and final parameters are all illustrated in Table I. The series resonant parameters (L_r and C_r) are selected identically to demonstrate the difference of magnetizing characteristic of the proposed topology and *LLC* converter. The picture of the prototype of the proposed converter is given in Fig. 15.

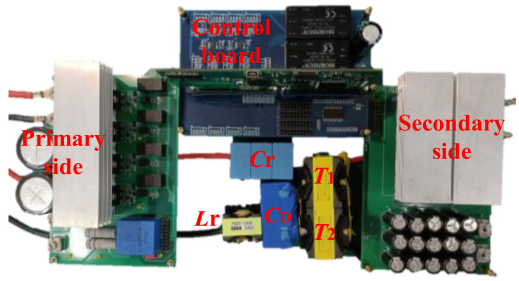

Fig. 15. Photograph of the designed converter prototype.

A. Designed Prototype and Power Loss Analysis

In this part, a step-by-step design case based on the design method in Section III is given and a complete theoretical power loss model is analyzed to make comparison between the proposed one and traditional one.

The design method considers primarily resonant parameters of the parallel branch from the efficiency and soft-switching point of view for unity voltage conversion ratio (400 V); and series resonant tank design for the minimum input voltage (250 V) based on voltage gain requirement and efficiency optimization.

The turns-ratio of the transformer is designed as 25:3 ($n = V_{i\_max}/V_o = 400$ V/48 V) to ensure that the secondary rectifiers are under ZCS operation. The series resonant frequency f_r is chosen empirically at 200 kHz considering the magnetic components design and fabrication, thermal design, and tradeoff of the conduction loss and switching loss in the switching device, and so on. The selection of f_{min} follows a similar strategy as the selection of the resonant frequency f_r, and especially the magnetic component design and EMI design should be critically considered. A widely accepted empirical value of f_{min} is between 0.5 to 0.8 times f_r [24]. In this prototype design, the minimum switching frequency is selected as 130 kHz with reasonable voltage gain margin.

As shown in Fig. 10, the k_{eq}-Q feasible region by (28) is first calculated as

$$\left(1 + \frac{1}{k_{eq}} - \frac{1}{0.4225 k_{eq}}\right)^2 + 0.79Q^2 < 0.25. \tag{33}$$

In the next step, all possible candidates are found by setting a specific design step. The k_{eq} will start from 3 to 7 and the increase step is 0.5; the lower limit of power factor Q is set at 0.2 and its upper limit is decided by (33), and its increase step is 0.05.

For each pair of design candidates, ZVS condition by (29) should be checked whether it can be achieved. In this design, substitute in (29) with V_{i_min}, C_{oss} according to the datasheet of IPA60R190C6, (29) in this case is expressed by

$$i_{Lr}\left(\frac{1}{2f_s}\right) > 2\text{A}. \tag{34}$$

Then, the currents relating to power loss are calculated for all feasible candidates by implementing time-domain model in the software, as shown in Fig. 13. After that, the conduction losses of primary MOSFET, series resonant tank, and primary

side of transformer are calculated using the rms value of resonant current I_{Lr} as

$$P_{\mathrm{S\_cond}} = 4 \cdot \left(\frac{I_{Lr}}{\sqrt{2}}\right)^2 \cdot R_{\mathrm{ds\_S}} = 2{I_{Lr}}^2 \cdot R_{\mathrm{ds\_S}}$$
$$P_{\mathrm{tank}} = {I_{Lr}}^2 \cdot (r_{Lr} + r_{C\mathrm{r}})$$
$$P_{\mathrm{T\_p}} = 2{I_{Lr}}^2 \cdot r_{\mathrm{p}}. \tag{35}$$

In this design, $R_{\mathrm{ds\_S}}$ of 0.19 Ω is the conduction resistance of S1–S4; r_{Lr} as 12 mΩ and $r_{C\mathrm{r}}$ as 2 mΩ according to their design files are ac resistance of resonant inductor and film capacitor; r_{p} as 12 mΩ is the resistance of primary winding of transformer.

The switching loss of primary MOSFET can be evaluated with the turn-OFF current I_{OFF} using the empirical formula in [36]

$$P_{\mathrm{sw\_off}} = 4 \cdot f_{\mathrm{s}} \cdot \int_0^{t_{\mathrm{f}}} v_{\mathrm{ds}}(t) \cdot i_{\mathrm{ds}}(t) dt = V_i \cdot i_{\mathrm{off}} \cdot t_{\mathrm{f}} \cdot f_{\mathrm{s}}. \tag{36}$$

The corresponding t_{f} is turn-OFF time of primary MOSFET and can be obtained as 119 ns from its datasheet.

The rms value of secondary current I_{sec} contributes to the conduction loss of synchronous rectification MOSFETs as well as copper loss of secondary side of transformer. In this design, the rectifier MOSFETs have two switches named as IRFB4110pbf in parallel and their conduction loss are calculated as (37). $R_{\mathrm{ds\_Q}}$ of 4.5 mΩ is the conduction resistance of Q1–Q4; r_{s} as 0.2 mΩ is the resistance of secondary winding of transformer

$$P_{\mathrm{Q\_cond}} = 8 \cdot \left(\frac{I_{\mathrm{sec}}}{2\sqrt{2}}\right)^2 \cdot R_{\mathrm{ds\_Q}} = {I_{\mathrm{sec}}}^2 \cdot R_{\mathrm{ds\_Q}}$$
$$P_{\mathrm{T\_s}} = 2{I_{\mathrm{sec}}}^2 \cdot r_{\mathrm{s}}. \tag{37}$$

Other power losses, such as core loss of transformer and inductor and loss of auxiliary capacitor, are tentatively not taken into consideration during the process of k_{eq} and Q optimization for their complexity of model and relatively small proportion.

By implementing the traversal algorithm, the optimized design candidates can be obtained when $k_{\mathrm{eq}} = 4.2$ and $\mathrm{Q} = 0.398$. In this design example, substitute into (32) with $Q_{\mathrm{opt}} = 0.398$ and 200 kHz as f_{r}, the resonant inductor and capacitor are 20 μH and 30 nF, respectively.

Combining two equations of (26) and (31), the magnetizing inductances of T1 and T2 can be solved. In this case, L_{m1} is 50 μH and L_{m2} is 20 μH. At last, the corresponding C_{A} is 20 nF according to

$$C_{\mathrm{A}} = \frac{L_{\mathrm{r}}(L_{\mathrm{m1}} + L_{\mathrm{m2}})C_{\mathrm{r}}}{L_{\mathrm{m1}}L_{\mathrm{m2}}{m_{opt}}^2}. \tag{38}$$

After all parameters are optimally designed based on the design flowchart, the power loss breakdown of proposed converter is conducted and the comparison with *LLC* converter is made, as shown in Fig. 16. It is noticeable that the proposed converter has less primary MOSFET conduction loss and switching-OFF loss, which account for large proportion of the whole power loss. Conduction loss of secondary switches is nearly identical and power loss brought by auxiliary capacitor and transformer are taken into consideration to make a fair comparison. However, this part of loss is negligible and the whole efficiency of conventional *LLC* can be improved by the proposed topology and design method.

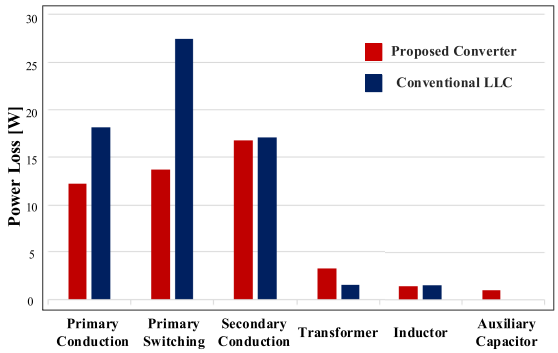

Fig. 16. Loss breakdown under full-load condition at 400 V input.

B. State-Plane Trajectory Analysis

The stored energy in resonant tank and the current and voltage stresses on components are all reflected intuitively by the graphical state-trajectory.

Fig. 17 depicts state-plane trajectories of the resonant tank based on measured experimental result and theoretical calculation. Comparison of state-plane trajectories between the proposed converter and *LLC* converter under full-load condition at 400 V input is made in Fig. 17(a). It is noticeable that the trajectories radius of the proposed converter is apparently less than that of *LLC* converter, which indicates that the former current stress and conduction loss are much smaller than the latter one. Also, the calculated trajectory of the proposed converter based on time-domain model has good agreement with the measured result except dead-time process. Furthermore, the turn-OFF of the proposed converter is reduced by half of *LLC* converter. Thus, the switching loss can be decreased significant with this solution, which is consistent with calculated loss breakdown in part A of this section.

Similar to the input 400 V case, Fig. 17(b) shows three state-plane trajectories under full-load at 250 V input. The switching frequency reduces to 130 kHz, and the equivalent inductance of parallel branch of the proposed converter decreases to the nearly same value of *LLC* converter. Thus, their state-plane trajectories nearly coincide. Besides, time-domain model in Fig. 17(a) and (b) can also match the measured curve, which verify the accuracy of previous time-domain analysis.

C. Steady-State Waveforms and Comparison

The experimental results in unity voltage conversion ratio are presented in Fig. 18. Fig. 18(a) and (b) shows the steady-state waveforms at 400 V input voltage and 2000 W load of proposed converter and *LLC* converter, respectively. According to the waveforms, one can find that the turn-OFF current and rms value of current in the primary side is largely reduced due to a larger equivalent magnetizing inductor in the proposed converter. Thereby, its conduction and switching loss are significantly

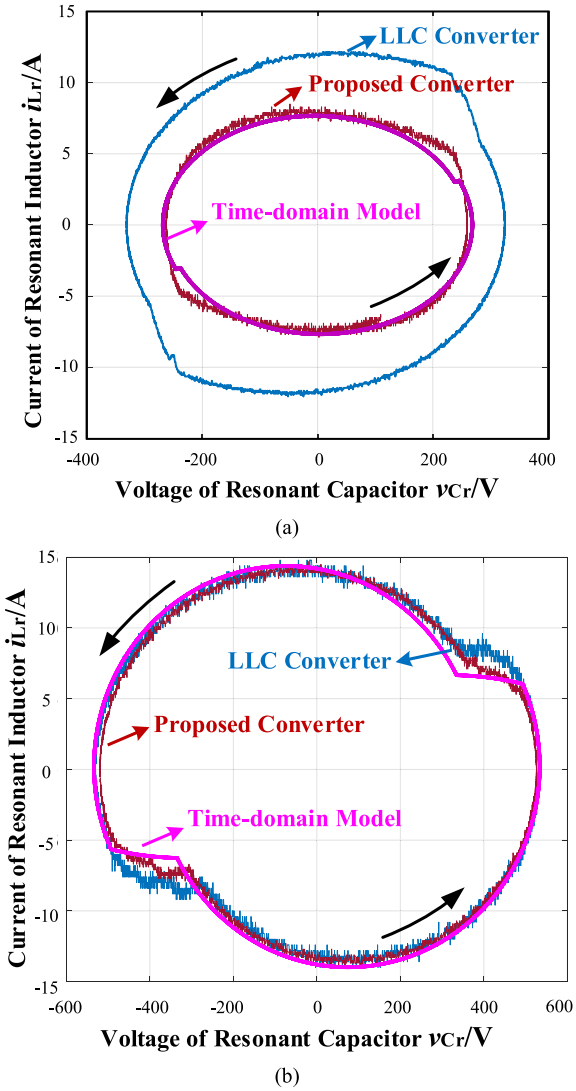

Fig. 17. State-plane trajectories of the resonant tank by experiment and theoretical calculation. (a) Unity voltage conversion ratio (Input 400 V). (b) Maximum voltage conversion ratio (Input 250 V).

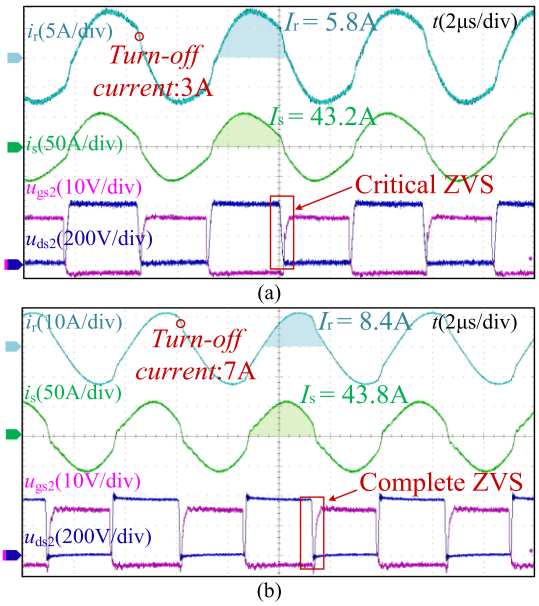

Fig. 18. Steady-state waveforms at 400 V and 2 kW. (a) Proposed converter. (b) *LLC* converter. .

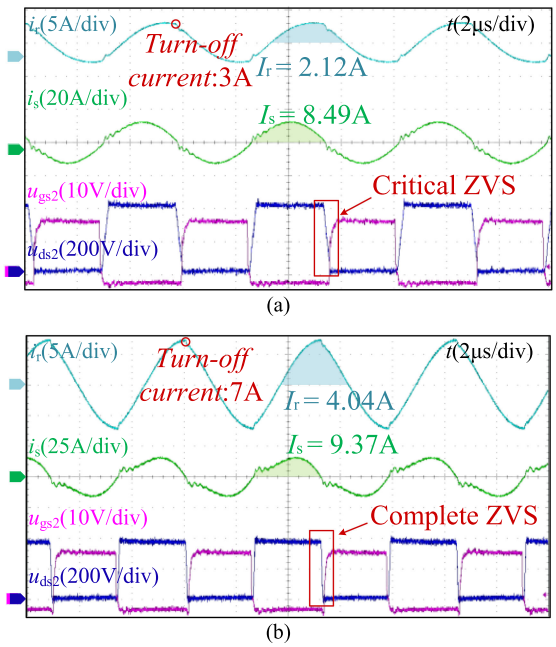

Fig. 19. Steady-state waveforms at 400 V and 500 W. (a) Proposed converter. (b) *LLC* converter.

reduced. Besides, the turn-OFF current of proposed converter is 3 A and it should be noted that the driving signal u_{gs2} begins to rise just at the moment of u_{ds2} reaching at zero. The parasitic capacitors of S_1–S_4 are just charged and discharged completely when the dead-time finishes and this characteristic is named as "Critical ZVS." Compared with this by *LLC* converter, it should be noted that there always exists an apparent gap between every rising edge of u_{gs2} and the corresponding falling edge of u_{ds2}, which is named as "complete ZVS." This is in accordance with the design principle as equation (26) that the magnetizing current of the proposed converter can be the smallest value that satisfies the ZVS condition only at unity voltage conversion ratio.

Fig. 19 illustrates the experimental results of light load in unity voltage conversion ratio. It should be noted that the turn-OFF currents of proposed converter (3A) and *LLC* converter (7A) are identical with full-load. The reason is that the parallel branch is always clamped by the voltage of nV_o. As shown in Fig. 19(a) and (b), compared with *LLC* converter with the same output power, the rms value of current in the primary side is reduced by nearly half, which means circulating current can be reduced significantly with the proposed way. Moreover, the rms value of current in the secondary side of proposed converter is smaller than that of *LLC* converter. This phenomenon is caused by discontinuous current in the secondary side of *LLC* converter, which is consistent with the theoretical analysis in Fig. 9. As a result, the efficiency can be greatly improved by the proposed topology in the light load.

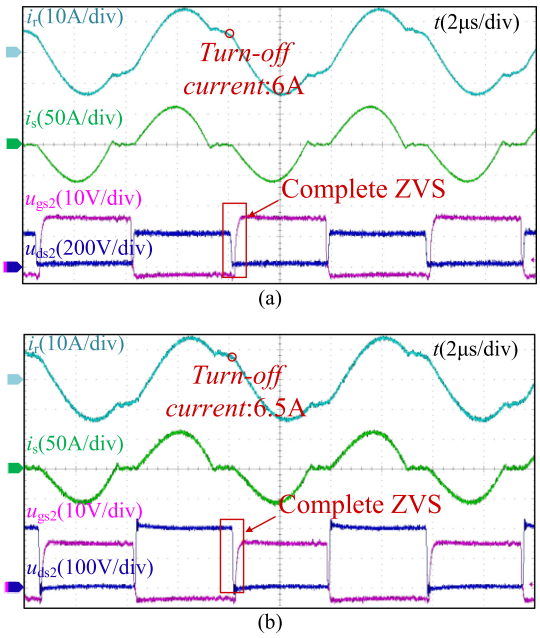

Fig. 20. Steady-state waveforms at 250 V and 2 kW. (a) Proposed converter. (b) *LLC* converter.

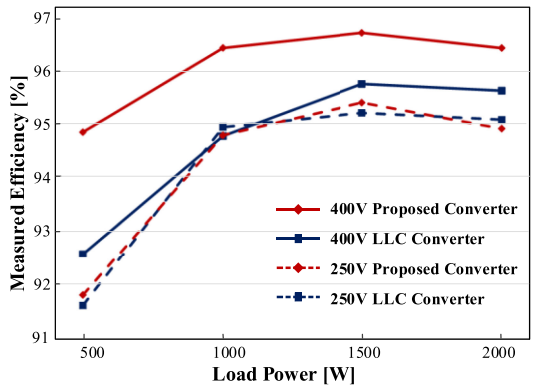

Fig. 21. Measured efficiency curves of proposed converter and *LLC* resonant converter.

Fig. 20 shows the steady-state waveforms of two comparative converters at 250 V and 2000 W. It can be seen that two converters have exceedingly similar resonant current wave and can achieve the same voltage gain at almost identical switching frequency. This is because the equivalent magnetizing inductance of proposed converter decreases to the magnetizing inductance of *LLC* converter as switching frequency decreases. Also, because the former impendence of parallel branch is reduced both of them have almost identical turn-OFF currents, as shown in Fig. 20(a) and (b).

The measured efficiency curves are illustrated in Fig. 21. It can be seen that at 400 V operating point, the efficiency of the proposed multielement resonant converter is improved by above 1% at whole load range, especially 2% at light load condition. Also, the proposed converter can achieve the same highest voltage gain almost without efficiency reduction at 250 V. In general, efficiency at whole voltage range except 250 V operating point can be improved to some extent.

V. Conclusion

In this article, a modified *LLC* resonant converter with *LC* antiresonant circuit in parallel branch is proposed to achieve wide voltage gain and high efficiency at the same time. The topology overcomes the drawback of the conventional *LLC* converter that reducing magnetizing inductance to obtain wide voltage gain results in a large circulating current and turn-OFF current in the primary side. This advantage mainly profits from has excellent magnetizing impedence characteristic that equivalent magnetizing inductance of the proposed converter decreases as switching frequency decreases within regulating frequency range. In addition, the conduction loss in the secondary side will be reduced, especially in the light load. The time-domain model can predict the state variables of resonant tank since the calculated accurately trajectories match the measured curve very well. With detailed analysis and step-by-step design, the comparative experiments are conducted and verify that the proposed converter improves whole load range efficiency at whole voltage range. Especially at resonant point, the turn-OFF current of primary MOSFET decreases by half and efficiency is improved by 1% at rated load and by 2% at light load.

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References

[1] F. C. Lee, P. Barbosa, P. Xu, J. Zhang, B. Yang, and F. Canales, "Topologies and design considerations for distributed power system applications," *Proc. IEEE*, vol. 89, no. 6, pp. 939–950, Jun. 2001.

[2] B. Yang, F. C. Lee, G. Lu, and A. Q. Huang, "Topology investigation for front end DC/DC power conversion for distributed power system," Ph.D. dissertation, Dept. Elect. Comput. Eng., Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2003.

[3] X. Wu, R. Li, and X. Cai, "A wide output voltage range LLC resonant converter based on topology reconfiguration method," *IEEE J. Emerg. Sel. Topics Power Electron.*, to be published, doi: 10.1109/JESTPE.2021.3097738.

[4] M. Mu and F. C. Lee, "Design and optimization of a 380–12 v high-frequency, high-current LLC converter with GaN devices and planar matrix transformers," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 854–862, Sep. 2016.

[5] X. Wu and H. Shi, "High efficiency high density 1 MHz 380–12 v DCX with low FoM devices," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1648–1656, Feb. 2020.

[6] R. Beiranvand, B. Rashidian, M. R. Zolghadri, and S. M. Hossein Alavi, "A design procedure for optimizing the LLC resonant converter as a wide output range voltage source," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3749–3763, Aug. 2012.

[7] Z. Hu, L. Wang, H. Wang, Y. Liu, and P. C. Sen, "An accurate design algorithm for LLC resonant converters—Part I," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5435–5447, Aug. 2016.

[8] Z. Hu, L. Wang, Y. Qiu, Y. Liu, and P. C. Sen, "An accurate design algorithm for LLC resonant converters—Part II," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5448–5460, Aug. 2016.

[9] J. Deng, S. Li, S. Hu, C. C. Mi, and R. Ma, "Design methodology of LLC resonant converters for electric vehicle battery chargers," *IEEE Trans. Veh. Technol.*, vol. 63, no. 4, pp. 1581–1592, May 2014.

[10] Y. Wei, Q. Luo, Z. Wang, and H. A. Mantooth, "A complete Step-by-Step optimal design for LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3674–3691, Apr. 2021.
[11] T. Jiang, J. Zhang, X. Wu, K. Sheng, and Y. Wang, "Bidirectional LLC resonant converter with automatic forward and backward mode transition," *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 757–770, Feb. 2015.
[12] H. Haga and F. Kurokawa, "Modulation method of a full-bridge three-level LLC resonant converter for battery charger of electrical vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2498–2507, Apr. 2017.
[13] H. Wu, X. Zhan, and Y. Xing, "Interleaved LLC resonant converter with hybrid rectifier and variable-frequency plus phase-shift control for wide output voltage range applications," *IEEE Trans. Power Electron.*, vol. 32, no. 6, pp. 4246–4257, Jun. 2017.
[14] H. Wu, K. Sun, Y. Li, and Y. Xing, "Fixed-frequency PWM-controlled bidirectional current-fed soft-switching series-resonant converter for energy storage applications," *IEEE Trans. Ind. Electron.*, vol. 64, no. 8, pp. 6190–6201, Aug. 2017.
[15] J. Kim, C. Kim, J. Kim, J. Lee, and G. Moon, "Analysis on load-adaptive phase-shift control for high efficiency full-bridge LLC resonant converter under light-load conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4942–4955, Jul. 2016.
[16] L. Shi, B. Liu, and S. Duan, "Burst-mode and phase-shift hybrid control method of LLC converters for wide output range applications," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1013–1023, Feb. 2020.
[17] B. Kim, K. Park, and G. Moon, "Asymmetric PWM control scheme during hold-up time for LLC resonant converter," *IEEE Trans. Ind. Electron.*, vol. 59, no. 7, pp. 2992–2997, Jul. 2012.
[18] H. Park and J. Jung, "PWM and PFM hybrid control method for LLC resonant converters in high switching frequency operation," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 253–263, Jan. 2017.
[19] S. Zong, G. Fan, and X. Yang, "Double voltage rectification modulation for bidirectional DC/DC resonant converters for wide voltage range operation," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6510–6521, Jul. 2019.
[20] M. I. Shahzad, S. Iqbal, and S. Taib, "A wide output range HB-2LLC resonant converter with hybrid rectifier for PEV battery charging," *IEEE Trans. Transp. Electrific.*, vol. 3, no. 2, pp. 520–531, Jun. 2017.
[21] D. Shu and H. Wang, "An ultrawide output range LLC resonant converter based on adjustable turns ratio transformer and reconfigurable bridge," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7115–7124, Aug. 2021.
[22] W. Sun, Y. Xing, H. Wu, and J. Ding, "Modified high-efficiency LLC converters with two split resonant branches for wide input-voltage range applications," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7867–7879, Sep. 2018.
[23] H. Wu, X. Jin, H. Hu, and Y. Xing, "Multielement resonant converters with a notch filter on secondary side," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 3999–4004, Jun. 2016.
[24] Y. Chen *et al.*, "LCLC converter with optimal capacitor utilization for hold-up mode operation," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2385–2396, Mar. 2019.
[25] D. Kim, S. Moon, C. Yeon, and G. Moon, "High-efficiency LLC resonant converter with high voltage gain using an auxiliary LC resonant circuit," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6901–6909, Oct. 2016.
[26] D. Huang, P. Kong, F. C. Lee, and D. Fu, "A novel integrated multi-elements resonant converter," in *Proc. IEEE Energy Convers. Congr. Expo.*, Phoenix, AZ, USA, 2011, pp. 3808–3815.
[27] D. Fu, F. C. Lee, Y. Liu, and M. Xu, "Novel multi-element resonant converter for front-end dc-dc converters," in *Proc. IEEE Power Electron. Special. Conf.*, Jun. 2008, pp. 250–256.
[28] H. Mizutani, T. Mishima, and M. Nakaoka, "A novel LLC multi-resonant dc-dc converter with an anti-resonant circuit," in *Proc. 7th Int. Power Electron. Motion Control Conf.*, Jun. 2012, pp. 1324–1335.
[29] T. Mishima, H. Mizutani, and M. Nakaoka, "An LLC resonant full–bridge inverter-link dc-dc converter with an anti-resonant circuit for practical voltage step-up/down regulation," in *Proc. IEEE Energy Convers. Congr. Expo.*, Sep. 2012, pp. 3533–3540.
[30] D. Kim, S. Moon, C. Yeon, and G. Moon, "High-efficiency LLC resonant converter with high voltage gain using an auxiliary LC resonant circuit," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 6901–6909, Oct. 2016.
[31] D. Kim, C. Yeon, J. Kim, Y. Jeong, and G. Moon, "LLC resonant converter with high voltage gain using auxiliary LC resonant circuit," in *Proc. 9th Int. Conf. Power Electron. ECCE Asia*, Seoul, South Korea, 2015, pp. 1505–1512.
[32] T. Mishima, H. Mizutani, and M. Nakaoka, "Experimental evaluations of a five-element multi-resonant dc-dc converter with an improved PFM control range," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, Apr. 2013, pp. 147–152.
[33] T. Mishima, H. Mizutani, and M. Nakaoka, "A sensitivity-improved PFM LLC resonant full-bridge DC–DC converter with LC antiresonant circuitry," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 310–324, Jan. 2017.
[34] R. Yu, G. K. Y. Ho, B. M. H. Pong, B. W. Ling, and J. Lam, "Computer-Aided design and optimization of high-efficiency LLC series resonant converter," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3243–3256, Jul. 2012.
[35] I. Lee and G. Moon, "The k-Q analysis for an LLC series resonant converter," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 13–16, Jan. 2014.
[36] C. Yang, T. Liang, K. Chen, J. Li, and J. Lee, "Loss analysis of half-bridge LLC resonant converter," in *Proc. 1st Int. Future Energy Electron. Conf.*, 2013, pp. 155–160.

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