# Letters

# Dynamic *dv/dt* Control Strategy of SiC MOSFET for Switching Loss Reduction in the Operational Power Range

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***Abstract*—For silicon carbide power MOSFETs, high *dv/dt* in switching may bring about a high level of electromagnetic interference. This letter shows that the *dv/dt* rate decreases at lower load currents. A dynamic *dv/dt* control strategy is then proposed for switching loss reduction in the whole operating range, by maintaining the *dv/dt* at the maximum acceptable level. The effectiveness of the proposed control strategy is verified by an experiment, showing that the total switching loss can be reduced by as much as 22% at 30% load. Furthermore, the simulation shows that a power loss reduction of 11.4% can be obtained for an electric vehicle converter which typically operates at light loads for most of the time.**

***Index Terms*—*dv/dt* control, loss reduction, SiC MOSFET.**

## I. Introduction

WIDE-BAND-GAP power devices, such as silicon carbide metal–oxide–semiconductor field-effect transistors (SiC MOSFETs), are increasingly used in converters for high switching frequency, high working temperature, and/or high blocking voltage [1], [2]. Fast switching can bring about side effects such as electromagnetic interference (EMI) and insulation aging [3]–[5]. Therefore, the switching speed is limited [6].

Switching *dv/dt* is commonly controlled through active gate driving [7]–[11]. However, there is a tradeoff between the *dv/dt* and switching losses [12]. Simply reducing *dv/dt* increases the switching loss [13]. In addition to gate drive, the switching speed also depends on the current and temperature of the device [14].

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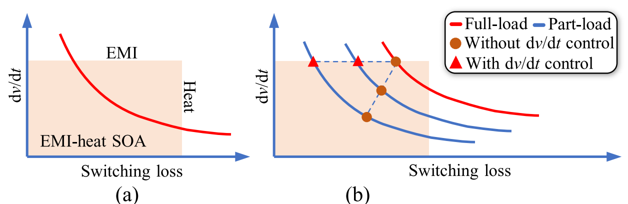


Fig. 1. (a) Tradeoff relationship between the *dv/dt* of power switch and switching loss at a certain load current. (b) Effect of load current.

This letter shows how to take into account the current effect and devise a *dv/dt* control strategy for power loss reduction.

Active gate drivers aim to balance the *dv/dt* and switching losses [15], [16]. A lookup table *dv/dt* control is applied to a half-bridge in [17] to increase the *dv/dt* related to the diodes. However, a closed-loop *dv/dt* control strategy including the load effect on the *dv/dt*-switching loss curve has not yet been proposed. The d*v*/d*t* tolerance is not fully used as the load reduces. By maintaining *dv/dt* at an acceptable upper limit, the *dv/dt* control strategy would reduce the switching loss without violating the EMI constraint. This is potentially beneficial in converter systems which mostly operate at light load levels, such as those found in electric vehicles (EVs).

This letter proposes a dynamic control strategy to follow the load current. A boost dc–dc converter is built using SiC MOSFETs to verify the proposed strategy. Switching loss reduction within the entire operational range is then evaluated. Simulation result to an actual load mission profile in EV application is obtained. The letter intends to provide a reference for SiC converter gate control.

The rest of this letter is organized as follows. Section II presents the proposed *dv/dt* control strategy. Section III describes the experimental test rig and presents the result of verification. Discussion from a viewpoint of application is conducted in Section IV. Finally, Section V concludes this letter.

## II. Proposed Control Strategy: To Make Full Use of *dv/dt* Tolerance

Fig. 1 depicts the qualitative shape of the *dv/dt*-switching loss relationship which will become obvious next. The tradeoff

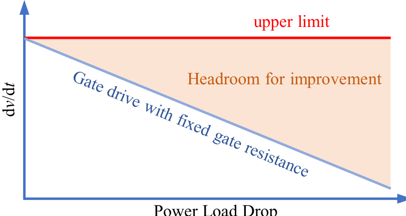


Fig. 2. Illustration of the proposed *dv*/*dt* control strategy.

between *dv*/*dt* and switching loss is the key in this letter. Derived for ideal switching processes of the MOSFET [18], the relationship can be expressed as follows:

$$E_{\text{off}} = \frac{1}{2} I_{\text{L}} V_{\text{DS}} \left( \frac{V_{\text{DS}}}{\frac{dv}{dt}(\text{off})} + \frac{I_{\text{L}}}{\frac{di}{dt}(\text{off})} \right) \quad (1)$$

$$E_{\text{on}} = \frac{1}{2} I_{\text{L}} V_{\text{DS}} \left( \frac{V_{\text{DS}}}{\frac{dv}{dt}(\text{on})} + \frac{I_{\text{L}}}{\frac{di}{dt}(\text{on})} \right) \quad (2)$$

where $dv/dt_{(\text{OFF})}$ and $dv/dt_{(\text{ON})}$ are the voltage rising and falling slopes of the MOSFET, while $di/dt_{(\text{OFF})}$ and $di/dt_{(\text{ON})}$ are the current falling and rising slopes.

For certain load current, the higher the *dv*/*dt*, the lower the switching losses would be. However, the *dv*/*dt* of the MOSFET cannot be too high due to EMI while the switching loss cannot be too large either due to heat dissipation constraint. It can be seen in Fig. 1(a) that the working point should not exceed the EMI-heat safe operating area (SOA).

Another point is the effect of the load level on the *dv*/*dt*-switching loss curve as shown in Fig. 1(b). The expressions for *dv*/*dt* in both turn-OFF and turn-ON processes are [18] as follows:

$$\left| \frac{dv_{\text{ds}}}{dt}(off) \right| = \frac{V_{\text{th}} + \frac{I_{\text{L}}}{g_{\text{m}}} - V_{\text{EE}}}{C_{\text{gd}} \cdot R_{\text{Goff}}} \quad (3)$$

$$\left| \frac{dv_{\text{ds}}}{dt}(on) \right| = \frac{V_{\text{DD}} - \frac{I_{\text{L}}}{g_{\text{m}}} - V_{\text{th}}}{C_{\text{gd}} \cdot R_{\text{Gon}}} \quad (4)$$

where $V_{\text{th}}$ is the threshold voltage in V, $g_{\text{m}}$ is the device transconductance in A/V, $C_{\text{gd}}$ is the device gate–drain capacitance in F, $V_{\text{EE}}$ is the negative gate drive voltage in V, and $V_{\text{DD}}$ is the positive gate drive voltage in V. $R_{\text{Goff}}$ and $R_{\text{Gon}}$ are the gate resistance during turn-OFF and turn-ON, respectively.

As the load decreases, the *dv*/*dt* will reduce inside the EMI-heat SOA [19]. Therefore, in the load range, there exists a maximum *dv*/*dt* with the conventional fixed gate drive. This value can be set as the target *dv*/*dt* in the proposed control strategy.

The basic idea is to maintain the *dv*/*dt* at partial load to the acceptable upper limit as shown in Fig. 2. If the maximum *dv*/*dt* at full load is acceptable in the designed converter with a fixed gate drive, the *dv*/*dt* in the entire operational range can be kept at the same level without violating the EMI constraint. In this case, the switching losses are reduced at light loads.

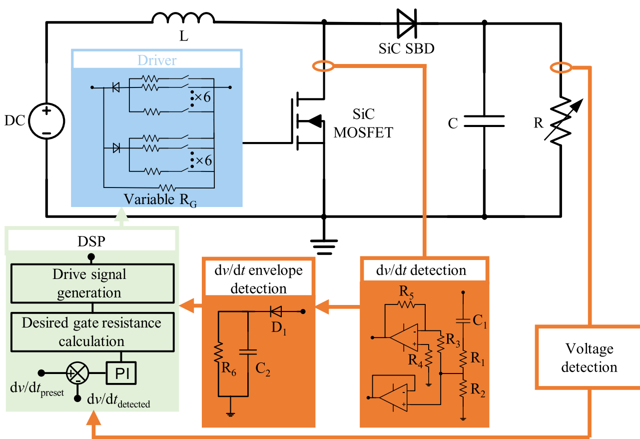


Fig. 3. Schematic of an experimental circuit with proposed *dv*/*dt* control strategy. Feedback signals include turn-ON *dv*/*dt*, turn-OFF *dv*/*dt,* and output voltage. A variable gate resistor gate driver is implemented.

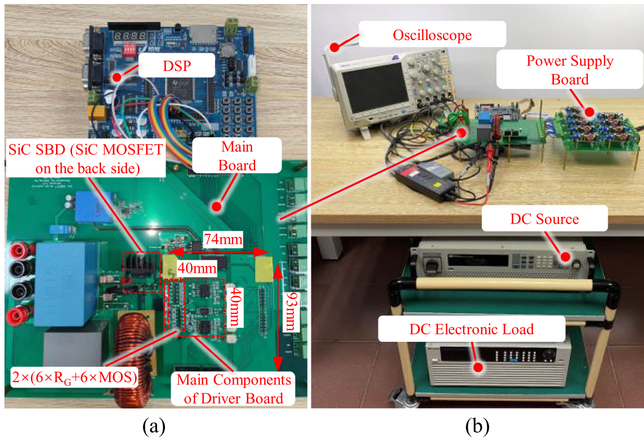


Fig. 4. (a) Main circuit board of boost dc–dc converter with turn-ON and turn-OFF *dv*/*dt* control gate drives, and DSP controller. (b) Experimental test bench.

## III. Experimental Verification

### A. *Experimental Test Rig*

A dc–dc converter test rig is set up to verify the proposed *dv*/*dt* control strategy. The schematic is shown in Fig. 3, including the proposed controller configuration.

The experimental test rig includes the dc–dc converter board, a digital signal processor (DSP) controller, a power supply board, a dc power source, and a variable dc electronic load as shown in Fig. 4. The components of the modified gate driver are populated in an area of 40 $\times$ 40 mm; an increase of 25%–35% is caused in the homemade driver board due to the variable gate resistance stage. The detection circuits, made of physically small components due to the fast transient, are next to the main SiC MOSFET switch on the backside of the mainboard. It would be possible in the future to develop specific ICs to provide such added gate drive functions and further reduce the footprint [20].

The main parameters of the verification rig are listed in Table I. The part numbers of the SiC Schottky barrier diode (SBD)

TABLE I
SYSTEM PARAMETERS

| Parameters | Value | Parameters | Value |
|---|---|---|---|
| Input voltage | 100 V | Switching frequency | 100 kHz |
| Output voltage | 300 V | DC Bus Capacitor | 60 µF |
| Inductor | 250 µH | Filter Capacitors | 3×0.1 µF |

and SiC MOSFET used are IDW30G65C5 and SCT3120AL, respectively.

The system contains circuits for voltage detection, *dv/dt* detection, *dv/dt* envelope detection for both turn-ON and turn-OFF processes, and variable gate resistor combinations. As shown in Fig. 3, the *dv/dt* of the SiC MOSFET can be detected from capacitor $C_1$ in series with resistors $R_1$ and $R_2$. $C_1$ is far smaller than the parasitic capacitance of the SiC MOSFET to avoid affecting the switching process. Resistors $R_1$ and $R_2$ should be carefully selected by considering the capacitance of $C_1$, the *dv/dt* target value, and the input voltage range of the downstream op-amps. The design formulae for parameters $R_1$ and $R_2$ can be derived as follows:

$$R_1 + R_2 \leq \frac{\sigma \cdot V_{\rm ds}}{C_1 \frac{{\rm d}V_{\rm ds}}{{\rm d}t}} \tag{5}$$

$$R_2 \leq \frac{V_{\rm in-limit}}{C_1 \frac{{\rm d}V_{\rm ds}}{{\rm d}t}} \tag{6}$$

where $\sigma$ is the ratio of the voltage across resistors $R_1$ and $R_2$ over the drain-to-source voltage, and $V_{\rm in\text{-}limit}$ is the input voltage limit of the downstream op-amps in V.

In addition to the maximum values calculated above, $R_2$ should not be too small to provide enough input voltage to the downstream op-amps and to ensure the accuracy of the *dv/dt* detection circuit.

A 120-MHz bandwidth and high slew rate op-amp LM7372 is used in the *dv/dt* detection circuit which also provides dc isolation. A diode-based envelope detection circuit is then used to dynamically detect the peak values of the *dv/dt* of the SiC MOSFET. The bandwidths of the *dv/dt* detector and control system are greater than 75 and 5 MHz, respectively. The bandwidths are mainly limited by the op-amp used in the circuit and the proportional–integral (PI) control gains.

A variable resistance gate drive is implemented to achieve the target *dv/dt* value. Variable external gate resistance for *dv/dt* control is achieved through six resistors which are switched in or out of the parallel circuit using MOSFETs of low voltage and current. This gives 63 combinations of different equivalent resistance values between 0.8 and 62 Ω. The turn-ON and turn-OFF processes are independently controlled. The target resistance is derived from a PI control algorithm aiming to send the *dv/dt* to the target value. The control signals of these switches are isolated through optocoupler driver chips. A dead band is set for the feedback error in line with the discrete nature of the achievable resistance.

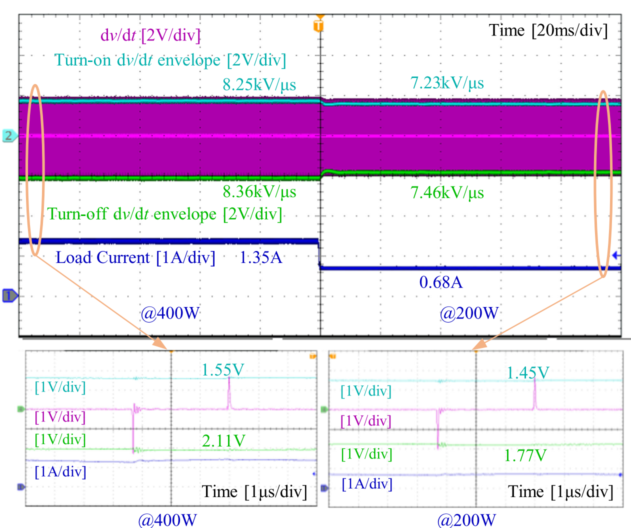


Fig. 5. Response of *dv/dt* as load power changes from 400 to 200 W without *dv/dt* control. Turn-OFF *dv/dt* envelope is inverted on oscilloscope.

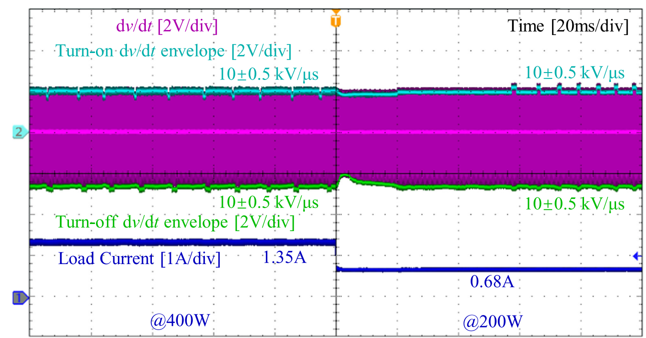


Fig. 6. Dynamic response of *dv/dt* when the load power changes from 400 to 200 W with *dv/dt* control. The target *dv/dt* value is set to 10kV/$\mu$s. Turn-OFF *dv/dt* envelope is inverted on the oscilloscope.

## B. Experimental Results

A test is conducted first to verify the variation of the *dv/dt* with the load power (current). The external gate resistance is set to 43 Ω for turn-ON and 30 Ω for the turn-OFF. With these, the *dv/dt* is 10 kV/$\mu$s at the maximum load power of 600 W [21].

Fig. 5 shows that *dv/dt* decreases to 8.25 kV/$\mu$s and 8.36 kV/$\mu$s for turn-ON and turn-OFF, respectively, as the load reduces to 400 W (1.35 A). At 200 W (0.68 A), these values are further reduced to 7.23 kV/$\mu$s and 7.46 kV/$\mu$s, respectively.

Fig. 6 shows the controlled response of *dv/dt* when the load current undergoes a step change. The target *dv/dt* is set as 10 kV/$\mu$s. It is clear that within 20 ms, the *dv/dt* returns to the target value, within a tolerance of $\pm$0.5 kV/$\mu$s which is caused by the discrete nature of the achievable gate resistance.

The switching loss is compared to confirm the effectiveness of the proposed *dv/dt* control strategy. Fig. 7 shows the switching waveforms at a power level of 180 W, without and with *dv/dt* control. Without *dv/dt* control, the gate resistance is fixed at 43 Ω or 30 Ω. At the reduced power level, the reduced average *dv/dt* is measured to be about 7.3 kV/$\mu$s and 7.2 kV/$\mu$s, for turn-OFF and

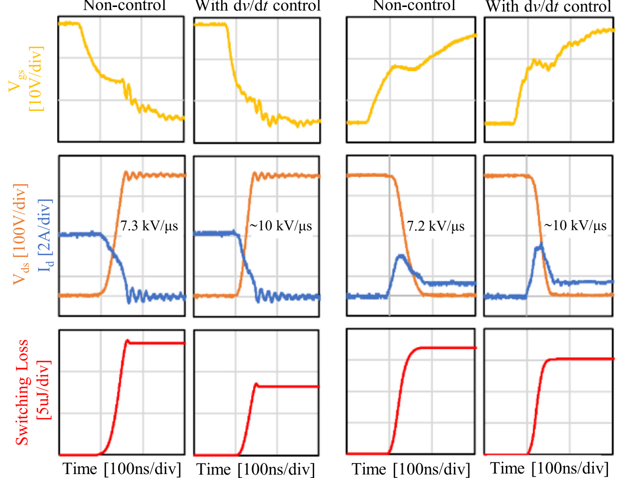


Fig. 7. Comparison between cases without and with *dv*/*dt* control of turn-ON and turn-OFF transients at load level of 180 W.

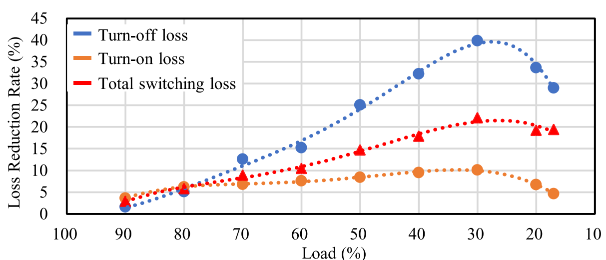


Fig. 8. Experimental results of turn-ON and turn-OFF loss reduction rate in the operational power range. The full-load is 600 W.

turn-ON, respectively. The corresponding switching energy loss is 13.3 $\mu$J and 16.7 $\mu$J, respectively. With control, the *dv*/*dt* is restored to 10 kV/$\mu$s and the switching energy losses are reduced to 8.23 $\mu$J and 15 $\mu$J. This reduces the total switching loss by 22% and the total power loss by 19.5%, and the latter is also confirmed on a power analyzer. The switching frequency is 100 kHz.

The switching loss reduction rate is shown in Fig. 8 for both turn-ON and turn-OFF transients within the operational power range. The turn-ON switching loss can be reduced in almost the entire load power range. The largest turn-ON loss reduction is about 10% at around 30% partial load. The loss reduction rate starts to decline when the load is lighter than 30%. The turn-ON loss is closely related to the *dv*/*dt*, *di*/*dt*, and current overshoot of the switching transient. The reduced gate resistance can increase the *dv*/*dt* to the preset target value but also bring about an increased current overshoot which tends to increase the loss.

A maximum turn-OFF loss reduction of up to 38% can be obtained as shown in Fig. 8. Above 30% load, the turn-OFF loss reduction rate is increasing with the increase of *dv*/*dt*. Once the load is lighter than 30%, the turn-OFF gate resistor has already reached its minimum value. Due to the limitation of *dv*/*dt* controllability below 30% load, the turn-OFF loss reduction rate also started to decline at about 30% load.

Fig. 8 also shows that the switching loss can be reduced in the entire power range. The maximum total switching loss reduction rate can be up to 22% at about 30% partial load. In the operational power range, the turn-OFF loss reduction rate is much higher than the turn-ON loss due to the latter being significantly affected by the current overshoot which offsets the benefit of *dv*/*dt* control.

## IV. Discussion

In this letter, the effect of switching loss reduction of the proposed *dv*/*dt* control strategy is verified. But some issues should be taken into account in application.

For applications with multiple SiC MOSFET devices, the trade-off between the number of the gate resistor branches and the *dv*/*dt* control accuracy is needed to be considered. More resistor branches can improve *dv*/*dt* control, but at the expense of more I/O resources from the DSP.

The *dv*/*dt* is controlled to the target value in the entire power range. But the *dv*/*dt* controllability is also limited by the internal gate resistance of the SiC MOSFET.

To limit the switching speed and avoid current localization among the cells in individual chips of the SiC MOSFET module, the manufacturer often builds a gate resistor inside the chip, so the actual gate resistance is as follows:

$$R_{\rm G} = R_{\rm Gint} + R_{\rm Gext} \quad (7)$$

where $R_{\rm Gint}$ is the internal gate resistance in $\Omega$, and $R_{\rm Gext}$ is the equivalent external gate resistance in $\Omega$.

The *dv*/*dt* controllability limit caused by $R_{\rm Gint}$ is also a reason why the switching loss reduction rate starts to decline at a light load level. A current source active gate drive can be used to avoid the *dv*/*dt* controllability fading-away.

For a given switching frequency, the upper limit of the tolerable *dv*/*dt* may be determined by several factors, such as EMI constraint, insulation degradation of the load motor, etc. Therefore, the target *dv*/*dt* value varies case by case and should be carefully devised during the convertor design. For instance, the partial discharge and progressive insulation aging problem would require the maximum *dv*/*dt* to be limited to 6–12 kV/$\mu$s in variable speed drives [21].

The effectiveness of the *dv*/*dt* control strategy, i.e., the switching loss reduction rate, is closely related to the *dv*/*dt* fluctuation during the mission profile. Larger *dv*/*dt* fluctuation implies there is more headroom to be utilized for loss reduction by gate resistance reduction. As a result, one can expects that the proposed control strategy is more suitable for applications for most of the time working at light load. The temperature may affect some of the device parameters in (3) and (4). This letter has ignored the temperature effect. Results shown in Fig. 7 were obtained at room temperature (∼25 °C). Those shown in Figs. 5 and 6 were obtained with an ambient temperature of ∼25 °C, but the temperatures of the SiC MOSFET and SBD were not measured. The temperature effect will be a subject of future investigation.

Fig. 9 shows the distribution of load levels in an EV power system. It is noteworthy that for over 80% of the time, the load level is below 55%. With the proposed *dv*/*dt* control strategy and using the 600 W boost dc–dc converter as a unit, a total

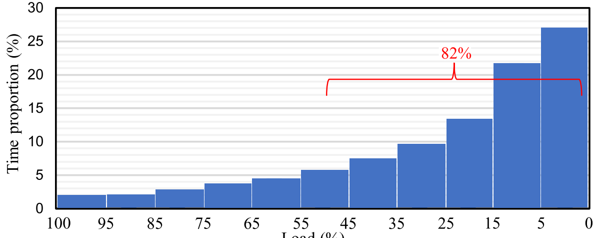


Fig. 9. Typical load level distribution of an electric vehicle (source: Chongqing Changan New Energy Vehicle Technology Co., Ltd).

power loss reduction of up to 11.4% could be achieved, which is beneficial to the convertor efficiency and power device reliability improvement.

In practice, voltage and current overshoots and resonance during switching should be considered. The control tends to increase the overshoots and resonance. Therefore, it is crucial to optimize the converter layout to reduce these parasitic effects.

The study also suggests that it might be useful to enhance EMC and insulation designs for the benefit of loss reduction. It is hoped that the study could be a useful reference.

## V. Conclusion

A dynamic $dv/dt$ control strategy of SiC MOSFET for switching loss reduction within the entire operational power range is proposed. To verify the proposed control strategy, a variable gate resistance method is implemented with a closed-loop control to regulate the $dv/dt$. It is shown that the effectiveness of the switching loss reduction varies with the percentage of power load. At 30% power load, the turn-ON and turn-OFF losses can be reduced by up to 10% and 38%, respectively, and the total switching losses can be reduced by up to 22%. With the proposed $dv/dt$ control strategy, a total power loss reduction of up to 11.4% could be achieved for an EV converter which mostly operates at light load levels. The proposed $dv/dt$ control strategy and the experimental results could be a reference for future SiC converter designs.

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