Design Procedure and Efficiency Analysis of a 99.3% Efficient 10 kW Three-Phase Three-Level Hybrid GaN/Si Active Neutral Point Clamped Converter

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***Abstract*—High-efficient and power-dense ac–dc power electronic converters are demanded for a wide range of applications, such as motor drives and active rectifiers. The utilization of wide bandgap devices, such as gallium-nitride (GaN) transistors, is a key feature to improve both the efficiency and the power density of power electronic converters. Owing to the superiority of GaN switches, this article achieves a high-efficiency three-level active-neutral-point-clamped converter. However, using GaN transistors is critically dependent on the layout configuration to achieve smooth switching transient and, as equally important, efficient cooling. Therefore, this article presents layout optimization and considers different layout configurations to achieve a low power loop inductance and as efficient heatsink assembly/performance. Two configurations of the switch boards are built by GaN/Si MOSFETs, and a power loop inductance comparison is presented. Furthermore, a comprehensive loss model is performed to fine-tune the switching frequency from the efficiency and the size point of view. A 10 kW laboratory prototype voltage source converter, including an electromagnetic interference (EMI) filter, is built with the switching frequency of 140 kHz. The efficiency measurement is performed and confirmed the full load efficiency of 99% and peak efficiency of 99.34%. Moreover, the CISPR11 Class A conducted EMI standard is fulfilled.**

***Index Terms*—Active neutral point clamped (ANPC), efficiency, electromagnetic interference (EMI) filter, multilevel converter, power-factor correction (PFC), volume minimization.**

I. Introduction

IN RECENT years, the power demanding for dc loads, such as electric vehicle battery charging, LED lighting equipment, information and communication technology equipment, modern data centers, and variable-speed drives are increasing drastically [1]. Typically, to supply these dc loads with the range of kilowatts and more, an ac–dc stage as an interface between the conventional ac grids and dc is employed. Considering high power levels of these loads and grid tie standards, sinusoidal ac input currents are required. Therefore, the applications of three-phase active rectifiers are more considered in which a regulated dc voltage at the output is provided while the sinusoidal ac input current is in-phase with the input voltage.

Compared with the conventional two-level converters, multilevel converters provide a staircase output voltage, lower voltage across semiconductors, lower *dv/dt*, improved current and voltage total harmonic distortion (THD), and smaller filter size [2], [3]. Among various multilevel topologies, considering the number of switches and complexity of modulation techniques, three-level converters are attractive for industries. The neutral point clamped (NPC) converter and T-type converter are the two well-known structures in the industry. The advantages and disadvantages of each of these topologies have been thoroughly investigated in the literature. T-type converter presents lower conduction loss and higher switching losses due to blocking the full dc-link voltage. In general, T-type converter is more employed in applications with the lower switching frequency, while NPC shows more advantages at higher switching frequency [4]. The main drawback of NPC converter is unequal distribution of power losses, which limits the maximum power rating and switching frequency of the converter [5]–[7]. To solve these, active NPC (ANPC) converter was proposed in which the clamping diodes are replaced with active switches [7]. With this modification, more redundant switching states are obtained, which are utilized to balance the loss distribution.

In applications, such as electric vehicle battery charging and power supplies for data centers, high-efficient and power-dense converters are required [4]. One way to decrease the size of converters is to increase the switching frequency, which results in ac filter size reduction. However, there is a limitation about increasing the switching frequency due to the switching frequency range of Si technology. Meanwhile, the advent of wide-bandgap (WBG) devices, such as silicon-carbide (SiC) and gallium-nitride (GaN), enables power electronic converters to reach higher switching frequency, efficiency, and more power density. The SiC and GaN based materials have

Manuscript received May 21, 2021; revised August 26, 2021 and October 11, 2021; accepted November 20, 2021. Date of publication December 1, 2021; date of current version February 18, 2022. This work was supported by APETT Project, funded by Innovation Fund Denmark. Recommended for publication by Associate Editor D. Zhang. *(Corresponding author: Mohammad Najjar.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TPEL.2021.3131955.

Digital Object Identifier 10.1109/TPEL.2021.3131955

higher breakdown voltage, shorter switching time, and lower switching losses [8]. As a result, employment of WBG devices in multilevel topologies can result in highly power dense and efficient converters. Therefore, many multilevel typologies, including ANPC have been modified by employing WBG devices.

On the other hand, the fast switching transition (*dv/dt* and *di/dt*) of WBG switches introduces overvoltage, ringing, and electromagnetic interference (EMI) issues [9]–[11]. The switch capacitors, packaging inductance and parasitic inductances of printed circuit board (PCB) layout are the main causes of these unwanted behaviors. Therefore, properly designing the layout can reduce the overvoltage and ringing issues. In addition, increasing the switching frequency propagates harmonics with higher amplitude to high-frequency (HF) range, especially in the EMI range (>150 kHz). To attenuate HF harmonics [i.e., common mode (CM) noise and differential mode (DM) noise] regarding EMI standards, high-order filter structure should be employed [12], [13]. Increasing the order of EMI filter provides more attenuation for both DM and CM noises; however, it reduces the power density and efficiency of the converter. Therefore, an EMI filter should be designed employing few stages and a careful selection of components.

Apart from the topology of the converter, the modulation technique can affect the efficiency and power density. Different modulation techniques have been presented for three-level ANPC. In the first group of modulation techniques, some of the switches have different switching frequency in positive and negative half-cycle [14], [15]; meanwhile, in the second group, the switching frequency of devices are constant during positive and negative half-cycle [4], [16]. In various cases of the second group, the switching frequency of some switches is grid frequency (e.g., 50 Hz). Based on the number of switches with grid frequency, two different cases can be defined: 1) four out of six switches are low-frequency (LF) switches, 2) two of the switches are modulating with grid frequency. In these two cases, different switch technologies can be used, for example, Si/IGBTs as LF switches and SiC/GaNs as HF switches. In these cases, the losses related to the LF switches are mainly the conduction loss and the switching loss can be neglected.

This article presents the design procedure of a high efficient 10 kW three-level ANPC converter. Considering the employment of a hybrid modulation technique, in which switches are controlled at different switching frequencies, two different switch technologies, including Si MOSFETs and enhancement-mode GaN transistors, are employed in the structure of the converter. Due to the effects of stray inductances on the performance of GaN transistors, the Q3D Extractor from ANSYS is utilized to find out and compare the optimum placement of HF switches on the switch board. Two different switch board layout configurations are considered and built. Regarding the power loop inductance and mechanical assembly, one of the configurations is selected. A comprehensive loss analysis, including conduction and switching losses, is performed to find the efficiency behavior of the switch board at different switching frequencies. Considering the effect of various switching frequencies on the converter size and efficiency, 140 kHz switching frequency is selected, and an EMI filter is designed. To improve the efficiency of the converter, a discrete pulsewidth modulation (PWM) technique is used. As a result, the current ripple of the converter side inductor is thoroughly studied to determine the core loss. Moreover, the design procedure of the EMI filter to obtain a compact size is also presented. The efficiency performance of constructed converter and the output EMI results are experimentally validated.

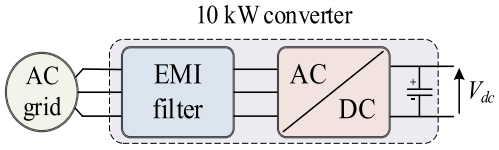

Fig. 1. Structure of grid connected active rectifier.

In summary, the main contributions of this article are as follows.

1) Design procedure of a high-efficient and power-dense ANPC converter that includes a compact EMI filter.
2) Hybrid use of Si/GaN switches in the structure of ANPC converter.
3) Comparison of two distinct ANPC switch board layout configurations in terms of the power loop inductances, thermal performances, and mechanical assemblies.
4) Analysis of the converter side inductor current ripple when discrete PWM 1 (DPWM1) is applied.
5) Comprehensive loss examination of the converter, which includes the loss calculation of switches, capacitors, and filter components.

The rest of this article is organized as follows. The system description and the overall design procedure of the converter are presented in Section II. Section III presents design procedure and power loss analysis of the hybrid switch board. The cooling system and dc-link capacitor selection are described in Section IV. The structure of the EMI filter is presented in Section V. The experimental results are demonstrated in Section VI. Finally, Section VII concludes this article.

II. System Description, Design Procedure, and Structure of the Converter

A. System Description and Design Procedure

The schematic of the system is shown in Fig. 1. The converter is comprised of the EMI filter and the ac–dc stage. The main tasks of the active rectifier are to keep the unit power factor and to provide a fixed dc-link voltage. The system specifications are listed in Table I. As can be seen, the dc-link voltage is regulated at 570 V; therefore, the converter operates in the overmodulation region. In fact, by reducing the dc-link voltage, the switching losses of converters and the filter size are reduced, and consequently, the efficiency is improved. Among various carrier-based overmodulation techniques, DPWM1 is chosen to reduce the switching loss.

The design procedure of the converter is shown as a flowchart in Fig. 2. Based on the system parameters the topology can be chosen. Owing to the ANPC structure, in which the voltage across the devices is half of the dc-link voltage, 650 V GaN

TABLE I
SYSTEM SPECIFICATION

Parameter	Specification
Nominal power (P_{nom})	10 kW
Input voltage (V_g)	230 V_{ac} (RMS)
Nominal current (I_{nom})	14.5 A (RMS)
Grid frequency (f_g)	50 Hz
dc-link voltage (V_{dc})	570 V
Efficiency	> 98.5 %
Current THD	< 3 %
Size	< 5 liters
Power factor	> 0.98
EMI standard	CISPR 11 class A
Modulation technique	DPWM1

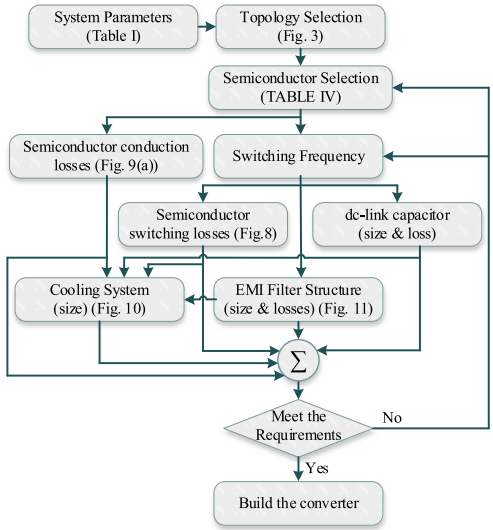

Fig. 2. Flowchart of the design procedure.

transistors can be used and consequently give considerable benefits over T-type and two-level configurations in terms of higher efficiency and power density [17]. In addition, ANPC provides output voltage harmonics with lower amplitude compared to two-level structure. Therefore, the size of passive components of the output filter is smaller. Regarding the switching frequency and modulation techniques, semiconductors are selected and the conduction and switching losses can be calculated. The effects of different switching frequencies on the efficiency and size of the converter are studied. Therefore, the switching frequency which meets all the requirements is selected. Finally, the EMI filter and cooling system are designed.

B. ANPC Structure and Hybrid Modulation Techniques

The one-phase structure of the three-level ANPC converter is shown in Fig. 3 in which six switches and two dc-link capacitors are employed. Three different output voltage levels (V_{out}) can be obtained through 14 combinations of devices.

One way to improve the efficiency of the converter is employing hybrid modulation techniques. In these methods, the switching frequency of devices is different and regarding the characteristics of devices various semiconductor technologies can be used. Considering the number of LF and HF switches, two

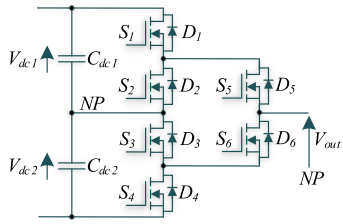

Fig. 3. Structure of three-level ANPC converter.

TABLE II
DIFFERENT HYBRID MODULATION TECHNIQUES FOR THREE-LEVEL ANPC

Hybrid Modulation techniques	LF switches	HF switches
Group I	S_5, S_6	S_1, S_2, S_3 and S_4
Group II	S_1, S_2, S_3 and S_4	S_5, S_6

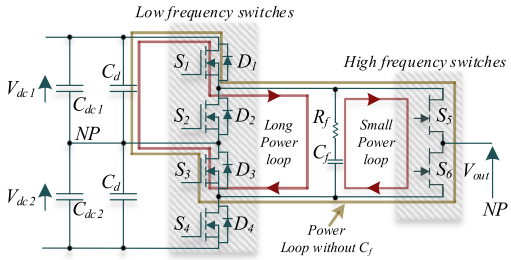

Fig. 4. Structure of three-level hybrid GaN/Si based ANPC converter. The figure includes the decoupling capacitors and power loops during the positive half-cycle operation.

TABLE III
SWITCHING STATES OF THREE-LEVEL HYBRID ANPC CONVERTER (GROUP II)

Output States	Switching states						Output Voltage
	S_1	S_2	S_3	S_4	S_5	S_6	
P	1	0	1	0	1	0	V_{dc1}
O^+	1	0	1	0	0	1	*0*
O^-	0	1	0	1	1	0	*0*
N	0	1	0	1	0	1	$-V_{dc2}$

different hybrid modulation techniques can be defined for three-level ANPC structure, which are listed in Table II [18]–[20]. In the first group, four switches are controlled with an HF carrier, meanwhile in the second group of hybrid modulation technique, two switches are modulating with a carrier frequency. However, employing LF switches in the second stage of the converter (S_5, S_6), introduce more switching losses. The reason is related to the output capacitor of the LF switches, which are in parallel with the output capacitors of HF switches. In fact, during each half cycle, the output capacitor of one of the LF switches, is charged and discharged with the switching frequency of the converter. Therefore, the second group of hybrid modulation technique is considered in this article. As a result, the structure of three-level ANPC is modified as shown in Fig. 4. As it can be seen, the switches are divided into two categories of LF and HF switches. The output states of the hybrid converter are listed in Table III in which three different output levels can be obtained through different switching patterns. During the positive half cycle, switches S_1 and S_3 are conducting; meanwhile, S_5 and S_6 are switching with the carrier frequency. In the negative half

TABLE IV
SPECIFICATIONS OF HF AND LF SWITCHES

Switch	GS66516T	NTHL033N65S3HF
Voltage	650 V	650 V
I_{DS} (25 °C)	60 A	70 A
I_{DS} (100 °C)	47 A	53 A
$R_{DS\text{-}on}$ (25 °C)	25 mΩ	28 mΩ
$R_{DS\text{-}on}$ (150 °C)	65 mΩ	60 mΩ
C_{iss}	518 pF @ 400 V	6720 pF @ 400 V
C_{oss}	126 pF @ 400 V	159 pF @ 400 V
C_{rss}	5.9 pF @ 400 V	25 pF @ 400 V
V_{th}	1.7 V	3 V
$V_{gs\text{-}max}$	-10 to +7	±30 V
Q_{rr}	0	1003 nC
Device Package	GaNPX®	TO−247

cycle, S_2 and S_4 are in the ON-state, and S_5 and S_6 are controlled with HF. By employing the hybrid modulation technique, the commutation of LF switches is kept at fundamental, and the main loss of these switches is conducting loss. On the other side, the HF switches are modulating with the carrier frequency. Consequently, both conduction and switching losses are presented at HF switches. The voltage across all the switches is half of the dc-link voltage by employing hybrid modulation technique. The utilized switches and their characteristics are listed in Table IV.

III. DESIGN AND POWER LOSS ANALYSIS OF AC–DC STAGE

A. *Designing the Switch Board*

The PCB layout creates a significant contribution of the stray power loop inductances when the GaN FETs with low parasitic packaging are utilized. The power loop inductances affect the switching losses at high switching frequency operation. To reduce the power loop inductances, several stages of decoupling capacitors (C_d, C_f) are inserted between dc-link capacitors and LF switches, as well as between LF and HF switches, as shown in Fig. 4. During the positive half cycle, the long power loop inductance ($L_{\text{loop-}L}$) is the sum of the package inductances of switches S_1 and S_3, and the PCB inductances between two stages of decoupling capacitors. Meanwhile, the small power loop inductance ($L_{\text{loop-}S}$) is comprised of package inductances of the two utilized GaNs in series with the PCB trace parasitic inductances. The PCB parasitic inductances in the small power loop consist of the inductance from the positive terminal of C_f up to the drain of top GaN, the trace inductance related to the distance between two HF switches and finally the inductance of the path between the source of the bottom switch and negative terminal of C_f. However, adding C_f introduces new issues such as a resonance current during the switching transition of HF switches [16], and current spikes and ringing during the commutation of LF switches [21]. The resonance current occurs between C_f and $L_{\text{loop-}L}$ [16]. In addition, the voltages of up-side and low-side of dc-link capacitors are not always equal due to nature of ANPC structure. Also, during the commutating of LF switches, one of the dc-link capacitors is connected in parallel with C_f, which has previously been connected to the opposite dc-link capacitor. Therefore, current spikes and ringing occur.

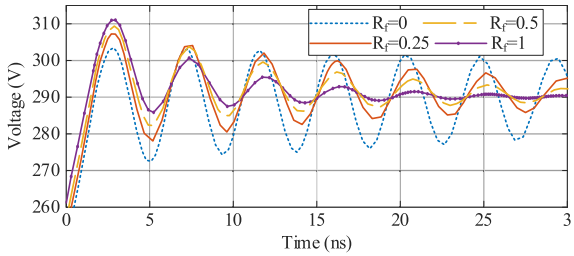

Fig. 5. LTspice simulation results for different values of R_f.

To minimize $L_{\text{loop-}L}$, the LF and HF switches, C_d and C_f are placed nearby on the switch board.

The voltage variation across the C_f is obtained as follows [16]:

$$\Delta V_{c_f} = I_p \sqrt{L_{\text{loop}-L}/C_f} \tag{1}$$

where I_p is the peak of the phase current. Therefore, the value of C_f can be calculated based on the maximum acceptable voltage variation across it. Furthermore, a low value resistor (R_f) is used in series with C_f. The R_f is not in the path of the main current; consequently, it does not contribute to the losses. During the transition of HF switches, the resistor helps dampen the HF resonances. In addition, the current spikes are reduced during the commutation of LF switches. Choosing a high value for this resistor can reduce the effects of C_f regarding reducing the value of power loops. In this article, R_f is mainly designed based on the damping of HF resonances. Considering the path of small power loop, a series *RLC* circuit is obtained. Therefore, the voltage across the switch can be assumed as follows:

$$\left(S^2 + \frac{R}{C_{oss@V_{\text{in}}}} S + \frac{1}{L_{\text{loop}-S} C_{oss@V_{\text{in}}}}\right) V_{\text{out}} = V_{\text{in}} \tag{2}$$

where $C_{oss@Vin}$ is the output capacitor of the HF switch at V_{in}, V_{in} is equal to half of the dc-link voltage, and R is the sum of R_f, the PCB resistance related to the small power loop, the turn-ON resistance of the HF switch and the ESR of C_f. The system response can be defined by a damping factor given as follows:

$$\xi = {}^{R}/_{2} \sqrt{{}^{C_{oss@V_{\text{in}}}}/_{L_{\text{loop}-S}}} > 0\,. \tag{3}$$

As a result, based on the considered damping factor, R_f is obtained. To show the effects of different R_f on the HF resonance, a comprehensive simulation is performed in LTspice. The voltage across one of the GaNs, where the hard switching occurs, is simulated for different values of R_f. The simulation results are shown in Fig. 5. As it can be seen, increasing the value of R_f reduces the damping time of HF resonance. However, the peak and frequency of the resonance change as the impedance of small power loop changes compared with the power loop without C_f (see Fig. 4).

One combination to reach a low small power loop inductance is when the HF switches are mirrored and mounted on both sides of the board, as can be seen in Fig. 6(a) (first case). With this combination, the distance between HF switches is limited to the thickness of the PCB. Moreover, a minimized small loop inductance can be obtained by placing the decoupling

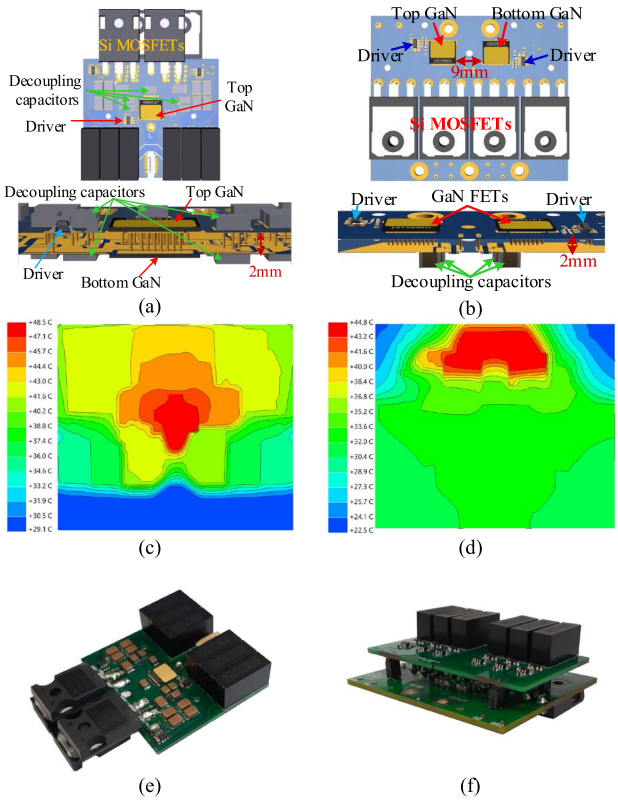

Fig. 6. Designed switch boards (a) GaN FETs are on both sides of the board (first case). (b) GaN FETs are in one side of the board (second case). (c) Thermal steady-state simulation of first case. (d) Thermal steady-state simulation of second case. (e) Built switch board of first combination. (f) Built switch board of second combination.

capacitors (C_f) close to HF switches. This combination provides the minimized small power loop inductance; however, it suffers from losses accumulation in a small area on the switch board. Moreover, designing a heatsink connected to both sides of the switch board is challenging. As a result, this combination suffers from heat accumulation and challenging regarding mechanical assembly. Other combination, as shown in Fig. 6(b) (second case), can be achieved by placing both HF switches on one side of the board, where one single heatsink can be employed for all the switches. Compared with the first case, this placement results in a larger small power loop inductance. Meanwhile, the losses are not localized in a small area. In both cases, eight layers are utilized for the boards. Also, the thickness of layers is set to be 2oz. To demonstrate the thermal effect of GaNs placement regarding the heat dissipation in PCBs, simulations are performed in Ansys Icepak. For both cases, a similar thermal environment with natural convection is applied. For each GaN, a 0.5 W loss is considered. The thermal results of both cases are shown in Fig. 6(c) and (d). As it can be seen, in the first case, the maximum temperature of the PCB is higher compared with the second case. The built switch boards are shown in Fig. 6(e) and (f).

The Q3D Extractor is utilized to obtain the values of PCB inductances. In the ANSYS simulations, the thickness of the layers and materials is taken from material datasheets and data

TABLE V
SIMULATION AND EXPERIMENTAL RESULTS FOR TWO DIFFERENT CASES

Case	I	II
L_{pcb} (Simulation- without package inductance)	0.55 nH	3.6 nH
L_{loop} (Experimental)	1.3 nH	4.4 nH

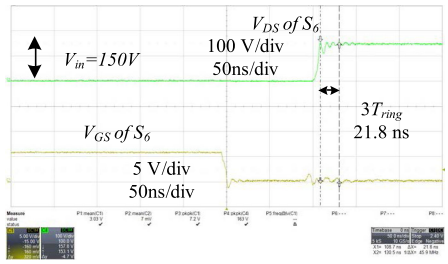

Fig. 7. Drain–source and gate–source voltage waveforms of S_6.

provided by the manufacturer. The obtained traces inductances are added in series and listed in Table V. Moreover, to verify the obtained results an experiment is done for both cases. In the implemented experiment, a dc voltage supply ($V_{\rm in}$) is placed across the HF switches and an RL load is connected in parallel with S_6. Both switches are switching complementary with a fixed duty cycle. To find the parasitic loop inductances, the resonance frequency of the voltage across the bottom GaN is measured after the top switch is turned ON. In this transition, the output capacitance of the switch and the stray small power loop inductance ring at the resonant frequency. Thus, the loop inductance can be calculated as follows:

$$L_{\text{loop}-S} = {T_{\text{ring}}}^2 / 4\pi^2 C_{oss@V_{\text{in}}} \tag{4}$$

where T_{ring} is the ringing time, $C_{\text{oss@Vin}}$ is the output capacitor of bottom GaN at input voltage of V_{in}.

The obtained results related to both cases are listed in Table V. The difference between results in each case can be related to the packaging inductance. In fact, the simulation results just give the stray inductances of the PCB traces. Meanwhile, the experimental results comprise both the stray inductances of the PCB traces and package inductances of the switches. In addition, the drain–source and gate–source voltages of S_6 for the second case are shown in Fig. 7. As can be seen, the resonance frequency is 137.7 MHz. Based on the value of output capacitor of S_6 ($C_{\text{oss@150V}}$), the small power loop of 4.4 nH is obtained. In the second case, four parallel decupling branches with $C_f = 100$ nF and $R_f = 0.3\ \Omega$ are used.

Considering the results, advantages and disadvantages of both cases, the second case is selected in this article. Therefore, the converter assembly is designed based on the second case.

B. Switching Loss

The switching energy losses are turn-ON (E_{on}) and turn-OFF (E_{off}). The turn-ON loss includes the VI overlapping ($E_{\text{VI-on}}$) and capacitor charging loss (E_{qoss}) [22], [23]. The source of the E_{qoss} is the output capacitor (C_{oss}) of the opposite device in the half-bridge circuit. The turn-OFF loss can be divided

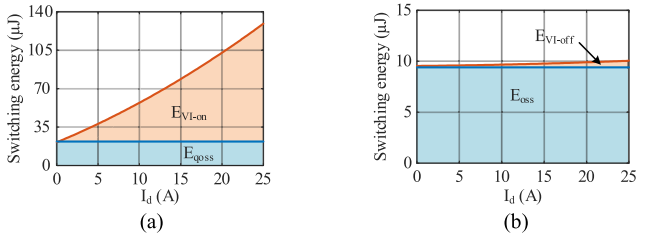

Fig. 8. Switching losses. (a) Turn-ON loss. (b) Turn-OFF loss.

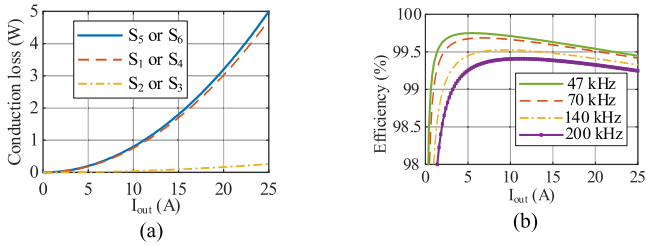

Fig. 9. Calculated results. (a) Conduction losses of different switches. (b) Efficiencies of the switch board for different switching frequency.

into VI overlapping ($E_{\text{VI-off}}$) and capacitor charging loss (E_{oss}). E_{oss} is related to the self-discharging of switch output capacitor [22], [23]. E_{oss} and $E_{q\text{oss}}$ are the outcomes from the nonlinear output capacitance (C_{oss}) and the voltage across the device (V_{DS}) and are independent of switching speed. E_{oss} and $E_{q\text{oss}}$ can be defined as follows [22], [23]:

$$E_{\text{oss}} = \int_0^{V_{\text{dc}}/2} V_{\text{DS}} . \text{C}_{\text{oss}}(V_{\text{DS}}) dV_{\text{DS}} \tag{5}$$

$$E_{q_{\text{oss}}} = \int_0^{V_{\text{dc}}/2} \left(\frac{V_{\text{dc}}}{2} - V_{\text{DS}} \right) . \text{C}_{\text{oss}}(V_{\text{DS}}) dV_{\text{DS}} \tag{6}$$

where V_{dc} is the dc-link voltage.

The $E_{\text{VI-on}}$ and $E_{\text{VI-off}}$ are related to the dynamic current provided by the gate driver and the total time of the switching transition. In fact, the magnitude of overlap losses depends on the turn-ON and turn-OFF gate resistors. Typically, a lower value for turn-OFF resistor is considered compared to turn-ON resistor. Meanwhile, using a low value of turn-OFF resistor can decrease the related overlap losses, which can be neglected.

A complete spice simulation is performed through LTspice to find E_{on} and E_{off} losses. First, the PCB layout was imported into the Q3D Extractor of ANSYS software. Then, the parasitic LCR values are extracted and imported as a spice model into LTspice. The spice model of HF devices from the manufacture is also utilized in the simulation environment. Finally, a comprehensive simulation is done, and the E_{on} and E_{off} are simulated for different currents. By utilizing curve-fitting tools, the switching losses are calculated. The obtained switching losses for HF switches are shown in Fig. 8. As can be seen, with increasing the output current, E_{on} is also increased. Meanwhile, E_{off} is almost constant for different currents due to applying a low turn-OFF resistor.

The LF switches have transition just during zero-crossing; therefore, the switching loss related to LF switches can be neglected.

C. Conduction Loss

The generalized equation of conduction loss is given as follows:

$$P_{\text{con}} = V_0 I_{\text{avg}} + R_{\text{DS-on}} {I_{\text{rms}}}^2 \tag{7}$$

where V_0 is the initial voltage drop, $R_{\text{DS-on}}$ is the drain–source equivalent resistance of the switch during conduction, I_{avg} is the average current, and I_{RMS} is the RMS current passing through the device.

In most power converters, an antiparallel diode is employed across the drain–source terminals of the switch. In some cases, it is inherent to the device structure (body-diode), such as Si MOSFET [24]. This body diode causes reverse recovery losses during the transition of the switch. For the GaN FETs, due to the lack of body diode, there is no reverse recovery loss of the body-diode. Meanwhile, a mechanism is embedded to conduct reverse current when the switch is OFF, allowing operation similar to a diode [24].

In the considered hybrid modulation technique, the gate signals of the LF switches are always kept in ON-state to enable the Si MOSFET channel. Therefore, the current goes through the channel instead of the body diode, if it is required. The body diode of LF switches is utilized for current commutation during the zero-crossing. Besides, during zero-crossing the current is relatively small when the converter works at unity power factor. Therefore, the body diode loss of LF switches can be neglected.

For the GaN FETs, the *I–V* curves with the same gate voltage are symmetrical in the first and third quadrants [23]. It means that, with a positive or negative current flow, the turn-ON voltage of the device is the same. Therefore, the device starts to conduct in the third quadrant whenever the V_{gd} (V_{gs}–V_{ds}) is higher than the threshold voltage V_{th} [23]. In this article, the zero-gate-voltage ($V_{\text{gs-off}} = 0$) is employed for the HF switches to keep the turn-OFF voltage around threshold voltage. Based on the characteristics of DPWM1, there is not any deadtime loss when the reference waveform is ± 1 due to the lack of switching transition [see Fig. 13(a) or the output voltage of the switch board]. In addition, the deadtime is set at 140 ns. For simplification, the losses related to the deadtime are neglected in this article.

For Si MOSFET and GaN FET V_0 is zero. Therefore, with neglection the body-diode loss, (4) can be rewritten as follows:

$$P_{\text{con}} = R_{\text{DS-on}} {I_{\text{rms}}}^2 . \tag{8}$$

To calculate the conduction losses, the RMS current for each device should be analytically calculated. The RMS current of each switch and body-diode in ANPC are presented in [25], when the sinusoidal PWM technique is utilized. Meanwhile, different modulation techniques change the RMS current of devices. Therefore, a modification should be considered. Based on an analytical approach similar to [25], the RMS current of each switch can be obtained as (9)–(11) when DPWM1 is

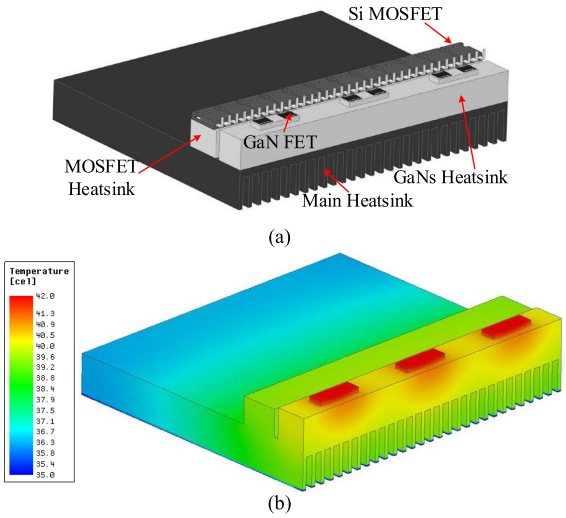

Fig. 10. Thermal system. (a) Designed heatsink. (b) Ansys Icepak steady-state simulation of the heatsink.

employed, (10) and (11) shown at the bottom of this page

$$I_{\mathrm{rms\_HF}} = \frac{I_p}{2} \tag{9}$$

where m is the modulation index as (12), I_p is the peak current and θ is the phase difference between the current and the voltage.

$$m = \frac{V_{\mathrm{ac}} 2\sqrt{2}}{V_{\mathrm{dc}}}\,. \tag{12}$$

The conduction losses of different switches are shown in Fig. 9(a). Due to the difference in the RMS current of LF switches, when DPWM1 is utilized, the main conduction losses of LF switches happen in outer switches (S_1 and S_4).

The calculated efficiency of the switch board for different switching frequencies are shown in Fig. 9(b). As it can be seen, with increasing the switching frequency, the peak of efficiency is reduced and happened at a higher output current.

IV. Cooling System and DC-Link Capacitors

The considered heatsink for the converter is shown in Fig. 10(a). As it can be seen, the heatsink is comprised of the following three parts: the main heatsink, the MOSFET, and the GaN heatsinks. The two aluminum bars are employed to connect all the switches of all three phases to the main heatsink. Considering the two constraints of mechanical assembly and maximum junction temperature of HF switches, the main heatsink is designed to be placed below the whole converter. To show the effectiveness of the heatsink, a thermal simulation is performed. In the simulation, the loss of each switch is calculated at full load and modeled as heat source. The result of steady-state simulation of heat dissipation is shown in Fig. 10(b). As it can be seen, the hotspots of the heatsink are the parts close to the HF switches, where the main losses occur. Considering the thermal resistance of the junction to case and insulation pads, which can be extracted from datasheets, the simulation results confirm the ability of the designed heatsink to keep the junction temperature of HF switches less than 70 °C.

The value of dc-link capacitor is determined based on the acceptable voltage ripple, which is defined by the capacitor current harmonics [26]. Assuming that all these harmonics are in phase, the dc-link capacitance is determined by [26]

$$C_{\mathrm{dc}} \geq \frac{2}{\Delta V_{\mathrm{dc-max}}} \cdot \sum \frac{I_h}{2\pi f_h} \tag{13}$$

where $\Delta V_{\mathrm{dc\text{-}max}}$ is the maximum acceptable dc-link voltage ripple, I_{h} and f_{h} are the amplitude and related frequency of the current harmonics, which flow through the dc-link capacitors and can be obtained through simulations software. Therefore, the dc-link capacitor faces both LF and HF current ripples. Meanwhile, the LF harmonics have the most effect on the capacitor voltage ripple. For the maximum voltage ripple of 5%, the value of each dc-link capacitors should be higher than 0.6 mF. Considering the main application of this converter, which is the front-end part of a variable frequency motor drive, the capacitance value of 1 mF is considered in the final design. Beside the voltage ripple in the dc-link capacitors, the thermal loss is an important factor. This loss is related to the ESR and RMS current of the capacitor. As a result, the RMS current of the dc-link capacitor for ANPC converter is calculated as follows [26]:

$$I_{\mathrm{RMS-dc,cap}} = I_p \sqrt{\frac{m\sqrt{3}\,\left(4\,\cos(\theta)^2 + 1\right)}{4\,\pi} - \frac{9\,m^2\,\cos(\theta)^2}{16}}\,. \tag{14}$$

Considering the RMS current, the required value of the dc-link capacitor, and physical constraints, the number of parallel electrolytic capacitors is chosen. In addition, the ESR of capacitors is not fixed for the whole frequency range. To reach a low ESR, both film capacitors are used in parallel with electrolytic capacitors in the converter structure.

$$I_{\mathrm{rms\_}S1,S4} = I_p \sqrt{\frac{\left(6\,m - 3\,\pi + 6\,\mathrm{asin}\left(\frac{1}{m}\right) + 6\,m\,\sqrt{\frac{m^2-1}{m^2}} + 2\,m\,\cos(2\,\theta) - 4\,m\,\cos(2\,\theta)\,\left(\frac{m^2-1}{m^2}\right)^{3/2}\right)}{12\pi}} \tag{10}$$

$$I_{\mathrm{rms\_}S2,S3} = I_p \sqrt{-\frac{\left(3\,m - 3\,\pi + 3\,\mathrm{asin}\left(\frac{1}{m}\right) + 3\,m\,\sqrt{\frac{m^2-1}{m^2}} + m\,\cos(2\,\theta) - 2\,m\,\cos(2\,\theta)\,\left(\frac{m^2-1}{m^2}\right)^{3/2}\right)}{6\pi}} \tag{11}$$

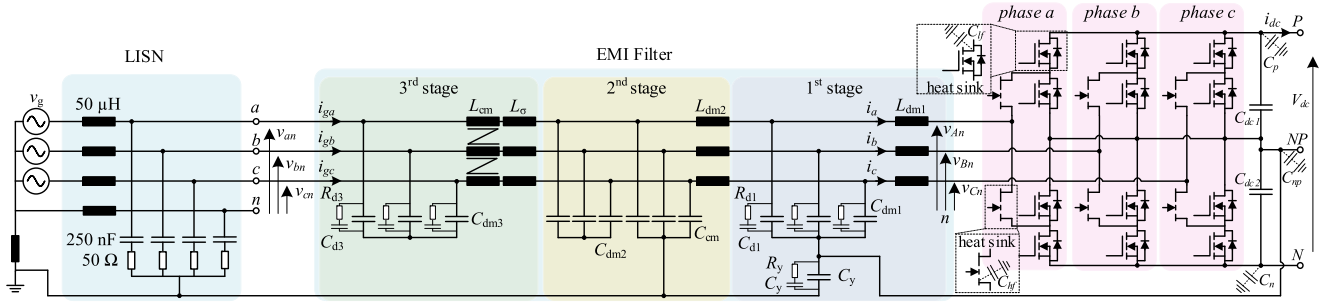

Fig. 11. EMI filter structure of three-phase active rectifier of Fig. 1.

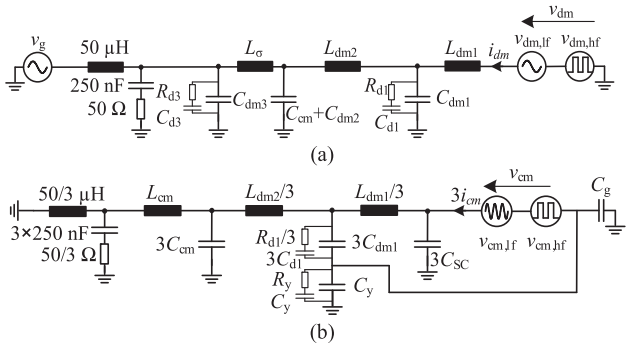

Fig. 12. Equivalent circuit (a) DM (b) CM, $v_{\mathrm{cm,lf}}$ is the zero-sequence component of DPWM1 technique, which enables the converter to operate in overmodulation range [12], [28].

V. EMI Filter Structure and Design Procedure

A. Filter Structure

The considered three-phase filter structure is shown in Fig. 11, in which three stages of *LC* filter are utilized. This configuration can provide enough attenuation for both DM and CM noises by employing few magnetic components. Moreover, the simplified model of the line impedance stabilization network (LISN) is added between the filter and grid [13], [27]. Fig. 12 shows the equivalent DM and CM circuits. The switch boards and dc-link capacitors (power stage) are modeled by LF and HF DM and CM voltage source, $v_{\mathrm{dm,lf}}$, $v_{\mathrm{dm,hf}}$, $v_{\mathrm{cm,lf}}$, $v_{\mathrm{cm,hf}}$ [12], [28].

The first filter stage is comprised of a boost inductor (first DM inductor—L_{dm1}) and DM capacitors. The star point of DM capacitors is connected to the middle point of dc link to provide a path for both LF and HF CM currents. A series connection of resistors and capacitors in parallel with DM capacitors is employed as the damping network. Moreover, the star point of DM capacitor is connected to the ground through a CM capacitor (C_y). To prevent resonance phenomena between the CM capacitor and DM inductor of the second stage, another damping branch in parallel with the CM capacitor is employed [29].

In the second stage of the filter DM inductors, DM and CM capacitors are used. The CM capacitors are directly connected to the ground provided by the power network. This combination includes attenuation for both DM and CM noises. The effect of DM inductor on CM noise is one/third of DM inductor ($L_{\mathrm{dm2}}/3$), wherein the effective CM capacitors is $3C_{\mathrm{cm}}$.

A CM inductor and DM capacitors are used as the third filter stage. Due to the leakage inductance of the windings (L_σ) and parasitic coupling between the stages, DM capacitors (C_{dm3}) are added at the mains side. In order to prevent HF resonance between the leakage inductance of CM inductor and DM capacitors, a damping network for DM capacitors is utilized in this stage.

The considered parasitic capacitors are shown in Fig. 11 [12], [28], [30]. The switches are mounted on the heatsink through an insulation pad. Considering the Si MOSFETs package (TO−247−3) and the thickness of the insulation pad, the parasitic capacitance of Si MOSFET to ground is assessed as around 45 pF. With the same consideration for HF switches, the parasitic capacitance of GaNs to the ground is considered as 9 pF. Therefore, the maximum parasitic capacitance at the output of switch board to the ground can be obtained when the output is connected to the positive dc-link rail [28] and can be assessed as follows:

$$\mathrm{C}_{sc} = 2C_{\mathrm{lf}} + C_{\mathrm{hf}} \approx 100\ \mathrm{pF}\ . \tag{15}$$

The parasitic capacitor of the output reduces the CM attenuation of the first filter stage through bypassing the first DM inductors [28]. The other considered parasitic capacitance is the summarization of dc-link parasitic capacitances, which are from the positive (C_p), negative (C_n), and middle point (C_{md}) of dc-link to ground. This value can be assumed as follows:

$$C_g = C_p + C_n + C_{\mathrm{np}} \approx 500\mathrm{pF}\ . \tag{16}$$

Meanwhile, the dc-link parasitic capacitor is in parallel with C_y. C_g should be considered for the low values of C_y. However, this parasitic capacitor can be neglected for C_y values above 10 nF.

B. EMI Standard and Switching Frequency

The considered EMI standard in this article is CISPR11 class A [31] (see Table I), in which the quasi-peak of the measured voltage through LISN should be less than 79 dBμV in the frequency range of 150–500 kHz and less than 73 dBμV in the frequency range of 500 kHz–30 MHz.

The EMI filter is designed based on the first major harmonic falling inside the EMI range ($f > 150$ kHz). Therefore, different

switching frequencies can affect the required attenuation and, consequently, the EMI filter [13]. The frequency ranges can be divided into 37.6–49.9 kHz, 51–74.9 kHz, 75.1–149.9 kHz, and finally above 150 kHz. In each of these frequency ranges, the minimal filter size can be obtained at the end of the frequency range [13]. For example, for the switching frequency ($f_{\rm sw}$) in the range from 37.51–49.9 kHz, the filter is designed based on the harmonic magnitude at $4f_{\rm sw}$. For the switching frequency in the EMI range, the filter is designed based on the harmonic content at switching frequency (biggest harmonic). As discussed in [13], decreasing the size of EMI filter through increasing the switching frequency is not applicable for all switching frequency ranges. In addition, increasing the switching frequency reduces the efficiency of switch board [see Fig. 9(b)]. Therefore, to decrease the size of the EMI filter and to improve the total efficiency of the converter, a proper switching frequency should be selected. Considering efficiency of switch board [see Fig. 9(b)], the size of the cooling system and the EMI filter switching frequency of 140 kHz is selected in this study. Accordingly, the EMI filter is designed based on harmonic content at 280 kHz ($2f_{\rm sw}$).

C. Filter Design

The required attenuation for DM and CM noises are calculated 90 and 85 dB at 280 kHz ($2f_{\rm s}$), respectively. The required attenuations are distributed between stages. In each state, maximum reactive power of 1.5% is considered for capacitors. In addition, the total inductance is constrained to less than 2% of nominal power to limit the voltage drop across inductors.

To design the DM inductors, powder E-cores (XFlux E-cores) from Magnetics are used. The powder core materials are the right candidate for high ripple current conditions due to the constant losses despite increasing the ripple of magnetic field intensity [28]. Moreover, the high permeability nanocrystalline material (VITROPERM from VAC) is employed to design the CM inductor.

1) First Filter Stage: The boost inductor ($L_{\rm dm1}$) is designed based on the maximum acceptable output current ripple, usually limited to 10%–40% of the nominal current peak. Therefore, this inductor is designed to limit the current ripple to 3 A ($0.15 \times \sqrt{2} \times 14.5$). It can be assumed that the voltage after the boost inductor or the voltage across the first DM capacitor ($V_{\rm Cdm1}$) is sinusoidal, and the amplitude is close to the grid voltage (V_g) if the first stage of the filter is designed correctly [32]. Therefore, the voltage across $L_{\rm dm1}$ can be calculated as follows:

$$v_{\rm Ldm1}(t) = v_{\rm Cdm1}(t) - v_{\rm An}(t) \tag{17}$$

where $v_{\rm An}(t)$ is the output voltage of the switch board. Consequently, the general current waveform of the boost inductor can be depicted as it is shown in Fig. 13(a), in which the converter is operating in overmodulation region. Additionally, it is assumed that the converter is operating at a unity power factor. Therefore, the current ripple for $L_{\rm dm1}$ can be calculated as follows [32]:

$$\Delta i_{\rm Ldm1} = \frac{v_{\rm Cdm1}(t) - v_{\rm An}(t)}{L_{\rm dm1}} \Delta t \tag{18}$$

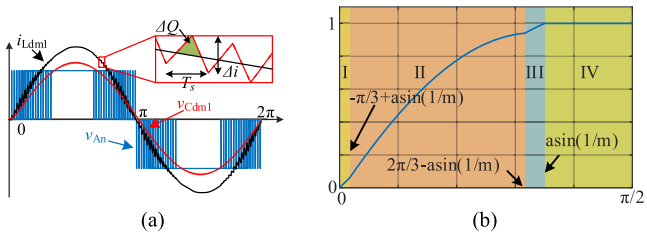

Fig. 13. Waveforms of DPWM1 for $m > 1$. (a) Current of the first DM inductor, the output voltage of the converter, and voltage across the first DM capacitor. (b) Reference waveform of DPWM1 and related regions.

where Δt is the time interval of the current ripple.

Employing DPWM1 changes the current ripple waveform and, consequently, the degree of the maximum current ripple. The reference waveform of DPWM1 and the associated regions are shown in Fig. 13(b). As it can be seen, the reference waveform has different equations in different sectors. As a result, the general waveform of the current ripple is divided into four regions as (19). Due to the absence of switching transitions in region IV, the current ripple is equal to zero

$$\Delta i_{\rm Ldm1} = \begin{cases} \frac{V_{\rm dc}}{2L_{\rm dm1}f_{\rm sw}}(1 - m\sin(\omega t)) \times m\sin(\omega t) & \text{I} \\ \begin{cases} \frac{V_{\rm dc}}{2L_{\rm dm1}f_{\rm sw}}(1-x)\times x \\ x = m(\sin(\omega t) - \sin(\omega t - \frac{2\pi}{3}) + (1/m)) \end{cases} & \text{II} \\ \frac{V_{\rm dc}}{2L_{\rm dm1}f_{\rm sw}}(1 - m\sin(\omega t)) \times m\sin(\omega t) & \text{III} \\ 0 & \text{IV} \end{cases} \tag{19}$$

where ω is the angular frequency of the reference waveform and $f_{\rm sw}$ is the switching frequency.

The degree that the maximum current ripple occurs can be obtained by solving $d(\Delta i_{\rm Ldm1})/d\omega t = 0$. Therefore, the maximum current ripple is obtained as (20), and consequently, the minimum $L_{\rm dm1}$ to limit the maximum acceptable current ripple can be obtained.

$$\Delta i_{\rm Ldm1,max} = \frac{V_{\rm dc}}{8L_{\rm dm1}f_{\rm sw}}. \tag{20}$$

Considering (20) and maximum current ripple less than 3 A, an inductor with the value of 160 μH is required. Additionally, to reach the maximum increasing temperature of 45 °C, the core material and size are selected [33]. Based on [33], the core with small size and maximum number of turning is chosen. As a result, the winding area is completely occupied.

Normally, the HF current ripple flows through the filter capacitor [32]. Therefore, the minimum required capacitance value for the first DM capacitor ($C_{\rm dm1}$) can be obtained through the calculation of the maximum converter current ripple. The maximum voltage ripple in $C_{\rm dm1}$ can be calculated as follows:

$$\Delta V_{\rm ripple} = \frac{\Delta Q_{\max}}{C_{\rm dm1}} \approx \frac{1}{C_{\rm dm1}} \frac{1}{2} \frac{\Delta i_{\rm Ldm1,max}}{2} \frac{T_s}{2} \tag{21}$$

where $\Delta Q_{\max}$ represents the maximum charge in the filter capacitor as the shaded area in Fig. 13(a).

From (21), it can be concluded that the minimum required filter capacitance is inversely dependent on the $L_{\rm dm1}$ value and proportional to the square of the switching frequency. As a result,

TABLE VI
EMI FILTER COMPONENTS

Parameter	Design Value	Hardware Realization	Volume (cm^3)
L_{dm1}	160μH	E-cores (00X4020E060) N= 39, A=22×0.15mm (copper foil)	46.32
C_{dm1}	0.5μF	0.68 μF (B32924A4684M, EPCOS)	7.26
C_{d1}	0.2μF	0.2 μF (B32912A3224M, EPCOS)	2.8
R_{d1}	90Ω	180 Ω ‖ 180 Ω (2w resistor)	0.47
C_y	10nF	10 nF (B32021A3103M, EPCOS)	0.94
R_y	90Ω	180 Ω ‖ 180 Ω (2w resistor)	0.47
L_{dm2}	80μH	E-cores (00X4317E060) N= 25, A=15×0.2 mm (copper foil)	18.45
C_{cm}	1μF	1 μF (B32024A3105M, EPCOS)	25.29
C_{dm2}	1μF	1 μF (BFC233926105, Vishay)	5.07
L_{cm}	1mH	toroidal cores (T60006-L2045-V118, VAC), N =9, d=1.9 mm (enameled wire)	39.25
C_{dm3}	400nF	470nF (R523I347050P0K, KEMET)	2.22
R_{d3}	5Ω	5.6 Ω (0.6W resistor)	0.03

Total volume of filter components is equal to 372.56 cm^3 (26 kW/dm^3).

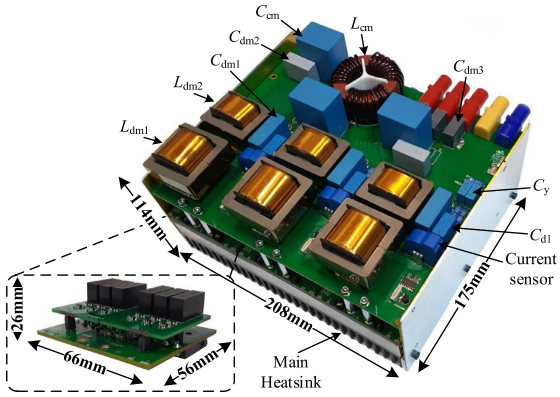

Fig. 14. 10 kW hardware prototype of three-level ANPC and the designed switch board employing GaN/Si MOSFETs. The EMI filter components are mounted on a PCB. The EMI filter is on the top of the converter. The overall converter size is 4150 cm^3 (17.5×20.8×11.4), which equals to 2.4 kW/dm^3. Filter box volume is 1480 cm^3 (6.75 kW/dm^3). The volume of switch board (56×66×26 mm) is 96.096 cm^3; consequently, the power density of 34.68 kW/dm^3 is obtained.

the value of the filter capacitor is determined as follows [34]:

$$C_{\rm dm1} > \frac{V_{\rm dc}}{64\Delta V_{\rm ripple} L_{\rm dm1} {f_{\rm sw}}^2}. \tag{22}$$

Moreover, the first DM capacitor is designed to limit the voltage ripple across it to less than 2%. This combination provides 48 dB attenuation for DM; meanwhile, the filter parasitic reduces the CM attenuation of the first filter to 30 dB. The damping branch elements of DM capacitors are designed for $C_{d1}/C_{\rm dm1} = 0.3$ and a maximum resonant gain of 20 dB [12].

2) Second and Third Filter Stage: The designing factors for $L_{\rm dm2}$ are to reduce the current ripple to 0.2% of the peak current [32] and to provide the remaining required attenuation for DM noise. Therefore, an inductor with value of 80 μH is used. The combination of $L_{\rm dm2}$ and $C_{\rm dm2}+C_{\rm cm}$ provides the DM attenuation of this stage. In addition, the combination of $L_{\rm dm2}$, $C_{\rm cm}$, and $L_{\rm cm}$ should provide the rest of required attenuation for the CM noise. The CM inductor of the third filter stage is considered based on [12], [35] as follows:

$$L_{\rm cm} = L_{\rm choke}\frac{1+2k_{\rm cm}}{3}, k_{\rm cm} = \frac{L_{\rm choke}-L_\sigma}{L_{\rm choke}} \tag{23}$$

where $k_{\rm cm}$ is the coupling factor, and $L_{\rm choke}$ is the self-inductance of phase winding. To reduce the conduction loss in $L_{\rm cm}$, a solid wire with diameter of 1.9 mm and 9 turns is used to reach an inductance value of 1 mH. Considering the value of $L_{\rm cm}$, $C_{\rm cm}$ can be calculated to reach the attenuation for CM noise.

The $C_{\rm dm3}$ is designed to shift the HF resonance between this capacitor and L_σ to less than switching frequency. The selected components related to the EMI filter are listed in Table VI. The total volume of all EMI components is measured as 372.56 cm^3.

VI. EXPERIMENTAL RESULTS AND COMPARISON

The constructed converter, including the EMI filter, is shown in Fig. 14. As it can be seen, the EMI filter is placed on top of the converter. The overall converter size is measured as 4150 cm^3 (2.4 kW/dm^3) in which the empty spaces inside the converter is also considered. Meanwhile, the total converter size without the heatsink and empty spaces is 1986 cm^3 (5 kW/dm^3).

The dSPACE's Micro-Lab Box ds1202, including an FPGA, is utilized to control the converter. The employed signals for the controller are shown in Fig. 11, which are the current of $L_{\rm dm1}$ and the main side voltage. To mitigate current distortion during zero-crossing, the idea of [6] is implemented.

The experimental results are shown in Fig. 15, when the converter is connected to a grid simulator (MX45 ac Power Source) and the converter is acting as an active rectifier. The three-phase input currents of the converter are shown in Fig. 15(a). The distortions at the current peak are related to the DPWM1 technique and deadtime effect in the corresponding phase. These distortions cause increasing the magnitude of LF harmonics. Meanwhile, the THD of the input current is less than 1.9%, which satisfies grid-tie standards. Fig. 15(b) depicts the input phase voltage and current. Based on the phase difference between phase voltage and current, it can be calculated that the controller adjusts the power factor to be more than 0.98. The NP voltage is regulated by the controller in which the voltages of dc-link capacitors are balanced at 285 V [see Fig. 15(c)]. Moreover, the output voltage of the switch-board is shown in Fig. 15(c).

To measure the efficiency of the converter, another test is performed. In this case, a YOKOGAWA-WT3000 precision power analyzer is utilized. Both the ac [$v_{\rm an}$, $v_{\rm bn}$, $v_{\rm cn}$, and $i_{\rm ga}$, $i_{\rm gb}$, $i_{\rm gc}$, see Fig. 11] and dc [$V_{\rm dc}$ and $i_{\rm dc}$] sides are connected to the power analyzer; therefore, the EMI filter and dc-link losses are included in the measurement. However, the power consumption of a fan (OD9225-24HSS), gate drives, protection circuits and sensors are not included in the measurements. Meanwhile, at full load the total power loss of these circuits is 11 W.

In this case, the load step is applied to the system, and to make sure that the converter is thermally stabilized after at least 10 min the efficiency is recorded. In addition, an average mode of the measurement is active and taking an average of over 256 cycles. The efficiency measurements are performed for both

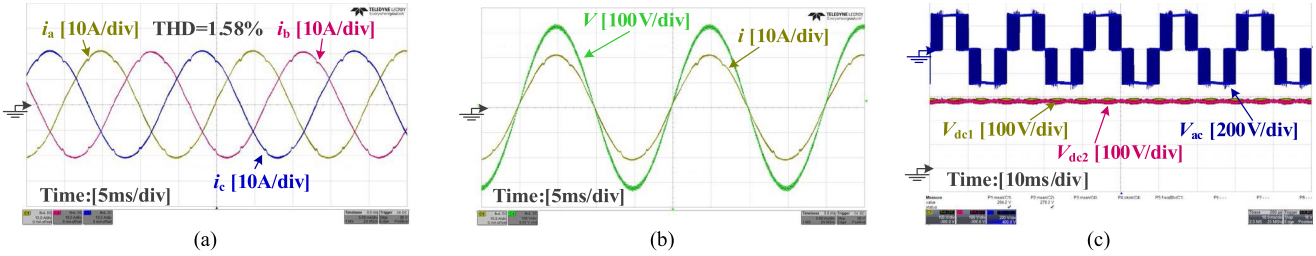

Fig. 15. Experimental measurements, (a) Input three-phase currents. (b) Phase voltage and current (unit power factor). (c) Output voltage of switch board (to the NP voltage), and dc-link capacitor voltages.

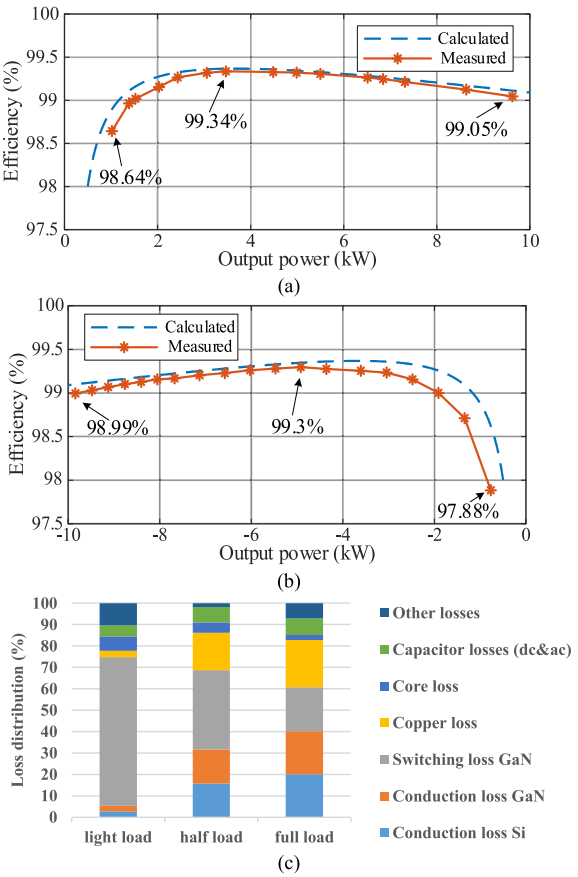

Fig. 16. Efficiency results, (a) calculated and measured efficiency at rectifier mode based on dc output power, (b) calculated and measured efficiency at inverter mode based on ac output power, and (c) loss distribution for different loads at rectifier mode.

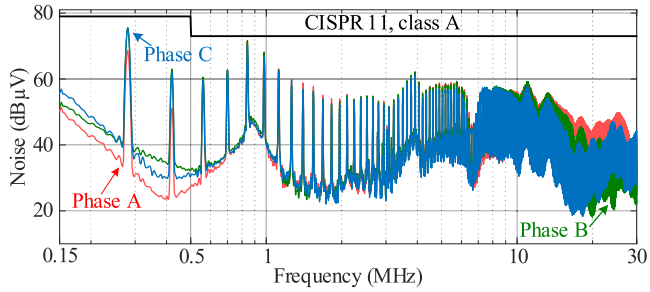

Fig. 17. Measured EMI result (DM+CM noises) at switching frequency 140 kHz.

active rectifier mode, which the converter is connected to the grid, and inverter mode, where just a resistive load is connected at the ac side of converter and the dc side is supplied through a dc source. Fig. 16(a) shows the calculated and measured efficiency curves of the converter in active rectifier mode. As it can be seen, there is a close similarity between these two curves. For the wide range of output powers, the efficiency is above 99%, and the peak efficiency of 99.34% is recorded as around half of the output power. Fig. 16(b) shows the efficiency curve of the converter at inverter mode. A close similarity can be seen between efficiency curves in both operation modes. Obtaining the flat efficiency curve for a wide range of output power ($P > 2$ kW) can be considered as a noticeable achievement of the designed converter. The loss distribution of the converter for three different output power levels is shown in Fig. 16(c), in which the percentage of each loss at different output power is shown. To calculate the conduction loss of each device, (9)–(11), (14) are employed. The switching losses are calculated through the $E_{\rm on}$ and $E_{\rm off}$ losses shown in Fig. 8. The main filter losses are associated with the core and copper losses. The resistance of each winding is calculated by knowing the cross-sectional area and the length of it. As a result, the conduction loss of each inductor is obtained. Considering the current harmonics at HF is relatively small compared to the fundamental, only the copper loss at fundamental frequency is considered. Due to the change in the magnetic flux field or the HF current ripple in the boost inductor, the core loss related to this inductor is considered. The core loss is calculated using the current tipple from (19) in $L_{\rm dm1}$. The inductance value of the inductor at different currents is modeled based on the dc bias performance of the core and the number of turns [33]. Therefore, the magnetizing field (H), flux density (B), and related core loss is calculated through equations provided in [33] and [36]. It is assumed that the current passes through $L_{\rm dm2}$ is without current ripple. Therefore, the core loss related to this inductor is neglected. The difference between the calculated and measured efficiencies is considered as the other loss. PCB copper losses and neglected losses can be counted as the main source of these losses. For example, the reverse conduction loss of HF switches during the deadtime is 0.8 W at full load, which contributes to less than 1% of the total losses of the converter. Nevertheless, the percentage of other losses is less than 10%.

The measured conducted EMI through the LISN and the EMI receiver for three phases are shown in Fig. 17. The first major harmonic happens at 280 kHz, which the filter is designed based

TABLE VII
COMPARISON OF OTHER THREE-PHASE VOLTAGE SOURCE CONVERTERS

Ref	Power (kW)	Switch Type	dc-link voltage (V)	Switching Frequency (kHz)	Power Density (kW/ dm^3)	Filter Structure	Peak Efficiency	EMI Standard
[4]	4.2	Si/SiC	650	30	n/a	L	99.5	n/a
[21]	12.5	Super-junction	690	16	3.4	LCLCL	99.35	CISPR 11 Class A
[30]	10	CoolMOS -SiC-Si	800	1000	14.1	LCLCLC	93.8	CISPR 11 Class A
[37]	10	SiC	600	40	n/a	LCL	98.78	n/a
[38]	5	SiC	565	50	n/a	LCL	99.1	n/a
[39]	5	SiC	750	48	n/a	L	97.8	n/a
[39]	5	Si-IGBT	750	16	n/a	L	96.5	n/a
[40]	10	SiC	580	16	0.94	LCL	99.1	n/a
[41]	10	SiC	580	40	3.16	LCL	98.8	n/a
[41]	10	SiC	580	80	5.23	LCL	98.2	n/a
[42]	3	SiC	650	22.4	1.5	L	99.12	n/a
This work	10	GaN/Si	570	140	2.4	LCLCLC	99.34	CISPR 11 Class A

on this harmonic. As it can be seen, the CISPR 11 class A is completely fulfilled for the whole EMI range.

A comparison is provided between related literature and this article and listed in Table VII. A few works consider efficiency, power density, and EMI filter, all at the same time. Comparing the efficiencies and power densities confirms the comprehensive and efficient design procedure of this article.

VII. CONCLUSION

This article summarizes comprehensive design procedure, loss and efficiency analyses of a 10 kW hybrid GaN/Si based ANPC converter. By employing the hybrid modulation technique, only two out of six switches operate with carrier-frequency. Therefore, two different switch technologies are applied in the structure of the converter. To find the finest placement of switches and to minimize the power loop inductance, the Q3D Extractor from ANSYS was utilized. A comparison regarding power loop inductance and mechanical assembly of two different combinations of the placement of GaN transistors was provided. Considering the employed overmodulation technique (DPWM1), the RMS current of each switch was calculated to model the conduction losses. Comparing the effects of different switching frequencies on the efficiency and converter size, the 140 kHz switching frequency was selected. To reduce the size of the EMI filter, a careful component selection was performed, in which an EMI structure with few magnetic components was selected. Due to careful designing of the converter, a flat efficiency curve with a peak efficiency of 99.34%, and a full load of 99% was achieved. In addition, the constructed EMI filter fulfils the CISPR 11 Class A conducted EMI standard.

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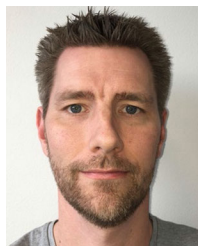

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