

# Letters

## Boosting Nine-Level Operation of Seven-Level Hybrid-Clamped (7L-HC) Converter

Hao Tian , Member, IEEE, Li Ding , Member, IEEE, and Yun Wei Li , Fellow, IEEE

**Abstract**—Seven-level hybrid clamped topology, which is a multilevel topology proposed in recent years, is a promising solution for motor drive systems due to its capability to operate in a wide frequency range. This letter enhances its favorable features by enabling the boosting nine-level operation, i.e., producing nine output voltage levels; wherein the peak phase voltage can be four-third of the dc voltage. This operation method does not require modifications to the topology or change in the voltage stress on capacitors and power switches. Instead, only minor modifications to the modulation are applied. This leads to the increase of the ac voltage range without any cost on hardware. This method shows great potential in speed expansion of the motor drive system. Experimental results validate the feasibility and performance of this method. This letter is accompanied by a video file demonstrating the speed expansion performance of the proposed method.

**Index Terms**—DC-AC power converters, pulse width modulation, variable speed drives.

### I. INTRODUCTION

MULTILEVEL topologies have wide applications due to their favorable features, such as reduced power semiconductor devices' blocking voltage, low output  $dv/dt$ , high output quality, favorable common-mode voltage profile, etc. [1]. In addition to successfully commercialized topologies, such as neutral-point-clamped (NPC) converter, T-type NPC converter, flying capacitor (FC) converter, active NPC converter (ANPC), modular multilevel converter (MMC), cascaded H-bridge (CHB) converter, etc., novel topologies are still being invented to meet various requirements in practice [2]–[4]. For example, the seven-level hybrid clamped (7L-HC) converter, shown in Fig. 1, is invented in recent years and has been considered to be a promising topology for motor drive systems due to its low device count, low blocking voltage of devices, and

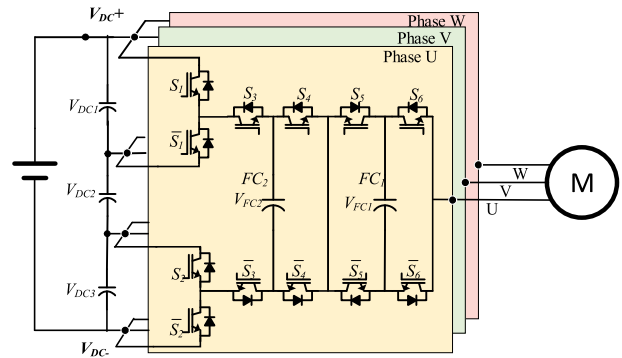


Fig. 1. 7L-HC converter topology and its application in motor drive systems.

the ability to balance its capacitors in wide ranges of modulation index and power factor [4], [5].

Besides inventing new topologies, extending the operating range of the existing topologies, e.g., producing more output levels or expanding the output range, is also a promising topic, which can unleash the potential of topologies and bring better features. One typical method to extend the operation of a multilevel converter is to change the voltage on floating capacitors so that more output levels can be produced [6], [7]. Alternatively, modifications in topologies, such as using the internal parallel concept [8], [9], can also bring new operation features for multilevel converters. Quan and Li [8] add paralleled half-bridge cell to 5L-ANPC converter and produce nine output levels with the help of interleaving. A boost mode is found in MMC with full-bridge submodules and the output range is expanded in [10].

In this letter, a boosting nine-level (9L) operation method is proposed for the 7L-HC converter. This operation method can help 7L-HC to produce nine output levels and when the extra levels are generated, the peak phase voltage can be four-third of dc voltage while the voltage stress on devices will not be increased. Such expansion of the output voltage is favored by motor drive systems [11], [12], as this can help increase the speed range of motors by simply increasing the voltage limitation. For converters without such boosting capability, expanding speed without changing devices' voltage stress can be achieved with flux weakening control [13], [14], where the voltage/current trajectory needs to be properly designed on the base of an accurate system model. Therefore, it is more complex and less

Manuscript received October 21, 2021; revised December 1, 2021; accepted December 26, 2021. Date of publication December 29, 2021; date of current version February 18, 2022. This work was supported in part by Canada First Excellent Research Fund (CFERF) and in part by the Natural Science and Engineering Research Council of Canada (NSERC). (Corresponding author: Li Ding.)

The authors are with the Department of Electrical and Electronic Engineering, University of Alberta, Edmonton, AB T6G 2V4, Canada (e-mail: tianhao1988@gmail.com; ldng@ualberta.ca; yunwei.li@ualberta.ca).

This article has supplementary material provided by the authors and color versions of one or more figures available at <https://doi.org/10.1109/TPEL.2021.3139220>.

Digital Object Identifier 10.1109/TPEL.2021.3139220

TABLE I  
COMPARISON BETWEEN 9L CONVERTERS AND THE PROPOSED OPERATION ON 7L-HC CONVERTER

	9L-CHB	9L Topology in [16]	Boosting operation on 7L-HC Topology
No. of Switches	48	36	36
Highest Voltage Stress on Switches	$V_{DC}/6$	$V_{DC}/2$	$V_{DC}/3$
Switches' total Blocking voltage	12 $V_{DC}$	12 $V_{DC}$	10 $V_{DC}$ * $1/m_{max}^1$
No. of Floating capacitors	0	2	2
No. of DC Capacitors	12	2	3
Isolated DC sources	16	0	0
Requirement on Transformer	Mandatory	Unnecessary	Unnecessary

<sup>1</sup>Total blocking voltage can be 7.6~9  $V_{DC}$  as different system designs can lead to different allowable maximum modulation index  $m_{max}$ .

reliable compared with the boosting operation in this letter. Also, it is worth noting that the boosting operation will not increase motors' insulation requirements as inverter-fed motors are designed to withstand high voltages (e.g., 2.04 ~ 3.1 times of rated line-to-line voltage [15]) to resist steep fronted waves with large  $dv/dt$  produced by power converters. The boosting 9L operation only increases the voltage to be 4/3 times of rated voltage while the  $dv/dt$  is not changed, i.e., still the typical  $dv/dt$  of 7L converters.

Besides, unique features are found in this operation method when compared with the existing extended operation method of multilevel converters.

1) it does not require modifications in topology, ensuring no extra hardware cost is needed.

2) it does not change the capacitor voltage so that it avoids the risks brought by changing the normal voltage on floating capacitors, which is a key parameter that can impact voltage stress on switches and output quality. As shown in Table I, with the proposed method, the converter can have a low device count and low total blocking voltages of switches when compared with other 9L converters that are also suitable for motor drives. Experimental results validate the feasibility and performance of the boosting 9L operation when the 7L-HC converter is feeding R-L load or motor.

## II. SWITCHING STATES AND MODULATION FOR NORMAL AND BOOSTING OPERATION

The normal 7L operation of the 7L-HC converter utilizes 22 switching states to produce desired output level. Most of the switching states are redundant states for balancing the floating and dc-link capacitor voltages. In addition to the 22 normal switching states, two more switching states can be added to generate the extra two output levels. All the switching states are shown in Table II, where switching states are represented as binaries whose bits indicate the ON/OFF-state of  $S_1\bar{S}_1-S_6\bar{S}_6$ , respectively. It can be observed that the switch  $S_n$  and  $\bar{S}_n$  ( $n = 1-6$ ) are always complementary so that the capacitors will not be short-circuited.  $S_1\bar{S}_1$  and  $S_2\bar{S}_2$  should always have the states, otherwise,  $S_3$  and  $\bar{S}_3$  may suffer doubled voltage stress. This

TABLE II  
APPLICABLE SWITCHING STATES FOR NORMAL AND BOOSTING OPERATION OF 7L-HC CONVERTER

Level	Output Voltage	State No.	Switching States ( $S_1\bar{S}_1-S_6\bar{S}_6$ )		
E0	$-2V_{DC}/3$	0A	01010101001		
N1	$-V_{DC}/2$	1A	01010101010		
		2A	010110011001		
		2B	010101101001		
		2C	101001011001		
N2	$-V_{DC}/3$	2D	010101010110		
		3A	101001010101		
		3B	010110010101		
		3C	010101101010		
N3	$-V_{DC}/6$	4A-	101010011001		
		4B-	101001101001		
		4C-	101001010110		
		4A+	010101100110		
		4B+	010110010110		
		4C+	010110101001		
		5A	010110101010		
		5B	101001101010		
N5	$V_{DC}/6$	5C	101010010101		
		6A	101001100110		
		6B	101010010110		
		6C	010110100110		
N6	$V_{DC}/3$	6D	101010101001		
		7A	101010101010		
		E8	2 $V_{DC}/3$	8A	101010100110

leads to 32 possible combinations but only 24 of them can produce unduplicated and proper output voltage for the normal 7L and boosting 9L operation.

In Table II, the output levels for normal operation are defined as N1~N7. Redundant switching states can be found for capacitor balancing for these levels. The extended two levels are represented as E0 and E8, and the corresponding switching states are defined as 0A and 8A, respectively. The current flow path for the two switching states of 0A and 8A are depicted in Fig. 2. As can be seen, *State 0A* for *Level E0* can produce  $-2V_{DC}/3$  and *State 8A* for *Level E8* can produce  $2V_{DC}/3$ , whereas N1~N7 can only generate voltages ranges between  $-V_{DC}/2 \sim V_{DC}/2$ . As a result, the two output levels can do boosting conversion, i.e., the peak ac voltage is higher than the dc voltage. Meanwhile, it can be easily found from Fig. 2 that *State 0A* and *State 8A* will not change the voltage stress on all power switches— $V_{DC}/3$  for  $S_1\bar{S}_1-S_4\bar{S}_4$  and  $V_{DC}/6$  for  $S_5\bar{S}_5-S_6\bar{S}_6$ .

Accordingly, the modulation range is expanded. A level-shift modulation method is shown in Fig. 3. To avoid interference to the normal operation, the extended modulation range is defined in the range of  $[-4/3, -1)$  and  $(14/3]$ . In this case, the modulation index can be increased to 1.33 without the third-order injection method applied. The expected extended boosting output levels will be produced when the modulation reference runs into the extended range. When the modulation index is lower than 1, active capacitor balancing will be performed to ensure the voltage on floating capacitors and dc-link capacitors, which is well discussed in [5].

## III. CONSTRAINTS OF THE BOOSTING OPERATION

As can be seen from Fig. 2, the boosting levels, *Level E0* and *E8*, do not contain redundant switching states for state

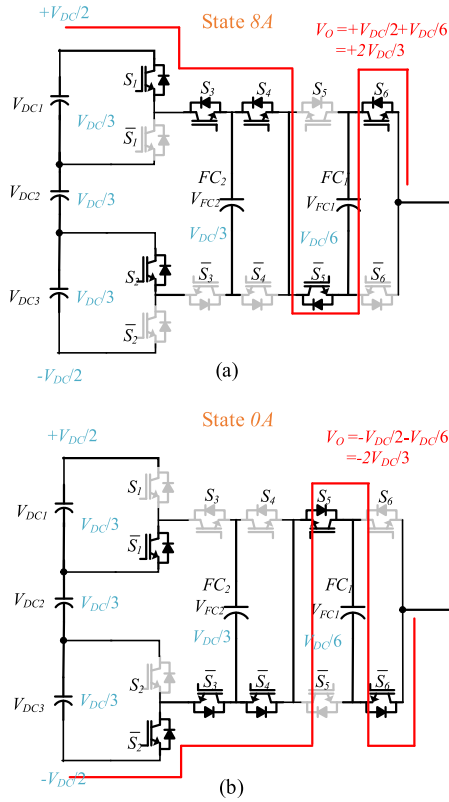


Fig. 2. Equivalent circuits of boosting levels. (a) State 8A. (b) State 0A.

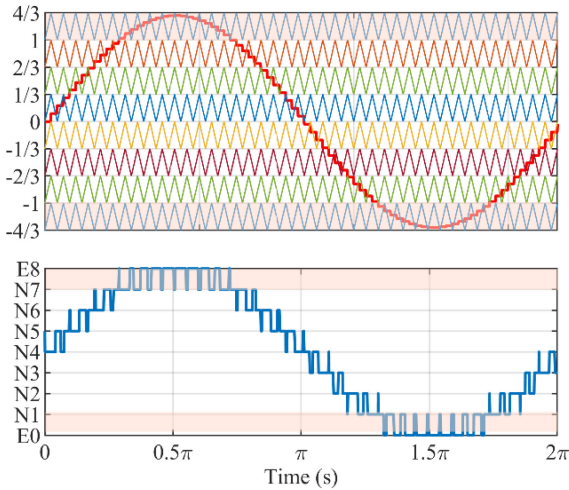


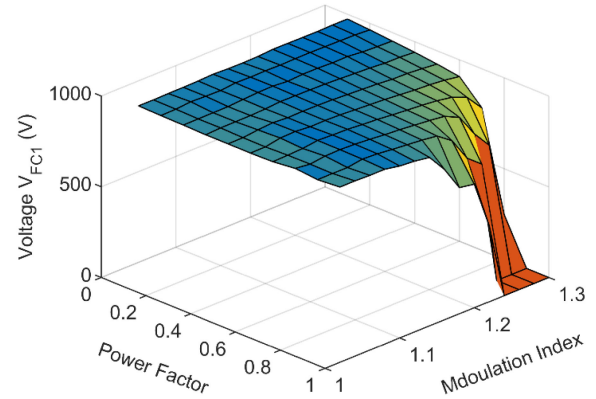
Fig. 3. Modulation and output voltage level for the boosting 9L operation.

balancing and the increased output voltage relies on the voltage of floating capacitor  $FC_1$ . As a result, when the boosting levels are produced, the capacitor  $FC_1$  will always be charging or discharging under a specific current direction-line frequency ripple will appear. And the voltage deviations can only be corrected under the opposite current direction or the normal levels N2–N6 can be applied.

The boosting 9L operation is expected to be enabled without adding extra hardware cost. In this case, the capacitance of floating capacitors should still be selected for a normal 7L converter.

 TABLE III  
PARAMETERS USED FOR ANALYSIS

Parameter	S.I values	p.u values
Rated DC Voltage	6000V	-
Rated AC Voltage	4160V	1.0
Rated Power	1 MW	1.0
Base Impedance	8.65 $\Omega$	1.0
Floating Capacitor $C_1$	1000 $\mu$ F	3.26
Floating Capacitor $C_2$	1000 $\mu$ F	3.26
DC link Capacitors $C_{dc}$	2700 $\mu$ F	8.8


 Fig. 4. Voltage of  $FC_1$  under different modulation and power factor when 0.5 p.u load is applied.

Generally, the floating capacitor can be designed as follows:

$$C_{FC} > \frac{I_{\max}}{\Delta V_C f_s (N - 1)} \quad (1)$$

where  $\Delta V_C$  is the maximum voltage ripple under rated conditions, which is generally 10% of rated voltage;  $f_s$  is the switching frequency,  $I_{\max}$  is the maximum output current. It is worth noting that the number of the output levels  $N$  should be 7, not 9, to ensure the proper operation.

For converter with parameters shown in Table III, the floating capacitor should be larger than 650  $\mu$ F if the switching frequency is 1020 Hz. Here 1000  $\mu$ F capacitor is used. When the load impedance is fixed to 0.5 p.u, the lowest voltage of  $V_{FC1}$  under different modulation index and power factors is shown in Fig. 4. It is revealed that the high modulation index and high power factor can lead to higher voltage variations and under some extreme conditions, the converter will completely lose the ability to maintain the voltage on  $FC_1$ .

A comprehensive analysis of the operating range of 7L-HC under boosting 9L operation is shown in Fig. 5. The results are obtained when the output frequency is 60 Hz. Since boosting 9L operation is generally enabled for speed expansion and the frequency is higher than 60 Hz, the results can be considered as the worst case. The combinations of load impedance, modulation index, and power factor which leads to more than 10% variation in  $V_{FC1}$  are considered to be nonoperable conditions, which are depicted as the blank region. On the other hand, operable conditions are filled blocks in Fig. 5. As can be seen, the converter cannot run with boosting 9L mode under high modulation index and high power factors even the load condition is low. However,

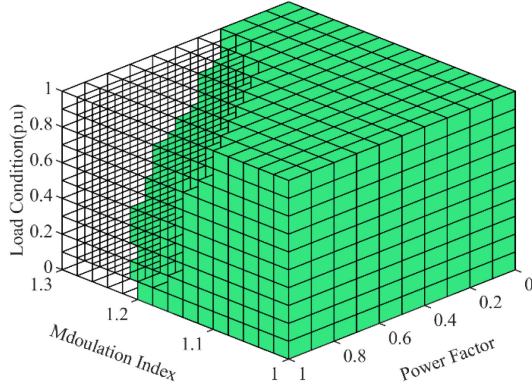


Fig. 5. Operation range under different loads, modulation indices, and power factors.

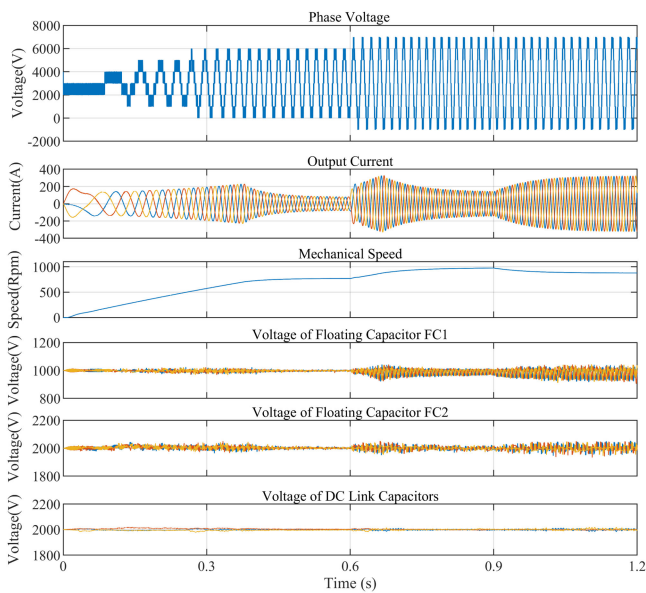


Fig. 6. Simulation results of motor drive system: start-up (0–0.6 s), speed expansion (0.6–0.9 s), step increase in torque (0.9–1.2 s).

it is possible to limit the modulation index, e.g., 1.1, and ensure operation under any combinations of load, modulation index, and power factor. Therefore, the boosting operation method can work properly in most cases. In particular, motors generally have a low power factor at light load conditions, which is generally the situation that speed expansion is applied.

#### IV. SIMULATION AND EXPERIMENTAL VALIDATIONS

To validate the boosting 9L operation and its application in the motor drive system, a medium voltage system is built-in MATLAB/Simulink, whose parameters are the same as Table III. As shown in Fig. 6, the motor start-up is finished under normal 7L operation during 0–0.6 s. The motor speed continuously increases to its nominal value and the 7L-HC converter's output frequency and voltage amplitude are also continuously increased to their rated value. Both the floating capacitor voltage and dc-link voltage are well regulated during this process. At 0.6 s, the speed expansion is enabled, the converter starts to produce

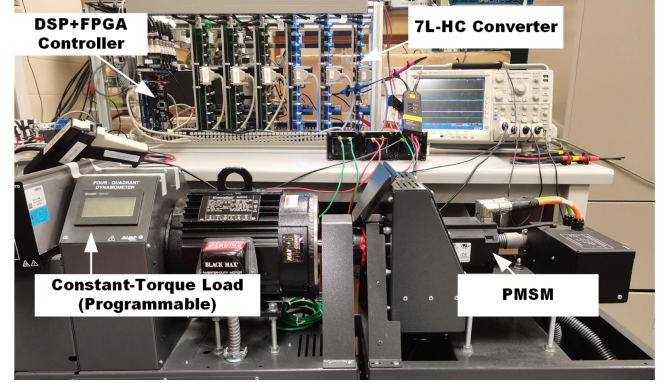


Fig. 7. Schematic diagram of the experimental setup.

TABLE IV  
PARAMETERS USED FOR EXPERIMENT

Parameter	S.I values	p.u values
Rated DC Voltage	150V	-
Rated AC Voltage	110V	1.0
Rated Power	1.4 kW	1.0
Base Impedance	8.64 $\Omega$	1.0
Floating Capacitor $C_1$	1000 $\mu$ F	3.26
Floating Capacitor $C_2$	1000 $\mu$ F	3.26
DC link Capacitors $C_{dc}$	2700 $\mu$ F	8.8
Switching Frequency	5000-Hz	-
Pole Pairs of Motor	5	-
Stator Resistance	0.54 $\Omega$	0.063
d-q axis Inductance	3.1mH	0.14
Magnet Flux Linkage	0.151Wb	-

extended output levels and runs in boosting 9L operation-phase voltage range is expanded from 0–6000 V to –1000–7000 V, and the speed is increased from 800 to 1000 r/min. At 0.9 s, the motor torque suffered a step change from 3000 to 6000 N·m, and the output current is significantly increased. However, the converter can still well regulate the floating capacitor voltage and dc-link capacitor voltage. This simulation validates that the proposed boosting 9L operation is feasible and significant speed expansion can be easily achieved.

The boosting 9L operation method is validated on the 7L-HC experimental setup with both R–L load and a permanent magnet synchronous motor, which are shown in Fig. 7. The key parameters of the converter and motor are shown in Table IV. Digital signal processor (DSP) and field-programmable gate array (FPGA) are used to control the experimental setup. To avoid interference of the modulation method and control method while solely validating the proposed operating method, open-loop tests and sinusoidal pulse width modulation (SPWM) without any third-order injection are used in the experiments. To facilitate the comparison with analysis, the parameters are selected to have the same base impedance with the medium voltage system shown in Table III, leading to the same per unit (p.u) values and International System of Units (S.I.) values for impedances in Tables III and IV.

Fig. 8 shows the experimental results of R–L load ( $L = 5$  mH and  $R = 22\Omega$ ) when the boosting 9L operation is enabled by increasing the modulation index from 1 to 1.1. As can be seen,

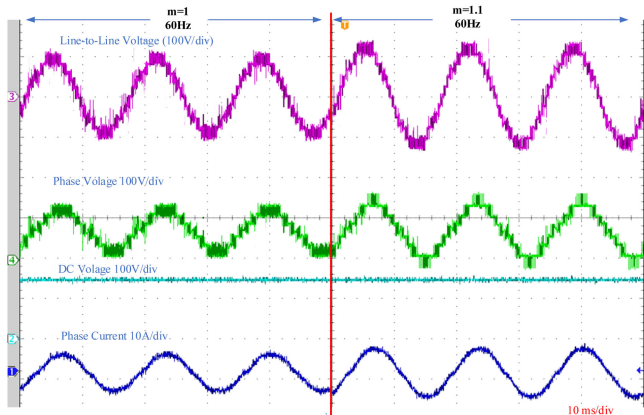


Fig. 8. Experimental results with R-L load: Step change of modulation index from 1.0 to 1.1 with SPWM.

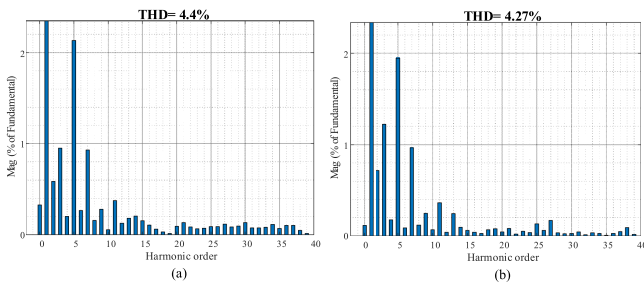


Fig. 9. FFT analysis of output current. (a) 7L-operation when  $m = 1$ , 60 Hz. (b) Boosting 9L operation  $m = 1.1$ , 60 Hz.

when the converter enters the boosting region, the output phase voltage is further increased. And the phase voltage is to be higher than the dc-link voltage, which is about 200 V under a 150 V<sub>DC</sub> in this test. Correspondingly, the line-to-line voltage and output current is also increased. This validates the ability to boost output voltage. Besides, it is worth noting that the voltage in Fig. 8 contains noticeable switching spikes which are not present in simulation results. The spikes are mainly caused by the commutation process when different switching vectors are applied, which is explained in [17]. The current quality is compared for the two operation modes. As shown in Fig. 9, the total harmonic distortion (THD) under 9L operation is slightly lower than the 7L operation, where the reduction from 4.4% to 4.27% is mainly caused by the higher fundamental current under the higher modulation index of 9L operation.

Fig. 10 shows the transient waveform when a significant change in both modulation index and the output frequency is applied. As can be seen, when the modulation index is abruptly changed from 0.3 to 1.1 with the frequency increases from 10 to 66 Hz, the converter can still well regulate the voltage of floating capacitors and ensure the proper operation. This will validate that the added boosting 9L operation can be used even the converter needs to deal with significant transients.

As discussed, this boosting operation method can help to increase the voltage limitation of the motor to support a higher speed operation. Fig. 11 shows the waveforms when the 7L-HC converter drives a motor with a 2 N·m load. As can be seen, when

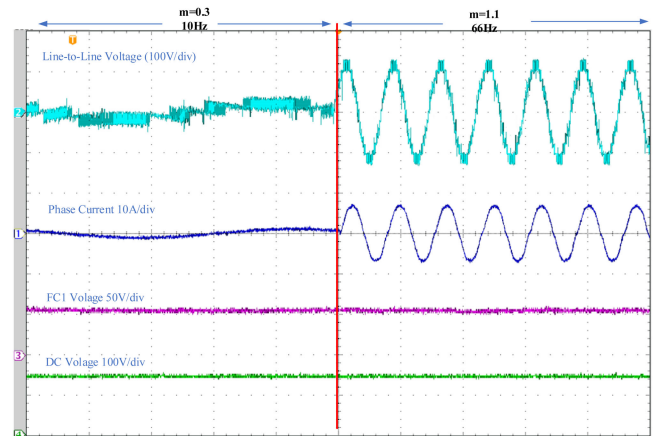


Fig. 10. Experimental results with R-L load: Step change of both modulation index and frequency (from  $m = 0.3$ , 10 Hz to 1.1, 66 Hz).

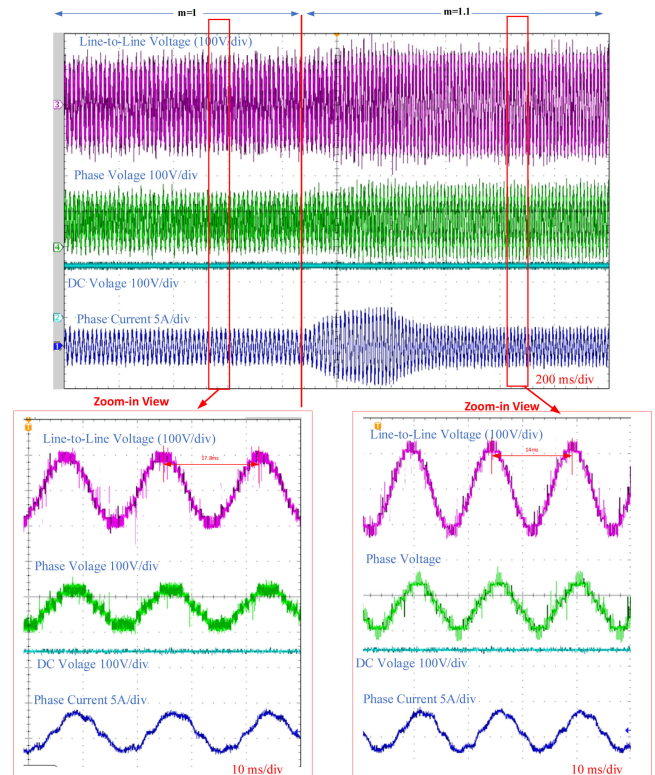


Fig. 11. Experimental results with motor: ramp change of modulation index from 1.0 to 1.1 with SPWM.

the modulation index ramps up to 1.1, the phase voltage and line-to-line voltage are increased. And the fundamental cycle is also changed due to the increase in motor speed, i.e., the fundamental cycle is shortened from 17.8 to 14.7 ms, matching the measured motor speeds—675 and 857 r/min, respectively. It is worth noting that the open-loop test leads to a nonideal back electromotive force, distortions can be observed in currents, but this will not impact the validations on the boosting operation. More operating conditions are tested and the results are concluded in Table V. As can be seen, the boosting operation

TABLE V  
MEASURED MOTOR SPEED UNDER DIFFERENT LOAD TORQUES AND  
OPERATING METHOD

Torque(N·m)	0.5	1	1.5	2
Speed under Normal Operation(r/min)	733	710	692	675
Speed under Boosting Operation (r/min)	883	844	825	811

can effectively increase the motor speed even the maximum modulation index is limited to 1.1.

## V. CONCLUSION

This letter proposes the boosting 9L operation method for the 7L-HC converter. This method can help 7L-HC to produce 9 output levels and boost the output voltage amplitude to be high than dc voltage. The operation method will not change voltage stress on power devices and thus yield no extra hardware costs. Considering that the added boosting levels do not contain sufficient switching states to balance the floating capacitor, the operating constraints are analyzed and the results reveal that this method can have a feasible operating range. Both R-L load and motor are used to validate the operating method experimentally.

## REFERENCES

- [1] B. Wu and M. Narimani, "Introduction," in *High-Power Converters and AC Drives*, B. Wu and M. Narimani, Eds. New York, NY, USA: Wiley, 2017, pp. 1–16.
- [2] J. Chen and C. Wang, "Dual T-type four-level converter," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp. 5594–5600, Jun. 2020.
- [3] A. Bahrami and M. Narimani, "A new five-level T-type nested neutral point clamped (T-NNPC) converter," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 10534–10545, Nov. 2019.
- [4] H. Tian, Y. Li, and Y. W. Li, "A novel seven-level hybrid-clamped (HC) topology for medium-voltage motor drives," *IEEE Trans. Power Electron.*, vol. 33, no. 7, pp. 5543–5547, Jul. 2018.
- [5] H. Tian and Y. W. Li, "An active capacitor voltage balancing method for seven-level hybrid clamped (7L-HC) converter in motor drives," *IEEE Trans. Power Electron.*, vol. 35, no. 3, pp. 2372–2388, Mar. 2020.
- [6] J. Huang and K. A. Corzine, "Extended operation of flying capacitor multilevel inverters," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 140–147, Jan. 2006.
- [7] S. Lu, S. Mariéthoz, and K. A. Corzine, "Asymmetrical cascade multilevel converters with noninteger or dynamically changing DC voltage ratios: Concepts and modulation techniques," *IEEE Trans. Power Electron.*, vol. 57, no. 7, pp. 2411–2418, Jul. 2010.
- [8] Z. Quan and Y. W. Li, "Multilevel voltage-source converter topologies with internal parallel modularity," *IEEE Trans. Ind. Appl.*, vol. 56, no. 1, pp. 378–389, Jan./Feb. 2020.
- [9] J. Fang, F. Blaabjerg, S. Liu, and S. M. Goetz, "A review of multilevel converters with parallel connectivity," *IEEE Trans. Power Electron.*, vol. 36, no. 11, pp. 12468–12489, Nov. 2021.
- [10] S. S. Thakur, M. Odavic, A. Allu, Z. Q. Zhu, and K. Atallah, "Analytical modelling and optimization of output voltage harmonic spectra of full-bridge modular multilevel converters in boost mode," *IEEE Trans. Power Electron.*, vol. 37, no. 3, pp. 3403–3420, Mar. 2022.
- [11] S. Yang, F. Z. Peng, Q. Lei, R. Inoshita, and Z. Qian, "Current-fed quasi-Z-source inverter with voltage buck-boost and regeneration capability," *IEEE Trans. Ind. Appl.*, vol. 47, no. 2, pp. 882–892, Mar./Apr. 2011.
- [12] S. S. Lee, C. S. Lim, Y. P. Siwakoti, and K. Lee, "Dual-T-type five-level cascaded multilevel inverter with double voltage boosting gain," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 9522–9529, Sep. 2020.
- [13] D. Stojan, D. Drevensek, Ž. Plantic, B. Grčar, and G. Stumberger, "Novel field-weakening control scheme for permanent-magnet synchronous machines based on voltage angle control," *IEEE Trans. Ind. Appl.*, vol. 48, no. 6, pp. 2390–2401, Nov./Dec. 2012.
- [14] Y. Hu, Y. Li, X. Ma, X. Li, and S. Huang, "Flux-weakening control of dual three-phase PMSM based on vector space decomposition control," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 8428–8438, Jul. 2021.
- [15] Definite Purpose Inverter-fed Polyphase Motors, National Electrical Manufacturers Association (NEMA) standards MG1, part 31, 2016.
- [16] K. Wang, Z. Zheng, D. Wei, B. Fan, and Y. Li, "Topology and capacitor voltage balancing control of a symmetrical hybrid nine-level inverter for high-speed motor drives," *IEEE Trans. Ind. Appl.*, vol. 53, no. 6, pp. 5563–5572, Nov./Dec. 2017.
- [17] H. Tian, Y. Li, and Y. W. Li, "Commutation scheme of seven-level hybrid-clamped converters with suppressed deadband-induced voltage spikes," *IEEE Trans. Ind. Electron.*, vol. 68, no. 12, pp. 11663–11672, Dec. 2021.